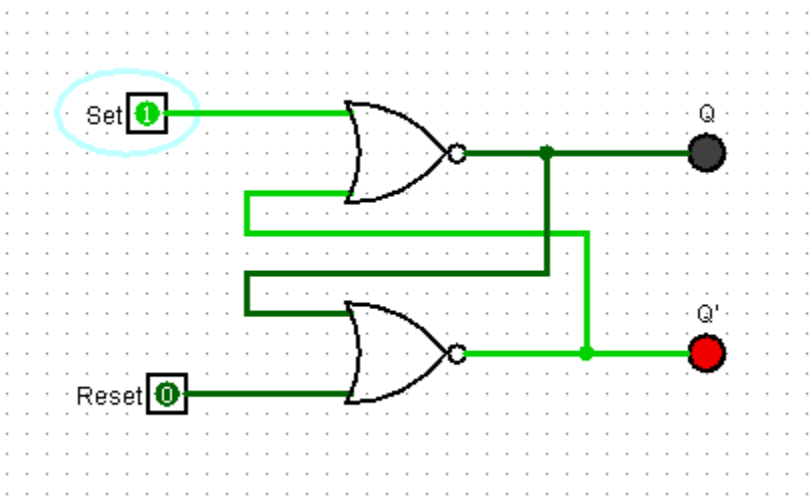
10.

| Set | Reset | Q | Q’ |
|---|---|---|---|
| **1** | 0 | 0 | 1 |
| **1** | 1 | 0 | 0 |
| **0** | 1 | 1 | 0 |
| **1** | 1 | 0 | 0 |




11.

The behaviour of the circuit:

When Set =1 and Reset=0 => Q’=1

In contrast when Set =0 and Reset=1 => Q=1

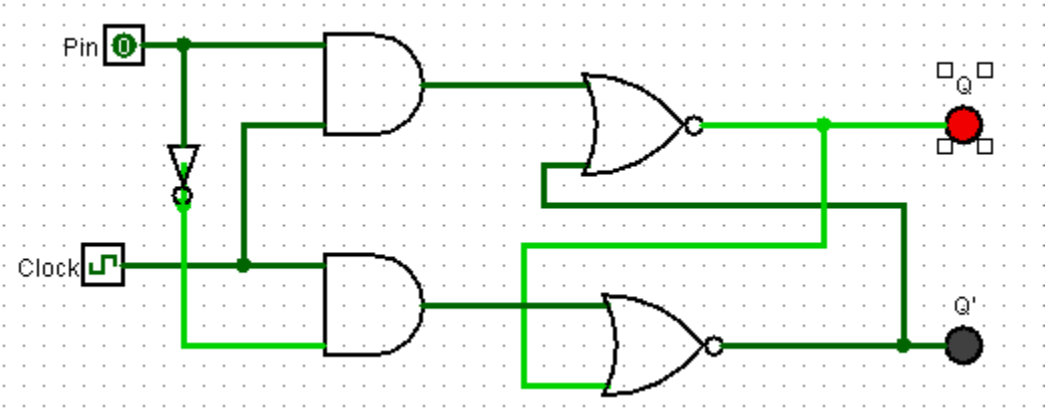
12.

If we set both the Set=1 and Reset=1, the outputs are both 0 and RS Flip Flop is reset to the undefined state.

This is the issue in digital circuit design since the design of circuit, Qa and Qb should be the opposite of each other, and the flip flop rule states that the outputs must be equal.

They complement and encourage one another. As a result, it violates the rule by being set in this way.

13.




14.

| Clock | Pin | Q | Q’ |
|---|---|---|---|
| **0** | 0 | 0 | 0 |
| **0** | 1 | 0 | 0 |
| **1** | 1 | 0 | 1 |
| **1** | 0 | 1 | 0 |

15.

The D Flip Flop has a single data input and uses the clock to regulate the signal (to hold a single bit), D (Data) generate both S and R, when the clock starts, Q is set to inverted as D, and Q’ is set to be same as D.

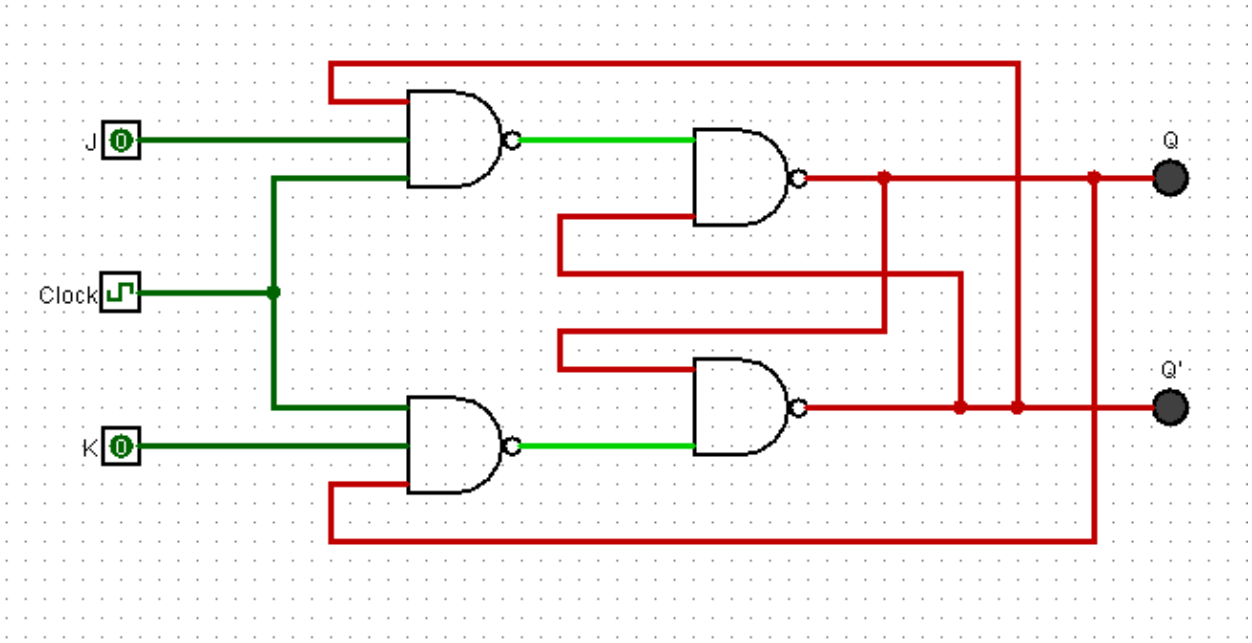
16.

The clock plays a very important role in D Flip Flop, is used to regulate the signal.

17.

Reason why D Flip Flop is chosen over RS Flip Flop is that D Flip Flop can help with data synchronization if we need to be timed.

18.




19.

| J | K | Q (when clocked) | Q' (when clocked) |
|---|---|---|---|
| **0** | 0 | No charge | No charge |
| **1** | 0 | 1 | 0 |
| **0** | 1 | 0 | 1 |
| **1** | 1 | Toggle | Toggle |

20.

JK Flip Flop was modified like a D Flip Flop but adding one extra input that links to (NAND gate) and the clock and removing some component (not gate)

21.

When both J and K input is set as 1, the JK Flip Flop act like a Toggle – T Flip Flop