Technical Information Manual

Revision n. 11

12 November 2015

MOD. DT5751
2-4 CHANNEL 10 BIT
2-1GS/S DIGITIZER
MANUAL REV.11

NPO:
00100/09:5751x.MUTx/11

CAEN will repair or replace any product within the guarantee period if the Guarantor declares that the product is defective due to workmanship or materials and has not been caused by mishandling, negligence on behalf of the User, accident or any abnormal conditions or operations.

CAEN declines all responsibility for damages or injuries caused by an improper use of the Modules due to negligence on behalf of the User. It is strongly recommended to read thoroughly the CAEN User's Manual before any kind of operation.

CAEN reserves the right to change partially or entirely the contents of this Manual at any time and without giving any notice.

Disposal of the Product

The product must never be dumped in the Municipal Waste. Please check your local regulations for disposal of electronics products.

MADE IN ITALY : We stress the fact that all the boards are made in Italy because in this globalized world, where getting the lowest possible price for products sometimes translates into poor pay and working conditions for the people who make them, at least you know that who made your board was reasonably paid and worked in a safe environment. (this obviously applies only to the boards marked "MADE IN ITALY", we cannot attest to the manufacturing process of "third party" boards).

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. General description

For any reference to registers in this user manual, please refer to “DT5751 Registers Description” document available at the digitizer web page.

1.1. Overview

Fig. 1.1: Mod. DT5751 Desktop Waveform Digitizer

The Mod. DT5751 is a 4 Channel 10 bit 1 GS/s Desktop Waveform Digitizer with 1 Vpp input dynamic range on single ended MCX coaxial connectors. Versions with 0.2 Vpp single ended customization are also available.

The DC offset is adjustable via a 16-bit DAC on each channel in the ±0.5V range @ 1Vpp or ±0.1V @ 0.2Vpp.

The Mod. DT5751 can work also as 2 Channel 10 bit 2 GS/s Flash ADC Waveform Digitizer (Dual Edge Sampling).

The module features a front panel clock In and a PLL for clock synthesis from internal/external references. The data stream is continuously written in a circular memory buffer. When the trigger occurs, the FPGA writes further N samples for the post trigger and freezes the buffer that can be read via USB or optical link. The acquisition can continue without dead time in a new buffer.

Each channel has a SRAM memory (see **Errore. L'origine riferimento non è stata trovata.** for the available meory sizes) divided in buffers of programmable size (1 – 1024). The size of the memory doubles when operating in DES mode). The readout (from USB or Optical link) of a frozen buffer is independent from the write operations in the active circular buffer (ADC data storage).

Mod. DT5751 supports multi-board synchronization: an external reference clock can be distributed to all modules (CLK IN) and a common input (GPI) can be used to align all event trigger time tags. When synchronized, all data will be aligned and coherent across multiple DT5751 boards.

The trigger signal can be provided via the front panel input as well as via the software, but it can also be generated internally with threshold auto trigger capability.
DT5751 houses USB 2.0 and Optical Link interfaces. USB 2.0 allows data transfers up to 30 MB/s. The Optical Link supports transfer rate of 80 MB/s, and offer daisy-chain capability. Therefore it is possible to connect up to 8 ADC modules to an A2818 Optical Link Controller or 32 modules to an A3818 (4 channel version).
CAEN provides also for this model a Digital Pulse Processing firmware for Physics Applications. This feature allows to perform on-line processing on detector signal directly digitized. DT5751 digitizers running DPP firmware accept signals directly from the detector and implement a digital replacement of dual gate QDC, discriminator and gate generator.

Table 1.1: Available models, related products and accessories

Code	Description
WDT5751XAAAA	DT5751 - 2/4 Ch. 10 bit 2/1 GS/s Digitizer: 3.6/1.8MS/ch, EP3C16, SE
WPERS0175102	x751 Customization - 200mVpp Input Range, SE
WA654XAAAAAA	A654 - Single Channel MCX to LEMO Cable Adapter
WA654K4AAAAA	A654 KIT4 - 4 MCX TO LEMO Cable Adapter
WA659XAAAAAA	A659 - Single Channel MCX to BNC Cable Adapter
WA659K4AAAAA	A659 KIT4 - 4 MCX TO BNC Cable Adapter
WA659K8AAAAA	A659 KIT8 - 8 MCX TO BNC Cable Adapter
WA2818XAAAAA	A2818 - PCI Optical Link
WA3818AXAAAA	A3818 - PCIe 1 Optical Link
WA3818BXAAAA	A3818 - PCIe 2 Optical Link
WA3818CXAAAA	A3818 - PCIe 4 Optical Link
WAI2730XAAAA	AI2730 - Optical Fibre 30 m. simplex
WAI2720XAAAA	AI2720 - Optical Fibre 20 m. simplex
WAI2705XAAAA	AI2705 - Optical Fibre 5 m. simplex
WAI2703XAAAA	AI2703 - Optical Fibre 30cm. simplex
WAY2730XAAAA	AY2730 - Optical Fibre 30 m. duplex
WAY2720XAAAA	AY2720 - Optical Fibre 20 m. duplex
WAY2705XAAAA	AY2705 - Optical Fibre 5 m. duplex
WFWDPPNGAA51(*)	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (x751)
WFWDPPZLAA51(*)	DPP-ZLE - Digital Pulse Processing Zero Length Encoding for (x751)

(*) Multi-license packs are also available. Please, refer to the Digitizer web page for the relevant ordering options.

1.2. Block Diagram

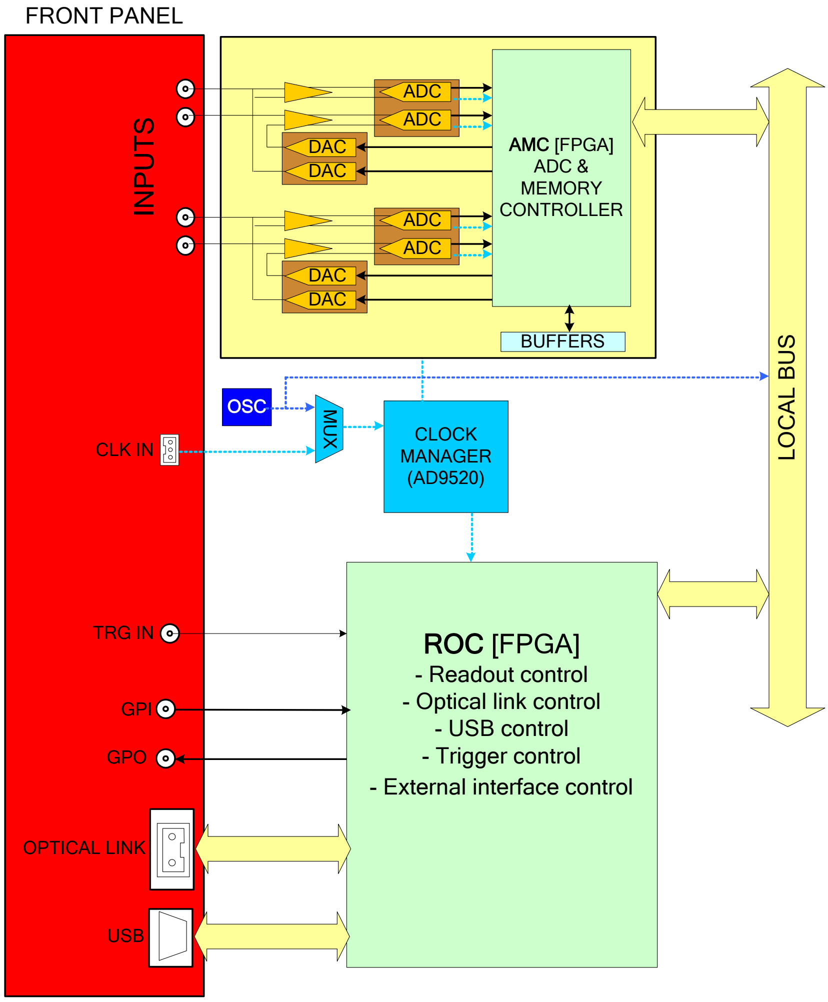

Fig. 1.1: Mod. DT5751 Block Diagram

The function of each block will be explained in detail in the subsequent sections.

2. Technical specifications

2.1. Packaging and Compliancy

The unit is a Desktop module housed in a 154x50x164 mm^3 alloy box.

2.2. Power requirements

The module is powered by the external AC/DC stabilized power supply provided with the digitizer and included in the delivered kit.

The board's typical power consumption is 1.8A (@+12V).

NOTE: Using a different power supply source, like battery or linear type, it is recommended the source to provide +12V and, at least, 2A; the power jack is a 2.1mm type, a suitable cable is the RS 656-3816 type (or similar).

2.3. Front and Back Panel

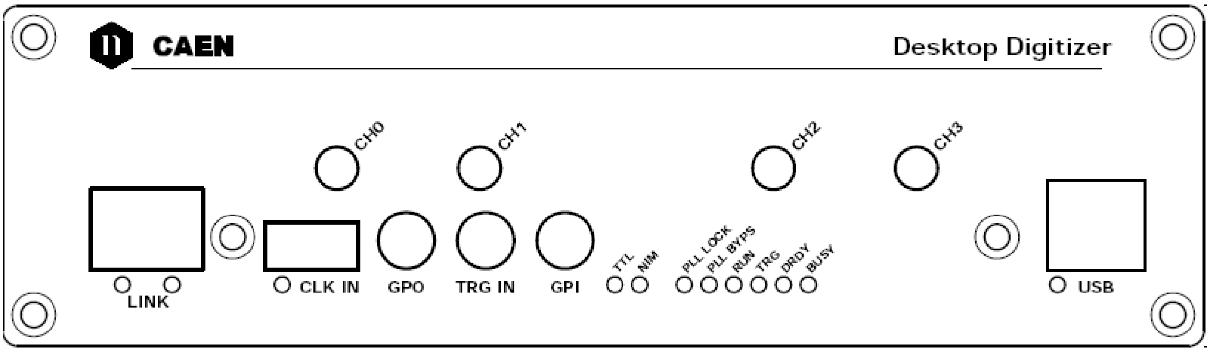

Fig. 2.1: Mod. DT5751 front panel

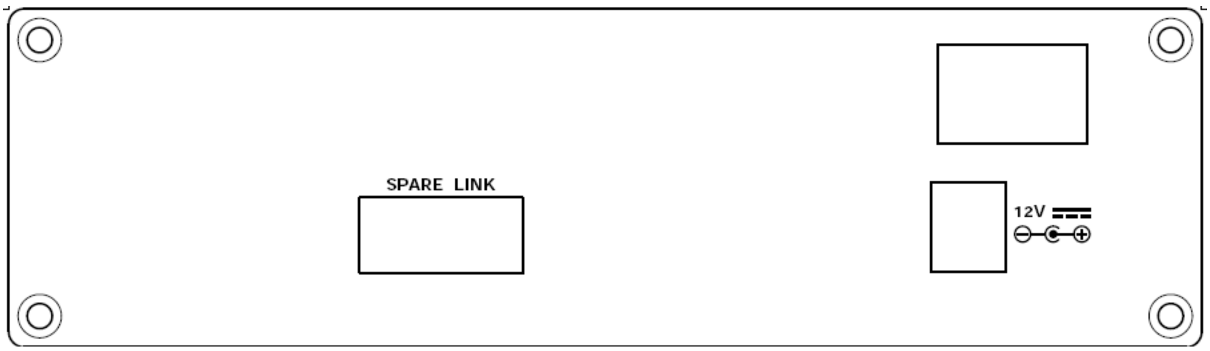

Fig. 2.2: Mod. DT5751 back panel

2.4. External connectors

2.4.1. ANALOG INPUT connectors

Fig. 2.3: MCX connector

Function:
Analog input, single ended, input dynamics: 1Vpp or 0.2Vpp, Zin=50Ω
Mechanical specifications:
MCX connector (CS 85MCX-50-0-16 SUHNER)

Absolute max analog input voltage (for 1Vpp FSR): 3Vpp (with Vrail max +3V or -3V) for any DAC offset in single ended configuration.

Absolute max analog input voltage (for 0.2Vpp FSR): 2Vpp (with Vrail max +2V or -2V) for any DAC offset in single ended configuration

2.4.2. CONTROL connectors

Function:
TRG IN: External trigger input (NIM/TTL, Zin= 50Ω)
Mechanical specifications:
00-type LEMO connectors

2.4.3. ADC REFERENCE CLOCK connectors

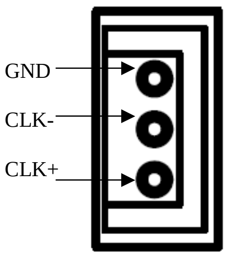

Fig. 2.4: AMP CLK IN Connector

Function:
CLK IN: External clock/Reference input, AC coupled (diff. LVDS, ECL, PECL, LVPECL, CML), Zdiff= 100Ω.
Mechanical specifications:
AMP 3-102203-4 AMP MODUII

2.4.4. Digital I/O connectors

Function:

- GPI: programmable front panel input (NIM/TTL, Zin=50Ω)
- GPO: programmable front panel output (NIM/TTL across 50Ω); used as output for trigger propagation

Mechanical specifications:
00-type LEMO connectors

2.4.5. Optical LINK connector

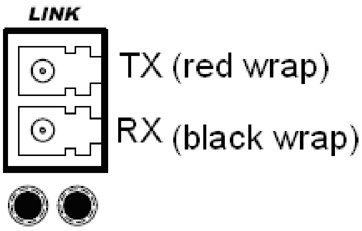

Fig. 2.5: LC Optical Connector

Mechanical specifications:
LC type connector; to be used with Multimode 62.5/125µm cable with LC connectors on both sides
Electrical specifications:
Optical link for data readout and slow control with transfer rate up to 80MB/s; daisy chainable.

2.4.6. USB Port

Mechanical specifications:
B type USB connector
Electrical specifications:
USB 2.0 and USB 1.1 compliant

2.4.7. 12V External

Mechanical specifications:
RAPC722X SWITCHCRAFT PCB DC Power Jack
Electrical specifications:
+12V DC Input

2.4.8. Spare Link

Mechanical specifications:
3M-7610-5002 connector
Electrical specifications:
T.B.D.

2.5. Other components

2.5.1. Displays

The front panel hosts the following LEDs:

Table 2.1: Front panel LEDs

Name:	Colour:	Function:
CLK_IN	green	External clock enabled.
NIM	green	Standard selection for GPO, TRG IN, GPI.
TTL	green	Standard selection for GPO, TRG IN, GPI.
USB	green	Data transfer activity
LINK	green/yellow	Network present; Data transfer activity
PLL _LOCK	green	The PLL is locked to the reference clock
PLL _BYPS	green	The reference clock drives directly ADC clocks; the PLL circuit is switched off and the PLL_LOCK LED is turned off.
RUN	green	RUN bit set
TRG	green	Triggers are accepted
DRDY	green	Event/data (depending on acquisition mode) are present in the Output Buffer
BUSY	red	All the buffers are full

2.6. Technical specifications table

Table 2.2: Mod. DT5751 technical specifications

Packaging	Desktop module; 154x50x164 mm^3 (WxHxD), Weight: 680 gr
Analog Input	4 channels, single-ended (SE); 2 channel in DES mode Input range: 1Vpp (default) or 0.2Vpp (on request) Bandwidth: 500MHz. Programmable DAC for Offset Adjustment per channel; adjustment range: ±0.5 V @ 1 Vpp, ±0.1 V @ 0.2 Vpp
Digital Conversion	Resolution: 10 bit; Sampling rate: 1GS/s (2GS/s in DUAL EDGE SAMPLING mode) simultaneously on each channel; multi board synchronization (one board can act as clock master). External Gate Clock capability (NIM/TTL) for burst or single sampling mode.
ADC Sampling Clock generation	Three operating modes: - PLL mode - internal reference (50 MHz loc. oscillator). - PLL mode - external reference on CLK_IN (±100ppm tolerance). - PLL Bypass mode: Ext. 1GHz clock on CLK_IN drives directly ADC clocks for 1GS/s; 2GS/s in DUAL EDGE SAMPLING mode).
Digital I/O	CLK_IN (AMP Modu II): - AC coupled differential input clock LVDS, ECL, PECL, LVPECL, CML (single ended NIM/TTL available with cable adapter) - Jitter<100ppm TRG_IN (LEMO, NIM/TTL, Zin = 50 Ohm) GPI (LEMO, NIM/TTL, Zin = 50 Ohm) GPO (LEMO, NIM/TTL, across 50 Ohm)
Memory Buffer	1.835 MSamples/ch size (becomes 3.6 MSamples/ch in Dual Edge Sampling mode); Multi Event Buffer with independent read and write access. Programmable event size and pre-post trigger. Divisible into 1 ÷ 1024 buffers.
Trigger	Common Trigger - TRG_IN (External signal) - Software (from USB or Optical Link) - Self trigger (Internal threshold auto-trigger) Daisy chain trigger propagation among boards (using GPO)
Trigger Time Stamp	31-bit counter – 16ns resolution - 17s range.
AMC FPGA	One Altera Cyclone EP3C16 per couple of channels
Multi Modules Synchronization	Allows data alignment and consistency across multiple DT5751 modules: - CLK_IN allows the synchronization to a common clock source - GPI ensures Trigger time stamps and start acquisition times alignment
USB interface	USB2.0 and USB1.1 compliant Up to 30 MB/s transfer rate
Optical Link	CAEN proprietary protocol, up to 80 MB/s transfer rate, with Optical Link Controller (Mod. A2818/A3818).
Upgrade	Firmware can be upgraded via Optical Link or USB interface
Software	General purpose C and LabView Libraries Demo and Software Tools for Windows and Linux
Electrical Power	Voltage range: 12 ± 10% Vdc Power consumptions (@12Vdc): 1.8 A (Typical)

3. Functional description

3.1. Analog Input

The default input dynamics is 1V (Zin= 50 Ω); a 0.2V (Zin= 50 Ω) single ended customization is also available (see Table 1.1). A 16-bit DAC allows to add up to ±0.5V DC offset (±0.1V @ 0.2 V_{pp}) to preserve the full dynamic range also with unipolar positive or negative input signals.
The input bandwidth ranges from DC to 500 MHz.

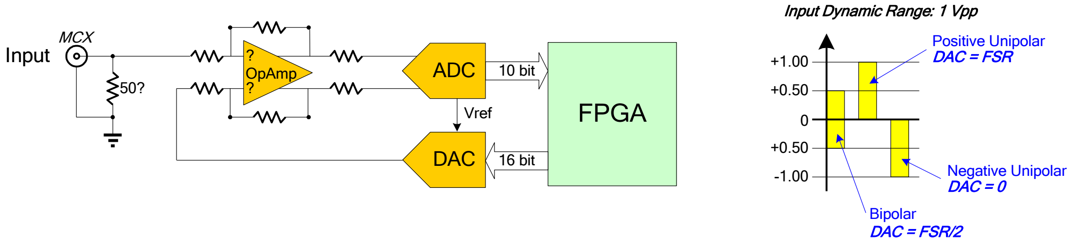

Fig. 3.1: Input diagram

3.2. Clock Distribution

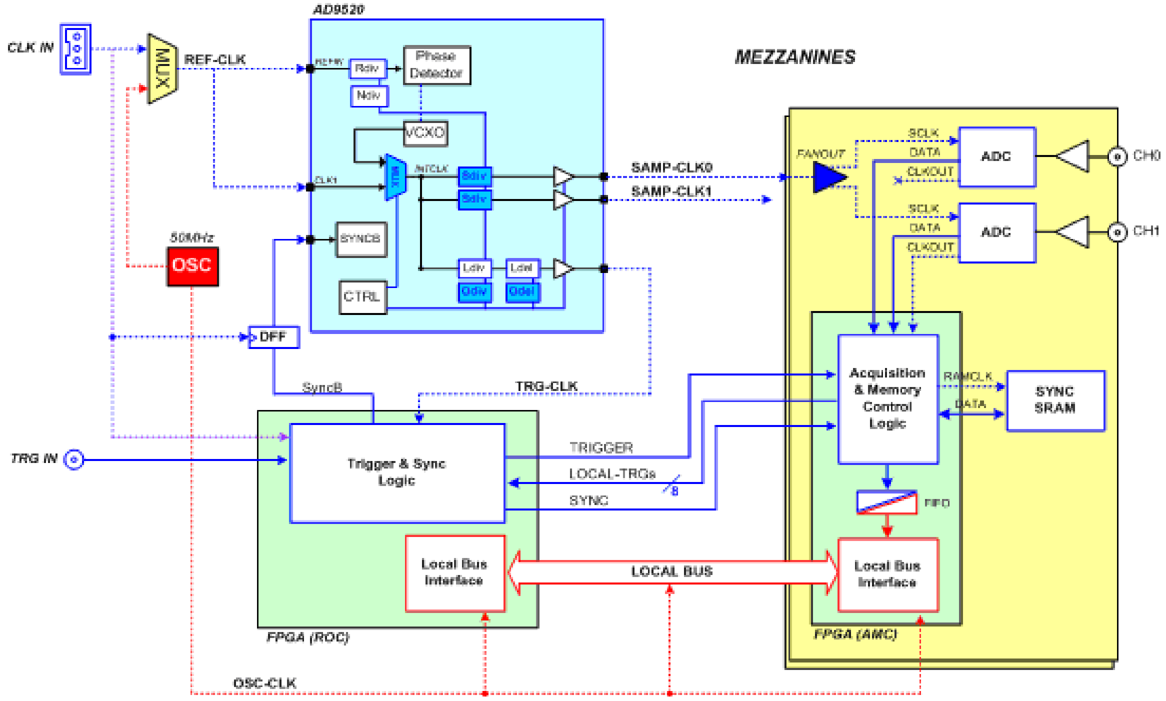

Fig. 3.2: Clock distribution diagram

The module clock distribution takes place on two domains: OSC-CLK and REF-CLK; the former is a fixed 50MHz clock provided by an on board oscillator, the latter provides the ADC sampling clock.
OSC-CLK handles Local Bus (communication between motherboard and mezzanine boards; see red traces in the figure above).
REF-CLK handles ADC sampling, trigger logic, acquisition logic (samples storage into RAM, buffer freezing on trigger) through a clock chain. Such domain can use either an external (via front panel signal) or an internal (via local oscillator) source, in the latter case OSC-CLK and REF-CLK will be synchronous (the operation mode remains the same anyway).
DT5751 uses an integrated phase-locked-loop (PLL) and clock distribution device (AD9520). It is used to generate the sampling clock for ADCs (SAMP-CLK0/SAMP-CLK1) and trigger logic synchronization clock (TRG-CLK).
Both clocks can be generated from the internal oscillator or from external clock input (CLK IN). By default, board uses the internal clock as PLL reference (REF-CLK). External clock can be selected by register access. AD9520 configuration can be changed and stored into non-volatile memory. AD9520 configuration change is primarly intended to be used for external PLL reference clock frequency change:
DT5751 locks to an external 50 MHz clock with default AD9520 configuration.

Please contact CAEN (support.frontend@caen.it) for more information and configuration tools.

Refer also to AD9520 data sheet for more details:
http://www.analog.com/UploadedFiles/Data_Sheets/AD9520.pdf

3.2.1. Trigger Clock

TRG-CLK signal has a frequency equal to 1/8 of SAMP-CLK; therefore a 8 samples “uncertainty” occurs over the acquisition window (16 samples uncertainty with DT5751 operated at 2GS/s).

3.2.2. DES Mode

The DT5751 can be programmed to operate in Dual Edge Sampling (DES) mode, at 2 GS/s.

DES Mode is configurable by setting to “1” the bit[12] of the *Channel Configuration Register* 0x8000 (see the Registers Description document).

NOTE: Only even channels are managed when operating the digitizer in DES mode.

3.3. Acquisition Modes

3.3.1. Channel calibration

In order to achieve best performance, a self channel calibration procedure should be run after the ADCs have stabilized their operating temperature. Whenever the operating temperature changes significantly, a new calibration procedure should be performed.
The calibration is performed through a write access to either Broadcast ADC Configuration or Channel n ADC Configuration register; in order to obtain a better result, it is strongly suggested to calibrate the channels through the Broadcast ADC Configuration register.

3.3.1.1. Normal mode self calibration

- Set to 0 the Calibration bit of Broadcast ADC Configuration register.
- Set such bit to 1. The self calibration process will start and the flag "Calibrating bit" of Channel n Status register will be set to 0.
- Polling on the flag "Calibrating bit" until it returns to 1 (few milliseconds).
- Set again to 0 the Calibration bit of Broadcast ADC Configuration register

3.3.1.2. Dual Edge Sampling mode self calibration

- Make sure that the EVEN channels are <u>disconnected</u>
- Disable (mask) EVEN channels
- Select Dual Edge Sampling mode (bit[12] of the channel configuration register
- Set to 0 the Calibration bit of Broadcast ADC Configuration register.
- Set such bit to 1. The self calibration process will start and the flag "Calibrating bit" of Channel n Status register will be set to 0.
- Polling on the flag "Calibrating bit" until it returns to 1 (few milliseconds).
- Set again to 0 the Calibration bit of Broadcast ADC Configuration register

Whenever switching from one mode (Normal or Dual Edge Sampling) to another, calibration must be repeated.

3.3.2. Acquisition run/stop

The acquisition can be started and stopped in different ways, according to bits[1:0] setting of *Acquisition Control* register (address 0x8100) and bit[2] of the same register:

- SW CONTROLLED (bits[1:0] = 00): Start and Stop take place by software command. Bit[2] = 0 means stopped, while bit[2] = 1 means running.
- GPI CONTROLLED MODE (bits[1:0] = 01): If the acquisition is armed (i.e. bit[2] = 1), then Run starts when GPI is asserted and stops when GPI returns inactive. If bit[2] = 0, the acquisition is always off.
- FIRST TRIGGER CONTROLLED (bits[1:0] = 10): bit[2] = 1 arms the acquisition and the Start is issued on the first trigger pulse (rising edge) on the TRG-IN connector. This pulse is not used as a trigger; actual triggers start from the second pulse on TRG-IN. The Stop acquisition must be SW controlled (i.e. reset of bit[2]).

3.3.3. *Acquisition Triggering: Samples and Events*

When the acquisition is running, a trigger signal allows to:

- store the 31-bit counter value of the Trigger Time Stamp (TTT).

  The counter (representing a time reference), like so the Trigger Logic Unit (see § 3.2) operates at a frequency of 125 MHz (i.e. 8 ns, that is to say 8 ADC clock cycles, or 16 if operating in DES mode). Due to the way the acquired data are written into the board internal memory (i.e in 4-sample bunches), the TTT counter is read every 2 trigger logic clock cycles, which means the trigger time stamp resolution results in 16 ns (i.e. 62.5 MHz). Basing on that, the LSB of the TTT is always "0";

- increment the EVENT COUNTER;
- fill the active buffer with the pre/post-trigger samples, whose number is programmable (Acquisition window width), freezing then the buffer for readout purposes, while acquisition continues on another buffer; buffer size is programmable through the Buffer Organization (0x800C) register.

Table 3.1: Buffer Organization

REGISTER	BUFFER NUMBER	SIZE of one BUFFER (samples)	
		SRAM @ 1 GS/s	SRAM @ 2 GS/s
0x00	1	1.75M	3.5M
0x01	2	896k	1.75M
0x02	4	448k	896k
0x03	8	224k	448k
0x04	16	112k	224k
0x05	32	56k	112k
0x06	64	28k	56k
0x07	128	14k	28k
0x08	256	7k	14k
0x09	512	3584	7k
0x0A	1024	1792	3584

An event is therefore composed by the trigger time tag, pre- and post-trigger samples and the event counter.
Overlap between "acquisition windows" may occur (a new trigger occurs while the board is still storing the samples related to the previous trigger); this overlap can be either rejected or accepted (programmable via software).
If the board is programmed to accept the overlapped triggers, as the "overlapping" trigger arrives, the current active buffer is filled up, then the samples storage continues on the subsequent one.

In this case events will not have all the same size (see Fig. 3.3).

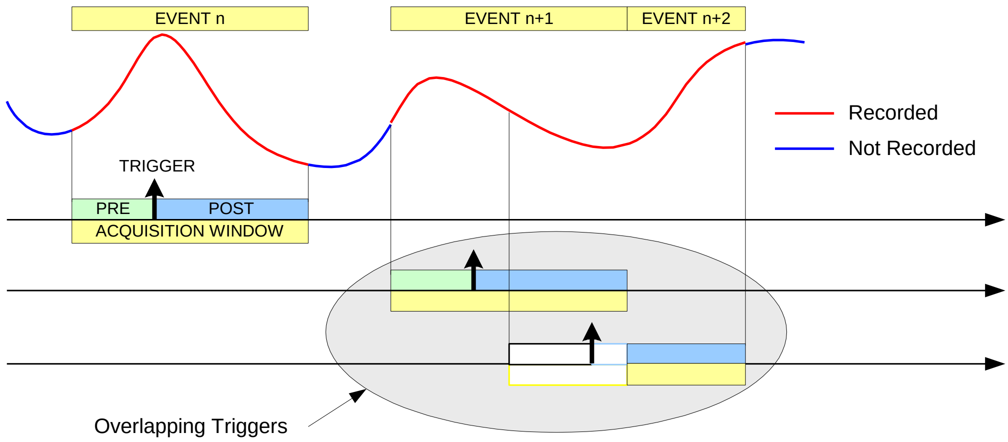

Fig. 3.3: Trigger Overlap

A trigger can be refused for the following causes:

– acquisition is not active
– memory is FULL and therefore there are no available buffers
– the required number of samples for building the pre-trigger of the event is not reached yet; this happens typically as the trigger occurs too early either with respect to the RUN_ACQUISITION command (see § 3.3.2) or with respect to a buffer emptying after a MEMORY_FULL status
– the trigger overlaps the previous one and the board is not enabled for accepting overlapped triggers

As a trigger is refused, the current buffer is not frozen and the acquisition continues writing on it. The Event Counter can be programmed in order to be either incremented or not. If this function is enabled, the Event Counter value identifies the number of the triggers sent (but the event number sequence is lost); if the function is not enabled, the Event Counter value coincides with the sequence of buffers saved and readout.

3.3.3.1. Custom size events

It is possible to make events with a number of Memory locations, which depends on Buffer Organization register setting smaller than the default value. One memory location contains 7 ADC samples and the maximum number of memory locations N_{LOC} is NS = 256K/Nblocks.

Smaller N_{LOC} values can be achieved by writing the number of locations N_{LOC} into the Custom Size register.

N_{LOC} = 0 means “default size events”, i.e. the number of memory locations is the maximum allowed.

N_{LOC} = N1means that one event will be made of 7*N1 or 14*N1 (DES mode).

3.3.4. Event structure

An event is structured as follows:

- Header (four 32-bit words)
- Data (variable size)

The event can be readout either via USB or Optical Link; data format is 32 bit long word.

3.3.4.1. Header

It is composed by four words, namely:

- Size of the event (number of 32 bit long words)
- Bit24; data format: 0; Channel Mask (=1: channels participating to event; ex CH2 and CH3 participating → Ch Mask: 0xC, this information must be used by the software to acknowledge which channel the samples are coming from)
- Event Counter: It is the trigger counter; it can count either accepted triggers only, or all triggers.
- Trigger Time Tag: it is a 31-bit counter (31 bit count + 1 bit as roll over flag), which is reset either as acquisition starts, and is incremented every 8 ADC clock cycles (or 16 if in DES mode). It represents the trigger time reference.
  TTT resolution is 16 ns and ranges up to 17 s (i.e 8 ns*(2^{31}-1)).

3.3.4.2. Samples

Stored samples; data from masked channels are not read. When operating DT5751 at 2 GS/s, “EVEN” channels are automatically disabled. Bit [31,30] are useful to acknowledge how many samples are in the last word of an event (1 to 3); example in § 3.3.4.3. shows a case with two samples in the last word.

3.3.4.3. Event format example

The event format is shown in the following figure (case of 4 channels enabled):

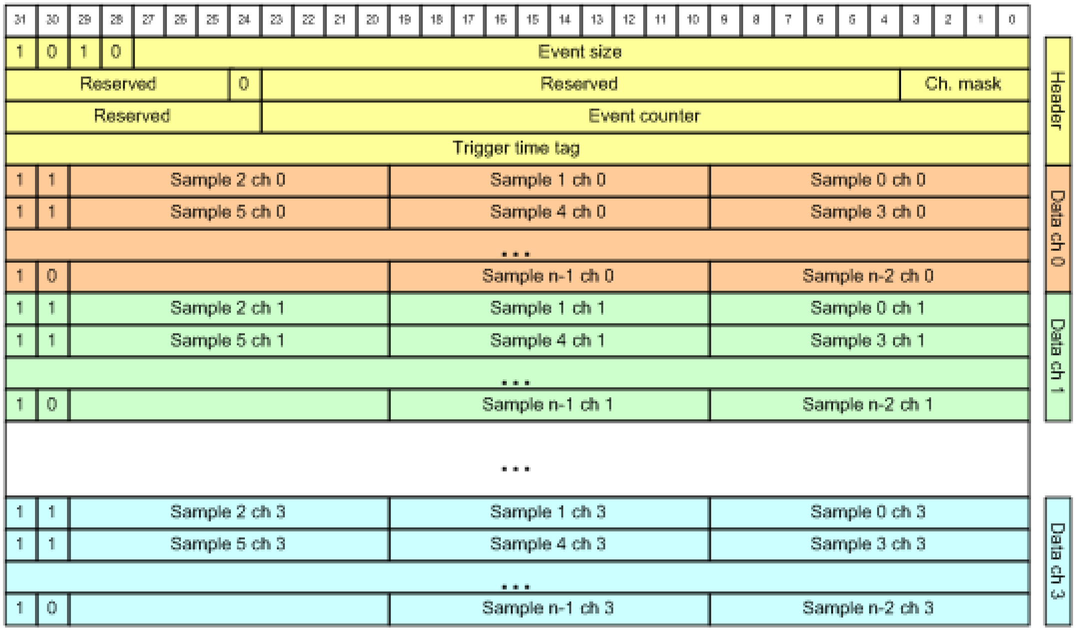

Fig. 3.4: Event Organization

3.3.5. Acquisition Synchronization

Each channel of the digitizer is provided with a SRAM memory that can be organized in a programmable number N of circular buffers (N = [1:1024], see Table 3.1). When the trigger occurs, the FPGA writes further a programmable number of samples for the post-trigger and freezes the buffer, so that the stored data can be read via USB or Optical Link. The acquisition can continue without dead-time in a new buffer.

When all buffers are filled, the board is considered FULL: no trigger is accepted and the acquisition stops (i.e. the samples coming from the ADC are not written into the memory, so they are lost). As soon as one buffer is readout and becomes free, the board exits the FULL condition and acquisition restarts.

IMPORTANT NOTICE: When the acquisition restarts, no trigger is accepted until at least the entire buffer is written. This means that the dead time is extended for a certain time (depending on the size of the acquisition window) after the board exits the FULL condition.

A way to eliminate this extra dead time is by setting bit[5] = 1 in the Acquisition Control register. The board is so programmed to enter the FULL condition when N-1 buffers are filled: no trigger is then accepted, but samples writing continues in the last available buffer. As soon as one buffer is readout and becomes free, the boards exits the FULL condition and can immediately accept a new trigger. This way, the FULL reflects the BUSY condition of the board (i.e. inability to accept triggers); if required, the BUSY signal can be provided out on the digitzer front panel through the TRG-OUT LEMO connector (bits[19:18] and bits[17:16]).

NOTE: when bit[5] = 1, the minimum number of circular buffers to be programmed is N = 2.

In some cases, the BUSY propagation from the digitizer to other parts of the system has some latency and it can happen that one or more triggers occur while the digitizer is already FULL and unable to accept those triggers. This condition causes event loss and it is particularly unsuitable when there are multiple digitizers running synchronously, because the triggers accepted by one board and not by other boards cause event misalignment.

In this cases, it is possible to program the BUSY signal to be asserted when the digitizer is close to FULL condition, but it has still some free buffers (Almost FULL condition). In this mode, the digitizer remains able to accept some more triggers even after the BUSY assertion and the system can tolerate a delay in the inhibit of the trigger generation. When the Almost FULL condition is enabled by setting the Almost FULL level (Memory Almost FULL Level register, address 0x816C) to X, the BUSY signal is asserted as soon as X buffers are filled, although the board still goes FULL (and rejects triggers) when the number of filled buffers is N or N-1, depending on bit[5] in the Acquisition Control Register as described above.

3.4. Trigger management

All the channels in a board share the same trigger: this means that all the channels store an event at the same time and in the same way (same number of samples and same position with respect to the trigger); several trigger sources are available.

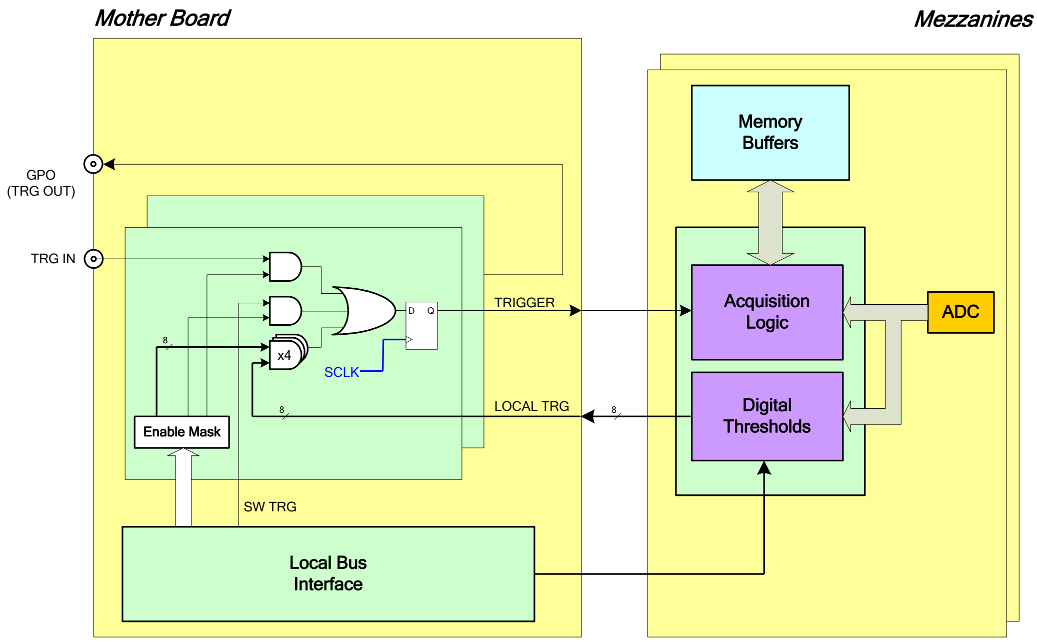

Fig. 3.5: Block diagram of Trigger management

3.4.1. External trigger

External trigger can be NIM/TTL signal on LEMO front panel connector, 50 Ohm impedance. The external trigger is synchronised with the internal clock (see § 3.2.1); if External trigger is not synchronised with the internal clock, a one clock period jitter occurs.

3.4.2. Software trigger

Software trigger are generated INTERNALLY (write access in the relevant register).

3.4.3. Local channel auto-trigger

Each channel can generate a local trigger as the digitized signal exceeds the Vth threshold (ramping up or down, depending on Channel Configuration settings. The Vth digital threshold, the edge type are programmable via register accesses.

NOTE: the local trigger signal does not start directly the event acquisition on the relevant channel; such signal is propagated to the central logic which produces the global trigger, which is distributed to all channels (see § 3.4.4).

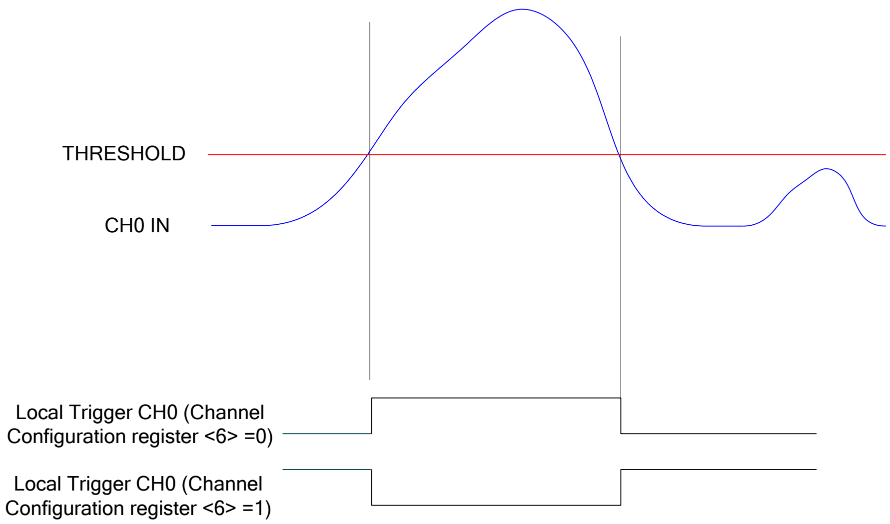

Fig. 3.6: Local trigger generation

3.4.3.1. Trigger coincidence level

In the standard operating, the board's acquisition trigger is a global trigger generated as in § 3.4.4 This global trigger allows the coincidence acquisition mode to be performed through the Majority operation. Enabling the coincidences is possible by writing in the Trigger Source enable Mask register (address 0x810C):

– Bits[3:0] enable the specific channel to participate to the coincidence;
– Bits[23:20] set the coincidence window (T_{TVAW});
– Bits[26:24] set the Majority (i.e. Coincidence) level; the coincidence takes place when:

Number of enabled local auto-triggers > Majority level

Supposing bits[3:0] = FF (i.e. all channels are enabled) and bits[26:24] = 01 (i.e. Majority level = 1), a global trigger is issued whenever at least two of the enabled local channel auto-triggers are in coincidence within the programmed T_{TVAW}.
The Majority level must be smaller than the number of channels enabled via bits[3:0] mask. By default, bits[26:24] = 00 (i.e. Majority level = 0), which means the coincidence acquisition mode is disabled and the T_{TVAW} is meaningless. In this case, the global trigger is simple OR of the enabled local channel auto-triggers.

Fig. 3.7 shows the trigger management in case the coincidences are disabled.

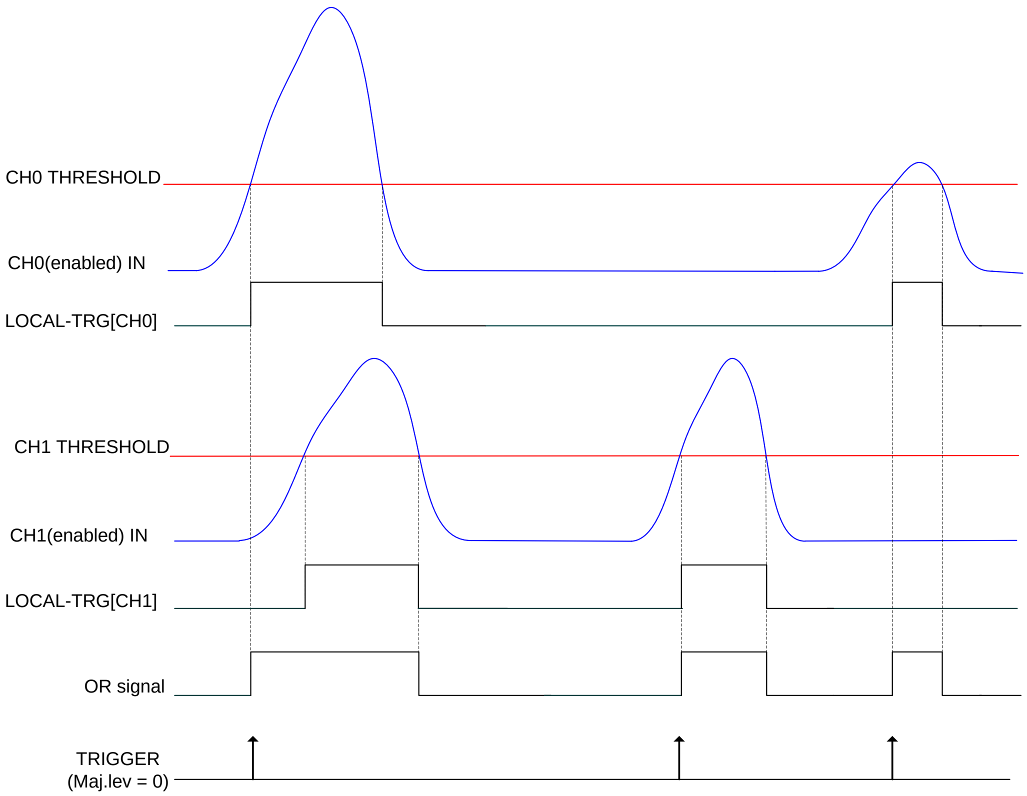

Fig. 3.7: Local trigger relationship with Majority level = 0

Fig. 3.8 and shows the trigger management in case the coincidences are enabled with Majority level = 1 and T_{TVAW} is a value different from 0.

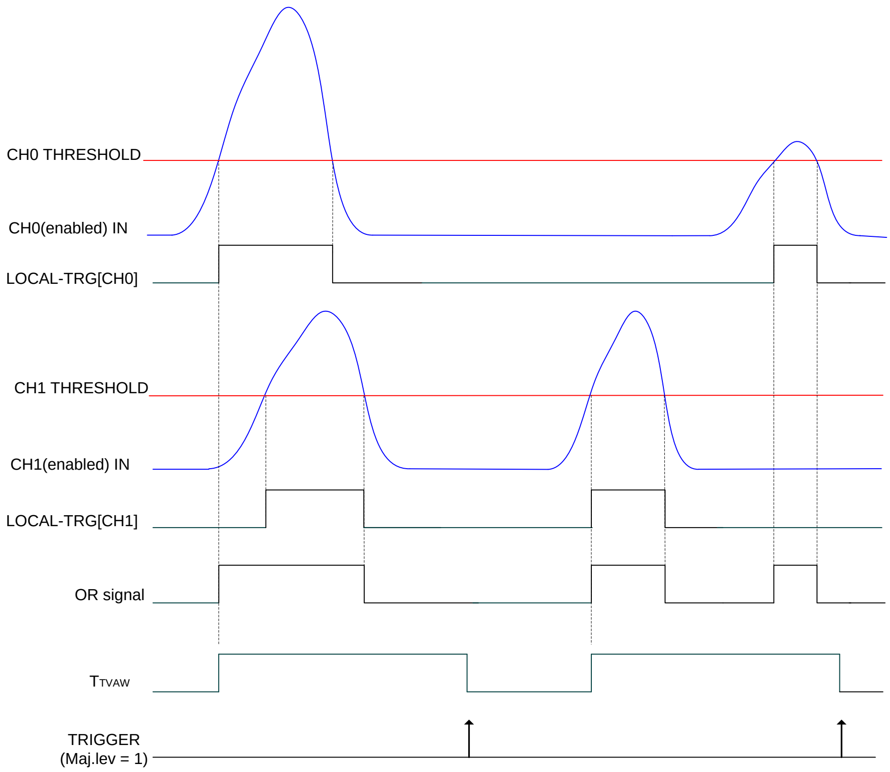

Fig. 3.8: Local trigger relationship with Majority level = 1 and $T_{TVAW} \neq 0$

NOTE: with respect to the position where the global trigger is generated, the portion of input signal stored depends on the programmed length of the acquisition window and on the post trigger setting.

Fig. 3.9 shows the trigger management in case the coincidences are enabled with Majority level = 1 and T_{TVAW} = 0 (i.e. 1 clock cycle)

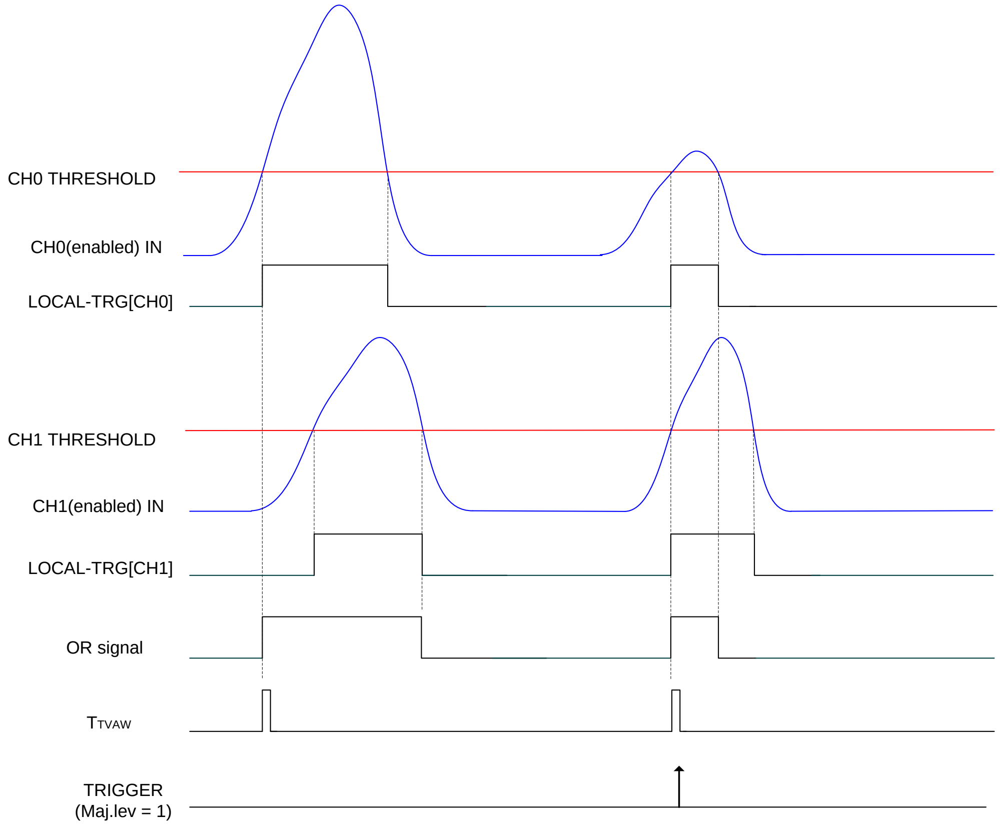

Fig. 3.9: Local trigger relationship with Majority level = 1 and T_{TVAW} = 0

In this case, the global trigger is issued if at least two of the enabled local channel auto-triggers are in coincidence within 1 clock cycle.

NOTE: a practical example of making coincidences with the digitizer in the standard operating is detailed in the document:

GD2817 - How to make coincidences with CAEN digitizers (web available).

3.4.4. Trigger distribution

The OR of all the enabled trigger sources, after being synchronised with the internal clock, becomes the global trigger of the board and is fed in parallel to all the channels, which store an event.
A Trigger Out is also generated on the relevant front panel GPO connector (NIM or TTL), and allows to extend the trigger signal to other boards.
For example, in order to start the acquisition on all the channels in the crate, as one of the channels ramps over threshold, the Local Trigger must be enabled as Trigger Out, the Trigger Out must then be fed to a Fan Out unit; the obtained signal has to be fed to the External Trigger Input of all the boards in the crate (including the board which generated the Trigger Out signal).

3.5. Data transfer capabilities

The board can be accessed by using software drivers and libraries developed by CAEN. Single 16/32 register read/write cycles, multi read cycles and block transfers are supported by the provided library (please consult the relevant documentation for details) Sustained readout rate is up to 60 MB/s for optical link, using block transfers, and up to 30 MB/s for a USB 2.0 link, using block transfers as well.

3.6. Events readout

Event readout is done by accessing the Event Readout Buffer, a FIFO (First-In First-Out) memory that can be accessed into the 0x0000-0x0FFC address space.
Data transfer is always aligned to the programmed number N of events; let X the size of the event expected or read from dedicated register:

- If the event size is known, a read cycle equal to N*X will return all data without interruptions.
- If the number of data read from the Event Readout Buffer is higher than N*X, transfer will be terminated anyway by DT5751 at the end of N*X data.
- If the event size X is unknown (for example in case of overlapping triggers), there are two cases:
  - data transfer ≤ N*X : all data will be returned.
  - data transfer > N*X : only N*X data will be returned.

Once an event is read, the corrisponding acquisition buffers are available to store new data.
During readout, the board can continue to store events in memory up to the maximum number of programmed buffers available; the acquisition process is therefore "dead-timeless": event storage is only interrupted if the combination of trigger and readout rate causes a memory full situation: all acquisition buffers are used and they have not been read yet.
In order to exploit the maximum readout rate allowed by the communication path (USB or optical link), it is suggested to perform block transfer read cycles of at least N*X data with N set to its maximum value, whether possible.

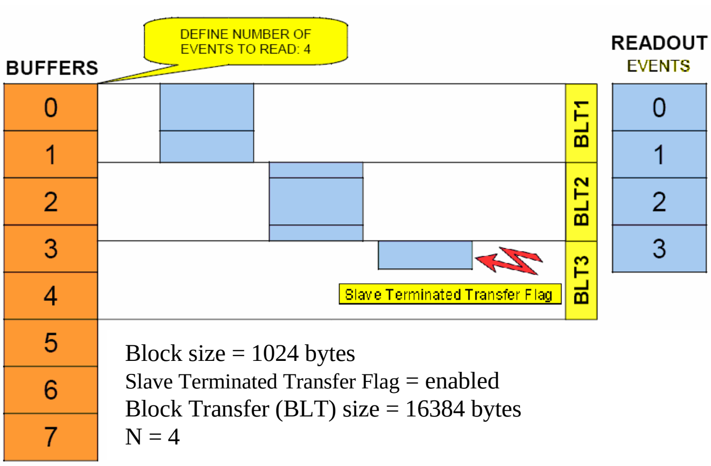

Fig. 3.10: Example of block transfer readout

3.7. Optical Link and USB access

The board houses a USB2.0 compliant port, providing a transfer rate up to 30 MB/s, and a daisy chainable Optical Link able to transfer data at 80 MB/s; the latter allows to connect up to eight DT5751 to a single Optical Link Controller: for more information, see www.caen.it (path: Products / Front End / PCI/PCIe / Optical Controller)

The parameters for read/write accesses via optical link are Address Modifier, Base Address, data Width, etc; wrong parameter settings cause Bus Error.

Control Register bit 3 allows to enable the module to broadcast an interrupt request on the Optical Link; the enabled Optical Link Controllers propagate the interrupt on the PCI bus as a request from the Optical Link is sensed.

4. Software tools

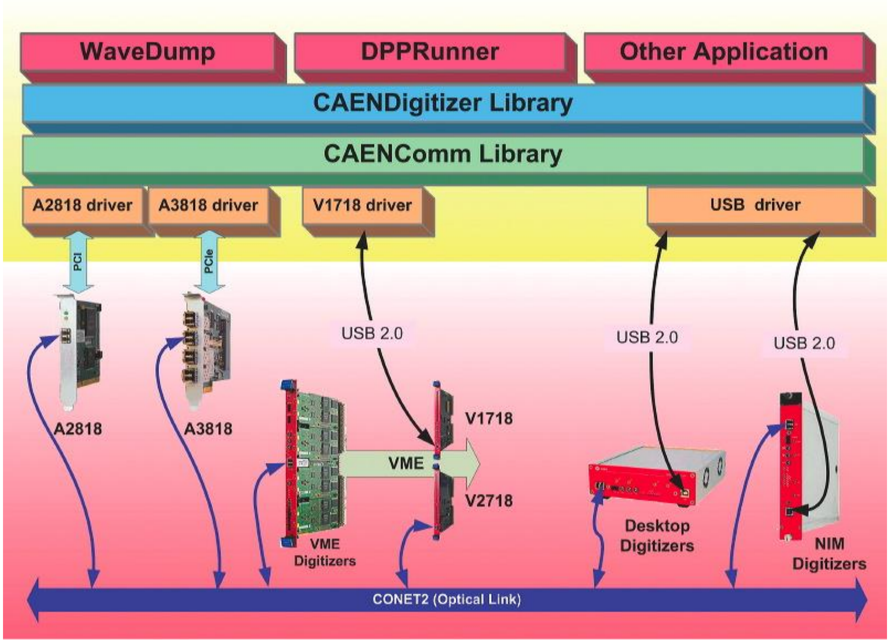

Fig. 4.1: Block diagram of the software layers

CAEN provides drivers for both the physical communication channels (USB and the proprietary CONET Optical Link managed by the A2818 PCI card or A3818 PCIe cards; see § 5.4), a set of C and LabView libraries, demo applications and utilities. Windows and Linux are both supported. The available software is the following:

- **CAENComm** library contains the basic functions for access to hardware; the aim of this library is to provide a unique interface to the higher layers regardless the type of physical communication channel. The CAENComm requires the CAENVMELib library to be installed even in the cases where the VME is not used.
- **CAENDigitizer** is a library of functions designed specifically for the digitizer family and it supports also the boards running special DPP (Digital Pulse Processing) firmware. The purpose of this library is to allow the user to open the digitizer, program it and manage the data acquisition in an easy way: with few lines of code the user can make a simple readout program without the necessity to know the details of the registers and the event data format. The CAENDigitizer library implements a common interface to the higher software layers, masking the details of the physical channel and its protocol, thus making the libraries and applications that rely on the CAENDigitizer independent from the physical layer. The library is based on the CAENComm library that manages the communication at low level (read and write access). CAENVMELib and CAENComm libraries must be already installed on the host PC before installing the CAENDigitizer; however, both CAENVMELib and CAENComm libraries are completely transparent to the user.

- **WaveDump** is a Console application that allows to program the digitizer (according to a text configuration file that contains a list of parameters and instructions), to start the acquisition, read the data, display the readout and trigger rate, apply some post processing (such as FFT and amplitude histogram), save data to a file and also plot the waveforms using the external plotting tool “gnuplot”, available on internet for free. This program is quite basic and has no graphics but it is an excellent example of C code that demonstrates the use of libraries and methods for an efficient readout and data analysis. **NOTE:** WaveDump does not work with digitizers running DPP firmware. The users who intend to write the software on their own are suggested to start with this demo and modify it according to their needs. For more details please see the WaveDump User Manual and Quick Start Guide (Doc nr.: UM2091, GD2084).

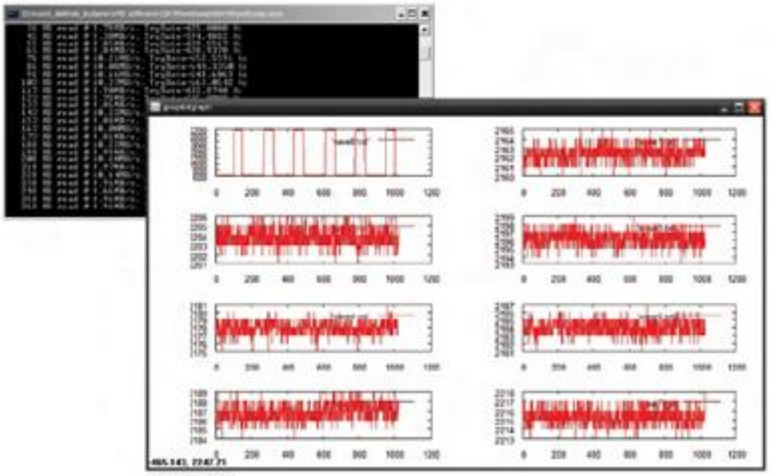

Fig. 4.2: WaveDump output waveforms

- **CAENScope** is a fully graphical program that implements a simple oscilloscope: it allows to see the waveforms, set the trigger thresholds, change the scales of time and amplitude, perform simple mathematical operations between the channels, save data to file and other operations. CAENscope is provided as an executable file; the source codes are not distributed. **NOTE:** CAENScope does not work with digitizers running DPP firmware and it is not compliant with x742 digitizer family. For more details please see the CAENScope Quick Start Guide GD2484.

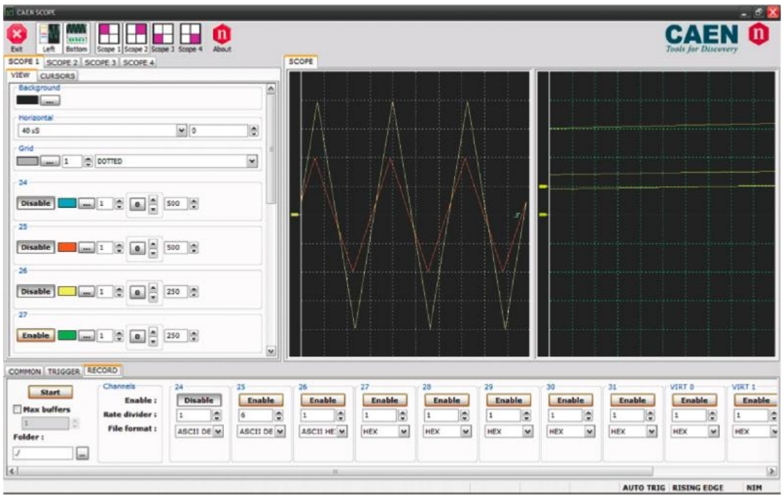

Fig. 4.3: CAENScope oscilloscope tab

- **CAENUpgrader** is a software composed of command line tools together with a Java Graphical User Interface (for Windows and Linux OS). CAENUpgrader allows in few easy steps to upload different firmware versions on CAEN boards, to upgrade the VME digitizers PLL, to get board information and to manage the firmware license. CAENUpgrader requires the installation of 2 CAEN libraries (CAENComm, CAENVMELib) and Java SE6 (or later). CAENComm allows CAENUpgrader to access target boards via USB or via CAEN proprietary CONET optical link.

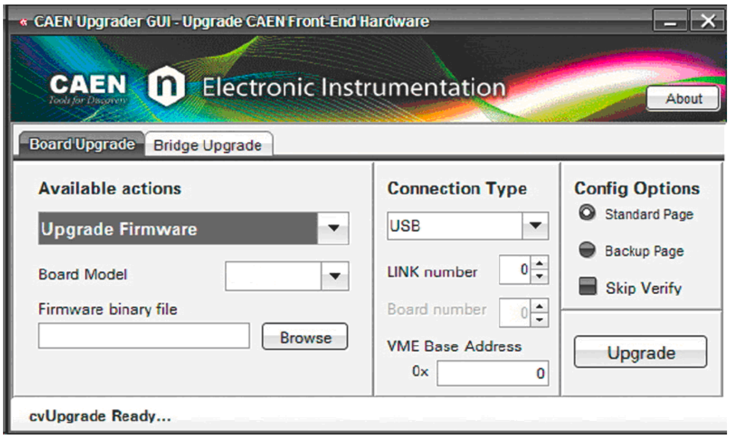

Fig. 4.4: CAENUpgrader Graphical User Interface

- **DPP Control Software** is an application that manages the acquisition in the digitizers which have DPP firmware installed on it. The program is made of different parts: there is a GUI whose purpose is to set all the parameters for the DPP and for the acquisition; the GUI generates a textual configuration file that contains all the parameters. This file is read by the Acquisition Engine (**DPPrunner)**, which is a C console application that programs the digitizer according to the parameters, starts the acquisition and manage the data readout. The data, that can be waveforms, time stamps, energies or other quantities of interest, can be saved to output files or plotted using gnuplot as an external plotting tool, exactly like in WaveDump. <u>**NOTE:** so far DPP Control Software is developed for 720, 724, 730 and 751 digitizer series.</u>

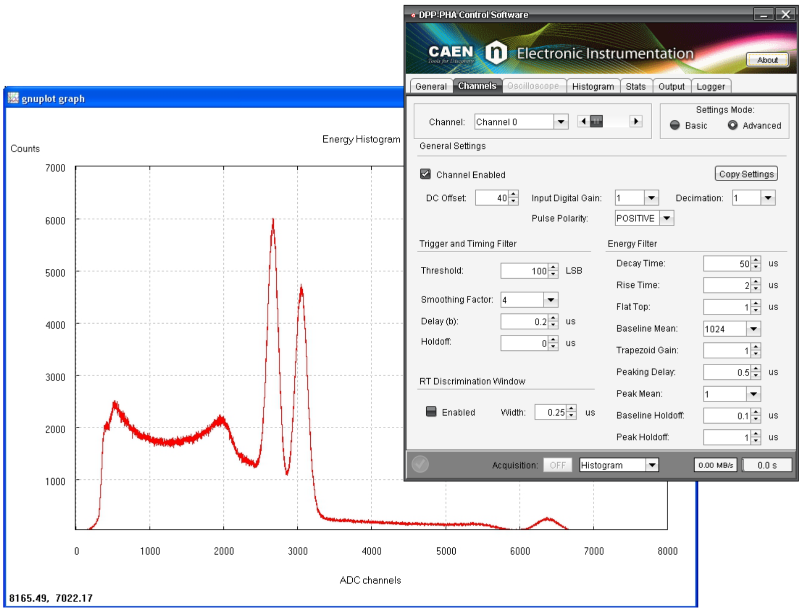

Fig. 4.5: DPP Control Software Graphical User Interface and Energy plot

5. Installation

5.1. Power ON sequence

To power ON the board follow this procedure:

1. connect the 12V dc power supply to the DT5751
2. power up the DT5751

5.2. Power ON status

At power ON the module is in the following status:

- the Output Buffer is cleared;
- registers are set to their default configuration

5.3. Firmware upgrade

The DT5751 firmware is stored onto on-board FLASH memory. Two copies of the firmware are stored in two different pages of the FLASH, called Standard (STD) and Backup (BKP); at power on, a microcontroller reads the Flash memory and programs the module with the firmware version that is the STD one by default.
CAEN provides the DeskBoot software utility in case the firmware version from the BKP page of the Flash Memory needs to be loaded. For instructions to use the program, please refer to the document:

GD2812 - DeskBoot QuickStart Guide (web available)

It is possible to upgarde the board firmware via USB or Optical Link by writing the FLASH with the CAENUpgrader software (see § 4). For instructions to use the program, please refer to the document:

GD2512 - CAENUpgrader QuickStart Guide (web available)

It is strongly suggested to upgrade ONLY one of the stored firmware revisions (generally the STD one): if both revision are simultaneously updated and a failure occurs, it will not be possible to upload the firmware via USB or Optical Link again!

5.3.1. DT5751 Upgrade files description

The board hosts one FPGA on the mainboard and one FPGA on each mezzanine (i.e. one FPGA per couple of adiacent channels). The channel FPGAs firmware is identical. A unique file is provided that will updated all the FPGA at the same time.

ROC FPGA MAINBOARD FPGA (Readout Controller + VME interface):

FPGA Altera Cyclone EP1C20.

AMC FPGA CHANNEL FPGA (ADC readout/Memory Controller):

FPGA Altera Cyclone EP3C16.

The programming file has the extension .CFA (CAEN Firmware Archive) and is a sort of archive format file aggregating all the standard firmware files compatible with the same family of digitizers.

CFA and its name follows this general scheme:

x751_revX.Y_W.Z.CFA

where:

- x751 are all the boards the file is compliant to: DT5751, N6751, V1751, VX1751
- X.Y is the major/minor revision number of the mainboard FPGA
- W.Z is the major/minor revision number of the channel FPGA

WARNING: in case of programming failures that compromise the communication with the board, a first recovering attempt can be performed by the help of DeskBoot utility (refer to the program documention as in § 5.3).

If the problem still remains, please contact CAEN technical support (see § 6) for further instructions.

5.4. Drivers

DT5751 needs CAEN USB driver to be installed in order to use the USB communication channel:

- **Download** the driver package compliant to your Operating System (Windows or Linux) on CAEN web site in the ‘Software/Firmware’ area at the digitizer page.
- **Uncompress** the package to your host.
- **For Windows users:**
  - **Installer option:** with the hardware not connected, run the single installer file and complete the installation Wizard. Then, connect the hardware and the driver will be automatically find by the OS.
  - **Driver files option:** connect the hardware; then, perform the driver installation by pointing Windows to the folder where driver files have been extracted.
- **For Linux users:** follow the installation instructions inside the README file in the package.

NOTE: for a detailed procedure in Windows OSs, please refer to the document:

GD2783 - First Installation Guide to Desktop Digitizers & MCA (web available).

Concerning the OPTICAL LINK communication channel, please refer to A2818 PCI card or A3818 PCIe cards User Manual for driver installation.

6. Technical support

CAEN support services are available for the user by accessing the *Support & Services* area on CAEN website at www.caen.it.

6.1. Returns and Repairs

Users who need for product(s) return and repair have to fill and send the Product Return Form (PRF) in the Returns and Repairs area at *Home / Support & Services*, describing the specific failure. A printed copy of the PRF must also be included in the package to be shipped.

Contacts for shipping are reported on the website at *Home / Contacts*.

6.2. Technical Support Service

CAEN makes available the technical support of its specialists at the e-mail addresses below:

support.nuclear@caen.it
(for questions about the hardware)

support.computing@caen.it
(for questions about software and libraries)