DT5751
Registers
Description

29 April 2013

MOD. DT5751
2-4 CHANNEL 10 BIT
2-1GS/S DIGITIZER

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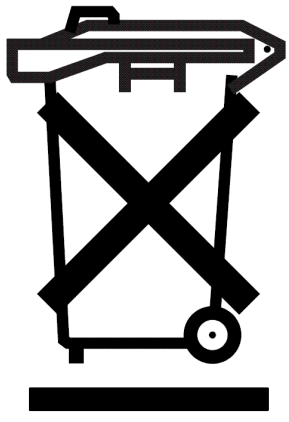
CAEN reserves the right to change partially or entirely the contents of this Manual at any time and without giving any notice.

Disposal of the Product

The product must never be dumped in the Municipal Waste. Please check your local regulations for disposal of electronics products.



MADE IN ITALY : We stress the fact that all the boards are made in Italy because in this globalized world, where getting the lowest possible price for products sometimes translates into poor pay and working conditions for the people who make them, at least you know that who made your board was reasonably paid and worked in a safe environment. (this obviously applies only to the boards marked "MADE IN ITALY", we can not attest to the manufacturing process of "third party" boards).

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1. Important Notices

The content of this document has been extracted from:

DT5751 User Manual – Revision N. 8 – Date: 26 November, 2011

FOR RELEASES OF THE ROC FPGA FIRMWARE HIGHER THAN 3.8 THE CONTENT OF THIS DOCUMENT MAY RESULT NOT FULLY COMPLIANT.

IT IS INTENDED TO BE REPLACED BY A NEW DOCUMENT UNIFYING THE REGISTERS DESCRIPTIONS OF CAEN DIGITIZERS CURRENTLY IN PROGRESS.

2. Board internal registers

The following sections will describe in detail the registers (accessible via software in D32 mode) content.

⚠ N.B.: bit fields that are not described in the register bit map are reserved and must not be over written by the User.

2.1. Registers address map

Table 2.1: Address Map for the Model DT5751

REGISTER NAME	ADDRESS	MODE	H_RES	S_RES	CLR
EVENT READOUT BUFFER	0x0000-0x0FFC	R	X	X	X
Channel n THRESHOLD	0x1n80	R/W	X	X	
Channel n STATUS	0x1n88	R	X	X	
Channel n AMC FPGA FIRMWARE REVISION	0x1n8C	R			
Channel n BUFFER OCCUPANCY	0x1n94	R	X	X	X
Channel n DAC	0x1n98	R/W	X	X	
Channel n ADC CONFIGURATION	0x1n9C	R/W	X	X	
Channel n TEMPERATURE MONITOR	0x1nA8	R/W	X	X	
CHANNEL CONFIGURATION	0x8000	R/W	X	X	
CHANNEL CONFIGURATION BIT SET	0x8004	W	X	X	
CHANNEL CONFIGURATION BIT CLEAR	0x8008	W	X	X	
BUFFER ORGANIZATION	0x800C	R/W	X	X	
BUFFER FREE	0x8010	R/W			
CUSTOM SIZE	0x8020	R/W	X	X	
BROADCAST ADC CONFIGURATION	0x809C	R/W	X	X	
ACQUISITION CONTROL	0x8100	R/W	X	X	
ACQUISITION STATUS	0x8104	R			
SW TRIGGER	0x8108	W			
TRIGGER SOURCE ENABLE MASK	0x810C	R/W	X	X	
FRONT PANEL TRIGGER OUT ENABLE MASK	0x8110	R/W	X	X	
POST TRIGGER SETTING	0x8114	R/W	X	X	
FRONT PANEL I/O CONTROL	0x811C	R/W	X	X	
CHANNEL ENABLE MASK	0x8120	R/W	X	X	
ROC FPGA FIRMWARE REVISION	0x8124	R			
EVENT STORED	0x812C	R	X	X	X
BOARD INFO	0x8140	R			
EVENT SIZE	0x814C	R	X	X	X
CONTROL	0xEF00	R/W	X		
STATUS	0xEF04	R			
INTERRUPT STATUS ID	0xEF14	R/W	X		
INTERRUPT EVENT NUMBER	0xEF18	R/W	X	X	
BLT EVENT NUMBER	0xEF1C	R/W	X	X	
SCRATCH	0xEF20	R/W	X	X	
SW RESET	0xEF24	W			
SW CLEAR	0xEF28	W			
FLASH ENABLE	0xEF2C	R/W	X		
FLASH DATA	0xEF30	R/W	X		
CONFIGURATION RELOAD	0xEF34	W			
CONFIGURATION ROM	0xF000-0xF088	R			

2.2. Configuration ROM (0xF000-0xF088; r)

The following registers contain some module's information, they are D32 accessible (read only):

- **OUI**: manufacturer identifier (IEEE OUI)
- **Version**: purchased version
- **Board ID**: Board identifier
- **Revision**: hardware revision identifier
- **Serial MSB**: serial number (MSB)
- **Serial LSB**: serial number (LSB)

Table 2.2: ROM Address Map for the Model DT5751

Description	Address	Content
checksum	0xF000	*0xA4*
checksum_length2	0xF004	0x00
checksum_length1	0xF008	0x00
checksum_length0	0xF00C	0x20
constant2	0xF010	0x83
constant1	0xF014	0x84
constant0	0xF018	0x01
c_code	0xF01C	0x43
r_code	0xF020	0x52
oui2	0xF024	0x00
oui1	0xF028	0x40
oui0	0xF02C	0xE6
vers	0xF030	0x60
board2	0xF034	0x02
board1	0xF038	0x16
board0	0xF03C	0x77
revis3	0xF040	*0x00*
revis2	0xF044	*0x00*
revis1	0xF048	*0x00*
revis0	0xF04C	*0x00*
sernum1	0xF080	
sernum0 VCXO type	0xF084 0xF088	 0x00 (AD9520-3)

These data are written into one Flash page; at Power ON the Flash content is loaded into the Configuration RAM, where it is available for readout.

2.3. Channel n Threshold (0x1n80; r/w)

Bit	Function
[9:0]	Threshold Value for Trigger Generation

Each channel can generate a local trigger as the digitized signal exceeds the Vth threshold. This register allows to set Vth (LSB=input range/10bit).

2.4. Channel n Status (0x1n88; r)

Bit	Function
[8]	Over temperature flag 0 = Ch temperature OK 1 = Ch Over temperature
[7]	Power down flag 0 = Ch Power OK 1 = Ch Power Down
[6]	Calibrating: 1 = calibration done 0 = calibration in progress
[5]	Buffer free error: 1 = trying to free a number of buffers too large
[3,4]	reserved
[2]	Channel n DAC Channel n DAC / ADC bus Busy (see § 2.7) 1 = Busy 0 = Ready
[1]	Memory empty
[0]	Memory full

2.5. Channel n AMC FPGA Firmware (0x1n8C; r)

Bit	Function
[31:16]	Revision date in Y/M/DD format
[15:8]	Firmware Revision (X)
[7:0]	Firmware Revision (Y)

Bits [31:16] contain the Revision date in Y/M/DD format.
Bits [15:0] contain the firmware revision number coded on 16 bit (X.Y format).
Example: revision 1.3 of 12th June 2007 is: 0x7612103

2.6. Channel n Buffer Occupancy (0x1n94; r)

Bit	Function
[10:0]	Occupied buffers (0..1024)

2.7. Channel n DAC (0x1n98; r/w)

Bit	Function
[15:0]	DAC Data

Bits [15:0] allow to define a DC offset to be added the input signal in the ±0.5V range. When Channel n Status bit 2 is set to 0, DC offset is updated (see § 2.4).

2.8. Channel n ADC Configuration (0x1n9C; w)

Bit	Function
[1]	Calibration
[0]	Power Down configuration 0 = Ch Power OK 1 = Ch Power Down

This register allows to pilot the relevant ADC signal.

2.9. Channel n Temperature Monitor (0x1nA8; r)

Bit	Function
[7:0]	Monitored Temperature (°C)

These registers allow to monitor the temperature of ADC chips; since each ADC houses two channels (0-1, 2-3. 4-5, 6-7) these registers provide identical values in pairs.

2.10. Channel Configuration (0x8000; r/w)

Bit	Function
[12]	0 = 1 GS/s rate 1 = 2 GS/s rate (D*ual Edge Sampling*)
[11:7]	reserved
[6]	0 = Trigger Output on Input Over Threshold 1 = Trigger Output on Input Under Threshold allows to generate local trigger either on channel over or under threshold (see § 2.3)
[5]	reserved
[4]	0 = Memory Random Access 1 = Memory Sequential Access
[3]	0 = Test Pattern Generation Disabled 1 = Test Pattern Generation Enabled
[2]	reserved
[1]	0 = Trigger Overlapping Not Enabled 1 = Trigger Overlapping Enabled Allows to handle trigger overlap
[0]	reserved

This register allows to perform settings which apply to all channels.
It is possible to perform selective set/clear of the Channel Configuration register bits writing to 1 the corresponding set and clear bit at address 0x8004 (set) or 0x8008 (clear) see the following § 2.11 and 2.12. Default value is 0x10.

2.11. Channel Configuration Bit Set (0x8004; w)

Bit	Function
[12:0]	Bits set to 1 means that the corresponding bits in the Channel Configuration register are set to 1.

2.12. Channel Configuration Bit Clear (0x8008; w)

Bit	Function
[12:0]	Bits set to 1 means that the corresponding bits in the Channel Configuration register are set to 0.

2.13. Buffer Organization (0x800C; r/w)

Bit	Function
[3:0]	BUFFER CODE

The BUFFER CODE allows to divide the available Output Buffer Memory into a certain number of blocks.
A write access to this register causes a Software Clear, see § 2.36. This register must not be written while acquisition is running.

2.14. Buffer Free (0x8010; r/w)

Bit	Function
[11:0]	N = Frees the first N Output Buffer Memory Blocks, see § 2.13

2.15. Custom Size (0x8020; r/w)

Bit	Function
[31:0]	0= Custom Size disabled N_{LOC} (≠0) = Number of memory locations per event (1 location = 7 samples @ 1GS/s; 14 samples @ 2GS/s)

This register must not be written while acquisition is running.

2.16. Broadcast ADC Configuration (0x809C; w)

Bit	Function
[1]	Calibration
[0]	Power Down; must always be 0

This register allows to pilot all the relevant ADC signal.

2.17. Acquisition Control (0x8100; r/w)

Bit	Function
[3]	0 = COUNT ACCEPTED TRIGGERS 1 = COUNT ALL TRIGGERS allows to reject overlapping triggers
[2]	0 = Acquisition STOP 1 = Acquisition RUN allows to RUN/STOP Acquisition
[1]	Reserved (set to 0)
[0]	0 = REGISTER-CONTROLLED RUN MODE 1 = GPI CONTROLLED RUN MODE

Bit [2] allows to Run and Stop data acquisition; when such bit is set to 1 the board enters Run mode and a Memory Reset is automatically performed. When bit [2] is reset to 0 the stored data are kept available for readout. In Stop Mode all triggers are neglected.
Bit [0] descritpion:
0 = REGISTER-CONTROLLED RUN MODE: multiboard synchronisation via GPI front panel signal
- RUN control: start/stop via set/clear of bit[2]
- GATE always active (Continuous Gate Mode)

1 = GPI CONTROLLED RUN MODE: Multiboard synchronisation via GPI front panel signal
- GPI works both as SYNC and RUN_START command
- GATE always active (Continuous Gate Mode)

2.18. Acquisition Status (0x8104; r)

Bit	Function
[8]	Board ready for acquisition (PLL and ADCs are synchronised correctly) 0 = not ready 1 = ready This bit should be checked after software reset to ensure that the board will enter immediatly run mode after RUN mode setting; otherwise a latency between RUN mode setting and Acquisition start might occur.
[7]	PLL Status Flag: 0 = PLL loss of lock 1 = no PLL loss of lock NOTE: flag can be restored to 1 via read access to Status Register
[6]	PLL Bypass mode: 0 = No bypass mode 1 = Bypass mode
[5]	Clock source: 0 = Internal 1 = External
[4]	EVENT FULL: it is set to 1 as the maximum nr. of events to be read is reached
[3]	EVENT READY: it is set to 1 as at least one event is available to readout
[2]	0 = RUN off 1 = RUN on
[1:0]	*reserved*

2.19. Software Trigger (0x8108; w)

Bit	Function
[31:0]	A write access to this location generates a trigger via software

2.20. Trigger Source Enable Mask (0x810C; r/w)

Bit	Function
[31]	0 = Software Trigger Disabled 1 = Software Trigger Enabled
[30]	0 = External Trigger Disabled 1 = External Trigger Enabled
[29:27]	*reserved*
[26:24]	Local trigger coincidence level (default = 0)
[23:4]	*reserved*
[3]	0 = Channel 3 trigger disabled 1 = Channel 3 trigger enabled
[2]	0 = Channel 2 trigger disabled 1 = Channel 2 trigger enabled
[1]	0 = Channel 1 trigger disabled 1 = Channel 1 trigger enabled
[0]	0 = Channel 0 trigger disabled 1 = Channel 0 trigger enabled

This register bits[0,3] enable the channels to generate a local trigger as the digitised signal exceeds the Vth threshold. Bit0 enables Ch0 to generate the trigger, bit1 enables Ch1 to generate the trigger and so on.
Bits [26:24] allows to set minimum number of channels that must be over threshold, beyond the triggering channel, in order to actually generate the local trigger signal; for example if bit[3:0]=F (all channels enabled) and Local trigger coincidence level = 1, whenever one channel exceeds the threshold, the trigger will be generated only if at least another channel is over threshold at that moment. Local trigger coincidence level must be smaller than the number of channels enabled via bit[3:0] mask.
EXTERNAL TRIGGER ENABLE (bit30) enables the board to sense TRG-IN signals
SW TRIGGER ENABLE (bit 31) enables the board to sense software trigger (see § 2.19).

2.21. Front Panel Trigger Out Enable Mask (0x8110; r/w)

Bit	Function
[31]	0 = Software Trigger Disabled 1 = Software Trigger Enabled
[30]	0 = External Trigger Disabled 1 = External Trigger Enabled
[29:4]	*reserved*
[3]	0 = Channel 3 trigger disabled 1 = Channel 3 trigger enabled
[2]	0 = Channel 2 trigger disabled 1 = Channel 2 trigger enabled
[1]	0 = Channel 1 trigger disabled 1 = Channel 1 trigger enabled
[0]	0 = Channel 0 trigger disabled 1 = Channel 0 trigger enabled

This register bits[0,3] enable the channels to generate a TRG_OUT front panel signal on GPO output as the digitised signal exceeds the Vth threshold.
Bit0 enables Ch0 to generate the TRG_OUT, bit1 enables Ch1 to generate the TRG_OUT and so on.
EXTERNAL TRIGGER ENABLE (bit30) enables the board to generate the TRG_OUT
SW TRIGGER ENABLE (bit 31) enables the board to generate TRG_OUT (see § 2.19).

2.22. Post Trigger Setting (0x8114; r/w)

Bit	Function
[31:0]	Post trigger value

The register value sets the number of post trigger samples. The number of post trigger samples is

$N_S=[(N_{PV} + N_{DEL}) \cdot 16 \pm 15]$

This formula becomes $N_S= 2 \cdot [(N_{PV} + N_{DEL}) \cdot 16 \pm 15]$ in DES mode

N_S = number of post trigger samples.

N_{PV} = PostTriggerValue = Content of this register.

N_{DEL} = ConstantLatency = constant number of samples added due to the latency associated to the trigger processing logic in the ROC FPGA; N_{DEL} is 4 with external trigger and 8 with internal trigger.

2.23. Front Panel I/O Control (0x811C; r/w)

Bit	Function
[15:2]	*reserved*
[1]	0= panel output signals (GPO) enabled 1= panel output signals (GPO) enabled in high impedance
[0]	0 = GPI/GPO/TRG-IN are NIM I/O Levels 1 = GPI/GPO/TRG-IN are TTL I/O Levels

2.24. Channel Enable Mask (0x8120; r/w)

Bit	Function
[7:4]	*reserved*
[3]	0 = Channel 3 disabled 1 = Channel 3 enabled
[2]	0 = Channel 2 disabled 1 = Channel 2 enabled
[1]	0 = Channel 1 disabled 1 = Channel 1 enabled
[0]	0 = Channel 0 disabled 1 = Channel 0 enabled

Enabled channels provide the samples which are stored into the events (and not erased). The mask cannot be changed while acquisition is running.

2.25. ROC FPGA Firmware Revision (0x8124; r)

Bit	Function
[31:16]	Revision date in Y/M/DD format
[15:8]	Firmware Revision (X)
[7:0]	Firmware Revision (Y)

Bits [31:16] contain the Revision date in Y/M/DD format.

Bits [15:0] contain the firmware revision number coded on 16 bit (X.Y format).

2.26. Event Stored (0x812C; r)

Bit	Function
[31:0]	This register contains the number of events currently stored in the Output Buffer

This register value cannot exceed the maximum number of available buffers according to setting of buffer size register.

2.27. Board Info (0x8140; r)

Bit	Function
[23:16]	Number of channels (DT5751: 0x04)
[15:8]	Memory size code (DT5751: 0x02)
[7:0]	Board Type (DT5751: 0x05)

2.28. Event Size (0x814C; r)

Bit	Function
[31:0]	Nr. of 32 bit words in the next event

2.29. Control (0xEF00; r/w)

Bit	Function
[7]	Reserved; must be set to 0, Release On Register Access (RORA) Interrupt mode
[6]	Reserved, must be set to 0
[5]	Reserved, must be set to 0
[4]	Reserved, must be set to 1
[3]	0 = interrupt disabled 1 = interrupt enabled
[2,1]	Reserved
[0]	Reserved (must be set to 0)

Interrupt request can be removed by accessing this register and disabling the active interrupt level

2.30. Status (0xEF04; r)

Bit	Function
[2]	0 = Slave Terminated Transfer Flag: no terminated transfer 1 = Slave Terminated Transfer Flag: one transfer has been terminated by DT5751 (unsupported register access or block transfer prematurely terminated in event aligned reaout)
[1]	0 = The Output Buffer is not FULL; 1 = The Output Buffer is FULL.
[0]	0 = No Data Ready; 1 = Event Ready

2.31. Interrupt Status ID (0xEF14; r/w)

Bit	Function
[31..0]	This register contains the STATUS/ID that the module places on the data stream during the Interrupt Acknowledge cycle

2.32. Interrupt Event Number (0xEF18; r/w)

Bit	Function
[9:0]	INTERRUPT EVENT NUMBER

If interrupts are enabled, the module generates a request whenever it has stored in memory a Number of events > INTERRUPT EVENT NUMBER

2.33. Block Transfer Event Number (0xEF1C; r/w)

Bit	Function
[15:0]	This register contains the number of complete events which has to be transferred via Block Transfer.

2.34. Scratch (0xEF20; r/w)

Bit	Function
[31:0]	Scratch (*to be used to write/read words for test purposes*)

2.35. Software Reset (0xEF24; w)

Bit	Function
[31:0]	A write access to this location allows to perform a software reset

2.36. Software Clear (0xEF28; w)

Bit	Function
[31:0]	A write access to this location clears all the memories

2.37. Flash Enable (0xEF2C; r/w)

Bit	Function
[0]	Reserved for Firmware upgrade tool

2.38. Flash Data (0xEF30; r/w)

Bit	Function
[7:0]	Data to be serialized towards the SPI On board Flash

This register is handled by the Firmware upgrade tool.

2.39. Configuration Reload (0xEF34; w)

Bit	Function
[31:0]	A write access to this register causes a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.