

## 16-CHANNEL CONSTANT-CURRENT LED SINK DRIVERS

### FEATURES

- 16 Constant-Current Output Channels
- Output Current Adjusted By External Resistor
- Constant Output Current Range: 5 mA to 120 mA
- Constant Output Current Invariant to Load Voltage Change
- Open-Load, Shorted-Load and Overtemperature Detection
- 256-Step Programmable Global Current Gain
- Excellent Output-Current Accuracy:
  - Between Channels:  $< \pm 6\%$  (Max), 10 mA to 50 mA
  - Between ICs:  $< \pm 6\%$  (Max), 10 mA to 50 mA
- 30-MHz Clock Frequency
- Schmitt-Trigger Input
- 3.3-V or 5-V Supply Voltage
- Thermal Shutdown for Overtemperature Protection
- ESD Performance: 2-kV HBM

### APPLICATIONS

- General LED Lighting Applications
- LED Display Systems
- LED Signage
- Automotive LED Lighting
- White Goods

### DESCRIPTION/ORDERING INFORMATION

The TLC5926/TLC5927 is designed for LED displays and LED lighting applications with open-load, shorted-load, and overtemperature detection, and constant-current control. The TLC5926/TLC5927 contains a 16-bit shift register and data latches, which convert serial input data into parallel output format. At the TLC5926/TLC5927 output stage, 16 regulated-current ports provide uniform and constant current for driving LEDs within a wide range of  $V_F$  (Forward Voltage) variations. Used in systems designed for LED display applications (e.g., LED panels), TLC5926/TLC5927 provides great flexibility and device performance. Users can adjust the output current from 5 mA to 120 mA through an external resistor,  $R_{ext}$ , which gives flexibility in controlling the light intensity of LEDs. TLC5926/TLC5927 is designed for up to 17 V at the output port. The high clock frequency, 30 MHz, also satisfies the system requirements of high-volume data transmission.

The TLC5926/TLC5927 provides a Special Mode in which two functions are included, Error Detection and Current Gain Control. In the TLC5926/TLC5927 there are two operation modes and three phases: Normal Mode phase, Mode Switching transition phase, and Special mode phase. The signal on the multiple-function pin  $\overline{OE}(ED2)$  is monitored, and when an one-clock-wide short pulse appears on  $\overline{OE}(ED2)$ , TLC5926/TLC5927 enters the Mode Switching phase. At this time, the voltage level on  $LE(ED1)$  determines the next mode into which the TLC5926/TLC5927 switches.

In the Normal Mode phase, the serial data is transferred into TLC5926/TLC5927 via SDI, shifted in the shift register, and transferred out via SDO.  $LE(ED1)$  can latch the serial data in the shift register to the output latch.  $\overline{OE}(ED2)$  enables the output drivers to sink current.

In the Special Mode phase, the low-voltage-level signal  $\overline{OE}(ED2)$  can enable output channels and detect the status of the output current, to tell if the driving current level is enough or not. The detected error status is loaded into the 16-bit shift register and shifted out via SDO, along with the CLK signal. The system controller can read the error status to determine whether or not the LEDs are properly lit. In the Special Mode phase, TLC5926/TLC5927 also allows users to adjust the output current level by setting a runtime-programmable Configuration Code. The code is sent into TLC5926/TLC5927 via SDI. The positive pulse of  $LE(ED1)$  latches the code in the shift register into a built-in 8-bit configuration latch, instead of the output latch. The code affects the voltage at  $R_{EXT}$  and controls the output-current regulator. The output current can be adjusted finely by a gain ranging from 1/12 to 127/128 in 256 steps. Therefore, the current skew between ICs can be compensated within less than 1%, and this feature is suitable for white balancing in LED color-display panels.



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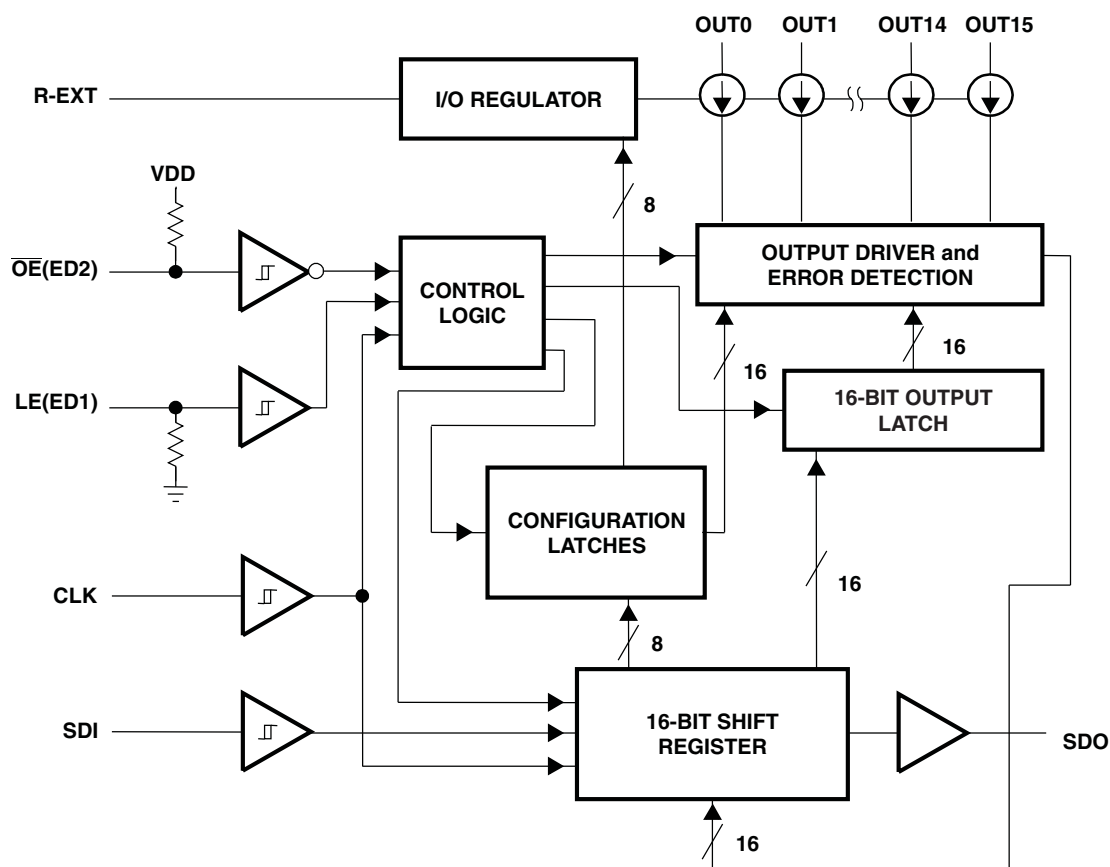
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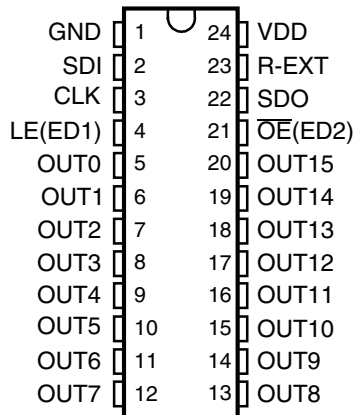
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**ORDERING INFORMATION<sup>(1)</sup>**

T <sub>A</sub>	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PowerPAD™ – PWP	Reel of 2000	TLC5926IPWPR	Y5926
			TLC5927IPWPR	Y5927
	W-SOIC – DW	Reel of 2000	TLC5926IDWR	TLC5926I
			TLC5927IDWR	TLC5927I
	SSOP – DBQ	Reel of 2000	TLC5926IDBQR	TLC5926I
			TLC5927IDBQR	TLC5927I

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

**BLOCK DIAGRAM**

**DBQ, DW, OR PWP PACKAGE  
(TOP VIEW)**

**Pin Descriptions**

PIN NAME	DESCRIPTION
CLK	Clock input pin for data shift on rising edge
GND	Ground pin for control logic and current sink
LE(ED1)	Data strobe input pin Serial data is transferred to the respective latch when LE(ED1) is high. The data is latched when LE(ED1) goes low. Also, a control signal input for an Error Detection mode and Current Adjust mode (See Timing Diagram). LE(ED1) has an internal pulldown.
$\overline{OE}(ED2)$	Output enable pin. When $\overline{OE}(ED2)$ (active) is low, the output drivers are enabled; when $\overline{OE}(ED2)$ is high, all output drivers are turned OFF (blanked). Also, a control signal input for an Error Detection mode and Current Adjust mode (See Timing Diagram). $\overline{OE}(ED2)$ has an internal pull-up.
OUT0–OUT15	Constant-current output pins
R-EXT	Input pin used to connect an external resistor for setting up all output currents
SDI	Serial-data input to the Shift register
SDO	Serial-data output to the following SDI of next driver IC or to the microcontroller
VDD	Supply voltage pin

**Diagnostic Features**

DEVICE <sup>(1)</sup>	OPEN-LOAD DETECTION	SHORT TO GND DETECTION	SHORT TO V <sub>LED</sub> DETECTION
TLC5926	x	x	
TLC5927	x	x	x

(1) The device has one single error register for all these conditions (one error bit per channel)

## Timing Diagrams

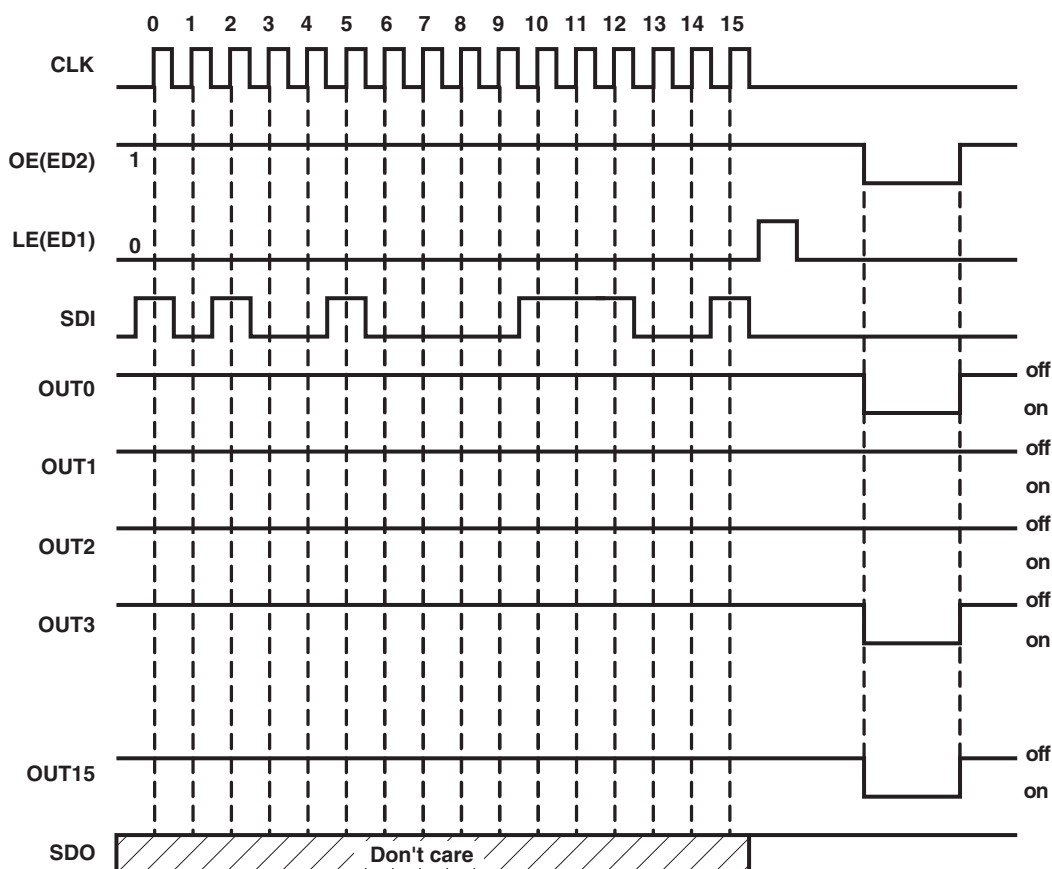


Figure 1. Normal Mode

Truth Table in Normal Mode

CLK	LE(ED1)	$\overline{OE}$ (ED2)	SDI	OUT0...OUT15	SDO
↑	H	L	Dn	Dn...Dn – 7...Dn – 15	Dn – 15
↑	L	L	Dn + 1	No change	Dn – 14
↑	H	L	Dn + 2	Dn + 2...Dn – 5...Dn – 13	Dn – 13
↓	X	L	Dn + 3	Dn + 2...Dn – 5...Dn – 13	Dn – 13
↓	X	H	Dn + 3	off	Dn – 13

The signal sequence shown in [Figure 2](#) makes the TLC5926/TLC5927 enter Current Adjust and Error Detection mode.

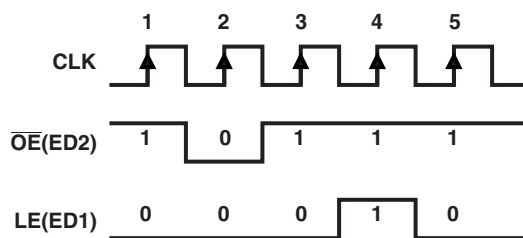
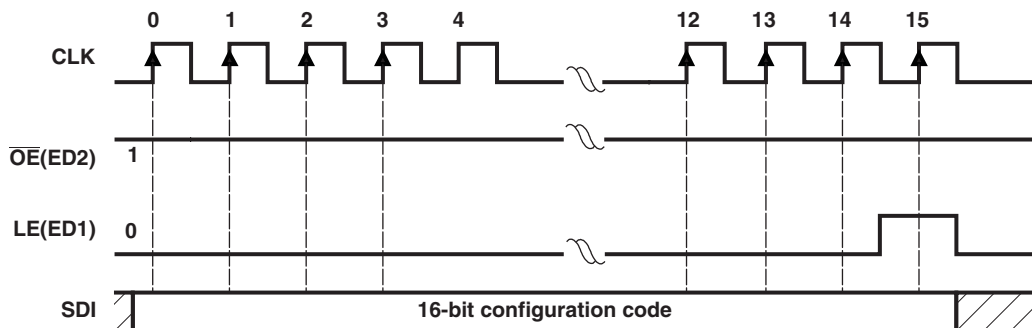


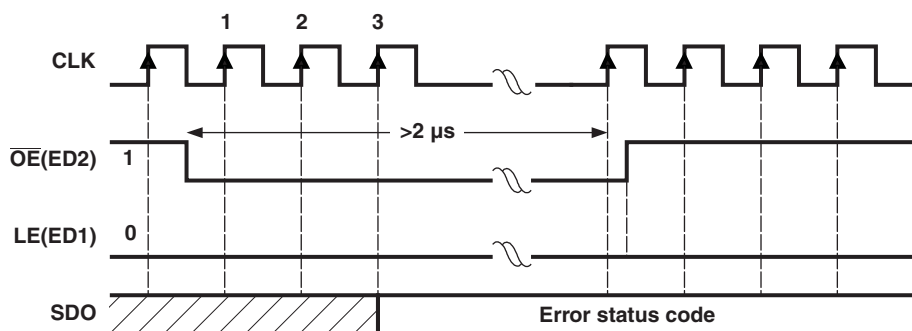
Figure 2. Switching to Special Mode

In the Current Adjust mode, sending the positive pulse of LE(ED1), the content of the shift register (a current adjust code) is written to the 16-bit configuration latch (see Figure 3).



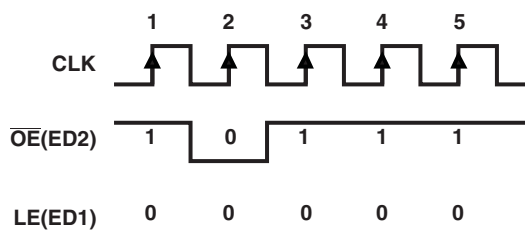
**Figure 3. Writing Configuration Code**

When the TLC5926/TLC5927 is in the error detection mode, the signal sequence shown in Figure 4 enables a system controller to read error status codes through SDO.



**Figure 4. Reading Error Status Code**

The signal sequence shown in Figure 5 makes TLC5926/TLC5927 resume the Normal mode. Switching to Normal mode resets all internal Error Status registers. OE (ED2) always enables the output port, whether the TLC5926/TLC5927 enters current adjust mode or not.



**Figure 5. Switching to Normal Mode**

## Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{DD}$	Supply voltage	0	7	V
$V_I$	Input voltage	−0.4	$V_{DD} + 0.4$	V
$V_O$	Output voltage	−0.5	20	V
$I_{OUT}$	Output current		120	mA
$I_{GND}$	GND terminal current		1920	mA
$T_A$	Free-air operating temperature range	−40	85	°C
$T_J$	Operating junction temperature range	−40	150	°C
$T_{stg}$	Storage temperature range	−55	150	°C
ESD	Electrostatic-Discharge Capability $V_{(HBMESD)}$ (100 pF, 1.5 kΩ)		2	kV

## Power Dissipation and Thermal Impedance

			MIN	MAX	UNIT
$P_D$	Power dissipation	DBQ package		1.6	W
		Mounted on JEDEC 4-layer board (JESD 51-7), No airflow, $T_A = 25^\circ\text{C}$ , $T_J = 125^\circ\text{C}$		2.2	
		DW package		2.3	
		PWP package		2.9	
$\theta_{JA}$	Thermal impedance, junction to free air	Mounted on JEDEC 4-layer board (JESD 51-5), No airflow, $T_A = 25^\circ\text{C}$ , $T_J = 125^\circ\text{C}$		2.9	°C/W
		DBQ package		99.8	
		Mounted on JEDEC 1-layer board (JESD 51-3), No airflow		80.5	
		DW package		63.9	
		PWP package		61.0	
		Mounted on JEDEC 4-layer board (JESD 51-7), No airflow		45.5	
		DW package		42.7	
		PWP package		34.5	
$\theta_{JP}$	Thermal impedance, junction to pad	PWP package		2.0	°C/W

## Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		TEST CONDITIONS	MIN	MAX	UNIT
$V_{DD}$	Supply voltage		3	5.5	V
$V_O$	Supply voltage to the output pins	OUT0–OUT15		17	V
$I_O$	Output current	DC test circuit	$V_O \geq 0.6\text{ V}$	5	mA
			$V_O \geq 1\text{ V}$	120	
$I_{OH}$	High-level output current	SDO		−1	mA
$I_{OL}$	Low-level output current	SDO		1	mA
$V_{IH}$	High-level input voltage	CLK, $\overline{OE}$ (ED2), LE(ED1), and SDI	$0.7 \times V_{DD}$	$V_{DD}$	V
$V_{IL}$	Low-level input voltage	CLK, $\overline{OE}$ (ED2), LE(ED1), and SDI	0	$0.3 \times V_{DD}$	V

## Recommended Timing

 $V_{DD} = 3\text{ V to }5.5\text{ V}$  (unless otherwise noted)

		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(L)}$	LE(ED1) pulse duration	Normal mode	20		ns
$t_{w(CLK)}$	CLK pulse duration	Normal mode	20		ns
$t_{w(OE)}$	$\overline{OE}$ (ED2) pulse duration	Normal mode	1000		ns
$t_{su(D)}$	Setup time for SDI	Normal mode	7		ns
$t_{h(D)}$	Hold time for SDI	Normal mode	3		ns
$t_{su(L)}$	Setup time for LE(ED1)	Normal mode	18		ns
$t_{h(L)}$	Hold time for LE(ED1)	Normal mode	18		ns
$t_{w(CLK)}$	CLK pulse duration	Error Detection mode	20		ns
$t_{w(ED2)}$	$\overline{OE}$ (ED2) pulse duration	Error Detection mode	2000		ns
$t_{su(ED1)}$	Setup time for LE(ED1)	Error Detection mode	7		ns
$t_{h(ED1)}$	Hold time for LE(ED1)	Error Detection mode	10		ns
$t_{su(ED2)}$	Setup time for $\overline{OE}$ (ED2)	Error Detection mode	7		ns
$t_{h(ED2)}$	Hold time for $\overline{OE}$ (ED2)	Error Detection mode	10		ns
$f_{CLK}$	Clock frequency	Cascade operation, $V_{DD} = 3\text{ V to }5.5\text{ V}$		30	MHz

## Electrical Characteristics

$V_{DD} = 3\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_O$	Supply voltage to the output pins				17	V
$I_O$	Output current	$V_O \geq 0.6\text{ V}$	5			mA
		$V_O \geq 1\text{ V}$			120	
$V_{IH}$	High-level input voltage		$0.7 \times V_{DD}$		$V_{DD}$	V
$V_{IL}$	Low-level input voltage		GND		$0.3 \times V_{DD}$	
$I_{leak}$	Output leakage current	$V_{OH} = 17\text{ V}$	$T_J = 25^\circ\text{C}$		0.5	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		1	
$V_{OH}$	High-level output voltage	SDO, $I_{OL} = -1\text{ mA}$	$V_{DD} - 0.4$			V
$V_{OL}$	Low-level output voltage	SDO, $I_{OH} = 1\text{ mA}$			0.4	V
$I_{O(1)}$	Output current 1	$V_{OUT} = 0.6\text{ V}$ , $R_{ext} = 720\ \Omega$ , CG = 0.992		26		mA
	Output current error, die-die	$I_{OL} = 26\text{ mA}$ , $V_O = 0.6\text{ V}$ , $R_{ext} = 720\ \Omega$ , $T_J = 25^\circ\text{C}$			$\pm 6$	%
	Output current error, channel-to-channel	$I_{OL} = 26\text{ mA}$ , $V_O = 0.6\text{ V}$ , $R_{ext} = 720\ \Omega$ , $T_J = 25^\circ\text{C}$			$\pm 6$	%
$I_{O(2)}$	Output current 2	$V_O = 0.8\text{ V}$ , $R_{ext} = 360\ \Omega$ , CG = 0.992		52		mA
	Output current error, die-die	$I_{OL} = 52\text{ mA}$ , $V_O = 0.8\text{ V}$ , $R_{ext} = 360\ \Omega$ , $T_J = 25^\circ\text{C}$			$\pm 6$	%
	Output current error, channel-to-channel	$I_{OL} = 52\text{ mA}$ , $V_O = 0.8\text{ V}$ , $R_{ext} = 360\ \Omega$ , $T_J = 25^\circ\text{C}$			$\pm 6$	%
$I_{OUT\text{ vs }V_{OUT}}$	Output current vs output voltage regulation	$V_O = 1\text{ V}$ to $3\text{ V}$ , $I_O = 26\text{ mA}$		$\pm 0.1$		% / V
$I_{OUT\text{ vs }V_{DD}}$	Output current vs supply voltage	$V_{DD} = 3.0\text{ V}$ to $5.5\text{ V}$ , $I_O = 26\text{ mA}/120\text{ mA}$		$\pm 1$		
	Pullup resistance	$\overline{OE}$ (ED2)	250	500	800	k $\Omega$
	Pulldown resistance	LE(ED1)	250	500	800	k $\Omega$
$T_{sd}$	Overtemperature shutdown <sup>(1)</sup>		150	175	200	$^\circ\text{C}$
$T_{hys}$	Restart temperature hysteresis			15		$^\circ\text{C}$
$I_{OUT,Th}$	Threshold current for open error detection	$I_{OUT,target} = 5\text{ mA}$ to $120\text{ mA}$		$0.5 \times I_{target}$		%
$V_{OUT,TTh}$	Trigger threshold voltage for short-error detection (TLC5927 only)	$I_{OUT,target} = 5\text{ mA}$ to $120\text{ mA}$	2.4	2.6	3.1	V
$V_{OUT,RTh}$	Return threshold voltage for short-error detection (TLC5927 only)	$I_{OUT,target} = 5\text{ mA}$ to $120\text{ mA}$	2.2			V
$I_{DD}$	Supply current	OUT0–OUT15 = off, $R_{ext}$ = Open, $\overline{OE} = V_{IH}$			10	mA
		OUT0–OUT15 = off, $R_{ext} = 720\ \Omega$ , $\overline{OE} = V_{IH}$			14	
		OUT0–OUT15 = off, $R_{ext} = 360\ \Omega$ , $\overline{OE} = V_{IH}$			18	
		OUT0–OUT15 = off, $R_{ext} = 180\ \Omega$ , $\overline{OE} = V_{IH}$			20	
		OUT0–OUT15 = on, $R_{ext} = 720\ \Omega$ , $\overline{OE} = V_{IL}$			14	
		OUT0–OUT15 = on, $R_{ext} = 360\ \Omega$ , $\overline{OE} = V_{IL}$			18	
		OUT0–OUT15 = on, $R_{ext} = 180\ \Omega$ , $\overline{OE} = V_{IL}$			20	

(1) Specified by design



## Electrical Characteristics

 $V_{DD} = 5.5\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_O$	Supply voltage to the output pins				17	V
$I_O$	Output current	$V_O \geq 0.6\text{ V}$	5			mA
		$V_O \geq 1\text{ V}$			120	
$V_{IH}$	High-level input voltage		$0.7 \times V_{DD}$		$V_{DD}$	V
$V_{IL}$	Low-level input voltage		GND		$0.3 \times V_{DD}$	
$I_{leak}$	Output leakage current	$V_{OH} = 17\text{ V}$	$T_J = 25^\circ\text{C}$		0.5	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		1	
$V_{OH}$	High-level output voltage	SDO, $I_{OL} = -1\text{ mA}$	$V_{DD} - 0.4$			V
$V_{OL}$	Low-level output voltage	SDO, $I_{OH} = 1\text{ mA}$			0.4	V
$I_{O(1)}$	Output current 1	$V_{OUT} = 0.6\text{ V}$ , $R_{ext} = 720\ \Omega$ , CG = 0.992		26		mA
	Output current error, die-die	$I_{OL} = 26\text{ mA}$ , $V_O = 0.6\text{ V}$ , $R_{ext} = 720\ \Omega$ , $T_J = 25^\circ\text{C}$			$\pm 6$	%
	Output current error, channel-to-channel	$I_{OL} = 26\text{ mA}$ , $V_O = 0.6\text{ V}$ , $R_{ext} = 720\ \Omega$ , $T_J = 25^\circ\text{C}$			$\pm 6$	%
$I_{O(2)}$	Output current 2	$V_O = 0.8\text{ V}$ , $R_{ext} = 360\ \Omega$ , CG = 0.992		52		mA
	Output current error, die-die	$I_{OL} = 52\text{ mA}$ , $V_O = 0.8\text{ V}$ , $R_{ext} = 360\ \Omega$ , $T_J = 25^\circ\text{C}$			$\pm 6$	%
	Output current error, channel-to-channel	$I_{OL} = 52\text{ mA}$ , $V_O = 0.8\text{ V}$ , $R_{ext} = 360\ \Omega$ , $T_J = 25^\circ\text{C}$			$\pm 6$	%
$I_{OUT\text{ vs }V_{OUT}}$	Output current vs output voltage regulation	$V_O = 1\text{ V}$ to $3\text{ V}$ , $I_O = 26\text{ mA}$		$\pm 0.1$		% / V
$I_{OUT\text{ vs }V_{DD}}$	Output current vs supply voltage	$V_{DD} = 3.0\text{ V}$ to $5.5\text{ V}$ , $I_O = 26\text{ mA}/120\text{ mA}$		$\pm 1$		
	Pullup resistance	$\overline{OE}(ED2)$ ,	250	500	800	k $\Omega$
	Pulldown resistance	LE(ED1),	250	500	800	k $\Omega$
$T_{sd}$	Overtemperature shutdown <sup>(1)</sup>		150	175	200	$^\circ\text{C}$
$T_{hys}$	Restart temperature hysteresis			15		$^\circ\text{C}$
$I_{OUT,Th}$	Threshold current for open error detection	$I_{OUT,target} = 5\text{ mA}$ to $120\text{ mA}$		$0.5 \times I_{target}$		%
$V_{OUT,TTh}$	Trigger threshold voltage for short-error detection (TLC5927 only)	$I_{OUT,target} = 5\text{ mA}$ to $120\text{ mA}$	2.4	2.6	3.1	V
$V_{OUT,RTh}$	Return threshold voltage for short-error detection (TLC5927 only)	$I_{OUT,target} = 5\text{ mA}$ to $120\text{ mA}$	2.2			V
$I_{DD}$	Supply current	OUT0–OUT15 = off, $R_{ext} = \text{Open}$ , $\overline{OE} = V_{IH}$			11	mA
		OUT0–OUT15 = off, $R_{ext} = 720\ \Omega$ , $\overline{OE} = V_{IH}$			17	
		OUT0–OUT15 = off, $R_{ext} = 360\ \Omega$ , $\overline{OE} = V_{IH}$			18	
		OUT0–OUT15 = off, $R_{ext} = 180\ \Omega$ , $\overline{OE} = V_{IH}$			25	
		OUT0–OUT15 = on, $R_{ext} = 720\ \Omega$ , $\overline{OE} = V_{IL}$			17	
		OUT0–OUT15 = on, $R_{ext} = 360\ \Omega$ , $\overline{OE} = V_{IL}$			18	
		OUT0–OUT15 = on, $R_{ext} = 180\ \Omega$ , $\overline{OE} = V_{IL}$			25	

(1) Specified by design

## Switching Characteristics

$V_{DD} = 3\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH1}$	Low-to-high propagation delay time, CLK to OUTn	$V_{IH} = V_{DD}$ , $V_{IL} = \text{GND}$ , $R_{ext} = 360\ \Omega$ , $V_L = 4\text{ V}$ , $R_L = 44\ \Omega$ , $C_L = 70\text{ pF}$ , $CG = 0.992$	35	65	105	ns
$t_{PLH2}$	Low-to-high propagation delay time, LE(ED1) to OUTn		35	65	105	ns
$t_{PLH3}$	Low-to-high propagation delay time, $\overline{OE}(ED2)$ to OUTn		35	65	105	ns
$t_{PLH4}$	Low-to-high propagation delay time, CLK to SDO			20	45	ns
$t_{PHL1}$	High-to-low propagation delay time, CLK to OUTn		200	300	470	ns
$t_{PHL2}$	High-to-low propagation delay time, LE(ED1) to OUTn		200	300	470	ns
$t_{PHL3}$	High-to-low propagation delay time, $\overline{OE}(ED2)$ to OUTn		200	300	470	ns
$t_{PHL4}$	High-to-low propagation delay time, CLK to SDO			20	40	ns
$t_{w(CLK)}$	Pulse duration, CLK		20			ns
$t_{w(L)}$	Pulse duration LE(ED1)		20			ns
$t_{w(OE)}$	Pulse duration, $\overline{OE}(ED2)$		1000			ns
$t_{w(ED2)}$	Pulse duration, $\overline{OE}(ED2)$ in Error Detection mode		2			$\mu\text{s}$
$t_{h(ED1,ED2)}$	Hold time, LE(ED1), and $\overline{OE}(ED2)$		10			ns
$t_{h(D)}$	Hold time, SDI		5			ns
$t_{su(D,ED1,ED2)}$	Setup time, SDI, LE(ED1), and $\overline{OE}(ED2)$		7			ns
$t_{h(L)}$	Hold time, LE(ED1), Normal mode		18			ns
$t_{su(L)}$	Setup time, LE(ED1), Normal mode		18			ns
$t_r$	Rise time, CLK <sup>(1)</sup>				500	ns
$t_f$	Fall time, CLK <sup>(1)</sup>				500	ns
$t_{or}$	Rise time, outputs (off)				245	ns
$t_{of}$	Rise time, outputs (on)				600	ns
$f_{CLK}$	Clock frequency	Cascade operation			30	MHz

- (1) If the devices are connected in cascade and  $t_r$  or  $t_f$  is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

## Switching Characteristics

 $V_{DD} = 5.5\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH1}$	Low-to-high propagation delay time, CLK to OUTn	$V_{IH} = V_{DD}$ , $V_{IL} = \text{GND}$ , $R_{ext} = 360\ \Omega$ , $V_L = 4\text{ V}$ , $R_L = 44\ \Omega$ , $C_L = 70\text{ pF}$ , $CG = 0.992$	27	65	95	ns
$t_{PLH2}$	Low-to-high propagation delay time, LE(ED1) to OUTn		27	65	95	ns
$t_{PLH3}$	Low-to-high propagation delay time, $\overline{OE}(ED2)$ to OUTn		27	65	95	ns
$t_{PLH4}$	Low-to-high propagation delay time, CLK to SDO			20	30	ns
$t_{PHL1}$	High-to-low propagation delay time, CLK to OUTn		180	300	445	ns
$t_{PHL2}$	High-to-low propagation delay time, LE(ED1) to OUTn		180	300	445	ns
$t_{PHL3}$	High-to-low propagation delay time, $\overline{OE}(ED2)$ to OUTn		180	300	445	ns
$t_{PHL4}$	High-to-low propagation delay time, CLK to SDO			20	30	ns
$t_{w(CLK)}$	Pulse duration, CLK		20			ns
$t_{w(L)}$	Pulse duration LE(ED1)		20			ns
$t_{w(OE)}$	Pulse duration, $\overline{OE}(ED2)$		1000			ns
$t_{w(ED2)}$	Pulse duration, $\overline{OE}(ED2)$ in Error Detection mode		2			$\mu\text{s}$
$t_{h(ED1,ED2)}$	Hold time, LE(ED1), and $\overline{OE}(ED2)$		10			ns
$t_{h(D)}$	Hold time, SDI		3			ns
$t_{su(D,ED1,ED2)}$	Setup time, SDI, LE(ED1), and $\overline{OE}(ED2)$		4			ns
$t_{h(L)}$	Hold time, LE(ED1), Normal mode		15			ns
$t_{su(L)}$	Setup time, LE(ED1), Normal mode		15			ns
$t_r$	Rise time, CLK <sup>(1)</sup>				500	ns
$t_f$	Fall time, CLK <sup>(1)</sup>				500	ns
$t_{or}$	Rise time, outputs (off)				245	ns
$t_{of}$	Rise time, outputs (on)				570	ns
$f_{CLK}$	Clock frequency	Cascade operation			30	MHz

(1) If the devices are connected in cascade and  $t_r$  or  $t_f$  is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

## PARAMETER MEASUREMENT INFORMATION

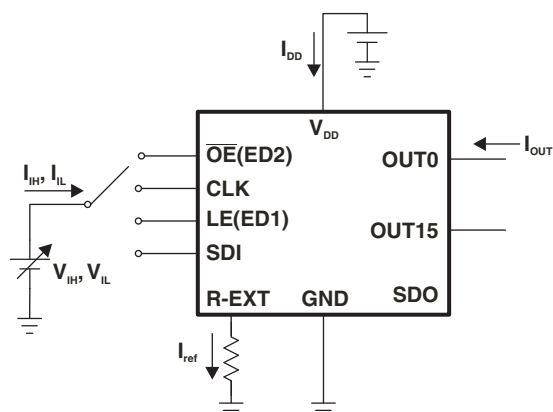


Figure 6. Test Circuit for Electrical Characteristics

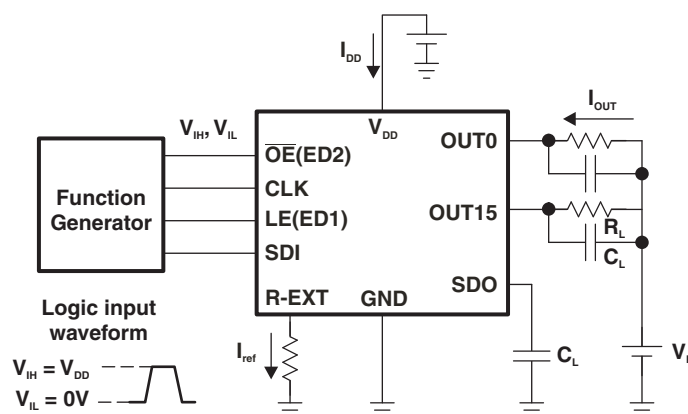


Figure 7. Test Circuit for Switching Characteristics

# PARAMETER MEASUREMENT INFORMATION (continued)

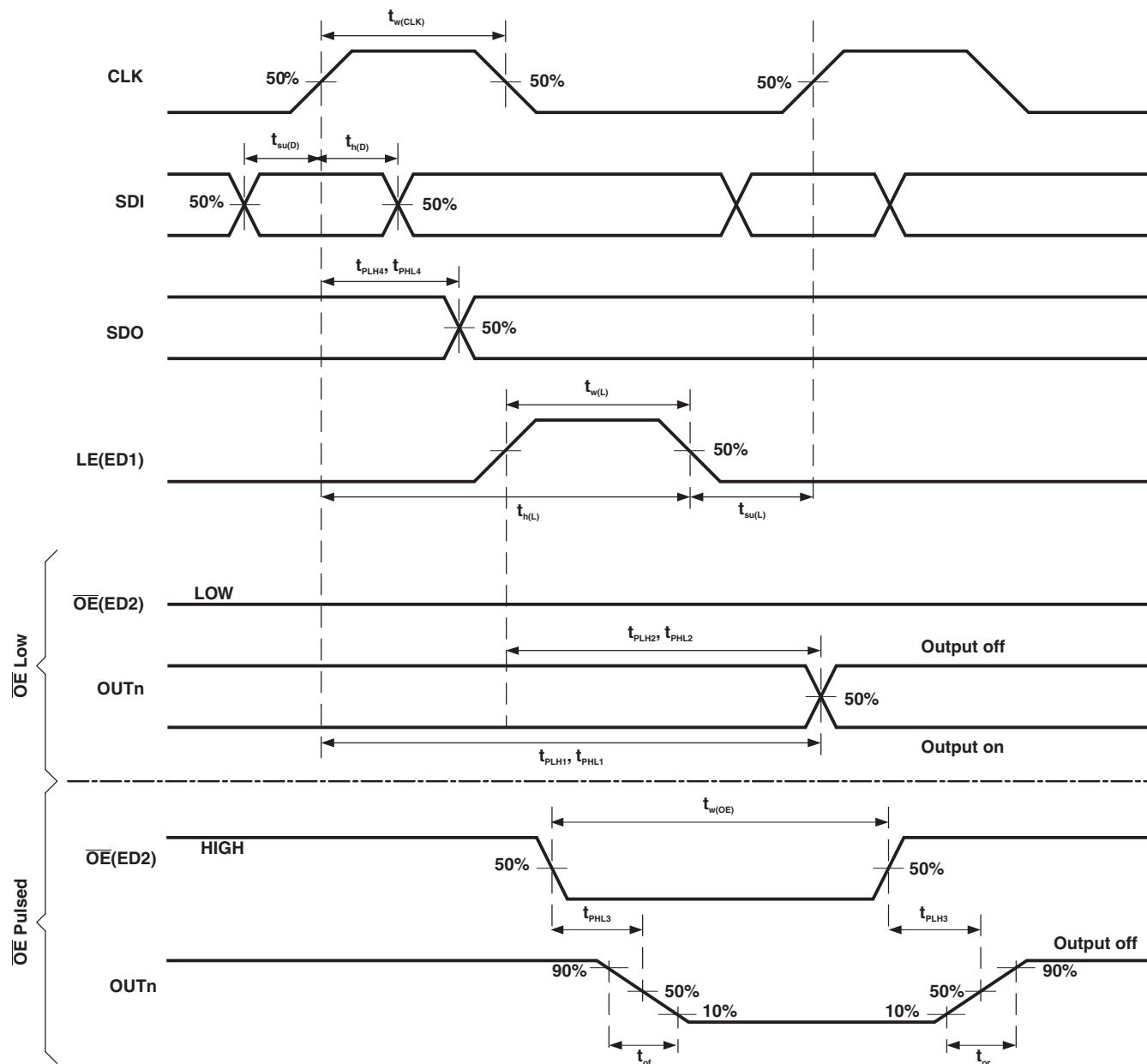
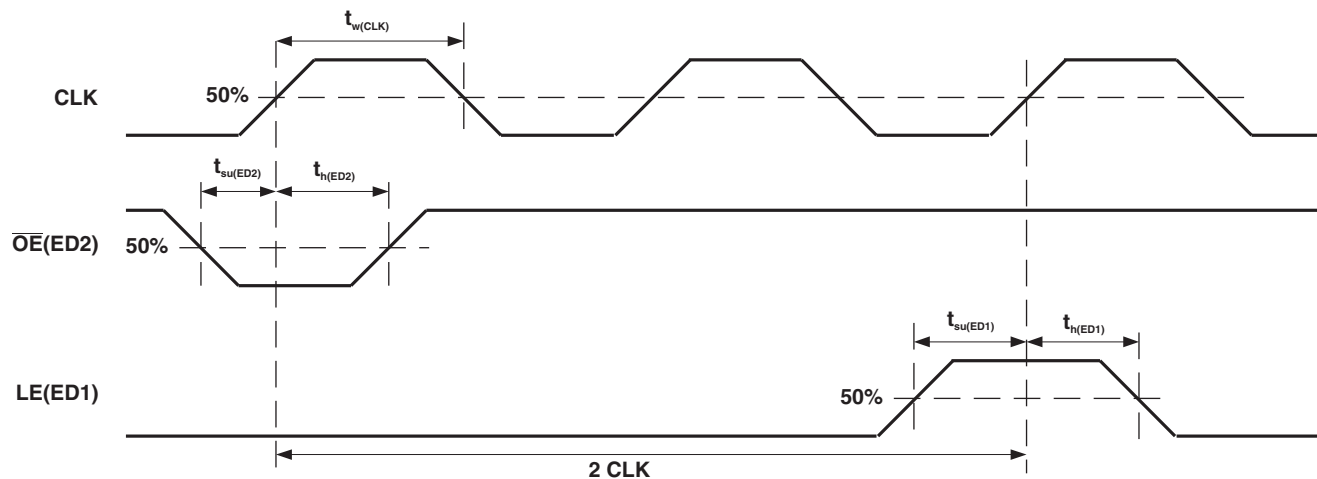
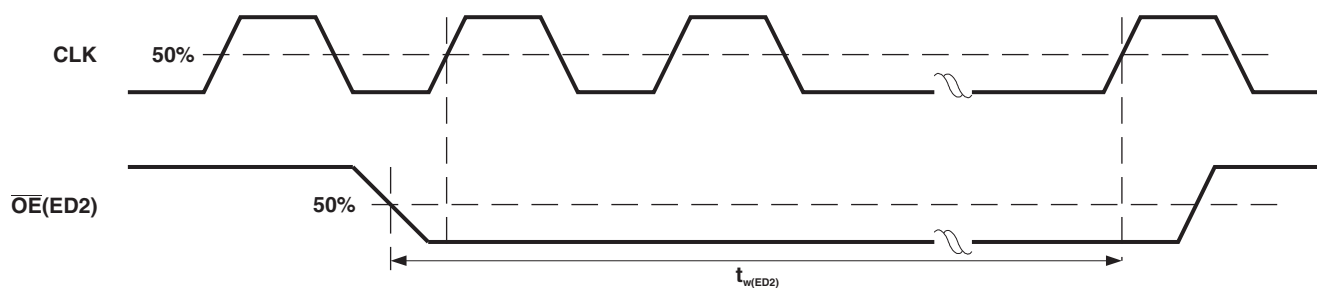


Figure 8. Normal Mode Timing Waveforms

**PARAMETER MEASUREMENT INFORMATION (continued)****Figure 9. Switching to Special Mode Timing Waveforms****Figure 10. Reading Error Status Code Timing Waveforms**

## APPLICATION INFORMATION

### Operating Principles

#### Constant Current

In LED display applications, TLC5926/TLC5927 provides nearly no current variations from channel to channel and from IC to IC. While  $I_{OUT} \leq 50$  mA, the maximum current skew between channels is less than  $\pm 6\%$  and between ICs is less than  $\pm 6\%$ .

#### Adjusting Output Current

TLC5926/TLC5927 scales up the reference current,  $I_{ref}$ , set by the external resistor  $R_{ext}$  to sink a current,  $I_{out}$ , at each output port. Users can follow the below formulas to calculate the target output current  $I_{OUT,target}$  in the saturation region:

$$V_{R-EXT} = 1.26 \text{ V} \times VG$$

$I_{ref} = V_{R-EXT}/R_{ext}$ , if another end of the external resistor  $R_{ext}$  is connected to ground.

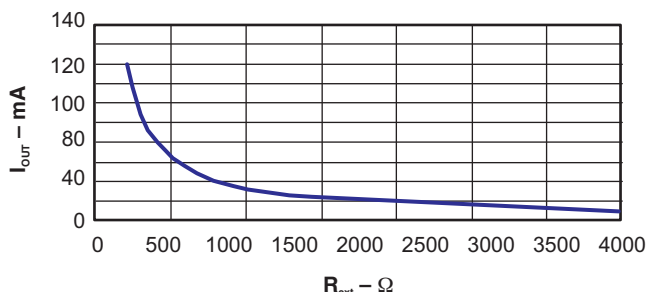
$$I_{OUT,target} = I_{ref} \times 15 \times 3^{CM-1}$$

Where  $R_{ext}$  is the resistance of the external resistor connected to the R-EXT terminal, and  $V_{R-EXT}$  is the voltage of R-EXT, which is controlled by the programmable voltage gain (VG), which is defined by the Configuration Code. The Current Multiplier (CM) determines that the ratio  $I_{OUT,target}/I_{ref}$  is 15 or 5. After power on, the default value of VG is  $127/128 = 0.992$ , and the default value of CM is 1, so that the ratio  $I_{OUT,target}/I_{ref} = 15$ . Based on the default VG and CM.

$$V_{R-EXT} = 1.26 \text{ V} \times 127/128 = 1.25 \text{ V}$$

$$I_{OUT,target} = (1.25 \text{ V}/R_{ext}) \times 15$$

Therefore, the default current is approximately 52 mA at 360  $\Omega$  and 26 mA at 720  $\Omega$ . The default relationship after power on between  $I_{OUT,target}$  and  $R_{ext}$  is shown in Figure 11.

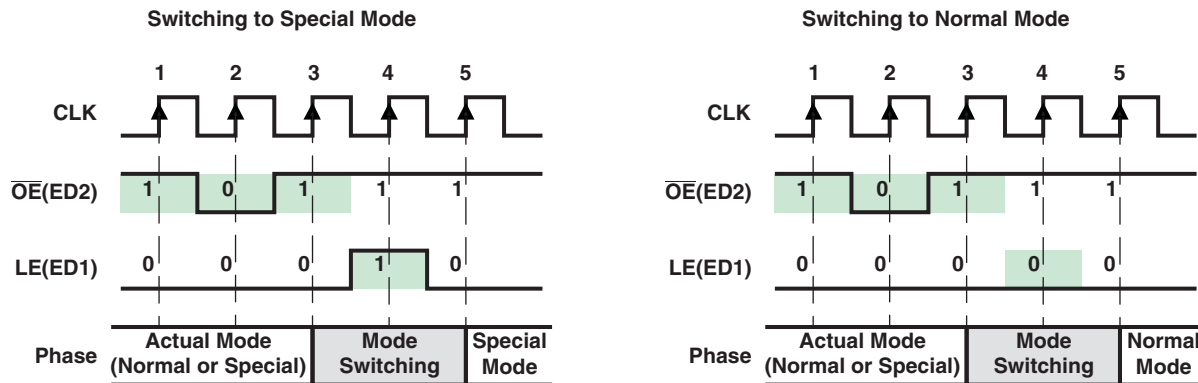


**Figure 11. Default Relationship Curve Between  $I_{OUT,target}$  and  $R_{ext}$**

## Operation Phases

### Operation Mode Switching

In order to switch between its two modes, TLC5926/TLC5927 monitors the signal  $\overline{OE}(ED2)$ . When a one-clock-wide pulse of  $\overline{OE}(ED2)$  appears, TLC5926/TLC5927 enters the two-clock-period transition phase, the Mode Switching phase. After power on, the default operation mode is the Normal Mode (see Figure 12).



**Figure 12. Mode Switching**

As shown in Figure 12, once a one-clock-wide short pulse (101) of  $\overline{OE}(ED2)$  appears, TLC5926/TLC5927 enters the Mode Switching phase. At the fourth rising edge of CLK, if LE(ED1) is sampled as voltage high, TLC5926/TLC5927 switches to Special mode; otherwise, it switches to Normal mode. The signal LE(ED1) between the third and the fifth rising edges of CLK cannot latch any data. Its level is used only to determine into which mode to switch. However, the short pulse of  $\overline{OE}(ED2)$  can still enable the output ports. During mode switching, the serial data can still be transferred through SDI and shifted out from SDO.

#### NOTES:

1. The signal sequence for the mode switching may be used frequently to ensure that the TLC5926/TLC5927 is in the proper mode.
2. The 1 and 0 on the LE(ED1) signal are sampled at the rising edge of CLK. The X means its level does not affect the result of mode switching mechanism.
3. After power on, the default operation mode is Normal mode.

### Normal Mode Phase

Serial data is transferred into TLC5926/TLC5927 via SDI, shifted in the Shift Register, and output via SDO. LE(ED1) can latch the serial data in the Shift Register to the Output Latch.  $\overline{OE}(ED2)$  enables the output drivers to sink current. These functions differ only as described in Operation Mode Switching, in which case, a short pulse triggers TLC5926/TLC5927 to switch the operation mode. However, as long as LE(ED1) is high in the Mode Switching phase, TLC5926/TLC5927 remains in the Normal mode, as if no mode switching occurred.

### Special Mode Phase

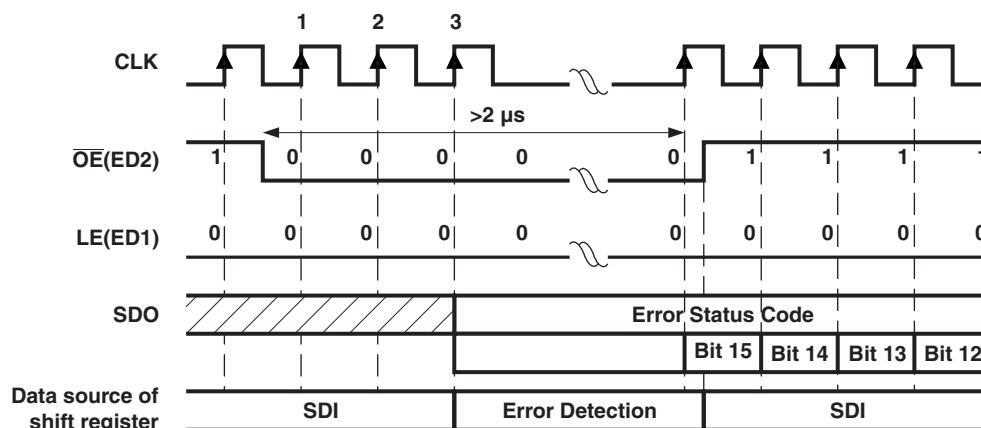
In the Special mode, as long as  $\overline{OE}(ED2)$  is not low, the serial data is shifted to the Shift Register via SDI and shifted out via SDO, as in the Normal mode. However, there are two differences between the Special Mode and the Normal Mode, as shown in the following sections.



### Reading Error Status Code in Special Mode

When  $\overline{OE}(ED2)$  is pulled low while in Special mode, error detection and load error status codes are loaded into the Shift Register, in addition to enabling output ports to sink current. Figure 13 shows the timing sequence for error detection. The 0 and 1 signal levels are sampled at the rising edge of each CLK. At least three zeros must be sampled at the voltage low signal  $\overline{OE}(ED2)$ . Immediately after the second 0 is sampled, the data input source of the Shift Register changes to the 16-bit parallel Error Status Code register, instead of from the serial data on SDI. Normally, the error status codes are generated at least 2  $\mu$ s after the falling edge of  $\overline{OE}(ED2)$ . The occurrence of the third or later 0 saves the detected error status codes into the Shift Register. Therefore, when  $\overline{OE}(ED2)$  is low, the serial data cannot be shifted into TLC5926/TLC5927 via SDI. When  $\overline{OE}(ED2)$  is pulled high, the data input source of the Shift Register is changed back to SDI. At the same time, the output ports are disabled and the error detection is completed. Then, the error status codes saved in the Shift Register can be shifted out via SDO bit-by-bit along with CLK, as well as the new serial data can be shifted into TLC5926/TLC5927 via SDI.

While in Special mode, the TLC5926/TLC5927 cannot simultaneously transfer serial data and detect LED load error status.

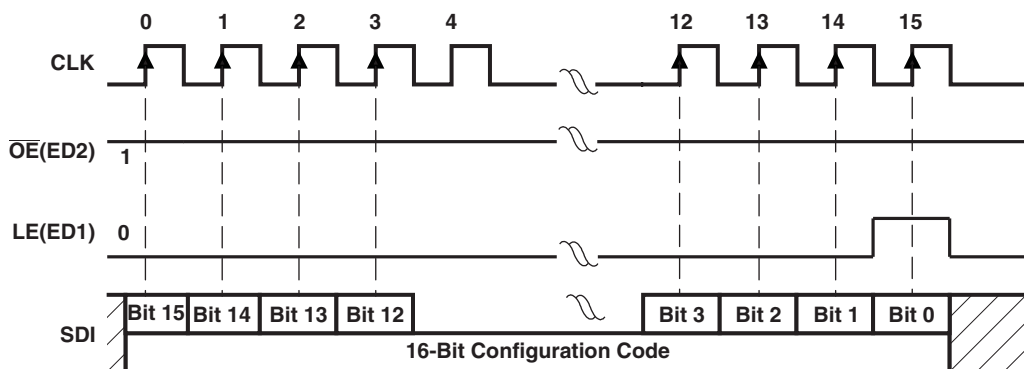


**Figure 13. Reading Error Status Code**

### Writing Configuration Code in Special Mode

When in Special mode, the active high signal LE(ED1) latches the serial data in the Shift Register to the Configuration Latch, instead of the Output Latch. The latched serial data is used as the Configuration Code.

The code is stored until power off or the Configuration Latch is rewritten. As shown in Figure 14, the timing for writing the Configuration Code is the same as the timing in the Normal Mode to latching output channel data. Both the Configuration Code and Error Status Code are transferred in the common 16-bit Shift Register. Users must pay attention to the sequence of error detection and current adjustment to avoid the Configuration Code being overwritten by Error Status Code.



**Figure 14. Writing Configuration Code**

## Open-Circuit Detection Principle

The LED Open-Circuit Detection compares the effective current level  $I_{OUT}$  with the open load detection threshold current  $I_{OUT,Th}$ . If  $I_{OUT}$  is below the  $I_{OUT,Th}$  threshold, the TLC5926/TLC5927 detects an open-load condition. This error status can be read as an error status code in the Special mode. For open-circuit error detection, a channel must be on.

**Table 1. Open-Circuit Detection**

STATE OF OUTPUT PORT	CONDITION OF OUTPUT CURRENT	ERROR STATUS CODE	MEANING
Off	$I_{OUT} = 0 \text{ mA}$	0	Detection not possible
On	$I_{OUT} < I_{OUT,Th}^{(1)}$	0	Open circuit
	$I_{OUT} \geq I_{OUT,Th}^{(1)}$	Channel n error status bit 1	Normal

(1)  $I_{OUT,Th} = 0.5 \times I_{OUT,target}$  (typical)

## Short-Circuit Detection Principle (TLC5927 Only)

The LED short-circuit detection compares the effective voltage level  $V_{OUT}$  with the shorted-load detection threshold voltages  $V_{OUT,TTh}$  and  $V_{OUT,RTh}$ . If  $V_{OUT}$  is above the  $V_{OUT,TTh}$  threshold, the TLC5927 detects an shorted-load condition. If the  $V_{OUT}$  is below  $V_{OUT,RTh}$  threshold, no error is detected and the error bit is reset. This error status can be read as an error status code in the Special mode. For short-circuit error detection, a channel must be on.

**Table 2. Short-Circuit Detection**

STATE OF OUTPUT PORT	CONDITION OF OUTPUT VOLTAGE	ERROR STATUS CODE	MEANING
Off	$I_{OUT} = 0 \text{ mA}$	0	Detection not possible
On	$V_{OUT} < V_{OUT,TTh}^{(1)}$	0	Short circuit
	$V_{OUT} < V_{OUT,RTh}^{(1)}$	Channel n error status bit 1	Normal

(1)  $I_{OUT,Th} = 0.5 \times I_{OUT,target}$  (typical)

## Overtemperature Detection and Shutdown

The TLC5926/TLC5927 is equipped with a global overtemperature sensor and 16 individual, channel-specific overtemperature sensors.

- When the global sensor reaches the trip temperature, all output channels are shutdown, and the error status is stored in the internal Error Status register of every channel. After shutdown, the channels automatically restart after cooling down, if the control signal (output latch) remains on. The stored error status is not reset after cooling down and can be read out as the error status code in the Special mode.
- When one of the channel-specific sensors reaches trip temperature, only the affected output channel is shut down, and the error status is stored only in the internal Error Status register of the affected channel. After shutdown, the channel automatically restarts after cooling down, if the control signal (output latch) remains on. The stored error status is not reset after cooling down and can be read out as error status code in the Special mode.

For channel-specific overtemperature error detection, a channel must be on.

The error status code is reset when the TLC5926/TLC5927 returns to Normal mode.

**Table 3. Overtemperature Detection<sup>(1)</sup>**

STATE OF OUTPUT PORT	CONDITION	ERROR STATUS CODE	MEANING
Off	$I_{OUT} = 0 \text{ mA}$	0	
On	$T_j < T_{j,trip} \text{ global}$	1	Normal
On → all channels Off	$T_j > T_{j,trip} \text{ global}$	All error status bits = 0	Global overtemperature
On	$T_j < T_{j,trip} \text{ channel n}$	1	Normal
On → Off	$T_j > T_{j,trip} \text{ channel n}$	Channel n error status bit = 0	Channel n overtemperature

(1) The global shutdown threshold temperature is approximately 170°C.

## 16-Bit Configuration Code and Current Gain

Bit definition of the Configuration Code in the Configuration Latch is shown in [Table 4](#).

**Table 4. Bit Definition of 8-Bit Configuration Code**

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8–15
Meaning	CM	HC	CC0	CC1	CC2	CC3	CC4	CC5	Don't care
Default	1	1	1	1	1	1	1	1	X

Bit 7 is first sent into TLC5926/TLC5927 via SDI. Bits 1 to 7 {HC, CC[0:5]} determine the voltage gain (VG) that affects the voltage at R-EXT and indirectly affects the reference current,  $I_{ref}$ , flowing through the external resistor at R-EXT. Bit 0 is the Current Multiplier (CM) that determines the ratio  $I_{OUT,target}/I_{ref}$ . Each combination of VG and CM gives a specific Current Gain (CG).

- VG: the relationship between {HC, CC[0:5]} and the voltage gain is calculated as shown below:  

$$VG = (1 + HC) \times (1 + D/64) / 4$$

$$D = CC0 \times 2^5 + CC1 \times 2^4 + CC2 \times 2^3 + CC3 \times 2^2 + CC4 \times 2^1 + CC5 \times 2^0$$
Where HC is 1 or 0, and D is the binary value of CC[0:5]. So, the VG could be regarded as a floating-point number with 1-bit exponent HC and 6-bit mantissa CC[0:5]. {HC, CC[0:5]} divides the programmable voltage gain VG into 128 steps and two sub-bands:  
Low voltage sub-band (HC = 0):  $VG = 1/4 \sim 127/256$ , linearly divided into 64 steps  
High voltage sub-band (HC = 1):  $VG = 1/2 \sim 127/128$ , linearly divided into 64 steps
- CM: In addition to determining the ratio  $I_{OUT,target}/I_{ref}$ , CM limits the output current range.  
High Current Multiplier (CM = 1):  $I_{OUT,target}/I_{ref} = 15$ , suitable for output current range  $I_{OUT} = 10 \text{ mA}$  to  $120 \text{ mA}$ .  
Low Current Multiplier (CM = 0):  $I_{OUT,target}/I_{ref} = 5$ , suitable for output current range  $I_{OUT} = 5 \text{ mA}$  to  $40 \text{ mA}$
- CG: The total Current Gain is defined as the following.  

$$V_{R-EXT} = 1.26 \text{ V} \times VG$$

$$I_{ref} = V_{R-EXT}/R_{ext}$$
, if the external resistor,  $R_{ext}$ , is connected to ground.  

$$I_{OUT,target} = I_{ref} \times 15 \times 3^{CM-1} = 1.26 \text{ V}/R_{ext} \times VG \times 15 \times 3^{CM-1} = (1.26 \text{ V}/R_{ext} \times 15) \times CG$$

$$CG = VG \times 3^{CM-1}$$
Therefore, CG = (1/12) to (127/128) divided into 256 steps.

### Examples

- Configuration Code {CM, HC, CC[0:5]} = {1, 1, 111111}  
 $VG = 127/128 = 0.992$  and  $CG = VG \times 3^0 = VG = 0.992$
- Configuration Code = {1, 1, 000000}  
 $VG = (1 + 1) \times (1 + 0/64)/4 = 1/2 = 0.5$ , and  $CG = 0.5$
- Configuration Code = {0, 0, 000000}  
 $VG = (1 + 0) \times (1 + 0/64)/4 = 1/4$ , and  $CG = (1/4) \times 3^{-1} = 1/12$

After power on, the default value of the Configuration Code {CM, HC, CC[0:5]} is {1, 1, 111111}. Therefore,  $VG = CG = 0.992$ . The relationship between the Configuration Code and the Current Gain is shown in [Figure 15](#).

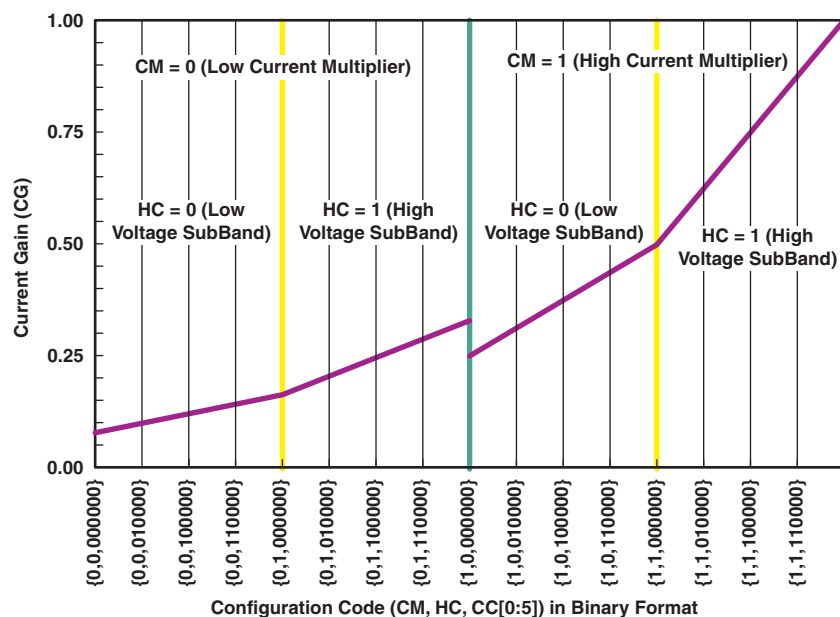


Figure 15. Current Gain vs Configuration Code

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC5926IDBQR	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLC5926I	<a href="#">Samples</a>
TLC5926IDWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC5926I	<a href="#">Samples</a>
TLC5926IPWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	Y5926	<a href="#">Samples</a>
TLC5926IPWPRG4	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	Y5926	<a href="#">Samples</a>
TLC5927IDBQR	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLC5927I	<a href="#">Samples</a>
TLC5927IDWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC5927I	<a href="#">Samples</a>
TLC5927IPWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	Y5927	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TLC5926, TLC5927 :**

- Automotive: [TLC5926-Q1](#), [TLC5927-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5926IDBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC5926IDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
TLC5926IPWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TLC5927IDBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC5927IDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
TLC5927IPWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5926IDBQR	SSOP	DBQ	24	2500	367.0	367.0	38.0
TLC5926IDWR	SOIC	DW	24	2000	350.0	350.0	43.0
TLC5926IPWPR	HTSSOP	PWP	24	2000	367.0	367.0	38.0
TLC5927IDBQR	SSOP	DBQ	24	2500	367.0	367.0	38.0
TLC5927IDWR	SOIC	DW	24	2000	350.0	350.0	43.0
TLC5927IPWPR	HTSSOP	PWP	24	2000	367.0	367.0	38.0



## GENERIC PACKAGE VIEW

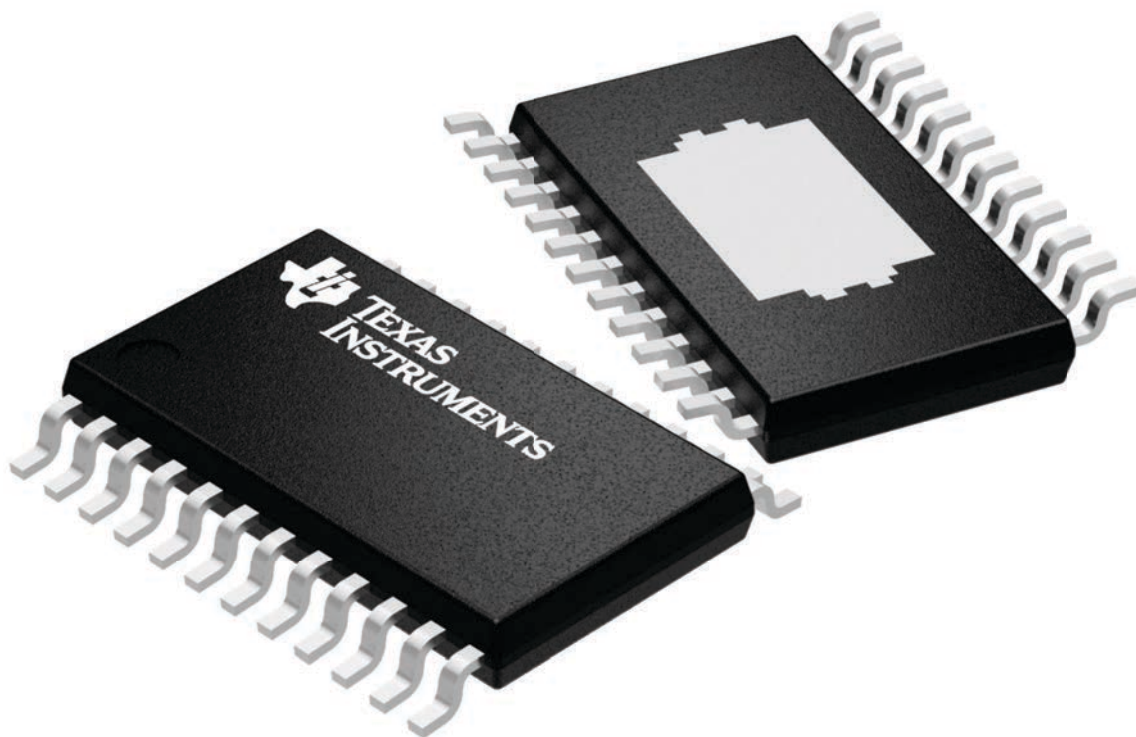
**PWP 24**

**PowerPAD™ TSSOP - 1.2 mm max height**

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224742/B



## PowerPAD™ TSSOP - 1.2 mm max height

## PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

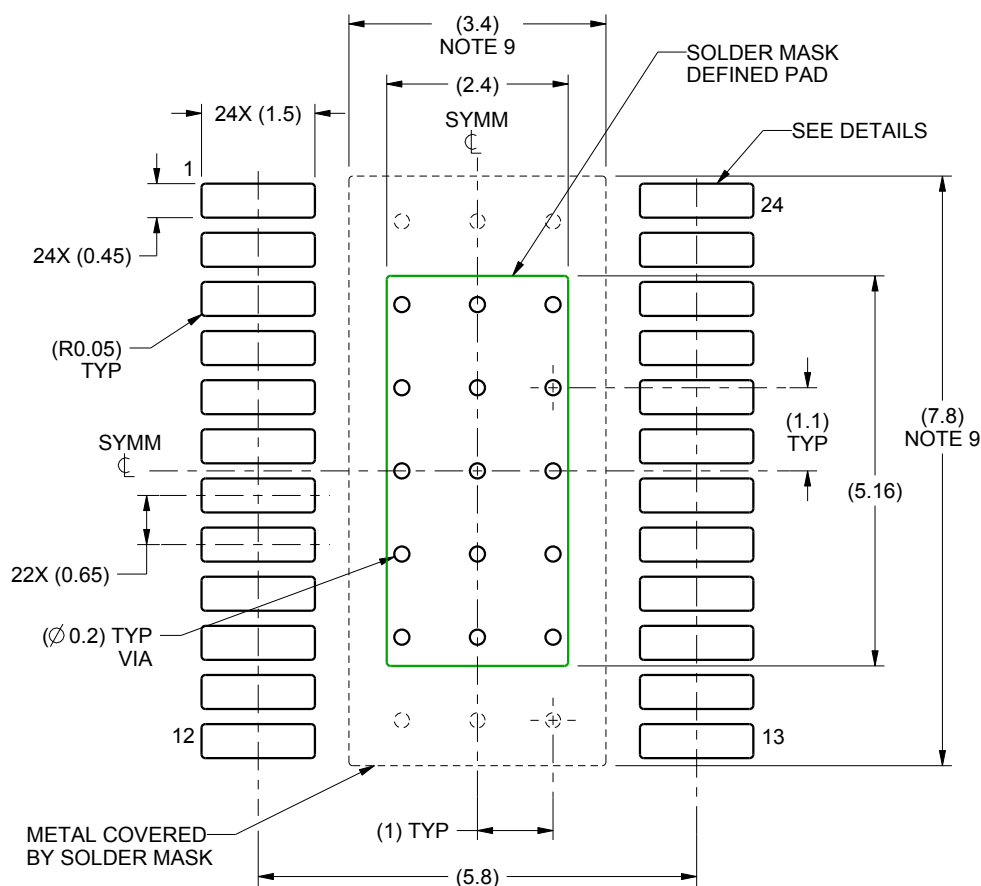
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present and may vary.

# EXAMPLE BOARD LAYOUT

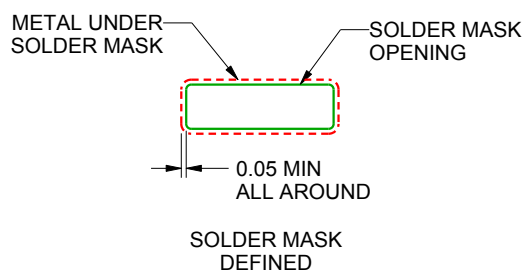
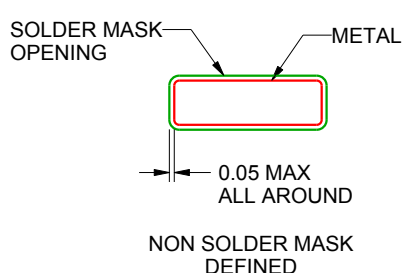
PWP0024B

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
PADS 1-24

4222709/A 02/2016

NOTES: (continued)

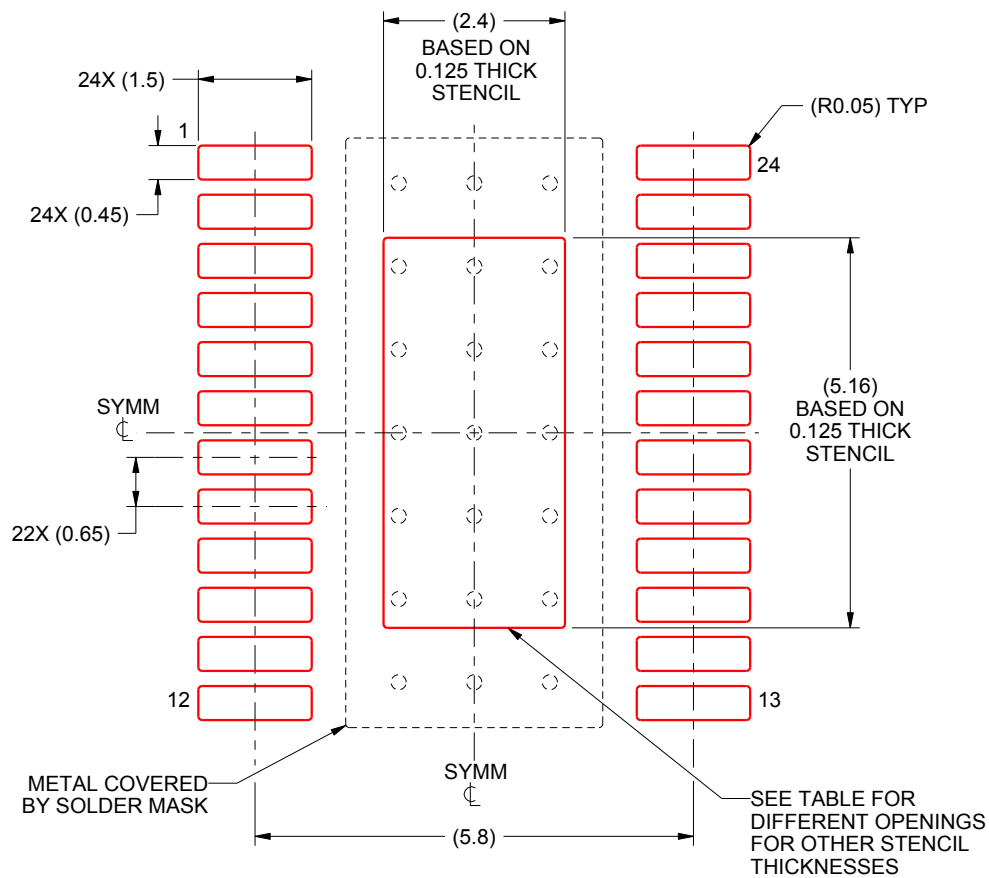
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

PWP0024B

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



**SOLDER PASTE EXAMPLE**  
EXPOSED PAD  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.68 X 5.77
0.125	2.4 X 5.16 (SHOWN)
0.15	2.19 X 4.71
0.175	2.03 X 4.36

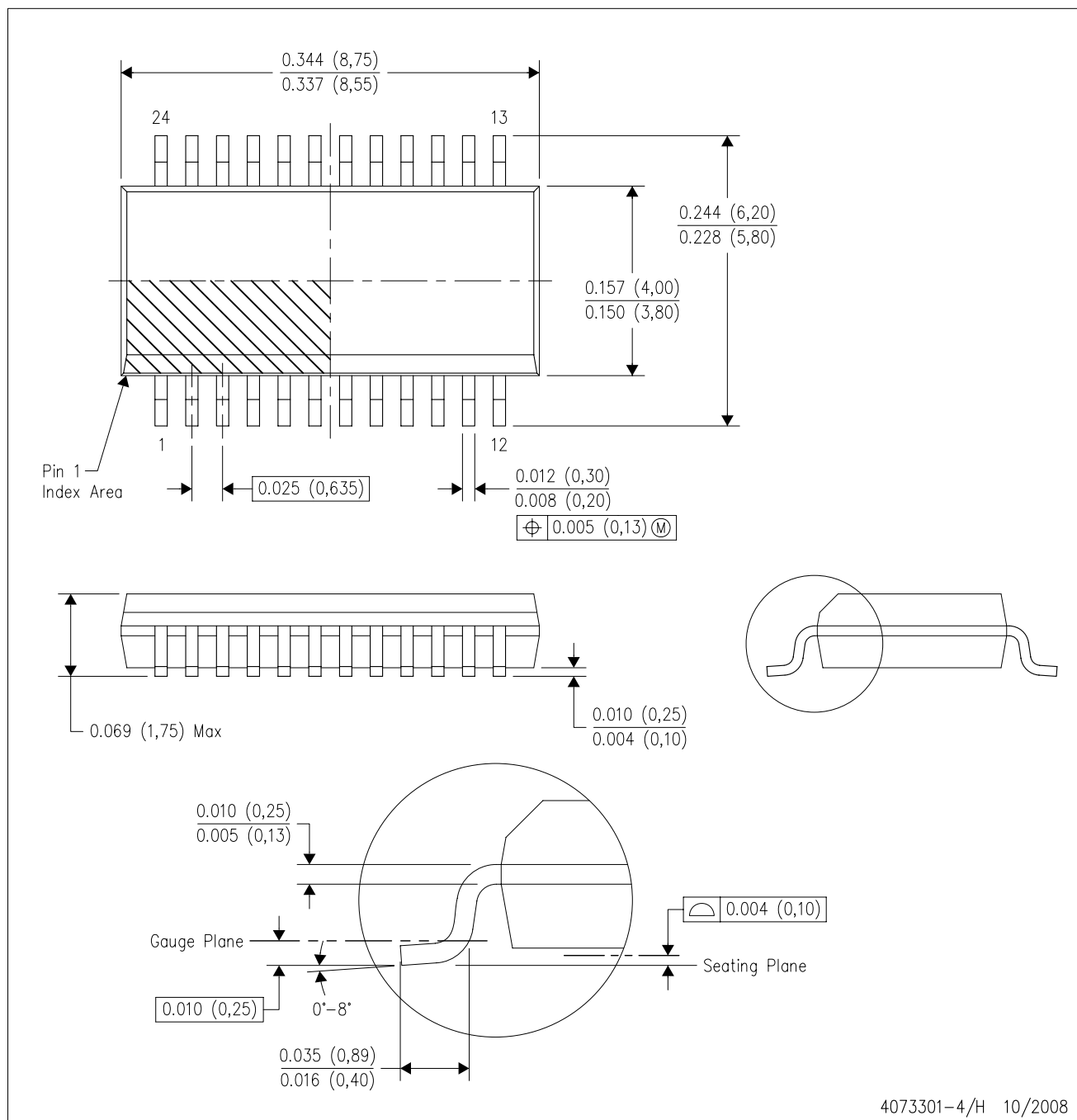
4222709/A 02/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

DBQ (R-PDSO-G24)

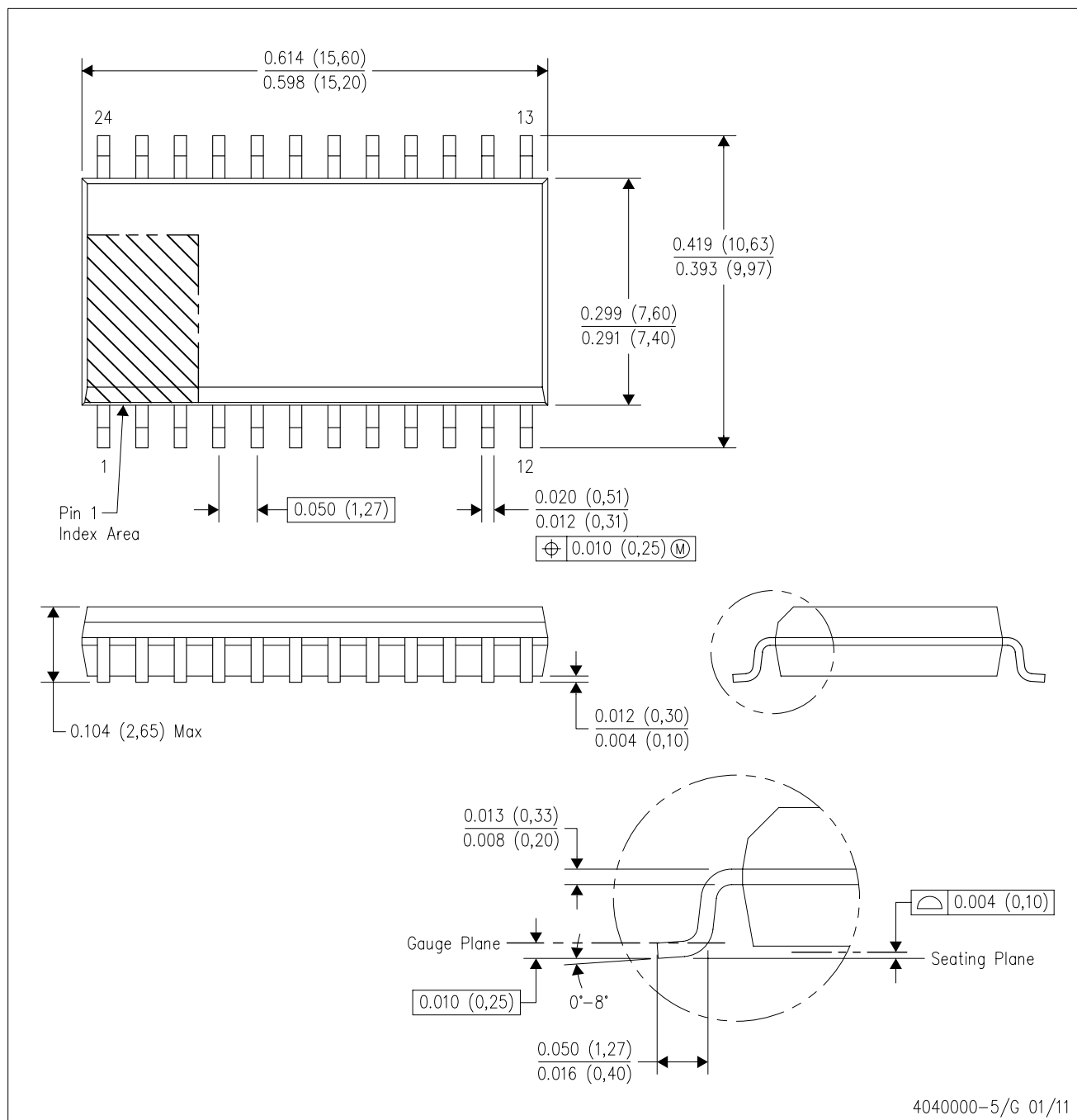
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - D. Falls within JEDEC MO-137 variation AE.

DW (R-PDSO-G24)

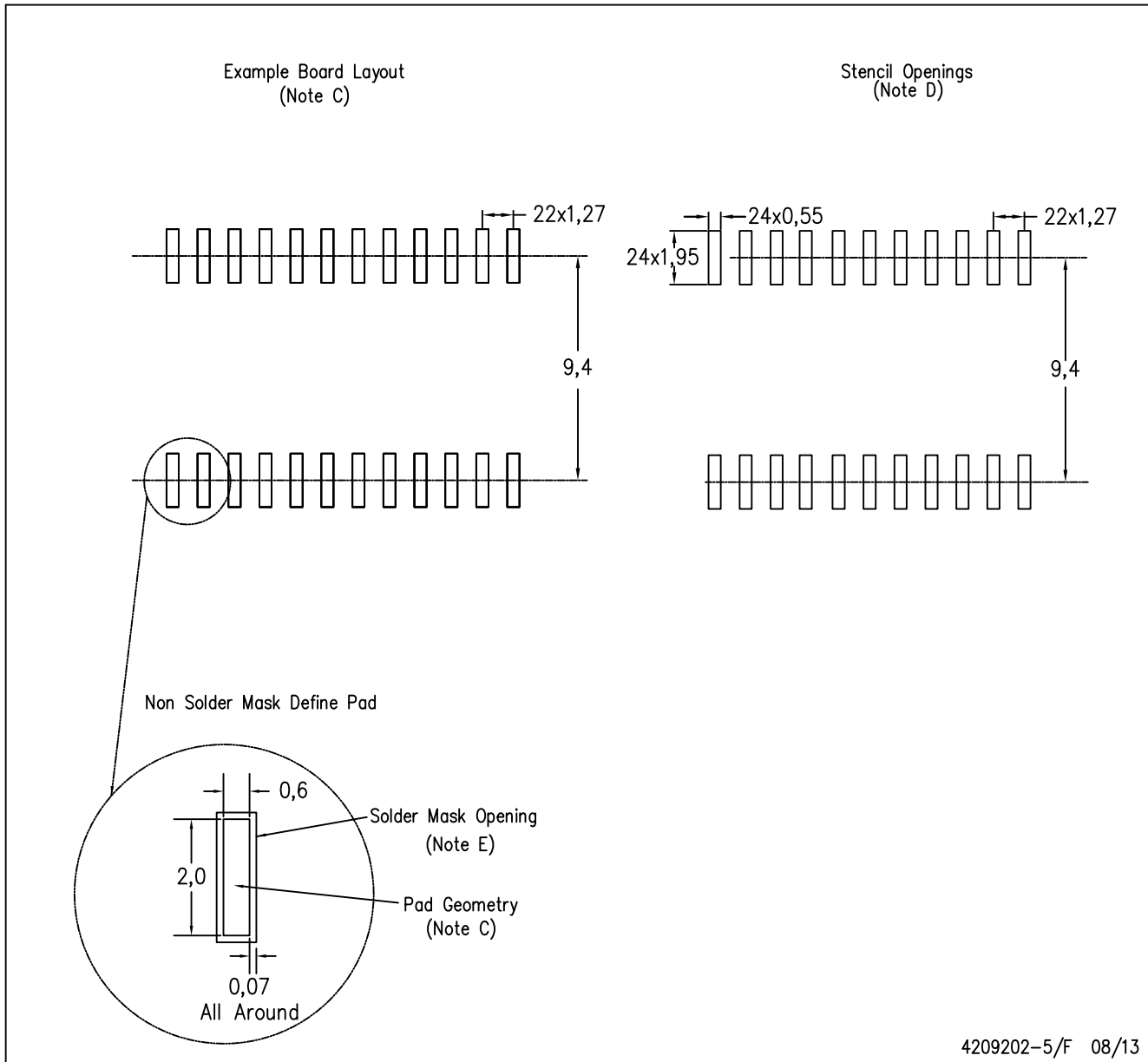
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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