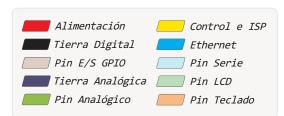
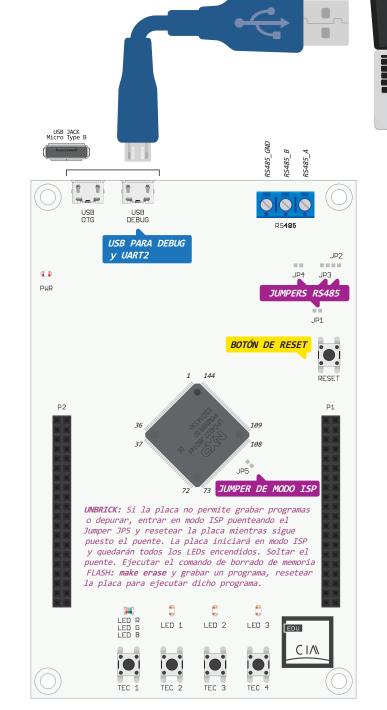
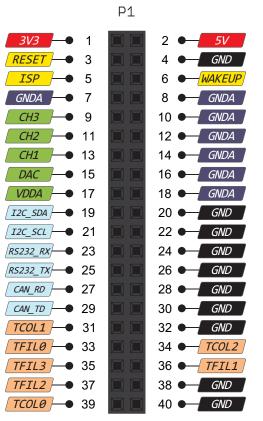


EDU-CIAA-NXP v1.1 Asignación de pines







5V *3V3* MDIO TXD0 TXD1 18 — SPI MISO 20 ← SPI SCK GND SPI_MOSI —● 21 22 **←** *LCD4* LCD EN— 24 **←** LCD RS 26 **►** *LCD3* GND 28 **←** *LCD2* GPI00 — 29 30 **←** *LCD1 GPI02* → 31 32 **●** *GPI01 GPI04* → 33 34 **●** *GPI03 GPI06* → 35 36 **●** *GPI05* 38 — *GPI07* GND 37 40 **←** *GPI08*

P2

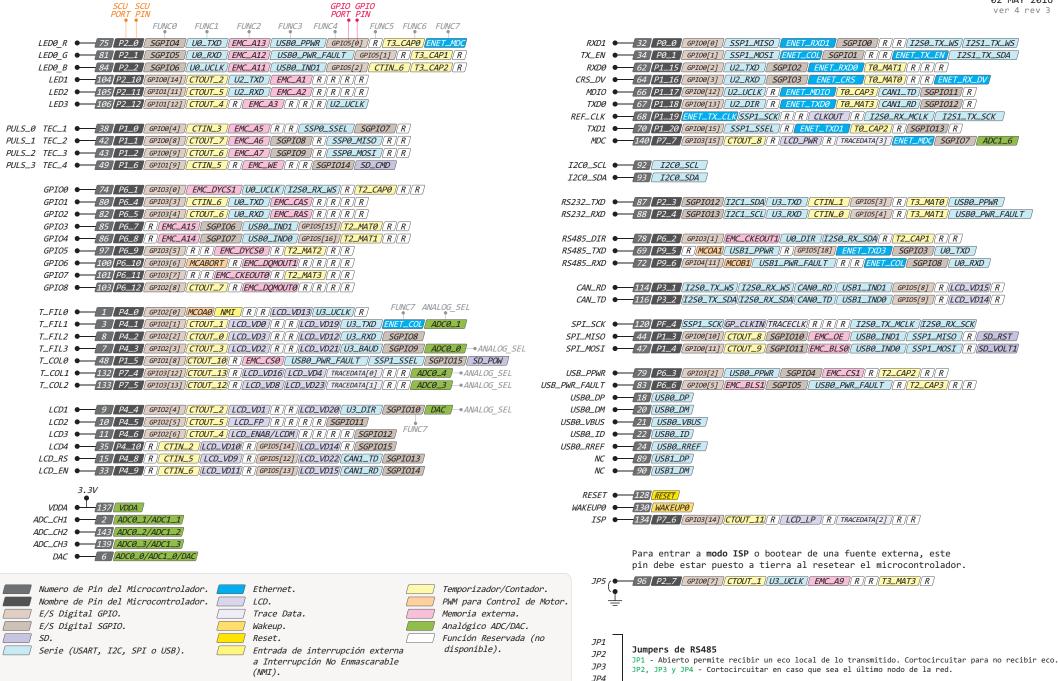
Tira de 40 pines hembra de 0.1"(2,54 mm) de espaciado

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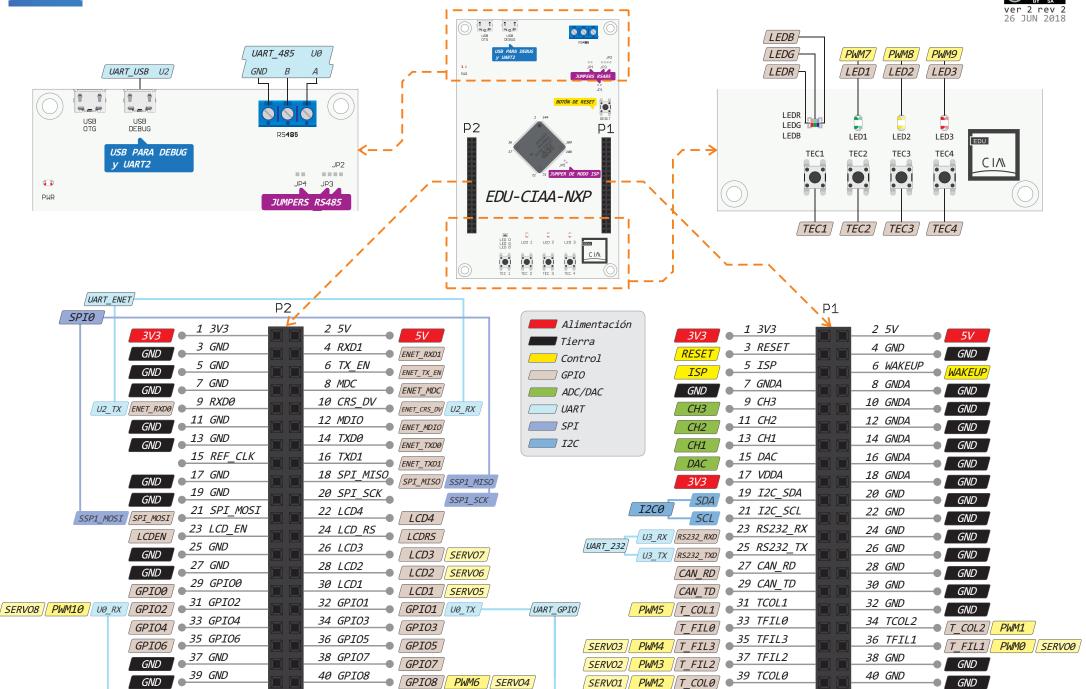
EDU-CIAA-NXP v1.1 Pines utilizados del NXP LPC4337 JBD144





EDU-CIAA-NXP v1.1 Mapeo de periféricos de la biblioteca sAPI





EDU-CIAA-NXP v1.1 Mapeo de periféricos CIANBOT



