

Dante Vasudevan

+1(408) 775-4665 | dantevasudevan@gmail.com | [LinkedIn](#) | [Personal Website](#)

EDUCATION

M.S. in Semiconductor Engineering , Northeastern University – Boston, MA	09/2025 – 05/2027
<ul style="list-style-type: none">Concentration in Devices and NanosystemsRelevant Coursework includes:<ul style="list-style-type: none">Micro and Nanoscale Manufacturing, Photonic Devices	
B.S. in Electrical Engineering , University of Illinois – Urbana, IL	Graduated 05/2024

B.S. in Electrical Engineering, University of Illinois – Urbana, IL

- Recipient of Samsung Technology Track Scholarship
- Relevant coursework includes:
 - Semiconductor Electronics, Semiconductor Device Fabrication, Photonics, Optics, Plasmas, E&M Fields and Waves 1 and 2, Digital Systems (FPGA Course), Analog and Digital Signal Processing, and Microelectronics (Small-signal analysis)

High School Degree, Willow Glen High School – San Jose, CA

- FIRST Robotics
 - Designed a robot to launch balls, lift itself, and spin a colored wheel
- Relevant coursework includes:
 - Integral and Differential Calculus, Multivariate Calculus, Chemistry, and Physics Mechanics

EXPERIENCE

Student Research , Electrical Engineering – University of Illinois	08/2020 – 05/2024
<ul style="list-style-type: none">NIR VCSEL Research supervised by Prof. Kent Choquette<ul style="list-style-type: none">Performed Near-Field and Far-Field Characterization on Coupled Photonic Crystal VCSELs across a range of current injections to search for the in-phase and out-of-phase supermodesBuilt a Model of Coupled Index-Guided VCSELS to analyze the fundamental gaussian modes and identify ideal design parametersWorked in a Class 1000 Clean Room<ul style="list-style-type: none">Built BJTs, Diodes, and FETs on silicon wafers using fabrication techniques (Oxidation, Photolithography, Etching, Ion Diffusion, and Metallization)Control Systems Research under Yogi Patel<ul style="list-style-type: none">Modeled and Built an Inverted Pendulum using LQR Feedback that stabilized within 2 secondsPresented Poster at PURE Symposium	
Intern/Engineer , ASIC Design – Auradine	06/2023 – 08/2023

Intern/Engineer, ASIC Design – Auradine

- Performed PVT timing analysis using foundry SPICE models across various technology nodes to determine the best performing process for ASIC fabrication.
- Performed IR Drop Analysis and PDN Simulations with PowerDC to identify potential hotspots or large power losses within the ASIC
- Explored thermoelectric power reduction ideas for the system to reduce power consumption

Intern/Engineer, Robotics – Ford Motor Company

- Developed a low-cost testing platform for autonomous vehicle interaction with Game Theory Algorithms
 - Built low-cost vehicles fitted with automatic line-following, to be used to test the various algorithms
 - Built a ROS2 Framework to support communication, mapping and localization, and negotiation

SKILLS

Software:	Python, MATLAB, Linux, ROS2 Foxy, Image Processing, Git
Electronics:	HSPICE, LTSPICE, KiCad (PCB Design), KLayout (PIC Design), Lumerical, PowerDC
Tools:	Spectrometer, OSA, SPA, Oscilloscope, Soldering
Languages:	English: Native Spanish: Professional fluency (ILR Level 4 / CEFR C1)