Dante Vasudevan

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EDUCATION

Master's in Semiconductor Engineering, Northeastern University – Boston, MA **09/2025 – 05/2027**

- Concentration in Devices and Nanosystems
- Relevant Coursework includes:
  - Micro and Nanoscale Manufacturing, Photonic Devices, VLSI Design, Solid State Devices

Bachelor's in Electrical Engineering, University of Illinois – Urbana, IL **Graduated 05/2024**

- Recipient of Samsung Technology Track Scholarship
- Relevant coursework includes:
  - Semiconductor Electronics, Semiconductor Device Fabrication, Photonics, Optics, Plasmas, E&M Fields and Waves 1 and 2, Digital Systems (FPGA Course), Analog and Digital Signal Processing, and Microelectronics (Small-signal analysis)

SKILLS

Software:	Python, MATLAB, Linux, ROS2 Foxy, Image Processing, Git
Electronics:	HSPICE, LTSPICE, KiCad (PCB Design), KLayout (PIC Design), Lumerical, PowerDC
Tools:	OSA, SPA, 4-Point Probe, Oscilloscope, Waveform Generator, Soldering
Languages:	English (Native), Spanish (Professional Fluency: ILR 4 / CEFR C1)

EXPERIENCE

Student Research, Photonics – University of Illinois – Urbana, IL **08/2023 – 05/2024**

- Performed near-field and far-field characterization on NIR Coupled Photonic Crystal VCSELs using an OSA/SPA/4PP testing system across a range of current injections to search for coupled supermodes
- Built a model of Coupled Index-Guided VCSELS to analyze the fundamental gaussian modes and identify ideal design parameters

Intern/Engineer, ASIC Design – Auradine – San Jose, CA **06/2023 – 08/2023**

- Performed PVT timing analysis using foundry SPICE models across various technology nodes to determine the best performing process for ASIC fabrication.
- Performed IR Drop Analysis and PDN Simulations with PowerDC to identify potential hotspots or large power losses within the ASIC
- Explored thermoelectric power reduction ideas for the system to reduce power consumption

Student Research, Process Engineering – University of Illinois – Urbana, IL **01/2023 – 05/2023**

- Worked in a Class 1000 clean room, building BJTs, Diodes, and FETs on silicon wafers using fabrication techniques (Oxidation, Photolithography, Etching, Ion Diffusion, and Metallization)
- Wet Lab Experience performing RCA Cleaning and Wet Etching on semiconductor wafers
- Tested the devices with a SPA/4PP testing system to characterize the devices as well as search for defects

Student Research, Control Systems – University of Illinois – Urbana, IL **09/2021 – 12/2021**

- Modeled and built an Inverted Pendulum in MATLAB using LQR Feedback, which stabilized within 2 seconds
- Presented poster at PURE Symposium

Intern/Engineer, Robotics – Ford Motor Company – Palo Alto, CA **05/2021 – 08/2021**

- Developed a low-cost testing platform for autonomous vehicle interaction with Game Theory Algorithms
- Built low-cost vehicles fitted with automatic line-following, to be used to test the various algorithms
- Built a ROS2 Framework to support communication, mapping and localization, and negotiation