Faults Analysis and Remedial Strategies in High Power Neutral Point Clamped Converters

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***Abstract*—Nowadays, multilevel power converter structures are intensively studied and investigated for several applications, such as railway traction systems, active filtering, reactive power compensation and large induction or synchronous motor drives. However, only a few papers deal with the analysis of faults and the development of adequate remedial strategies. This is one of the most important aspects that must be carefully considered and investigated when transferring converter systems from research laboratories to the applications. Failures of the components in static energy conversion systems must be adequately faced to prevent severe and widespread damages in the converter, or even extended to the load and the grid. In particular, in multilevel converters, system protection is more difficult when compared to simpler two-levels converters, mainly because current fault paths can be much more complex. Problems may be exalted in high power applications, as those considered in this paper, when several kVs and hundreds of kAs characterize the application. In this paper, a study and an analysis of important fault scenarios in a high power (up to 12 MVAs) IGCT based Neutral Point Clamped converter system are presented and possible remedial strategies are discussed. Although the study has been performed mainly by simulation, some interesting experimental results, obtained in the joint laboratory between Ansaldo Sistemi Industriali and the University of Genova, are also presented.**

I. INTRODUCTION

The increasing need for reliable high power (greater than 10 MW) motor drives, which should be connected to the medium voltage network, render the multilevel conversion concept [1-7] one of the most interesting approaches to face the technical problems posed by operating at voltages higher than the blocking voltage of the existing power semiconductor devices. The Neutral Point Clamped (NPC) converter structure was the first topology that has been considered for a real development [1], and today represents a challenge in some important new application fields. For instance, in ac motor drives for rolling mill applications, due to the need for high availability and high overload capability, the static energy converters most used in the past have been mainly limited to cycloconverters [8]. New high power switching devices, like IGCTs, have made attractive the use of voltage source inverters in these applications, where medium voltage induction or synchronous motors are often employed. However, the NPC converter structure is complex and requires a careful design of protection strategies and devices because of various possible fault current paths, as well as possible fault propagations among converter devices and the interactions of the converter with the load and the grid. The most critical faults are connected with internal short circuit caused by a non correct switching of the main power electronic devices and by possible overvoltage stresses on the DC-link capacitors. The paper discusses three typical and important fault scenarios in the NPC converter as well as some protection strategies aimed at limiting the fault damages.

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II. INTERNAL FAULT ANALYSIS

A. Semi DC-link short circuit

The naming convention for the controllable switches identifies the uppermost and lowermost switches of a phase leg with the numbers 1 and 4 respectively, as shown in Fig. 1. These are named "external" switches. The switch below 1 and the switch above 4 are identified with the numbers 2 and 3 respectively. They are named "internal" switches. A short circuit of the semi DC-link can occur in the three different ways, as shown in Fig. 2, where the phase fault examples are not correlated.

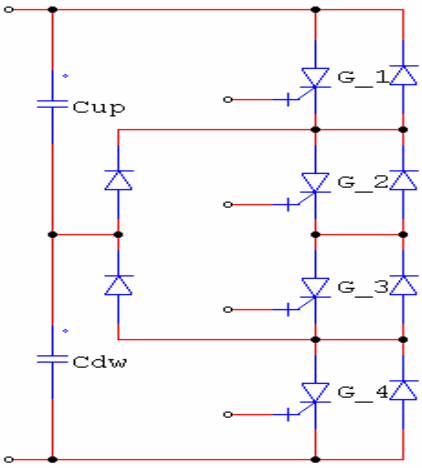


Figure 1. Valve schematic of a converter branch

1. The control system fails and is not able to detect the missed turn off of an external switch 1 (or 4) and then turns on its complementary 3 (or 2) switch (leftmost case in Fig. 2).
2. During the turn off of an external switch (1 or 4) an overvoltage capable of damaging in short circuit its anti-parallel diode may occur. As a consequence, at the next turn on of the internal complementary switch (2 or 3), the damaged diode together with two, still undamaged, IGCTs create a short circuit path for the semi DC bus (center case in Fig. 2).
3. During the turn on of an external switch 1 (or 4), the clamp diode on the positive (or negative) semi DC-link recovers. The consequent reverse overvoltage across its terminals can exceed the maximum sustainable value for a time interval long enough to damage the clamp diode in short circuit. This fault of the clamp diode short circuits the positive (or negative) semi DC-link capacitor (rightmost case in Fig. 2).

The semi DC-link short circuit causes the rapid discharge of the related DC-link capacitor through the fault path and the related current can rise up to 100 kA. Three factors concur to create such a high current peak: a) the energy stored in the DC-link capacitor which, in addition, generates a low damped second order transient, b) the energy drawn from the motor which becomes short-circuited through the diode path, c) the energy drawn from the grid until the opening of the grid-side medium voltage circuit breaker. To evaluate the effects of a semi DC-link short circuit fault the two following aspects must be considered: 1) In order to avoid risks of explosion, the squared time-integral of the current (I^2t) flowing through each semiconductor involved must remain below the limit specified in the device datasheet. 2) As Fig. 3 shows, the low damped second order nature of the discharge transient causes the current to flow through the diode of the undamaged phase when the DC-link voltage becomes negative. Such a current leads to a negative voltage drop across the IGCT connected in parallel to that specific diode. This negative voltage can be destructive for at least one IGCT junction, if it is not limited.

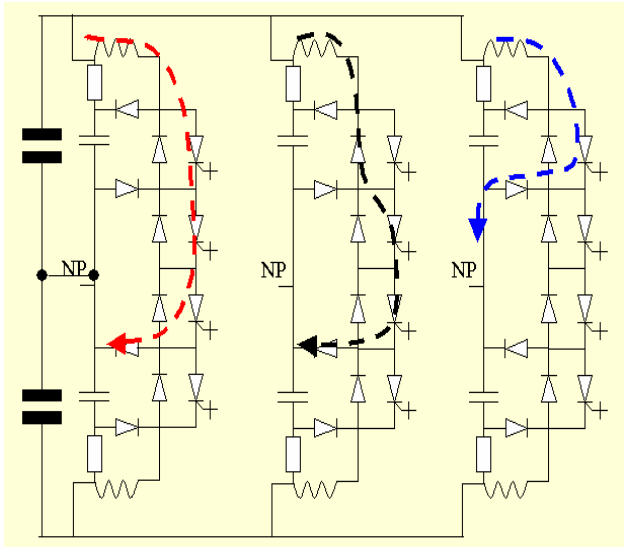


Figure 2. Possible internal short circuit paths

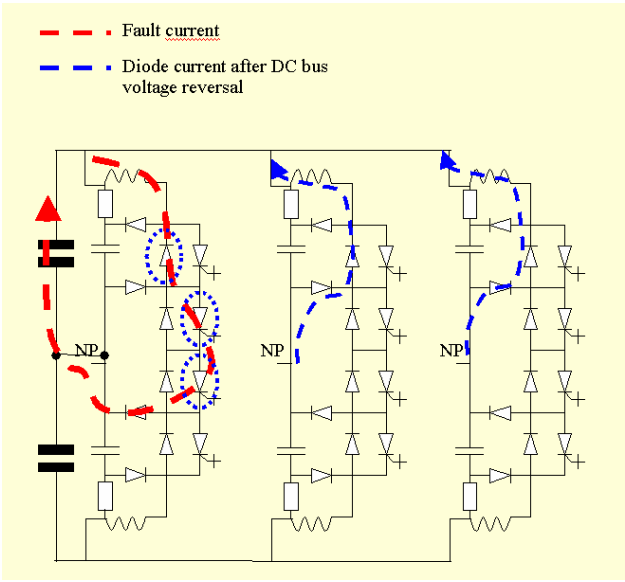


Figure 3. Reverse current on the freewheeling diode

For instance, if the devices used in this application are considered, we see from the related data sheet that the ABB 5SHY 35L4510 Asymmetric IGCT [9] has a maximum reverse voltage equal to 17 V in the off-state and equal to 10 V in the on-state. As regards the Eupec D1331SH Diode [10], it can be derived that fault currents in the order of 10-20 kA can lead to on-state voltages even greater than 10 V.

B. Overvoltage in one DC-link capacitor

As shown in Fig. 4 and Fig. 5, at least two conditions, capable of causing a dangerous increase of the total DC-link voltage, do exist. Both are based on an overvoltage condition in just one DC-link capacitor, which may arise after the action performed by the converter control system in a fault condition.

1. The lock of an internal IGCT in the on state.
2. The rectifying action of the damaged phases in semi DC-link short circuit operation.

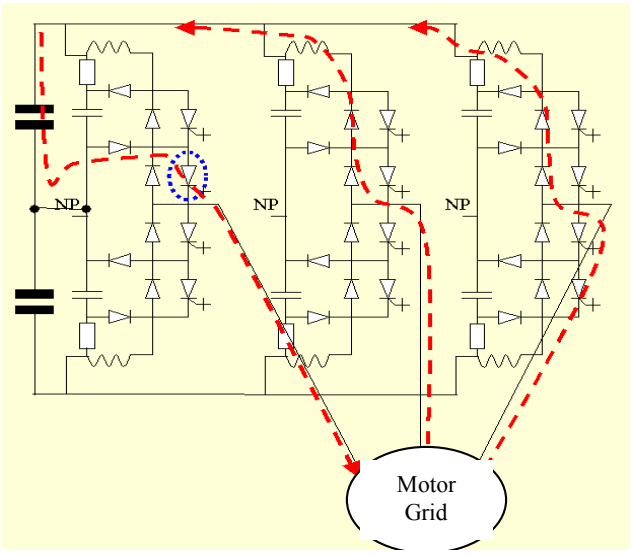


Figure 4. Charging of one semi DC-link capacitor for a lock in on state of an internal IGCT

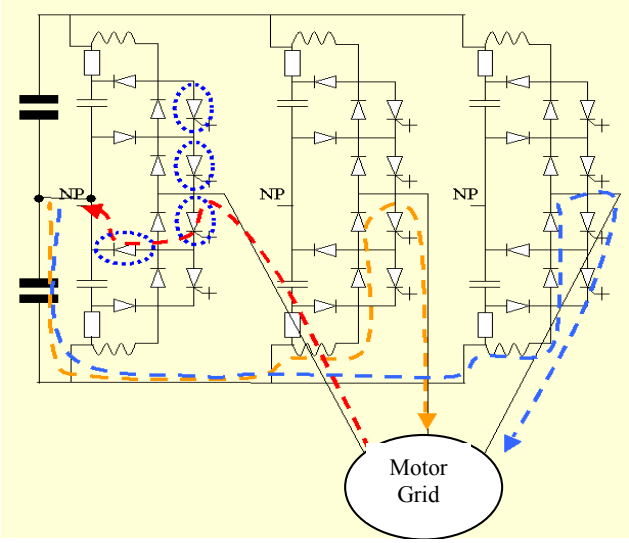


Figure 5. Charging of one semi DC-link capacitor for a short circuit in the semi DC-link

The damages brought by these events depend mainly on the peak of the grid and/or motor voltage.

C. *Lock of one external switch in the on state*

The lock in the on state of an external IGCT (1 or 4) is an event detected by the commutation monitoring circuit present inside the IGCT gate unit. If this happens, the inverter control system turns off all the IGCTs in all phases, with the exception of the internal one (2 or 3) belonging to the same phase in which the locked external IGCT is located.

As shown in Fig. 6 the motor undergoes a symmetrical short-circuit and the current paths in the undamaged phases involve diodes only. The three phase currents can be very different but the capacitor voltages remain constant since no fault current flows in any capacitor. On the other hand high stresses affect the freewheeling diodes, which are subjected to repetitive high reverse voltages and potentially exceeding their maximum I^2t values.

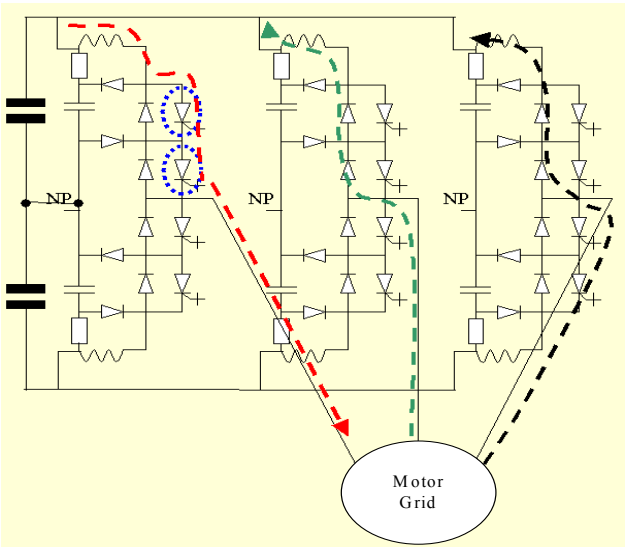


Figure 6. On state fault for an external IGCT

III. PROTECTION CIRCUITS BUILT IN THE POWER CONVERTERS

The protection circuits built inside the power converter are mainly aimed at protecting the DC-link capacitors from overvoltages and the undamaged phases from overcurrents. Two crowbars, as shown in Fig. 7, can be employed: a) The voltage crowbar (VCB), composed by a Light Triggered Thyristor (LTT) and a discharge resistor, b) The current crowbar (CCB), composed by a LTT and a transient-damping RL circuit. The VCB is activated by a specified threshold on the semi DC-link capacitor voltage and its purpose is to clamp such a voltage to a non-dangerous value. The CCB is activated by a specified threshold on the maximum among the first-order time derivatives of the currents flowing in the bus bars. Such derivatives are measured by Rogowski coils properly located inside the converter. The CCB has the purpose to damp and limit the fault current in the short-circuited semi DC-link and mainly to prevent such a current from flowing into phase legs still undamaged.

IV. SELECTED SIMULATION AND EXPERIMENTAL RESULTS

Some simulation tests on the CCB and VCB system have been performed using the PSIM software [11].

The behaviors of the voltages on the semi DC buses of the converter are reported in Fig. 8. At the time instant t = 0 s, a short circuit in the lower semi DC-link bus is set; the voltage on the capacitor bank of the lower DC bus goes down to zero with a low damped second order discharge (Fig. 8(b)), and the voltage on the upper DC bus rises up to a dangerous value (Fig. 8(a)).

The same quantities during the same test, but with the CCB and VCB system in operation, are shown in Fig. 9. When the fault appears, the protection system limits the stresses on the power converter.

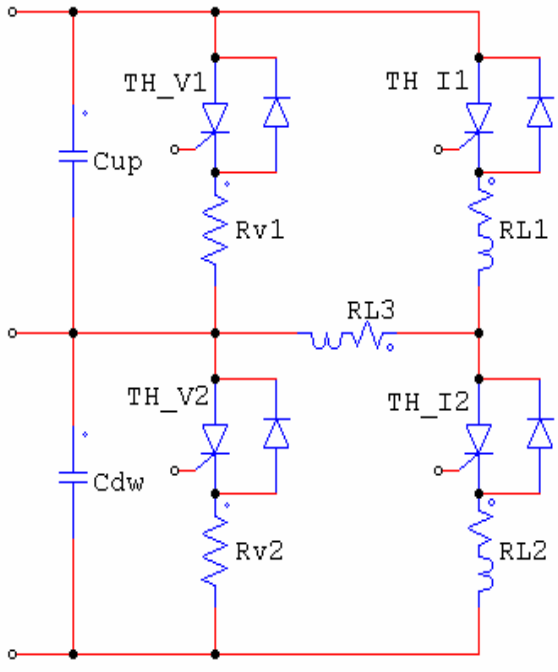
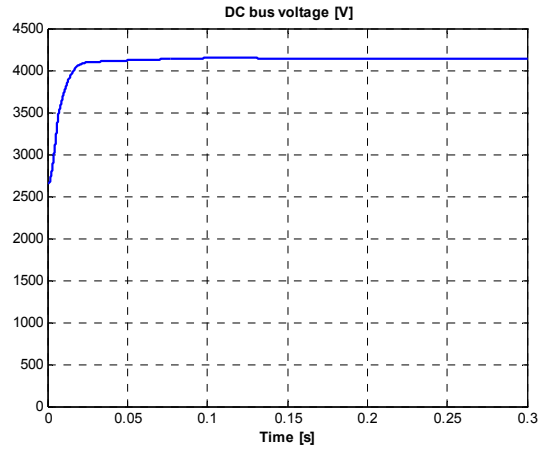
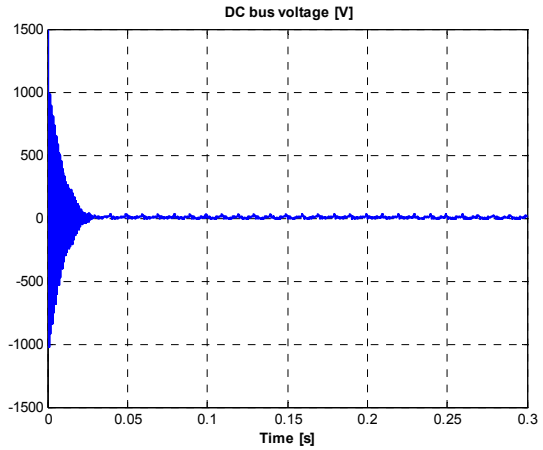


Figure 7. Current crow bar (CCB) TH_I1 TH_I2 and voltage crow bar (VCB) TH_V1 TH_V2

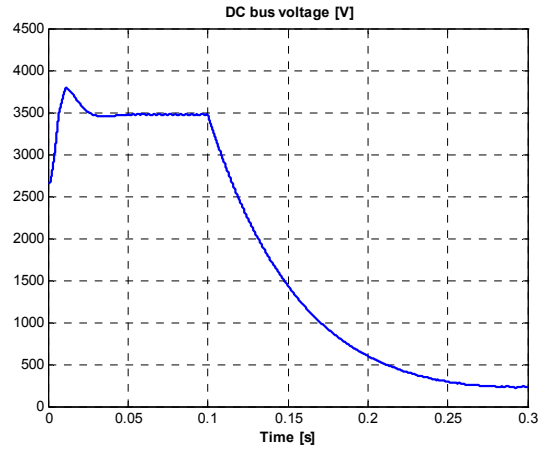


(a)

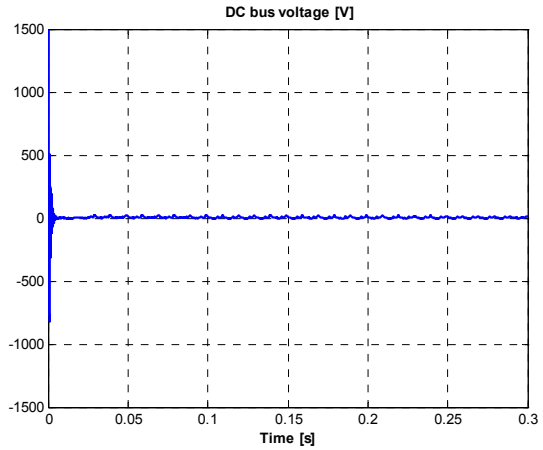


(b)

Figure 8. Voltage on the upper DC bus (a) and on the lower DC bus (b) without CCB and VCB system



(a)



(b)

Figure 9. Voltage on the upper DC bus (a) and on the lower DC bus (b) with CCB and VCB system

The voltage amplitude during the fast discharge transient of the lower capacitor is lower than the previous case, while the voltage on the upper capacitor is limited within a not dangerous value.

The electric components that build the CCB and VCB system have been chosen by using the PSIM simulation software. Particular care has been taken in designing the VCB resistance value. Table I shows the main results that have been obtained, where Rv represents the resistance value, Erv is the energy loss, Vpk_BUS is the maximum semi DC-link voltage and *Vhold is the semi DC-link transient voltage before the intervention of the line breaker. Given the rated voltage value of the DC-link capacitors (equal to 3100 V), a peak value equal to about 3800 V and a transient value lower than 3500 V have been considered adequate. Therefore, in order to also include an additional safety margin and to avoid too big energy losses, the final resistance value has been chosen to be equal to 1.5 Ω. Finally, the current values on the CB thyristor have been checked, as shown in Table II, with reference to the chosen resistance value. In Table II, I2t, Ipk and *Ihold represent, respectively, the squared time-integral of the current (I2t), the peak current and the transient current of the thyristor (the Eupec T4003NH LTT) just before the intervention of the line breaker, compared with the maximum limit values derived from

TABLE I.
VCB RESISTANCE SIZING

Rv [Ω]	Erv [J]	Vpk_BUS [V]	*Vhold [V]
infinite	0	4150	4150
2	8.20E+05	3800	3560
1.7	8.90E+05	3800	3530
1.5	9.50E+05	3800	3470
1.2	1.10E+06	3800	3370

TABLE II.
VCB THYRISTOR CURRENT STRESS

	I2t THY [A2s]	Ipk [A]	*Ihold [A]
Rv = 1.5 [Ω]	6.40E+05	2500	2315
Limit Value	5.00E+07	1.00E+05	7820

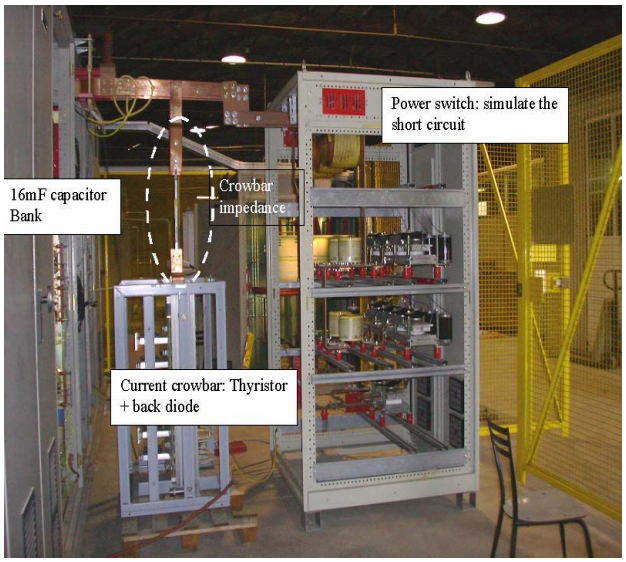


Figure 10. Setup for test on current crowbar (joint laboratory between Ansaldo Sistemi Industriali and University of Genova)

the LTT data-sheet. It can be noted that the values reported in the first row of Table II are considerably lower than the limits reported in the second row, so that the resistance sizing can be considered correct.

It is worth noting that the threshold on the semi DC-link capacitor voltage, related to VCB, and the threshold on the time derivatives of the currents flowing in the bus bars, related to CCB, must be carefully tuned, in order to avoid the undesired activation of the crow bars that cause the semi DC-link short circuit and the temporary stop of the converter system.

Some experimental tests have been performed on a CCB to verify the correct sizing of the circuit components for a 10 MVA (rated power) - 12 MVA (peak power) NPC converter. The experimental setup is composed by a 16mF capacitor bank charged at 3200V. A semi DC-link short circuit has been implemented. The capacitor bank is discharged through the thyristor and the load resistor. Fig. 10 shows a photograph of the experimental setup in the laboratory, whereas an experimental registration is shown in Fig. 11.

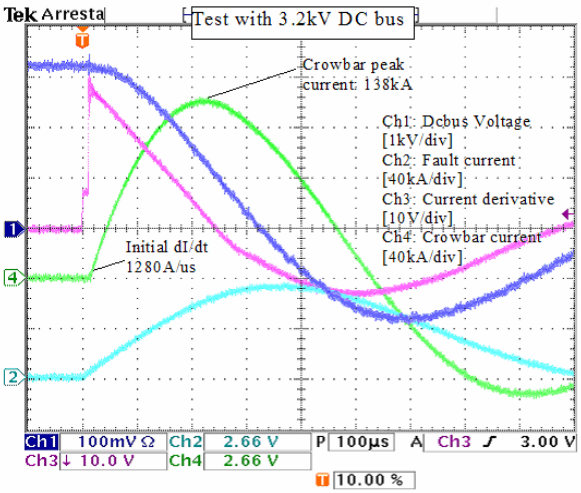


Figure 11. Recorded waveforms during the test on the current crowbar

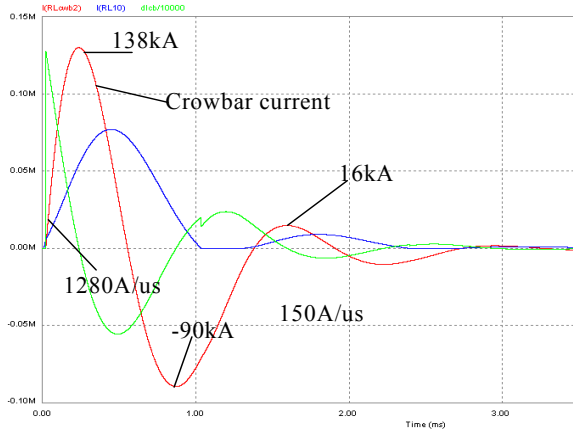


Figure 12. Simulation results related to the test on the current crowbar (same conditions of the experimental test); red line: crowbar current; green line: crowbar current derivative; blue line: fault current

The thyristor is turned on at 12 µs after the trip signal and one can observe that the current rises up to 138 kA. Fig. 12 shows a simulation result related to the same test performed.

V. CONCLUSION

The analysis of faults and the development of adequate remedial strategies is one of the most important aspects that must be carefully considered and investigated when transferring converter systems from research laboratories to the applications. In particular, in multilevel converters, system protection is more difficult when compared to simpler two-level converters, mainly because current fault paths can be much more complex.

A few fault scenarios in a high power (up to 12 MVAs) IGCT based Neutral Point Clamped converter system have been presented and the related proposed remedial strategies have been discussed, while presenting the most significant simulation and experimental results.

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