Modeling, Simulation and Analysis of Three-Level Neutral Point Clamped Inverter Using Matlab/Simulink/Power System Blockset

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Abstract— **Current and voltage harmonics have attracted growing interest with the increase in use of static power converters. These converters produce distorted current and voltage waveforms. The result is harmonic pollution that degrades the power quality. To provide safe operation and to meet harmonic standards such as IEEE 519, it is necessary to eliminate harmonic distortion and improve power quality of the system. This paper presents detailed modeling, simulation and analysis of Neutral Point Clamped Three-level Inverter. Various performance parameters of multilevel inverters have been investigated with three-phase induction motor load. Besides maintaining dc bus voltage balance, a significant reduction is seen in voltage distortion at neutral point in the simulation. The viability of using Three-level Neutral Point Clamped inverter in high power systems is proven by simulation using Matlab/Simulink/Power System Blockset. The space vector modulation (SVM) technique has been employed to get rid of common mode voltages by switching among different states in SVM.**

I. INTRODUCTION

Current and voltage harmonics have attracted growing interest with the increase in use of static power converters. These converters produce distorted current and voltage waveforms. The result is harmonic pollution that degrades the power quality. To provide safe operation and to meet harmonic standards such as IEEE 519 [1], it is necessary to eliminate harmonic distortion and improve power quality of the system. The multilevel inverters have found better counterpart to the conventional 2-level or PWM converter to meet these requirements. Main features of multilevel inverters i.e. less switching stress on devices, reduced harmonic contents, no need of extending the device rating, balanced capacitor voltages, reduced switching losses, reduced dv/dt, reduced (or even eliminated) common mode voltages, eliminate the problem of unequal device ratings and capacitor voltage balancing along with significant reduction in Device Count have motivated to work on this topic [2], [3].

This paper presents detailed modeling, simulation and analysis of Neutral Point Clamped Three-level Inverter. Various performance parameters of multilevel inverters have been investigated with three-phase induction motor load. Besides maintaining dc bus voltage balance, a significant reduction is seen in voltage distortion at neutral point in the simulation.

The viability of using Three-level Neutral Point Clamped inverter in high power systems is proven by simulation using Matlab/Simulink/Power System Blockset. Line voltage and its harmonic spectrum for specific harmonic elimination and line current harmonics for induction motor load are investigated in this paper. THD in line current at different output frequency of inverter, variation of THD with frequency for induction motor load and common mode voltage study have been carried out

Simulation study shows that 5^{th} harmonics is almost absent in the inverter output voltage. As the frequency of output voltage gets increased, harmonic contents in the output current are significantly reduced resulting more near sine wave. By selecting optimal firing angle of each switching device, low order harmonics can be reduced or even eliminated from the output. DC link capacitor voltage unbalancing problem has been rectified in the presented work.

Modulation index has a strong influence on the performance of neutral point clamped inverter. In this work an optimal value of modulation index has been derived to get much better performance. Common mode voltages are produced in conventional two-level inverter and commonly used multilevel inverters. Common mode voltages may induce motor shaft voltages, bearing currents and electromagnetic interference resulting in premature motor bearing failures [4], [5] and [6]. In this paper, a novel space vector modulation (SVM) technique has been employed to get rid of common mode voltages by switching among different states in SVM.

II. THREE LEVEL NEUTRAL POINT CLAMPED INVERTER

Three-level inverter has the advantages of having low harmonic distortion, low switching frequency, and lower common mode voltages, near sinusoidal output voltage, less requirement of filtering and above all it reduces the danger of motor failure due to high frequency switching dv/dt [6], [7] and [8]. Fig (1) shows three-phase three-level diode clamped inverter. It consists of capacitors, switching devices, dc voltage source and clamping diodes. Middle point of two capacitors is defined as neutral point. The output voltage has three states: $V_{dc}/2$, 0 and $-V_{dc}/2$ for 3-level NPC or five states: V_{dc}, $3V_{dc}/4$, $V_{dc}/2$, $V_{dc}/4$ and 0. To synthesize 3-level output phase voltage, switching sequence as given in Table I will be used. Table I gives the switch states for a-phase. Similar switching sequence will be derived for other phases taking into account for phase delays among phases. Thus three level inverter is used in high voltage, high power ac drives.

State condition 1 means switch ON and 0 means switch OFF. Fig (2) shows the phase and line voltage of 3-level diode clamped VSI. Now, it is clear that an m-level diode

clamped inverter consists of (m-1) capacitors on dc bus, output phase voltage has m-levels and output line voltage has (2m-1)-levels. Each active switching device has to withstand a blocking voltage of $V_{dc}/(m-1)$, even then clamping diode must have different voltage ratings for reverse voltage blocking. The number of diodes required for each phase will be (m-1) × (m-2).

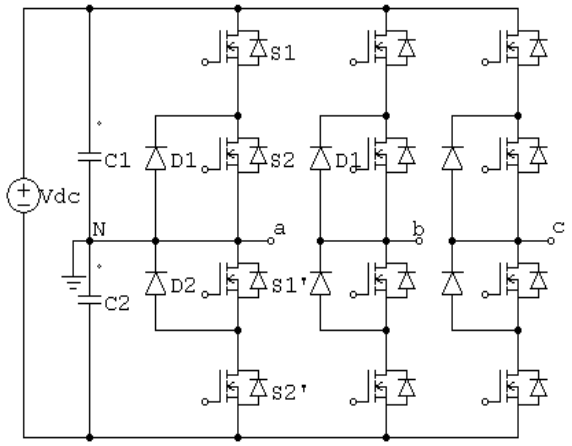
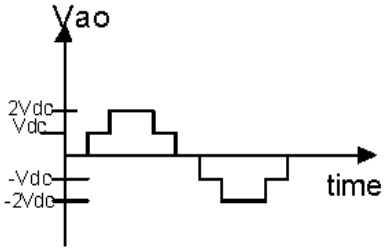


Fig (1) Three-phase, Three-Level Diode Clamped Inverter

From Table I, it is clear that when both the upper switches S_1 and S_2 are closed, full supply voltage will be available across the load. If two central switches S_1' and S_2 are closed then half of dc supply voltage will be obtained and zero voltage will be applied across load if lower switches S_1' and S_2' are closed. This switching strategy is used in the presented work.



Fig(2) Output phase voltage of 3-level NPCinverter

From harmonic reduction and high dc link voltage, three-level inverter approach seems to be most promising altemative. The harmonic content of a three level inverter are less than that of a two level inverter at the same switching frequency and the blocking voltages of the switching devices will be half of the dc link voltage.

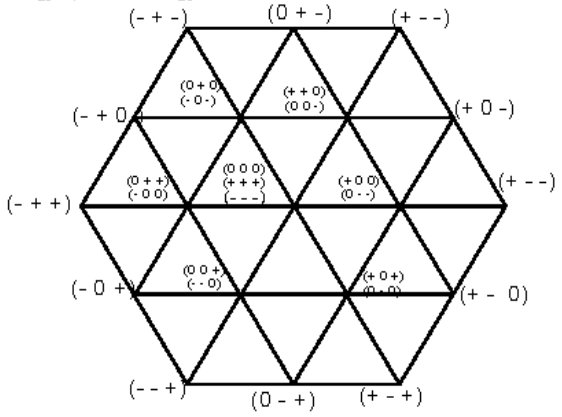
III DEVELOPMENT OF SPACE VECTOR MODULATION

The output stage of two level PWM inverters consists of three phase legs with two switches on each leg. Like conventional inverters, the main aim of the control strategy of multilevel inverters is to synthesize the output voltage as close as possible to the sinusoidal waveform. Many modulation techniques have been developed for harmonic reduction and switching loss minimization. However the conventional SPWM and the space vector modulation are still considered good choices for multilevel PWM inverters due to the overall improved performance. Therefore, detailed study of various performance indices of NPC VSI is presented in the paper.

TABLE I
THREE -LEVEL NPC INVERTER OUTPUT VOLTAGE LEVELS & THEIR SWITCHNIG STATES

Output Pole Voltage (Vao)	Switch States			
	S_1	S_2	S_1'	S_2'
0	0	0	1	1
$V_{dc}/2$	0	1	1	0
V_{dc}	1	1	0	0
$V_{dc}/2$	0	1	1	0

The basic idea of voltage space vector modulation is to control the inverter output voltages so that their Parks representation will be approximately equals the reference voltage vector. In the case of two level inverter, the output of each phase will be either $+V_{dc}/2$ or $-V_{dc}/2$. Therefore, the combination of three phase output voltages will result in 8 (2^3) switching states, i.e. (++-), (+--), (-++), (-+-), (+-+), (--+), (+++) & (---), where + means $+V_{dc}/2$ and – means $-V_{dc}/2$ voltage in the output voltage. There are two important features of Neutral Point Clamped (NPC) VSI compared to conventional two level inverters. First, four switches are used in series for each inverter leg instead of two. This will allow the off-state switches to sustain only half of the dc-bus voltage instead of full voltage. Second, the output voltage of each phase has three levels, i.e. $+V_{dc}/2$, 0 and $-V_{dc}/2$.



Fig(3) Possible Switching States of Three-Level Diode Clamped Inverter

An increased number of voltage levels results in increased switching states. In three-level NPC-VSI there are 27(3^3) states which creates 19 voltage vectors including a zero voltage vector as shown in Fig (3). These voltage vectors divides d-q plane into 24 triangular sections. When reference voltage vector falls in one of these sections, adjacent voltage vectors are selected to synthesize the desired voltage vector based on time averaging principle [3], [5], [6].

There are so many switching states in case of three-level inverters which causes very complex selection of switching state and the generation of switching pattern will be more difficult. So in this paper, focus will be on

generating the switching sequence to achieve improved inverter performance.

To produce desired performance, vectors are selected such that two zero vectors and two active vectors form the boundary of the sector in which the sample is located.

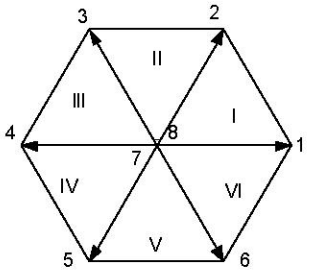


Fig (4) Sectors and Switching States of two level inverter.

As in the case of two level inverters with space vector modulation, durations for each vector have been calculated. We have the following equations governing the whole principle of space vector modulation for three-level inverter,

$$Vm1 = Vref.\sin(\omega t),$$
$$Vm2 = Vref.\sin(\omega t - 2\pi/3),$$
$$Vm2 = Vref.\sin(\omega t + 2\pi/3),$$
$$Va = (V1 - V2)/2,$$
$$Vb = (V2 - V3)/2,$$
$$Vc = (V3 - V1)/2,$$

Therefore the common mode voltage V_{com} is expressed as,

$$Vcom = (Va + Vb + Vc)/3 = 0$$

IV. SIMULATION

A. Basic Scheme:

Basic control block diagram is shown in fig (5). Simulation has been performed in Matlab/Simulink. Fig (6) and (7) shows the voltage waveform and total harmonic distortion in line voltage with 5th harmonics eliminated. THD was found to be 16.46%. Fig (8) shows output current wave of induction motor fed from three level inverter. Fig (9) indicates that with the increase in frequency, THD will decrease significantly. Fig (10) gives the harmonic spectrum of output current at 80 Hz frequency with THD of 9.29%. Simulation study shows that 5th harmonics is almost absent in the inverter output voltage.

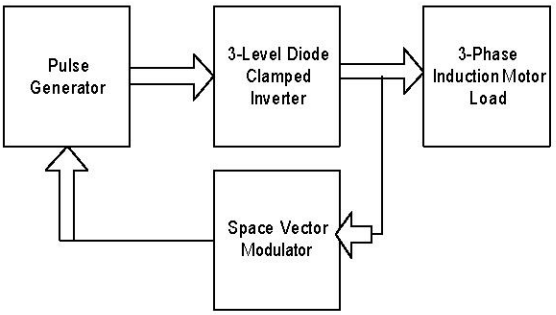


Fig (5) Block diagram of scheme.

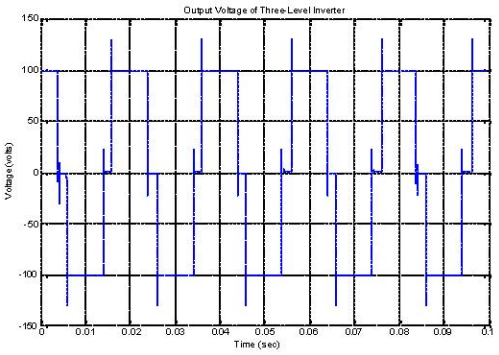


Fig (6) Output Phase Voltage of Three-Level Diode Clamped Inverter.

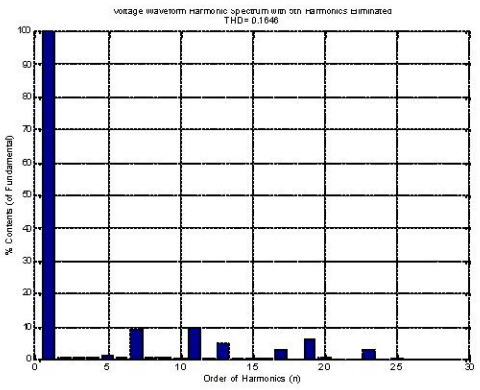


Fig (7) Line Voltage Waveform Harmonic Spectrum with 5th Harmonics Eliminated, THD = 16.46%

As the frequency of output voltage gets increased, harmonic contents in the output current are significantly reduced resulting more near sine wave. In this work an optimal value of modulation index has been derived to get much better performance. Common mode voltages are produced in conventional two-level inverter and commonly used multilevel inverters. Common mode voltages may induce motor shaft voltages, bearing currents and electromagnetic interference resulting in premature motor bearing failures [4], [5] and [9].

Fourier transform for line to line voltage output will be,

$$V(\omega t) = \frac{(4Vdc/\pi)\sum[\cos(n\theta 1) + \cos(n\theta 2) + ... + \cos(n\theta r)]\sin(n\omega t)]\sin(n\omega t)/n}{\pi}$$

.....(1)

when n = 1, 3, 5, 7, ….

Now the conduction angles are chosen so that the total harmonic distortion is minimum. Conduction angles $?_1$, $?_2$, $?_3$, …. $?_s$ can be calculated from equations formed as given below. For three level inverter, two equations can be o btained,

$$\cos(5\,?_1) + \cos(5\,?_2) = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots(2)$$
$$\cos(?_1) + \cos(?_2) = 2m_a \quad \ldots\ldots\ldots\ldots\ldots\ldots(3)$$

where, m_a is the modulation index. A Matlab program has been written to find out switching instants. The values of $?_1$ and $?_2$ have been found to be 14.744103^0 and 50.761725^0 for m_a of 0.8. Harmonic spectrum of fig(7) shows that 5^{th} harmonic is almost absent from the line voltage output. Fig (11) shows the simulation diagram made in Matlab for analysis purpose. This diagram is used to derive three phase version of inverter.

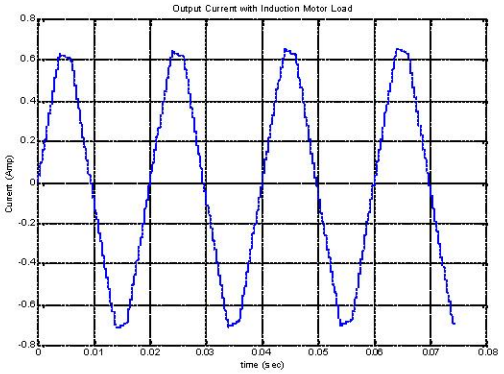


Fig (8) Output Current with Inductive Load R=10 O, L=600 mH

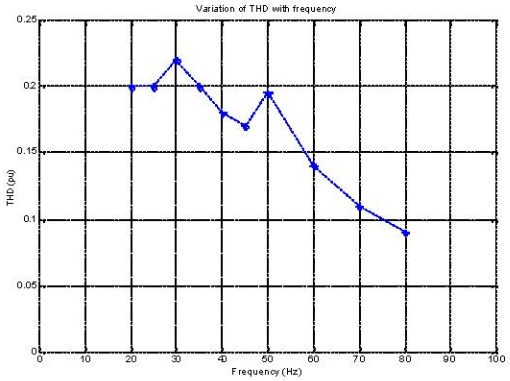


Fig (9) Variation of THD with frequency for Induction Motor supplied from three-level inverter.

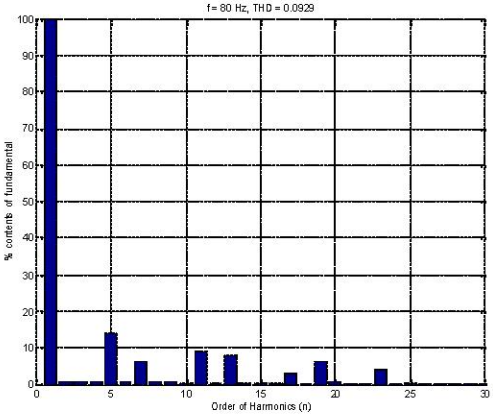


Fig (10) Harmonic spectrum at 80 Hz frequency and THD = 9.29%

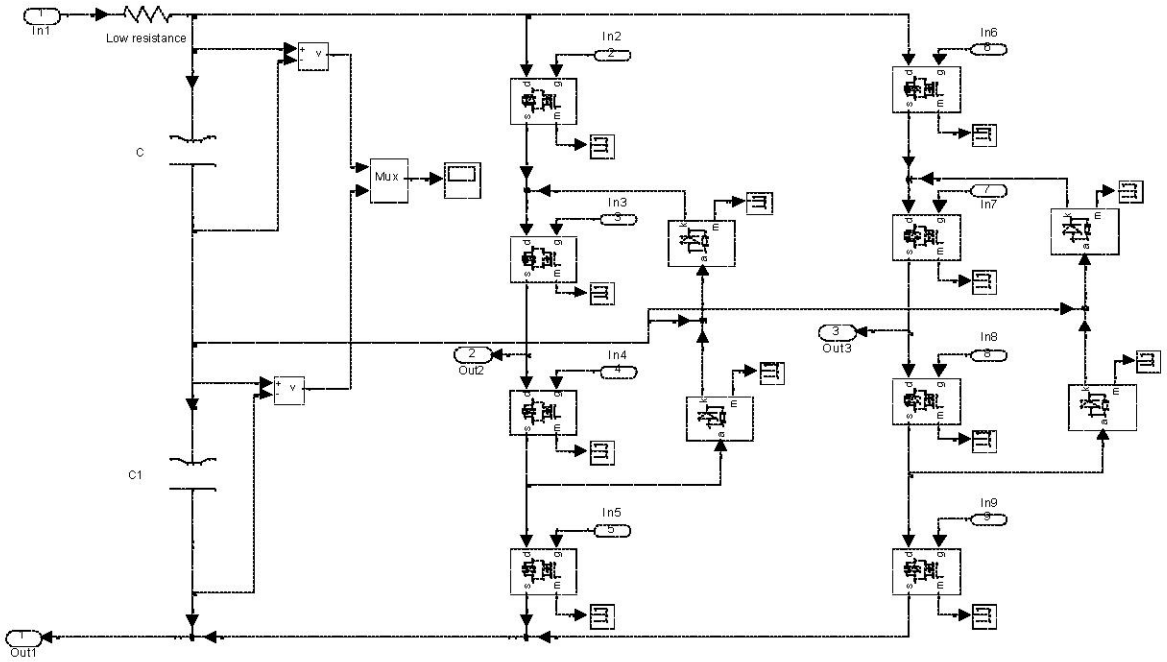


Fig (11) Matlab Diagram of Three-level Diode Clamped Inverter for single phase applications

Now the power factor for a fixed frequency is varied and the effect on the THD has been observed. Study shows that for low value of inductance or for power factor close to unity, THD is high. With the increase of inductance, the steps in output voltage smoothen out, reducing THD. This is due to filtering action of machine inductance. The effect of power factor on THD is shown in fig (12) and (13).

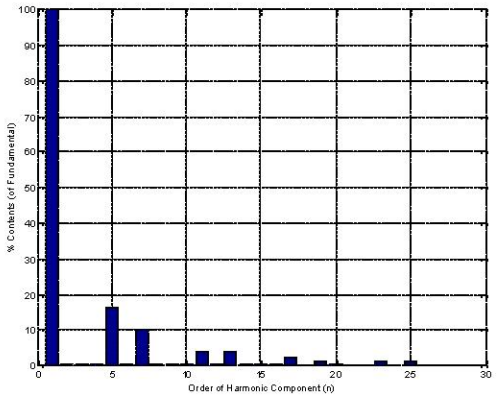


Fig (12) Harmonic spectrum of current waveform at a power factor of 0.9878, THD= 19.79%

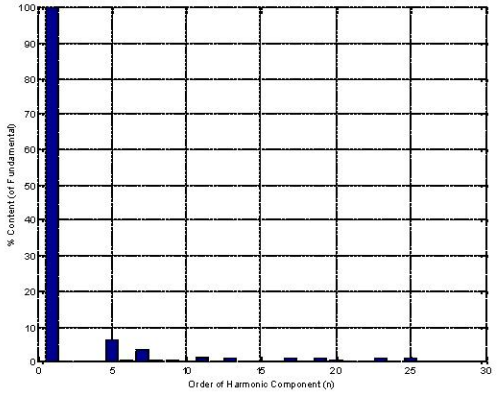


Fig (13) Harmonic spectrum of current waveform at a power factor of 0.6730, THD=6.17%

IV. CONCLUSION

Modeling, simulation and analysis of three-level diode clamped inverter is presented for induction motor load in Matlab environment. Space vector modulation has been presented to achieve zero common mode voltage and 5^{th} harmonic elimination. Line voltage, line current and their harmonic spectrum for specific harmonic elimination have been presented. Variation of THD with frequency, variation of THD with power factor for induction motor load have also been presented. Study also shows the capacitor voltage balancing.

Simulation study shows that 5^{th} harmonics is almost absent in the inverter output voltage. As the frequency of output voltage gets increased, harmonic contents in the output current are significantly reduced resulting more near sine wave. By selecting optimal firing angle of each switching device, low order harmonics can be reduced or even eliminated from the output. DC link capacitor voltage unbalancing problem has been rectified in the presented work. Common mode voltages are produced in conventional two-level inverter and commonly used multilevel inverters. Common mode voltages may induce motor shaft voltages, bearing currents and electromagnetic interference resulting in premature motor bearing failures.

In future work focus will be on DC link voltage control, Neutral Point voltage control and On-line Modulation Index control.

ACKNOWLEDGMENT

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REFERENCES

[1] Pradeep M. Bhagwat, V. R. Stefanovic, "Generalized Structure of a Multilevel Inverter", IEEE Trans. on Industrial Applications, Vol 19, No. 6, Nov/Dec 1983, pp 1057-1069.

[2] T. Salzmann, G. Kratz, C. Daubler, "High Power Drive System with Advanced Power Circuitry and Improved Digital Control", IEEE Trans. on Industrial Applications, Vol 29, No. 1, Jan/Feb 1993.

[3] F. Zeng Peng, "A Generalized Multilevel Inverter Topology with Self Voltage Balancing", IEEE Trans on Industry Applications, Vol. 37, No. 2, Mar/Apr 2001, pp 611-618.

[4] H. Zhang, A.V. Jouanne, S. Dai, A.K. Wallace, F. Wang, "Multilevel Inverter Modulation Schemes to Eliminate Common-Mode Voltages", IEEE Trans on Industry Applications, Vol. 36, No. 6, Nov/Dec 2000, pp 1645-1653.

[5] Leon M. Tolbert, Fang Z. Peng, T.G. Habetler, "Multilevel Converters for Large Electric Drives", IEEE Trans on Industry Applications, Vol. 35, No. 1, Jan/Feb 1999, pp 36-44.

[6] J.S. Lai, F.Z. Peng, "Multilevel Converters – A New Breed of Power Converters", IEEE Trans. on Industry Applications, Vol. 32, No. 3, May/Jun 1996, pp 509-517.

[7] T.A. Meynard and H. Foch, "Multilevel Conversions: High Voltage Choppers and Voltage Source Inverters", IEEE-PESC, 1992, pp. 397-403.

[8] J. Rodriguez, J.S. Lai, Fang Z. Peng, "Multilevel Inverters: A Survey of Topologies, Controls and Applications", IEEE Trans on Industrial Electronics, Vol 49, No 4, Aug 2002, pp 724-738.

[9] Leon M. Tolbert, T.G. Habetler, "Novel Multilevel Inverter Carrier-Based PWM Methods", IEEE IAS Annual Meeting, Oct. 10-15, 1998, pp 1424-1431.

[10] Surjeet Ghani Lalla, "Simulation and Performance Investigation of Multilevel Inverter Fed Induction Motor", M .Tech Thesis, Indian Institute of Technology, Roorkee, Uttaranchal, India, Feb 2003.