



User's Manual

ECOUSB™ Series

μPD720114

USB 2.0 Hub Controller



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[MEMO]

① **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② **HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ **PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ **STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ **POWER ON/OFF SEQUENCE**

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ **INPUT OF SIGNAL DURING POWER OFF STATE**

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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Major Revisions in this Edition

Page	Description
p. 48	Change of Table 6-4. Absolute Maximum Ratings

The mark <R> shows major revised points.

The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

PREFACE

Readers	This manual is intended for engineers who need to be familiar with the capability of the μ PD720114 in order to develop application systems based on it.												
Purpose	The purpose of this manual is to help users understand the hardware capabilities (listed below) of the μ PD720114.												
Configuration	<p>This manual consists of the following chapters:</p> <ul style="list-style-type: none">• Introduction• Pin functions• Descriptors information• USB requests information• How to connect to external discrete components• Product specifications• Application information												
Guidance	Readers of this manual should already have a general knowledge of electronics, logic circuits, and microcomputers.												
Notation	<p>This manual uses the following conventions:</p> <table><tr><td>Data bit significance:</td><td>High-order bits on the left side; low-order bits on the right side</td></tr><tr><td>Active low:</td><td>XXXXB (Pin and signal names are suffixed with B.)</td></tr><tr><td>Note:</td><td>Explanation of an indicated part of text</td></tr><tr><td>Caution:</td><td>Information requiring the user's special attention</td></tr><tr><td>Remark:</td><td>Supplementary information</td></tr><tr><td>Numerical value:</td><td>Binary ... xxxx or xxxxb Decimal ... xxxx Hexadecimal ... xxxh</td></tr></table>	Data bit significance:	High-order bits on the left side; low-order bits on the right side	Active low:	XXXXB (Pin and signal names are suffixed with B.)	Note:	Explanation of an indicated part of text	Caution:	Information requiring the user's special attention	Remark:	Supplementary information	Numerical value:	Binary ... xxxx or xxxxb Decimal ... xxxx Hexadecimal ... xxxh
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Related Document	<p>Use this manual in combination with the following document.</p> <p>The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.</p> <p>μPD720114 Data Sheet: S17462E</p>												

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CHAPTER 1 INTRODUCTION

The μ PD720114 is a USB 2.0 hub device that complies with the Universal Serial Bus (USB) Specification Revision 2.0 and works up to 480 Mbps. USB2.0 compliant transceivers are integrated for upstream and all downstream ports. The μ PD720114 works backward compatible either when any one of the downstream ports is connected to a USB 1.1 compliant device, or when the upstream port is connected to a USB 1.1 compliant host.

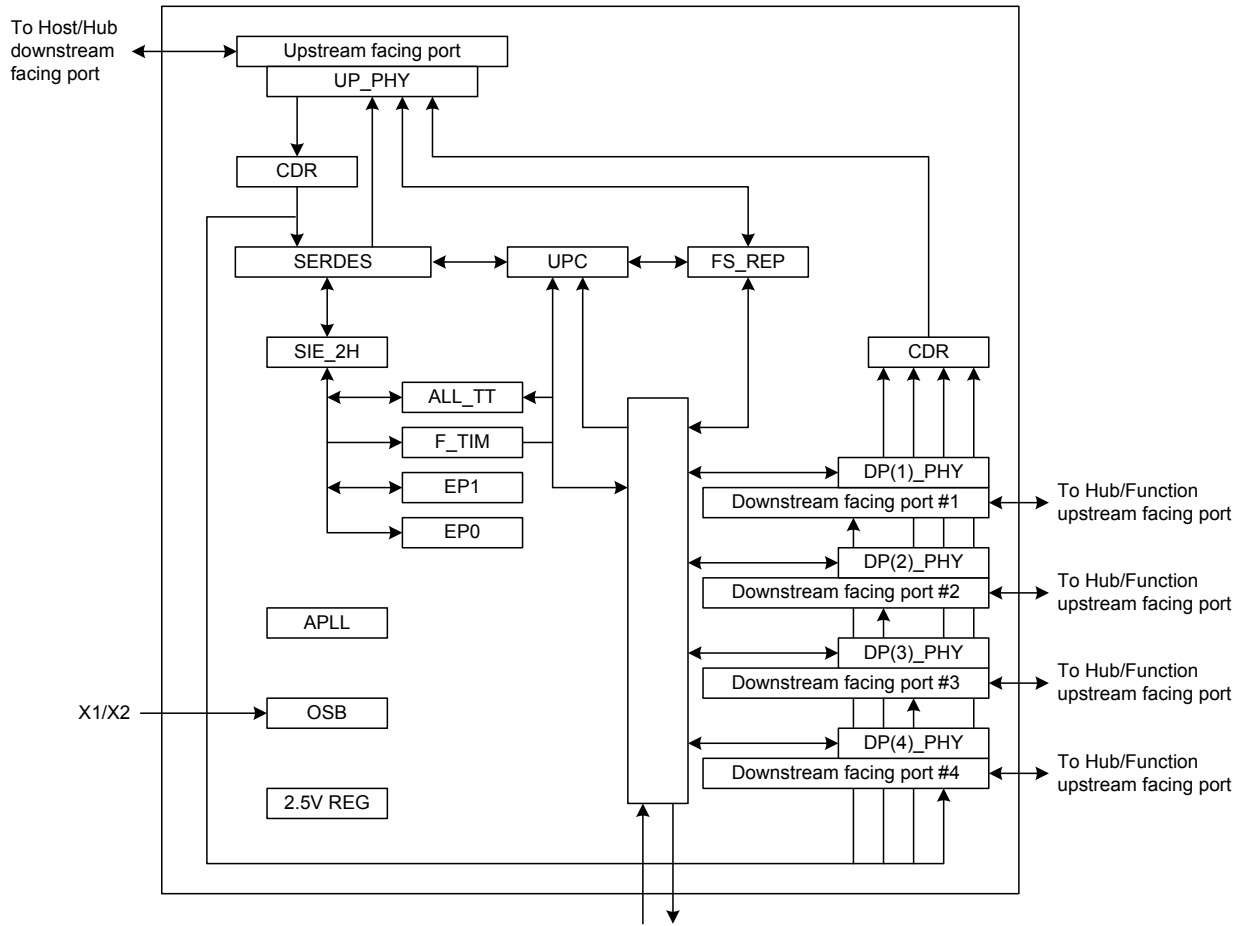
1.1 Features

- Compliant with Universal Serial Bus Specification Revision 2.0 (Data Rate 1.5/12/480 Mbps)
- High-speed or full-speed packet protocol sequencer for Endpoint 0/1
- 4 (Max.) downstream facing ports
- Low power consumption (10 μ A when hub in idle status, 149 mA when all parts run in HS mode)
- All downstream facing ports can handle high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) transaction.
- Supports split transaction to handle full-speed and low-speed transaction on downstream facing ports when Hub controller is working in high-speed mode.
- One Transaction Translator per Hub and supports four non-periodic buffers
- Supports self-powered and bus-powered mode
- Supports individual or global over-current detection and individual or ganged power control
- Supports downstream port status with LED
- Supports non-removable devices by I/O pin configuration
- Support Energy Star for PC peripheral system
- On chip Rpu, Rpd resistors and regulator (for core logic)
- Use 30 MHz crystal
- 3.3 V power supply

1.2 Ordering Information

Part Number	Package	Remark
μ PD720114GA-9EU-A	48-pin plastic TQFP (Fine pitch) (7 \times 7)	Lead-free product
μ PD720114GA-YEU-A	48-pin plastic TQFP (Fine pitch) (7 \times 7)	Lead-free product

1.3 Block Diagram



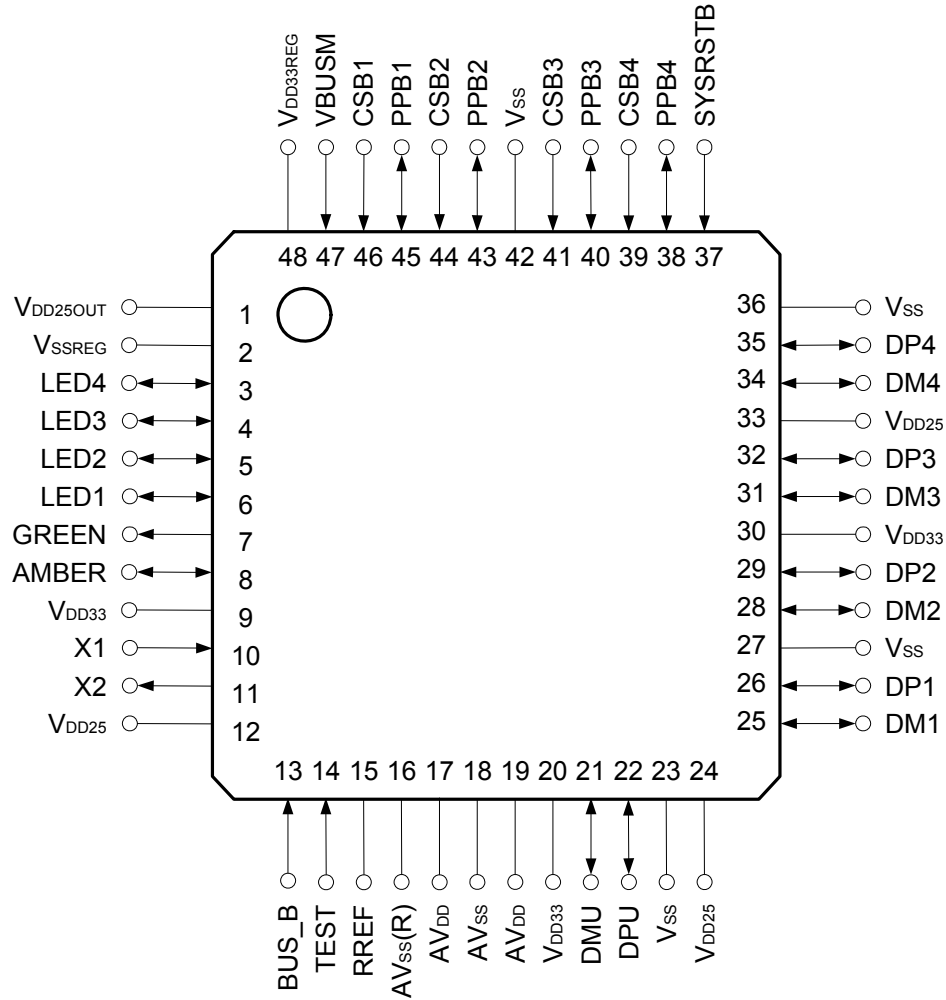
APLL	: Generates all clocks of Hub.
ALL_TT	: Translates the high-speed transactions (split transactions) for full/low-speed device to full/low-speed transactions. ALL_TT buffers the data transfer from either upstream or downstream direction. For OUT transaction, ALL_TT buffers data from upstream port and sends it out to the downstream facing ports after speed conversion from high-speed to full/low-speed. For IN transaction, ALL_TT buffers data from downstream ports and sends it out to the upstream facing ports after speed conversion from full/low-speed to high-speed.
CDR	: Data & clock recovery circuit
DPC	: Downstream Port Controller handles Port Reset, Enable, Disable, Suspend and Resume
DP(n)_PHY	: Downstream transceiver supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) transaction
EP0	: Endpoint 0 controller
EP1	: Endpoint 1 controller
F_TIM (Frame Timer)	: Manages hub's synchronization by using micro-SOF which is received at upstream port, and generates SOF packet when full/low-speed device is attached to downstream facing port.
FS_REP	: Full/low-speed repeater is enabled when the μ PD720114 is worked at full-speed mode
OSB	: Oscillator Block
2.5V REG	: On chip 2.5V regulator
SERDES	: Serializer and Deserializer
SIE_2H	: Serial Interface Engine (SIE) controls USB2.0 and 1.1 protocol sequencer.
UP_PHY	: Upstream Transceiver supports high-speed (480 Mbps), full-speed (12 Mbps) transaction
UPC	: Upstream Port Controller handles Suspend and Resume

1.4 Pin Configuration (Top View)

- 48-pin plastic TQFP (Fine pitch) (7 × 7)

μ PD720114GA-9EU-A

μ PD720114GA-YEU-A



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V _{DD25OUT}	13	BUS_B	25	DM1	37	SYSRSTB
2	V _{SSREG}	14	TEST	26	DP1	38	PPB4
3	LED4	15	RREF	27	V _{SS}	39	CSB4
4	LED3	16	AV _{SS} (R)	28	DM2	40	PPB3
5	LED2	17	AV _{DD}	29	DP2	41	CSB3
6	LED1	18	AV _{SS}	30	V _{DD33}	42	V _{SS}
7	GREEN	19	AV _{DD}	31	DM3	43	PPB2
8	AMBER	20	V _{DD33}	32	DP3	44	CSB2
9	V _{DD33}	21	DMU	33	V _{DD25}	45	PPB1
10	X1	22	DPU	34	DM4	46	CSB1
11	X2	23	V _{SS}	35	DP4	47	VBUSM
12	V _{DD25}	24	V _{DD25}	36	V _{SS}	48	V _{DD33REG}

Remark AV_{SS}(R) should be used to connect RREF through 1 % precision reference resistor of 2.43 kΩ.

1.5 Pin Information

Pin Name	I/O	Buffer Type	Active Level	Function
X1	I	2.5 V input		30 MHz crystal oscillator in
X2	O	2.5 V output		30 MHz crystal oscillator out
SYSRSTB	I	3.3 V Schmitt input	Low	Asynchronous chip hardware reset
DP(4:1)	I/O	USB D+ signal I/O		USB's downstream facing port D+ signal
DM(4:1)	I/O	USB D- signal I/O		USB's downstream facing port D- signal
DPU	I/O	USB D+ signal I/O		USB's upstream facing port D+ signal
DMU	I/O	USB D- signal I/O		USB's upstream facing port D- signal
BUS_B	I	3.3 V Schmitt input		Power mode select
RREF	A (O)	Analog		Reference resistor connection
CSB1	I	5 V tolerant Schmitt input	Low	Port's over-current status input
CSB(4:2)	I	3.3 V Schmitt input	Low	Port's over-current status input
PPB(4:1)	I/O	3.3 V output/input	Low	Port's power supply control output or hub configuration input
VBUSM	I	5 V tolerant Schmitt input		Upstream V _{BUS} monitor
AMBER	I/O	3.3V output/input		Amber colored LED control output or port indicator select
GREEN	O	3.3V output		Green colored LED control output or port indicator select
LED(4:1)	I/O	3.3V output/input	Low	LED indicator output show downstream port status or Removable/Non-removable select
TEST	I	3.3 V Schmitt input		Test signal
V _{DD25OUT}				On chip 2.5 V output, supply the V _{DD25} for the chip self, it must have a 22 μ F (or greater) capacitor to V _{SSREG} .
V _{DD33}				3.3 V V _{DD}
V _{DD33REG}				3.3 V V _{DD} for on chip 2.5 V regulator input, it must have a 4.7 μ F (or greater) capacitor to V _{SSREG}
V _{DD25}				2.5 V V _{DD} , These pins must be supplied from V _{DD25OUT} , output from internal regulator
AV _{DD}				2.5 V V _{DD} for analog circuit
V _{SS}				V _{SS}
V _{SSREG}				On chip 2.5 V regulator V _{SS}
AV _{SS}				V _{SS} for analog circuit
AV _{SS} (R)				V _{SS} for reference resistor, Connect to AV _{SS} .

Remark "5 V tolerant" means that the buffer is 3 V buffer with 5 V tolerant circuit.

CHAPTER 2 PIN FUNCTIONS

The pin type describes a signal either as analog, power, input, or I/O (bi-directional).

2.1 Power Supply

Pin	Pin No.	Direction	Function
V _{DD33}	9, 20, 30	Power	+3.3 V power supply
V _{DD33REG}	48	Power	+3.3 V power supply for on chip 2.5 V regulator input, it must have a 4.7 μ F (or greater) capacitor to V _{SSREG} .
V _{DD25}	12, 24, 33	Power	+2.5 V core power line, it must have a 0.1 μ F (or greater) capacitor to V _{SS} . These pins must be supplied from V _{DD25OUT} , output from internal regulator
V _{DD25OUT}	1	Power	On chip 2.5 V output, supply the V _{DD25} for the chip self, it must have a 22 μ F (or greater) capacitor to V _{SSREG} .
AV _{DD}	17, 19	Power	+2.5 V analog circuit power line, it must have a 0.1 μ F (or greater) capacitor to V _{SS} .
V _{SS}	23, 27, 36, 42	Power	Ground
V _{SSREG}	2	Power	Ground for on chip 2.5 V regulator
AV _{SS}	18	Power	Ground for analog circuit
AV _{SS} (R)	16	Power	Ground for reference resistor

Remark Self-Powered Hub System requires the capability of providing 500 mA for each downstream facing port. And additional power consumption of Hub Controller itself and other components in the Hub System should also be considered for overall power requirement. A power source that is able to supply at least 2.5 A may be best for a 4 port Self-Powered Hub System.

2.2 Analog Signaling

Pin	Pin No.	Direction	Function
RREF	15	Analog	RREF must be connected a 1 % precision reference resistor of 2.43 k Ω . The other side of the resistor must be connected to AV _{SS} (R) which must then it must be connected to AV _{SS} .

2.3 System Clock & Reset

Pin	Pin No.	Direction	Function
X1	10	I	Oscillator crystal input. Connect to 30-MHz crystal
X2	11	O	Oscillator crystal output. Connect through a series resistor to other end of 30-MHz crystal.
SYSRSTB	37	I	Asynchronous active low reset signal

2.4 USB Hub Interface

Pin	Pin No.	Direction	Function
CSB(4:1)	39, 41, 44, 46	I	Over-current status input of the downstream facing ports. 1: No over-current condition detected. 0: Over-current condition detected. If the pin is not used, connect to GND or V _{DD33} .
PPB(4:1)	38, 40, 43, 45	I/O	Power supply control output for downstream facing ports (open-drain). 1: Power supply OFF 0: Power supply ON By strapping PPB(4:1) pins before system reset (see Chapter 5 and 7), the active ports, power management mode and bPwrOn2PwrGood descriptor can configure as below: PPB [4:3] = 00: 2 downstream facing ports active. = 01: 3 downstream facing ports active = 11: 4 downstream facing ports active PPB2 = 0: ganged power management mode = 1: individual power management mode PPB1 = 0: bPwrOn2PwrGood = 00h(0 ms, with no power switches) = 1: bPwrOn2PwrGood = 32h(100 ms)
VBUSM	47	I	Upstream Vbus monitor.
LED(4:1)	3, 4, 5, 6	I/O	Connect to downstream facing port status indicator LED (open drain). See Figure 5-5. LED Connection . If port indicator is not used, connect GREEN to AMBER directly. The LED(4:1) can configure for removable/non-removable selection: 0: Removable 1: Non-removable
AMBER	8	I/O	Connect to amber colored LED. See Figure 5-5. LED Connection . The meaning of amber colored LED is described in section 4.6 PORT_INDICATOR . If port indicator is not used, connect it to GREEN directly.
GREEN	7	O	Connect to green colored LED. See Figure 5-5. LED Connection . The meaning of green colored LED is described in section 4.6 PORT_INDICATOR . If port indicator is not used, connect it to AMBER directly.

Remark VBUSM pin may be used to monitor the V_{BUS} line even if V_{DD33} is shut off. For example, the internal Rpu for the DPU pin is powered by VBUSM for port speed indication. The input voltage level for VBUSM pin should be less than 3.3 V in order not to exceed the absolute maximum rating. Refer to **Figure 5-1. USB Upstream Port Connection** and use voltage divider resistors to monitor V_{BUS}.

2.5 USB Interface

Pin	Pin No.	Direction	Function
DP(4:1)	35, 32, 29, 26	I/O	Connect to downstream port D+ signal line. If not using the downstream port, connect to GND.
DM(4:1)	34, 31, 28, 25	I/O	Connect to downstream port D– signal line. If not using the downstream port, connect to GND.
DPU	22	I/O	Connect to upstream facing port D+ signal line.
DMU	21	I/O	Connect to upstream facing port D– signal line.

2.6 System Interface

Pin	Pin No.	Direction	Function
BUS_B	13	I	Select power mode 0: Bus-powered 1: Self-powered

2.7 Test Signals

Pin	Pin No.	Direction	Caution
TEST	14	I	Should be tied to GND on circuit board.

CHAPTER 3 DESCRIPTORS INFORMATION

This chapter describes the descriptors implemented in hub controller. The μ PD720114 has following descriptors. Host reads these descriptors by using Get Descriptor request.

- Device Descriptor
- Device Qualifier Descriptor
- Configuration Descriptor
- Interface Descriptor
- Endpoint Descriptor
- Other Speed Configuration Descriptor
- Hub Class-specific Descriptor

The hub returns different descriptors depending on whether it is operating at high-speed or full-speed. The following section shows descriptor sets for full-speed operation and high-speed operation.

3.1 Device Descriptor

The hub returns Device descriptor by GET_DESCRIPTOR (Device) request.

Offset	Field Name	Full-speed	High-speed	Description
0	bLength	12h	12h	18 bytes
1	bDescriptorType	01h	01h	
2	bcdUSB	0200h	0200h	USB specification 2.0
4	bDeviceClass	09h	09h	Hub
5	bDeviceSubClass	00h	00h	
6	bDeviceProtocol	00h	01h	Single TT for high-speed
7	bMxPacketSize0	40h	40h	64 bytes
8	idVendor	0409h	0409h	"NEC"
10	idProduct	005Ah	005Ah	"USB 2.0 Hub Controller"
12	bcdDevice	0100h	0100h	"1.00"
14	iManufacturer	00h	00h	
15	iProduct	00h	00h	
16	iSerialNumber	00h	00h	
17	bNumConfigurations	01h	01h	One configuration

3.2 Device_Qualifier descriptor

The hub returns Device_Qualifier descriptor by GET_DESCRIPTOR (Device_Qualifier) request.

Offset	Field Name	Full-speed	High-speed	Description
0	bLength	0Ah	0Ah	10 bytes
1	bDescriptorType	06h	06h	
2	bcdUSB	0200h	0200h	USB specification 2.0
4	bDeviceClass	09h	09h	Hub
5	bDeviceSubClass	00h	00h	
6	bDeviceProtocol	01h	00h	Single TT for high-speed
7	bMaxPacketSize0	40h	40h	64 bytes
8	bNumConfigurations	01h	01h	
9	bReserved	00h	00h	

3.3 Configuration descriptor

The hub returns Configuration descriptor by GET_DESCRIPTOR (Configuration) request.

Offset	Field Name	Full-speed	High-speed	Description
0	bLength	09h	09h	9 bytes
1	bDescriptorType	02h	02h	
2	wTotalLength	0019h	0019h	25 bytes
4	bNumInterfaces	01h	01h	One interface
5	bConfigurationValue	01h	01h	
6	iConfiguration	00h	00h	
7	bmAttributes	E0h	E0h	
8	bMaxPower	32h	32h	100 mA

3.4 Interface descriptor

The hub returns Configuration descriptor followed by Interface descriptor.

Offset	Field Name	Full-speed	High-speed	Description
0	bLength	09h	09h	9 bytes
1	bDescriptorType	04h	04h	
2	bInterfaceNumber	00h	00h	
3	bAlternateSetting	00h	00h	
4	bNumEndpoints	01h	01h	
5	bInterfaceClass	09h	09h	
6	bInterfaceSubClass	00h	00h	
7	bInterfaceProtocol	00h	00h	
8	iInterface	00h	00h	

3.5 Endpoint descriptor

The hub returns Configuration/Interface descriptor followed by Endpoint descriptor.

Offset	Field Name	Full-speed	High-speed	Description
0	bLength	07h	07h	7 bytes
1	bDescriptorType	05h	05h	
2	bEndpointAddress	81h	81h	EP1, IN direction
3	bmAttributes	03h	03h	Interrupt endpoint
4	wMaxPacketSize	0001h	0001h	1 byte
6	bInterval	FFh	0Ch	Polling interval

3.6 Other_Speed_Configuration descriptor

The hub returns Other_Speed_Configuration descriptor by GET_DESCRIPTOR (Other_Speed_Configuration) request.

Offset	Field Name	Full-speed	High-speed	Description
0	bLength	09h	09h	9 bytes
1	bDescriptorType	07h	07h	
2	wTotalLength	0019h	0019h	25 bytes
4	bNumInterfaces	01h	01h	
5	bConfigurationValue	01h	01h	
6	iConfiguration	00h	00h	
7	bmAttributes	E0h	E0h	
8	bMaxPower	32h	32h	100 mA

3.7 String descriptors

The μ PD720114 doesn't support string descriptors, it will return "STALL" by GET_DESCRIPTOR (string) request.

3.8 Class Specified – Hub Class Descriptor

The hub returns Hub Class descriptors by GetHubDescriptor request.

Offset	Field Name	Value	Description	Pin configuration
0	bDescLength	09h	9 bytes	
1	bDescriptorType	29h	Hub	
2	bNbrPorts	04h 03h 02h	4 downstream facing ports 3 downstream facing ports 2 downstream facing ports	PPB [4:3] = 11 PPB [4:3] = 01 PPB [4:3] = 00
3	wHubCharacteristics	01b (D1:D0)	Individual port power switching	PPB2 = 1
		00b (D1:D0)	Ganged power switching	PPB2 = 0
		0b (D2)	Not compound device	All LEDx = 0 ^{Note 1}
		1b (D2)	Compound device	Any LEDx = 1
		01b (D4:D3)	Individual port over-current protection	PPB2 = 1
		00b (D4:D3)	Global over-current protection	PPB2 = 0
		01b (D6:D5)	TT Think Time is 16 FS bit time	
		1b (D7)	Support PORT_INDICATOR	LED connected ^{Note 2}
		0b	PORT_INDICATOR not support	GREEN = AMBER
5	bPwrOn2PwrGood	32h 00h	100 ms 0 ms	PPB1 = 1 ^{Note 3} PPB1 = 0
6	bHubContrCurrent	64h	Hub's current is "100 mA"	
7	DeviceRemovable	0b	Reserved	
		0b (D1)	Device is removable	LED1 = 0 ^{Note 1}
		1b (D1)	Device is not removable	LED1 = 1
		0b (D2)	Device is removable	LED2 = 0 ^{Note 1}
		1b (D2)	Device is not removable	LED2 = 1
		0b (D3)	Device is removable	LED3 = 0 ^{Note 1}
		1b (D3)	Device is not removable	LED3 = 1
		0b (D4)	Device is removable	LED4 = 0 ^{Note 1}
		1b (D4)	Device is not removable	LED4 = 1
8	PortPwrCtrlMask	FFh		

Notes 1. When port indicator is not used, connect GREEN to AMBER directly and the LED(4:1) can configure for removable/non-removable selection. Else if port indicator is used, connect LED with **Figure 5-5**, the downstream facing port of μ PD720114 will be fixed at removable.

2. When LEDs are connected (see **Figure 5-5**), μ PD720114 will report D7 of wHubCharacteristics with "1b" to host PC. Else if LEDs are not used, connect GREEN to AMBER directly; μ PD720114 will report D7 of wHubCharacteristics with "0b" to host PC.

3. Bus-powered hub requires power switches. PPBx are for power switch control (see **Figure 5-3**). For low BOM cost self-powered hub design with no power switches (over current protection by polymeric PTC for logical power switching mode), set PPB2 = PPB1 = 0 (see **Figure 5-4**), bPwrOn2PwrGood is set at 0. It complies with the USB Specification.

CHAPTER 4 USB REQUESTS INFORMATION

When the μ PD720114 is connected to a downstream facing port of a USB2.0 host controller or USB2.0 Hub, it operates in high-speed mode on the upstream facing port. The μ PD720114 uses USB2.0 high-speed protocols to communicate with other USB2.0 devices. On the other hand, when the μ PD720114 is connected to a downstream facing port of a USB1.x host controller or USB1.x Hub, it operates in full-speed mode. The μ PD720114 uses USB2.0 full-speed protocols to communicate with the upstream controller.

- Handles setup transactions for Endpoint 0 which are controlled by the hub itself.
- Repeats setup transactions to other devices.
- Handles interrupt transactions for Endpoint 1 which retrieve status change information
- Repeats interrupt transactions to other devices.
- Repeats bulk transactions to other devices.
- Repeats isochronous transactions to other devices.
- Translates split transactions for USB1.X devices which are attached to the downstream facing port.
- Repeats split transactions to a USB2.0 hub which is attached to the downstream facing port.

This section describes requests supported by the μ PD720114 default descriptor setting. Please refer to Chapter 9 and 11 in the USB specification rev. 2.0 for further detail.

4.1 Standard Requests

The μ PD720114 supports all standard requests except for SET_DESCRIPTOR() and SYNCH_FRAME(). The following table shows the standard requests at the default setting.

(1/2)

Request	bmRequestType	bRequest	wValue	wIndex	wLength	Return
CLEAR_FEATURE (Device: Remote Wakeup)	00000000b	01h	0001h	0000h	0000h	None
CLEAR_FEATURE (Endpoint 0 Halt)	00000010b	01h	0000h	0000h / 0080h	0000h	None
CLEAR_FEATURE (Endpoint 1 Halt)	00000010b	01h	0000h	0081h	0000h	None
GET_CONFIGURATION	10000000b	08h	0000h	0000h	0001h	Current configuration value
GET_DESCRIPTOR (Device)	10000000b	06h	0100h	0000h	0012h ^{Note}	Device descriptor
GET_DESCRIPTOR (Configuration)	10000000b	06h	0200h	0000h	0019h ^{Note}	Configuration / Interface / Endpoint descriptors
GET_DESCRIPTOR (Device_Qualifier)	10000000b	06h	0600h	0000h	000Ah ^{Note}	Device_Qualifier

Note The wLength field specifies the number of bytes to return. If the data to be returned is longer than the wLength field, only wLength bytes of the descriptor are returned. If the data to be returned is shorter than the wLength field, the device ends the control transfer by sending a short packet when more data is requested.

(2/2)

Request	bmRequestType	bRequest	wValue	wIndex	wLength	Return
GET_DESCRIPTOR (Other_Speed_Configuration)	10000000b	06h	0700h	0000h	0019h Note	Other_Speed_Configuration
GET_INTERFACE	10000001b	0Ah	0000h	0000h	0001h	00h
GET_STATUS (Device)	10000000b	00h	0000h	0000h	0002h	Device status
GET_STATUS (Interface)	10000001b	00h	0000h	0000h	0002h	0000h
GET_STATUS (Endpoint 0)	10000010b	00h	0000h	0000h/ 0080h	0002h	Endpoint 0 status
GET_STATUS (Endpoint 1)	10000010b	00h	0000h	0081h	0002h	Endpoint 1 status
SET_ADDRESS	00000000b	05h	0000h to 007Fh	0000h	0000h	None
SET_CONFIGURATION	00000000b	09h	0000h/ 0001h	0000h	0000h	None
SET_FEATURE (Device: Remote Wakeup)	00000000b	03h	0001h	0000h	0000h	None
SET_FEATURE (Endpoint 0 Halt)	00000010b	03h	0000h	0000h/ 0080h	0000h	None
SET_FEATURE (Endpoint 1 Halt)	00000010b	03h	0000h	0081h	0000h	None
SET_FEATURE (Test_J)	00000000b	03h	0002h	0100h	0000h	None
SET_FEATURE (Test_K)	00000000b	03h	0002h	0200h	0000h	None
SET_FEATURE (Test_SE0_NAK)	00000000b	03h	0002h	0300h	0000h	None
SET_FEATURE (Test_Packet)	00000000b	03h	0002h	0400h	0000h	None
SET_FEATURE (Test_Force_Enable)	00000000b	03h	0002h	0500h	0000h	None
SET_INTERFACE	00000001b	0Bh	0000h	0000h	0000h	None

Note The wLength field specifies the number of bytes to return. If the data to be returned is longer than the wLength field, only wLength bytes of the descriptor are returned. If the data to be returned is shorter than the wLength field, the device ends the control transfer by sending a short packet when more data is requested.

4.2 Class-Specific Requests

The μ PD720114 supports all class-specific requests except for SetHubDescriptor() and GetBusState(). The following table shows the class-specific requests at the default descriptor setting.

(1/2)

Request	bmRequestType	bRequest	wValue	wIndex	wLength	Return
ClearHubFeature (C_HUB_OVER_CURRENT)	00100000b	01h	0001h	0000h	0000h	None
ClearHubFeature (C_HUB_LOCAL_POWER)	00100000b	01h	0000h	0000h	0000h	None
ClearPortFeature (PORT_ENABLE)	00100011b	01h	0001h	0001h to 0004h	0000h	None
ClearPortFeature (PORT_SUSPEND)	00100011b	01h	0002h	0001h to 0004h	0000h	None
ClearPortFeature (PORT_POWER)	00100011b	01h	0008h	0001h to 0004h	0000h	None
ClearPortFeature (PORT_INDICATOR)	00100011b	01h	0016h	Note 1	0000h	None
ClearPortFeature (C_PORT_CONNECTION)	00100011b	01h	0010h	0001h to 0004h	0000h	None
ClearPortFeature (C_PORT_RESET)	00100011b	01h	0014h	0001h to 0004h	0000h	None
ClearPortFeature (C_PORT_ENABLE)	00100011b	01h	0011h	0001h to 0004h	0000h	None
ClearPortFeature (C_PORT_SUSPEND)	00100011b	01h	0012h	0001h to 0004h	0000h	None
ClearPortFeature (C_PORT_OVER_CURRENT)	00100011b	01h	0013h	0001h to 0004h	0000h	None
GetHubDescriptor	10100000b	06h	2900h	0000h	0009h Note 2	Hub descriptor
GetHubStatus	10100000b	00h	0000h	0000h	0004h	Hub status and change indicators. Refer to section 4.4.

Notes 1. The high byte of the wIndex field is the selector identifying the specific indicator. And the low byte of the wIndex field shows port number. Refer to **4.6 PORT_INDICATOR** for details.

Value	Port Indicator Color	Port Indicator Mode
0h	Default	Automatic
1h	Amber	Manual
2h	Green	
3h	Off	
4h to FFh	Reserved	Reserved

2. The wLength field specifies the number of bytes to return. If the data to be returned is longer than the wLength field, only wLength bytes of the descriptor are returned. If the data to be returned is shorter than the wLength field, the device ends the control transfer by sending a short packet when more data is requested.

(2/2)

Request	bmRequestType	bRequest	wValue	wIndex	wLength	Return
GetPortStatus	10100011b	00h	0000h	0001h to 0004h	0004h	Port status and change indicators. Refer to section 4.5.
SetPortFeature (PORT_RESET)	00100011b	03h	0004h	0001h to 0004h	0000h	None
SetPortFeature (PORT_SUSPEND)	00100011b	03h	0002h	0001h to 0004h	0000h	None
SetPortFeature (PORT_POWER)	00100011b	03h	0008h	0001h to 0004h	0000h	None
SetPortFeature (PORT_TEST: Test_J)	00100011b	03h	0015h	0101h to 0104h	0000h	None
SetPortFeature (PORT_TEST: Test_K)	00100011b	03h	0015h	0201h to 0204h	0000h	None
SetPortFeature (PORT_TEST: Test_SE0_NAK)	00100011b	03h	0015h	0301h to 0304h	0000h	None
SetPortFeature (PORT_TEST: Test_Packet)	00100011b	03h	0015h	0401h to 0404h	0000h	None
SetPortFeature (PORT_TEST: Test_Force_Enable)	00100011b	03h	0015h	0501h to 0504h	0000h	None
SetPortFeature (PORT_INDICATOR)	00100011b	03h	0016h	Note 1	0000h	None
ClearTTBuffer	00100011b	08h	Note 2	0001h	0000h	None
GetTTState	10100011b	0Ah	0000h	0001h	08D0h	TT state
ResetTT	00100011b	09h	0000h	0001h	0000h	None
StopTT	00100011b	0Bh	0000h	0001h	0000h	None

Notes 1. The high byte of the wIndex field is the selector identifying the specific indicator. And the low byte of the wIndex field shows port number. Refer to 4.6 **PORT_INDICATOR** for details.

Value	Port Indicator Color	Port Indicator Mode
0h	Default	Automatic
1h	Amber	Manual
2h	Green	
3h	Off	
4h to FFh	Reserved	Reserved

2. The wValue for ClearTTBuffer is as follows.

Bits	Field
3..0	Endpoint Number
10..4	Device Address
12..11	Endpoint Type
14..13	Reserved, must be zero
15	Direction, 1 = IN, 0 = OUT

4.3 The Response for Each Transaction

USB specification rev. 2.0 states the device behavior in some states and conditions are not specified. The section describes the response of the μ PD720114 in each state and condition at default setting.

(1/2)

Request		Condition				
		Default state	Address state	Configured state	Endpoint 0 halted	Invalid wValue
Standard Requests						
CLEAR_FEATURE						
	Device	STALL *	Request accepted	Request accepted	Request accepted	STALL
	Endpoint 0	STALL *	Request accepted	Request accepted	Request accepted	STALL
	Endpoint 1	STALL *	STALL	Request accepted	Request accepted	STALL
GET_CONFIGURATION		STALL *	Return data	Return data	STALL	STALL *
GET_DESCRIPTOR ^{Note}						
	Device	Return data	Return data	Return data	STALL	STALL
	Configuration	Return data	Return data	Return data	STALL	STALL
	String	STALL	STALL	STALL	STALL	STALL
	Device Qualifier	Return data	Return data	Return data	STALL	STALL
	Other Speed Configuration	Return data	Return data	Return data	STALL	STALL
GET_INTERFACE		STALL *	STALL	Return data	STALL	STALL *
GET_STATUS						
	Device	STALL *	Return data	Return data	Return data	STALL *
	Interface	STALL *	STALL	Return data	Return data	STALL *
	Endpoint 0	STALL *	Return data	Return data	Return data	STALL *
	Endpoint 1	STALL *	STALL	Return data	Return data	STALL *
SET_ADDRESS		Request accepted	Request accepted	STALL *	STALL	STALL *
SET_CONFIGURATION		STALL *	Request accepted	Request accepted	STALL	STALL *
SET_FEATURE						
	Device	STALL *	Request accepted	Request accepted	Request accepted	STALL
	Endpoint 0	STALL *	Request accepted	Request accepted	Request accepted	STALL
	Endpoint 1	STALL *	STALL	Request accepted	Request accepted	STALL
	TEST_MODE in HS mode	Request accepted	Request accepted	Request accepted	Request accepted	STALL
	TEST_MODE in FS mode	STALL	STALL	STALL	STALL	STALL
SET_INTERFACE		STALL *	STALL	Request accepted	STALL	STALL
Other Standard Requests		STALL	STALL	STALL	STALL	STALL

Note The wLength field specifies the number of bytes to return. If the data to be returned (or internal state of TT) is longer than the wLength field, only wLength bytes of the data (or internal state of TT) are returned. If the data to be returned (or internal state of TT) is shorter than the wLength field, the device ends the control transfer by sending a short packet when more data is requested.

(2/2)

Request		Condition				
		Default state	Address state	Configured state	Endpoint 0 halted	Invalid wValue
Class-specific Requests						
ClearHubFeature						
	C_HUB_LOCAL_POWER	No response *	No response *	Request accepted	Request accepted	STALL
	C_HUB_OVER_CURRENT	No response *	No response *	Request accepted	Request accepted	STALL
ClearPortFeature		No response *	No response *	Request accepted	Request accepted	STALL
GetHubDescriptor ^{Note 1, 2}		Return data *	Return data *	Return data	Return data	STALL
GetHubStatus		No response *	No response *	Return data	Return data	STALL
GetPortStatus		No response *	No response *	Return data	Return data	STALL
SetPortFeature ^{Note 3}						
	Except for <i>TEST_MODE</i>	No response *	No response *	Request accepted	Request accepted	STALL
	<i>TEST_MODE</i> in HS mode	No response *	No response *	Request accepted	Request accepted	STALL
	<i>TEST_MODE</i> in FS mode	STALL	STALL	STALL	STALL	STALL
ClearTTBuffer						
	In HS mode	No response *	No response *	Request accepted	Request accepted	Note 4
	In FS mode	STALL	STALL	STALL	STALL	STALL
GetTTState ^{Note 1}						
	In HS mode	No response *	No response *	Return data	Return data	STALL
	In FS mode	STALL	STALL	STALL	STALL	STALL
ResetTT						
	In HS mode	No response *	No response *	Request accepted	Request accepted	STALL
	In FS mode	STALL	STALL	STALL	STALL	STALL
StopTT						
	In HS mode	No response *	No response *	Request accepted	Request accepted	STALL
	In FS mode	STALL	STALL	STALL	STALL	STALL
Other Class-specific Requests		STALL	STALL	STALL	STALL	STALL
Normal transaction						
Interrupt for Endpoint 1		-	-	Return data	Return data	-

- Notes**
1. The wLength field specifies the number of bytes to return. If the data to be returned (or internal state of TT) is longer than the wLength field, only wLength bytes of the data (or internal state of TT) are returned. If the data to be returned (or internal state of TT) is shorter than the wLength field, the device ends the control transfer by sending a short packet when more data is requested.
 2. If the hub is not configured, the hub's response to GetHubDescriptor request is undefined in USB specification. The μ PD720114 will return data for the GetHubDescriptor request even in default or address state. It will not decode wValue field for GetHubDescriptor request and will ignore that field.
 3. When the downstream facing port is in *TEST_MODE*, the μ PD720114 returns ACK handshake for another SetPortFeature (*TEST_MODE*), but it discards that request. When the downstream facing port is in *TEST_MODE*, the μ PD720114 does not respond for SetFeature (*TEST_MODE*). When the port is not in Disable, Disconnect, or Suspend State, the μ PD720114 returns STALL handshake for SetPortFeature (*TEST_MODE*).
 4. The μ PD720114 decodes only bit14 and bit 13 for wValue field of ClearTTBuffer request. If wValue[14:13] does not match "00b", the μ PD720114 will return STALL handshake. On the other hand,

If wValue[14:13] matches “00b”, the μ PD720114 will return ACK handshake. And if the buffer for device address and endpoint number contained in wValue does not exist, this request will be ignored.

(1/2)

Request		Condition		
		Invalid wIndex	Invalid wLength	Endpoint 1 halted
Standard Requests				
CLEAR_FEATURE				
	Device	STALL	STALL *	-
	Endpoint 0	STALL	STALL *	-
	Endpoint 1	STALL	STALL *	-
GET_CONFIGURATION		STALL *	STALL *	-
GET_DESCRIPTOR ^{Note}				
	Device	STALL	-	-
	Configuration	STALL	-	-
	String	STALL	-	-
	Device Qualifier	STALL	-	-
	Other Speed Configuration	STALL	-	-
GET_INTERFACE		STALL	STALL *	-
GET_STATUS				
	Device	STALL *	STALL *	-
	Interface	STALL	STALL *	-
	Endpoint 0	STALL	STALL *	-
	Endpoint 1	STALL	STALL *	-
SET_ADDRESS		STALL *	STALL *	-
SET_CONFIGURATION		STALL *	STALL *	-
SET_FEATURE				
	Device	STALL	STALL *	-
	Endpoint 0	STALL	STALL *	-
	Endpoint 1	STALL	STALL *	-
	TEST_MODE in HS mode	STALL *	STALL *	-
	TEST_MODE in FS mode	STALL	STALL	-
SET_INTERFACE		STALL	STALL *	-
Other Standard Requests		STALL	STALL	-

Note The wLength field specifies the number of bytes to return. If the data to be returned (or internal state of TT) is longer than the wLength field, only wLength bytes of the data to be returned (or internal state of TT) are returned. If the data to be returned (or internal state of TT) is shorter than the wLength field, the device ends the control transfer by sending a short packet when more data is requested.

(2/2)

Request		Condition		
		Invalid wIndex	Invalid wLength	Endpoint 1 halted
Class-specific Requests				
ClearHubFeature		STALL	STALL	-
ClearPortFeature		STALL	STALL	-
GetHubDescriptor ^{Note 1, 2}		STALL	-	-
GetHubStatus		STALL	STALL	-
GetPortStatus		STALL	STALL	-
SetPortFeature ^{Note 3}				
	Except for <i>TEST_MODE</i>	STALL	STALL	-
	<i>TEST_MODE</i> in HS mode	STALL	STALL	-
	<i>TEST_MODE</i> in FS mode	STALL	STALL	-
ClearTTBuffer				
	In HS mode	STALL	STALL	-
	In FS mode	STALL	STALL	-
GetTTState ^{Note 1}				
	In HS mode	STALL	-	-
	In FS mode	STALL	STALL	-
ResetTT				
	In HS mode	STALL	STALL	-
	In FS mode	STALL	STALL	-
StopTT				
	In HS mode	STALL	STALL	-
	In FS mode	STALL	STALL	-
Other Class-specific Requests		STALL	STALL	-
Normal transaction				
Interrupt for Endpoint 1		-	-	STALL

- Notes**
1. The wLength field specifies the number of bytes to return. If the data (or internal state of TT) is longer than the wLength field, only wLength bytes of the data (or internal state of TT) are returned. If the data (or internal state of TT) is shorter than the wLength field, the device ends the control transfer by sending a short packet when more data is requested.
 2. If the hub is not configured, the hub's response to GetHubDescriptor request is undefined in USB specification. The μ PD720114 will return data for the GetHubDescriptor request even in default or address state. It will not decode wValue field for GetHubDescriptor request and will ignore that field.
 3. When the downstream facing port is in *TEST_MODE*, the μ PD720114 returns ACK handshake for another SetPortFeature (*TEST_MODE*), but it discards that request. When the downstream facing port is in *TEST_MODE*, the μ PD720114 does not respond for SetFeature (*TEST_MODE*). When the port is not in Disable, Disconnect, or Suspend State, the μ PD720114 returns STALL handshake for SetPortFeature (*TEST_MODE*).

- Remarks**
1. Asterisk (*) indicates that “Not Specified” or “undefined” is described in USB specification rev. 2.0.
 2. The requests, which are defined in USB specification rev. 2.0, are undefined in full-speed mode. So, the μ PD720114 will return STALL handshake for these requests when it is operating in full-speed mode.
 3. When μ PD720114's upstream facing port is in *TEST_MODE*, the μ PD720114 can not respond for any request.
 4. In high-speed mode, 4 additional requests for Transaction translator are provided.

Request	Function
ClearTTBuffer	Clears the state of a Transaction Translator (TT) bulk/control buffer after it has been left in a busy state due to high-speed errors. After successful completion of this request, the buffer can again be used by the TT with high-speed split transaction for full/low-speed transactions to attached full-/low-speed device.
GetTTState	Returns Internal state of TT for debugging purposes after StopTT request is completed.
ResetTT	Returns the TT in hub to a known state.
StopTT	Stops the normal execution of the TT to retrieve internal state of TT via GetTTState request for debugging purposes.

4.4 Hub Status Field and Hub Change Field

The section describes the value returned for GetHubStatus request. These fields may be set by SetHubFeature request and cleared by ClearHubFeature request.

Table 4-1. Hub Status Field, *wHubStatus*

Bit	Description
0	Local Power Source: This indicates the condition of the local power supply. This is 0 when power supply for hub is stable. 0 = Local power supply good 1 = Local power supply lost (inactive)
1	Over-current Indicator: reporting on a hub basis 0 = No over-current condition currently exists. 1 = A hub over-current condition exists.
2 to 15	Reserved These bits return 0 when read.

Table 4-2. Hub Change Field, *wHubChange*

Bit	Description
0	Local Power Status Change: (C_HUB_LOCAL_POWER) 0 = No change has occurred to Local Power Status. 1 = Local Power Status has changed.
1	Over-Current Indicator Change: (C_HUB_OVER_CURRENT) This field indicates if a change has occurred in the Over-current indicator field in <i>wHubStatus</i> . 0 = No change has occurred to the Over-Current Indicator. 1 = Over-Current Indicator has changed.
2 to 15	Reserved These bits return 0 when read.

4.5 Port Status Field and Port Change Field

The section describes the value returned for GetPortStatus request. These fields may be set by SetPortFeature request and cleared by ClearPortFeature request.

Table 4-3. Port Status Field, *wPortStatus*

Bit	Description
0	Current Connect Status: (PORT_CONNECTION) 0 = No device is present. 1 = A device is present on this port.
1	Port Enabled/Disabled: (PORT_ENABLE) 0 = Port is disabled. 1 = Port is enabled.
2	Suspend: (PORT_SUSPEND) 0 = Not suspended. 1 = Suspended or resuming.
3	Over-current Indicator: reporting on a per-port basis (PORT_OVER_CURRENT) 0 = No over-current condition occurred on this port. 1 = An over-current condition occurred on this port.
4	Reset: (PORT_RESET) 0 = Reset signaling not asserted. 1 = Reset signaling asserted.
5 to 7	Reserved These bits return 0 when read.
8	Port Power: (PORT_POWER) 0 = This port is in the Powered-off state. 1 = This port is not in the Powered-off state.
9	Low Speed Device Attached: (PORT_LOW_SPEED) 0 = Full-speed or High-speed device attached to this port. (Determined by bit 10) 1 = Low-speed device attached to this port.
10	Full or High Speed Device Attached: (PORT_HIGH_SPEED) 0 = Full-speed device attached to this port. 1 = High-speed device attached to this port.
11	Port Test Mode: (PORT_TEST) 0 = This port is not in the Port Test Mode. 1 = This port is in Port Test Mode.
12	Port Indicator Control: (PORT_INDICATOR) 0 = Port indicator displays default colors. 1 = Port indicator displays software controlled color.
13 to 15	Reserved These bits return 0 when read.

Table 4-4. Port Change Field, *wPortChange*

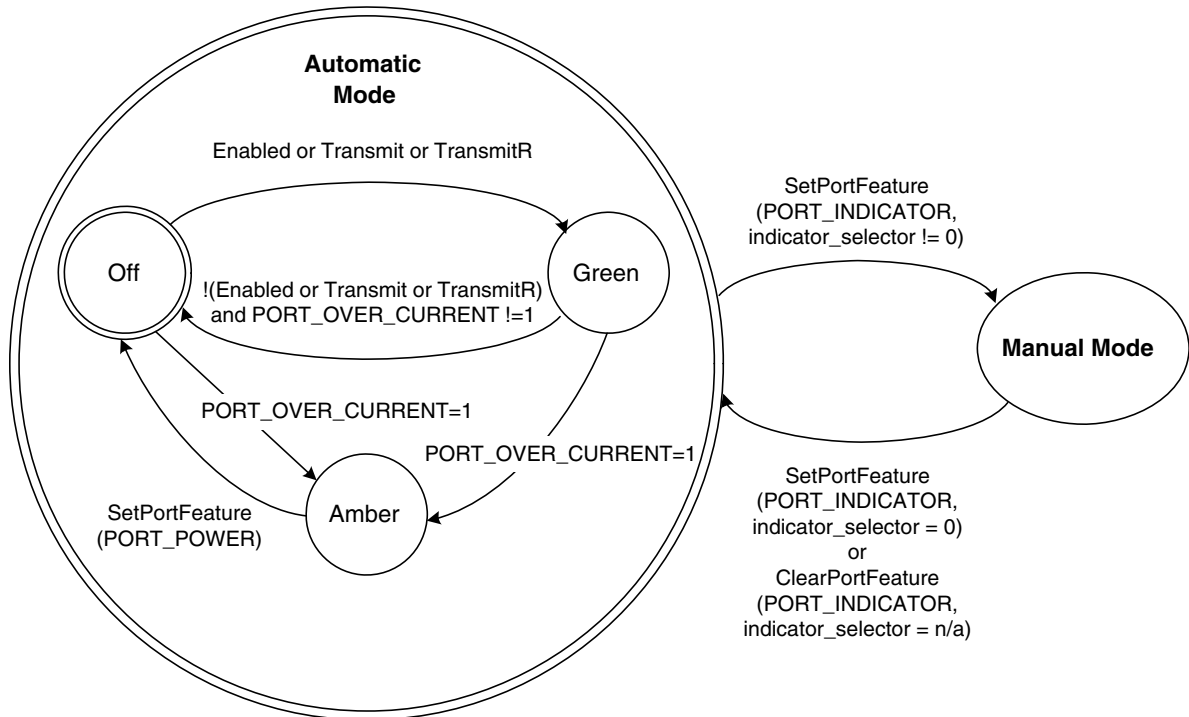
Bit	Description
0	Connect Status Change: (C_PORT_CONNECTION) This field indicates if a change has occurred in the Current Connect Status field in <i>wPortStatus</i> . 0 = No change has occurred to Current Connect status. 1 = Current Connect status has changed.
1	Port Enable/Disable Change: (C_PORT_ENABLE) This field is set to one when a port is disabled because of a Port_Error condition.
2	Suspend Change: (C_PORT_SUSPEND) This field indicates a change in the host-visible suspend state of the attached device. It indicates the device has transitioned out of the Suspend state. This field is set only when the entire resume process has completed. 0 = No change. 1 = Resume complete.
3	Over-Current Indicator Change: (C_PORT_OVER_CURRENT) This field indicates if a change has occurred in the Over-current Indicator field in <i>wPortStatus</i> . 0 = No change has occurred to Over-Current Indicator. 1 = Over-Current Indicator has changed.
4	Reset Change: (C_PORT_RESET) This field is set when reset processing on this port is complete. 0 = No change. 1 = Reset complete.
5 to 15	Reserved These bits return 0 when read.

4.6 PORT_INDICATOR

Each downstream facing port of a hub can support an optional status indicator. The presence of indicators for downstream facing ports is specified by bit 7 of the *wHubCharacteristics* field of the hub class descriptor.

The indicator uses two colors: Green and Amber. A combination of hardware and software control is used to inform the user about the current status of the port or the device attached to the port, and to guide the user through problem resolution. Colors and blinking are used to provide information to the user. A hub must automatically control the color of the indicator as specified in **Figure 4-1**.

Figure 4-1. Port Indicator State Diagram



In **Automatic Mode**, Amber colored LED indicates to detect over-current condition on the port. And Green colored LED indicates that the port is in Enabled, Transmit, or TransmitR. In **Manual Mode**, the color of a port indicator (Amber, Green, or Off) is set by a system software's USB Hub class request.

The following table defines port state as understood by the user:

Table 4-5. Indicator Colors and Port Status

Color	Port State
Off	Suspended, Disconnected, Disabled, or Not Configured
Amber	Error condition
Green	Fully operational
Blinking Off/Green	Software Attention
Blinking Off/Amber	Hardware Attention
Blinking Green/Amber	Reserved

Each specific indicator mode is specified by the Port Indicator selected of SetPortFeature (PORT_INDICATOR) request. As shown in **Table 4-6**, if the Port Indicator Selector is not “0”, Port Indicator will be put into **Manual Mode**. The GetPortStatus (PORT_INDICATOR) provides no standard mechanism to report a specific indicator mode, therefore system software must track which indicator mode was used.

Table 4-6. Port Indicator Selectors

Value	Indicator Mode Description
0h	Default as Automatic Mode
1h	Amber
2h	Green
3h	Off
4h to FFh	Reserved

For example, this feature should be used to require user intervention when host software detects following error conditions on a port.

- A high power device is plugged into a low power port.
- A defective device is plugged into a port (Babble conditions, excessive errors, etc.).
- An over-current condition occurs which causes software or hardware to set the indicator.

And many error conditions can be resolved if the user moves a device from one port to another that has the proper capabilities.

A typical scenario is when a user plugs a high power device into a bus-powered hub. If there is an available high power port, then the user can be directed to move the device from the low-power port to the high power port.

1. Host software would cycle the PORT_INDICATOR feature of the low power port to blink the indicator and display a message to the user to unplug the device from the port with the blinking indicator.
2. Using the C_PORT_CONNECTION status change feature host software can determine when the user physically removed the device from the low power port.
3. Host software would next issue a ClearPortFeature(PORT_INDICATOR) to the low power port (restoring the default color), begin cycling the PORT_INDICATOR of the high power port, and display a message telling the user to plug the device into to port with the blinking indicator.

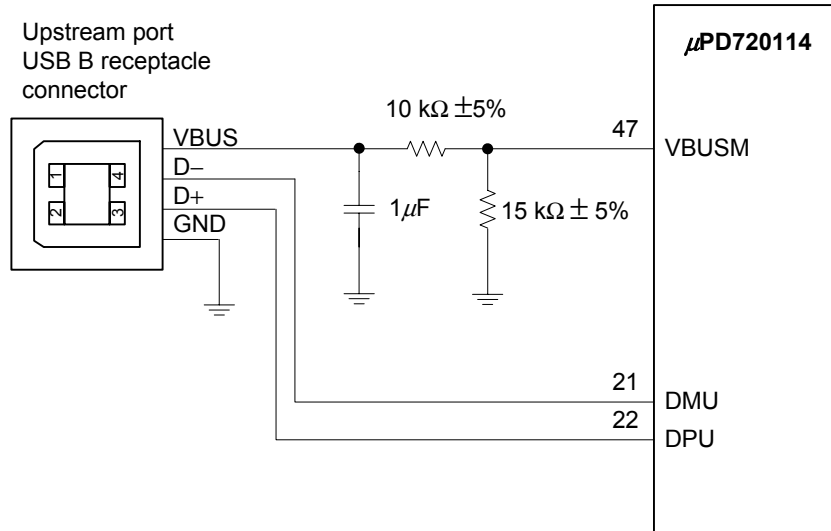
4. Using the C_PORT_CONNECTION status change feature host software can determine when the user physically inserted the device onto the high power port.

Host software must cycle the PORT_INDICATOR feature to blink the current color at approximately 0.5 Hz rate with a 30 to 50 % duty cycle.

CHAPTER 5 HOW TO CONNECT TO EXTERNAL DISCRETE COMPONENTS

5.1 USB Upstream Port Connection

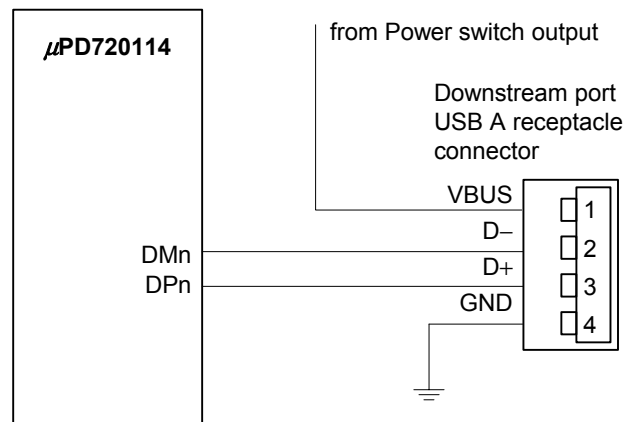
Figure 5-1. USB Upstream Port Connection



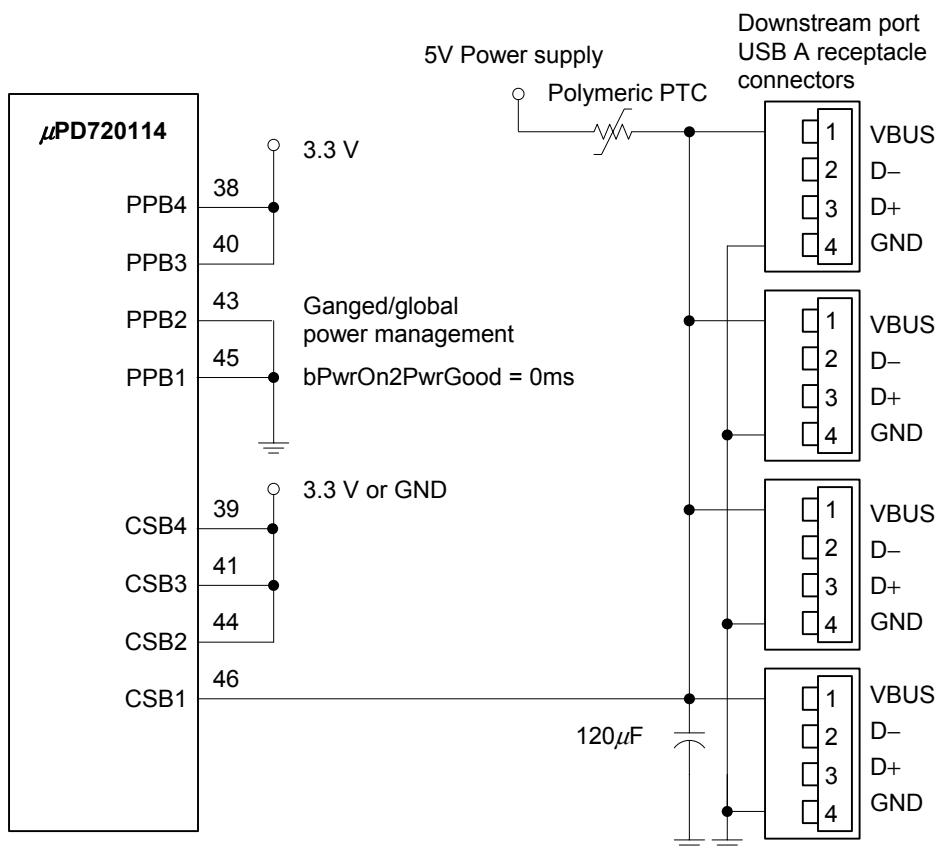
Note Rpu for DPU pin is internal.

5.2 USB Downstream Port Connection

Figure 5-2. USB Downstream Port Connection



Note Rpd resistances for DP and DM pins are internal.

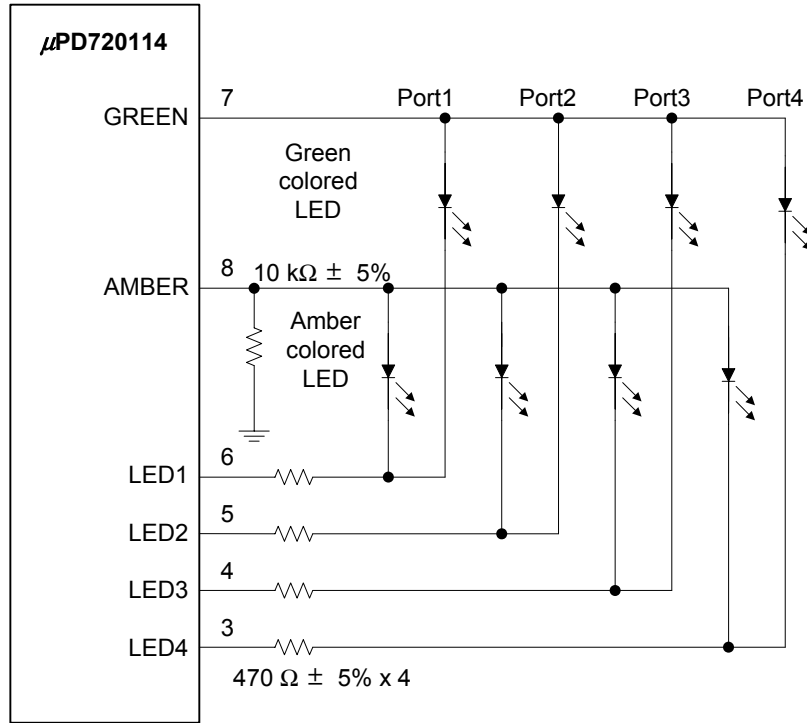
Figure 5-4. Self-powered, Global Over-current Protection by Polymeric PTC

Remark When no power switches are used, set $\text{PPB1} = 0$ ($\text{bPwrOn2PwrGood} = 0$) and $\text{PPB2} = 0$ (Logical ganged power switching, global over-current protection). This complies with the USB Specification. $\text{CSB}[4:2]$ are 3 V inputs and should connect to 3.3 V (not 5 V) or GND when using a PTC instead of power switches as shown.

5.4 LED Connection

Port_Indicator (LEDx, AMBER, GREEN) should be supported at default setting. At that case, each Amber colored LED should be connected from AMBER to LEDx with a series resistor, and each Green colored LED should be connected from GREEN to LEDx with a series resistor. AMBER pin should connect a 10 k Ω resistance to ground.

Figure 5-5. LED Connection



Remark Maximum load current of LEDx is 3 mA, and voltage between AMBER/GREEN and LEDx is 3.3 V nominal. Choose LED specification and series resistor value according to the electrical.

5.5 Crystal Connection

Figure 5-6. Crystal Connection

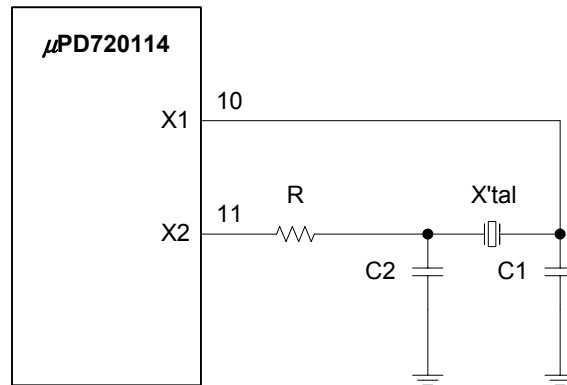


Figure 5-6 shows a 30 MHz fundamental crystal that is parallel loaded. In order to balance the frequency, negative resistance and the gain, the R, C1 and C2 should trim for the crystal. The following crystals are evaluated on our reference design board. Table 5-1 shows the external parameters.

Table 5-1. External Parameters

Vender	X'tal	R	C1	C2
KDS	AT-49 30.000 MHz ($C_L = 10$ pF)	33 Ω	12 pF	12 pF
NDK	AT-41 30.000 MHz ($C_L = 8$ pF)	150 Ω	10 pF	10 pF

Remark KDS: DAISHINKU CORP.

NDK: NIHON DEMPA KOGYO CO., LTD.

In using these crystals, contact KDS or NDK to get the specification on external components to be used in conjunction with the crystal.

KDS's home page: http://www.kds.info/index_en.htm

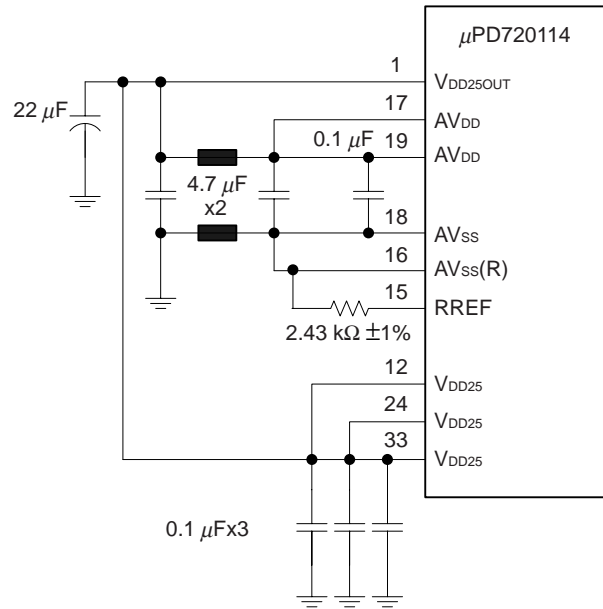
NDK's home page: <http://www.ndk.com/en/index.cfm>

Caution When you use an oscillator circuit, please keep following points.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always keep the ground point of the oscillator capacitor to the same potential as V_{SS} .
- Do not ground the capacitor to a ground pattern in which a high current flows.

5.6 RREF and Internal Regulator Connection

Figure 5-7. RREF and Internal Regulator Connection



Caution V_{DD25OUT} must be routed to only V_{DD25} (and AV_{DD}). In case that V_{DD25OUT} is also used for power supply of other ICs, this may cause unstable operation of the $\mu\text{PD720114}$.

Remark The board layout should minimize the total path length from pin 15 through the resistor to pin 16 and connect to the source of AV_{SS} (quiet AV_{SS}). V_{DD25} is powered by V_{DD25OUT} from internal regulator. It is not necessary to use external regulator for V_{DD25} .

5.7 Handling Unused Pins

Hubs using the $\mu\text{PD720114}$ can be implemented with less than 4 downstream ports. If a hub design is implemented with less than 4 ports, only the lower numbered ports shall be used or accessible to the users. For example, if only 2 ports are used in the design, only ports 1 to 2 shall be used, and port 3 and 4 shall not be used or accessible to the users.

To implement a hub with less than 4 ports, connect the unused pins of unused ports as shown below (where x indicates the unused port number).

Pin	Direction	Connection Method
DPx	I/O	Tied to GND directly or though resistor
DMx	I/O	Tied to GND directly or though resistor
TEST	I	Tied to GND directly or though resistor
CSB[4:2]	I	Tied to 3.3 V or GND

CHAPTER 6 PRODUCT SPECIFICATIONS

6.1 Buffer List

- 2.5 V Oscillator interface
X1, X2
- 5 V tolerant Schmitt input buffer
CSB1, VBUSM^{Note}
- 3.3 V Schmitt input buffer
CSB(4:2), BUS_B, SYSRSTB, TEST
- 3.3 V $I_{OL} = 12$ mA output buffer
GREEN
- 3.3 V input and 3.3 V $I_{OL} = 3$ mA output buffer
PPB(4:1), LED(4:1)
- 3.3 V input and $I_{OL} = 12$ mA output buffer
AMBER
- USB2.0 interface
DPU, DMU, DP(4:1), DM(4:1), RREF

Above, “5 V” refers to a 3 V input buffer that is 5 V tolerant (has 5 V maximum input voltage). Therefore, it is possible to have a 5 V connection for an external bus.

Note Although VBUSM is 5 V tolerant, voltage divider resistors are required as shown in Figure 5-1 due to the switching thresholds of the VBUSM input. CSB1 is 5 V tolerant so that it can be used ganged port power management as shown in Figure 5-4. CSB[4:2] are 3.3 V input so that it can be used individual port power management with power switch as shown in Figure 5-3 and it can not be used with poly metric PTC.

6.2 Terminology

Table 6-1. Terms Used in Absolute Maximum Ratings

Parameter	Symbol	Meaning
Power supply voltage	V_{DD33}	Indicates voltage range within which damage or reduced reliability will not result when power is applied to a V_{DD} pin.
Input voltage	V_I	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V_O	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Output current	I_O	Indicates absolute tolerance values for DC current to prevent damage or reduced reliability when current flows out of or into an output pin.
Operating temperature	T_A	Indicates the ambient temperature range for normal logic operations.
Storage temperature	T_{stg}	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current are applied to the device.

Table 6-2. Terms Used in Recommended Operating Range

Parameter	Symbol	Meaning
Power supply voltage	V_{DD33}	Indicates the voltage range for normal logic operations to occur when $V_{SS} = 0$ V.
High-level input voltage	V_{IH}	Indicates the voltage, applied to the input pins of the device, which indicates the high level state for normal operation of the input buffer. * If a voltage that is equal to or greater than the "Min." value is applied, the input voltage is guaranteed as high level voltage.
Low-level input voltage	V_{IL}	Indicates the voltage, applied to the input pins of the device, which indicates the low level state for normal operation of the input buffer. * If a voltage that is equal to or less than the "Max." value is applied, the input voltage is guaranteed as low level voltage.
Hysteresis voltage	V_H	Indicates the differential between the positive trigger voltage and the negative trigger voltage.
Input rise time	t_{ri}	Indicates allowable input signal transition time from $0.1 \times V_{DD}$ to $0.9 \times V_{DD}$.
Input fall time	t_{fi}	Indicates allowable input signal transition time from $0.9 \times V_{DD}$ to $0.1 \times V_{DD}$.

Table 6-3. Terms Used in DC Characteristics

Parameter	Symbol	Meaning
Off-state output leakage current	I_{OZ}	Indicates the current that flows into a 3-state output pin when it is in a high-impedance state and a voltage is applied to the pin.
Output short circuit current	I_{OS}	Indicates the current that flows from an output pin when it is shorted to GND while it is at high-level.
Input leakage current	I_I	Indicates the current that flows into an input pin when a voltage is applied to the pin.
Low-level output current	I_{OL}	Indicates the current that can flow into an output pin in the low-level state without raising the output voltage above the specified V_{OL} .
High-level output current	I_{OH}	Indicates the current that can flow out of an output pin in the high-level state without reducing the output voltage below the specified V_{OH} . (A negative current indicates current flowing out of the pin.)

6.3 Absolute Maximum Ratings

Table 6-4. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	$V_{DD33}, V_{DD33REG}$		-0.5 to +4.6	V
Input/output voltage	V_I/V_O			
3.3 V input/output voltage		$3.0\text{ V} \leq V_{DD33} \leq 3.6\text{ V}$ $V_I/V_O < V_{DD33} + 1.0\text{ V}$	-0.5 to +4.6	V
5 V input/out voltage		$3.0\text{ V} \leq V_{DD33} \leq 3.6\text{ V}$ $V_I/V_O < V_{DD33} + 3.0\text{ V}$	-0.5 to +6.6	V
Output current	I_O	$I_{OL} = 3\text{ mA}$ $I_{OL} = 12\text{ mA}$	10 40	mA mA
Operating temperature	T_A		0 to +85	°C
Storage temperature	T_{stg}		-65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameters. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

6.4 Recommended Operating Ranges

Table 6-5. Recommended Operating Ranges

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	$V_{DD33}, V_{DD33REG}$	3.3 V for V_{DD33} pins	3.14	3.30	3.46	V
High-level input voltage	V_{IH}					
3.3 V High-level input voltage			2.0		V_{DD33}	V
5.0 V High-level input voltage			2.0		5.5	V
Low-level input voltage	V_{IL}					
3.3 V Low-level input voltage			0		0.8	V
5.0 V Low-level input voltage			0		0.8	V
Hysteresis voltage	V_H					
5 V Hysteresis voltage			0.3		1.5	V
3.3 V Hysteresis voltage			0.2		1.0	V
Input rise time for SYSRSTB	t_{rst}				10	ms
Input rise time	t_{ri}					
Normal buffer			0		200	ns
Schmitt buffer			0		10	ms
Input fall time	t_{fi}					
Normal buffer			0		200	ns
Schmitt buffer			0		10	ms

6.5 DC Characteristics

DC characteristics are specified under following conditions: $V_{DD33} = 3.14$ to 3.46 V, $T_A = 0$ to $+70$ °C

Table 6-6. DC Characteristics (Control Pin Block)

Parameter	Symbol	Condition	Min.	Max.	Unit
Off-state output leakage current	I_{OZ}	$V_O = V_{DD33}, V_{DD25}$ or V_{SS}		± 10	μA
Output short circuit current	I_{OS} ^{Note}			-250	mA
Low-level output current	I_{OL}				
3.3 V low-level output current (3 mA)		$V_{OL} = 0.4$ V	3		mA
3.3 V low-level output current (12 mA)		$V_{OL} = 0.4$ V	12		mA
High-level output current	I_{OH}				
3.3 V high-level output current (3 mA)		$V_{OH} = 2.4$ V	-3		mA
3.3 V high-level output current (12 mA)		$V_{OH} = 2.4$ V	-12		mA
Input leakage current	I_I				
3.3 V buffer		$V_I = V_{DD}$ or V_{SS}		± 10	μA
5.0 V buffer		$V_I = V_{DD}$ or V_{SS}		± 10	μA

Note The output short circuit time is measured at one second or less and is tested with only one pin on the LSI.

Table 6-7. DC Characteristics (USB Interface Block)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Output pin impedance	Z_{HSDRV}	Includes R_S resistor	40.5	49.5	Ω
Termination voltage for upstream facing port pullup (full-speed)	V_{TERM}		3.0	3.6	V
Input Levels for Low-/full-speed:					
High-level input voltage (drive)	V_{IH}		2.0		V
High-level input voltage (floating)	V_{IHZ}		2.7	3.6	V
Low-level input voltage	V_{IL}			0.8	V
Differential input sensitivity	V_{DI}	$ (D+) - (D-) $	0.2		V
Differential common mode range	V_{CM}	Includes V_{DI} range	0.8	2.5	V
Output Levels for Low-/full-speed:					
High-level output voltage	V_{OH}	R_L of 14.25 k Ω to GND	2.8	3.6	V
Low-level output voltage	V_{OL}	R_L of 1.425 k Ω to 3.6 V	0.0	0.3	V
SE1	V_{OSE1}		0.8		V
Output signal crossover point voltage	V_{CRS}		1.3	2.0	V
Input Levels for High-speed:					
High-speed squelch detection threshold (differential signal)	V_{HSSQ}		100	150	mV
High-speed disconnect detection threshold (differential signal)	V_{HSDSC}		525	625	mV
High-speed data signaling common mode voltage range	V_{HSCM}		−50	+500	mV
High-speed differential input signaling levels	See Figure 6-4 .				
Output Levels for High-speed:					
High-speed idle state	V_{HSOI}		−10.0	+10	mV
High-speed data signaling high	V_{HSOH}		360	440	mV
High-speed data signaling low	V_{HSOL}		−10.0	+10	mV
Chirp J level (different signal)	V_{CHIRPJ}		700	1100	mV
Chirp K level (different signal)	V_{CHIRPK}		−900	−500	mV

Figure 6-1. Differential Input Sensitivity Range for Low-/full-speed

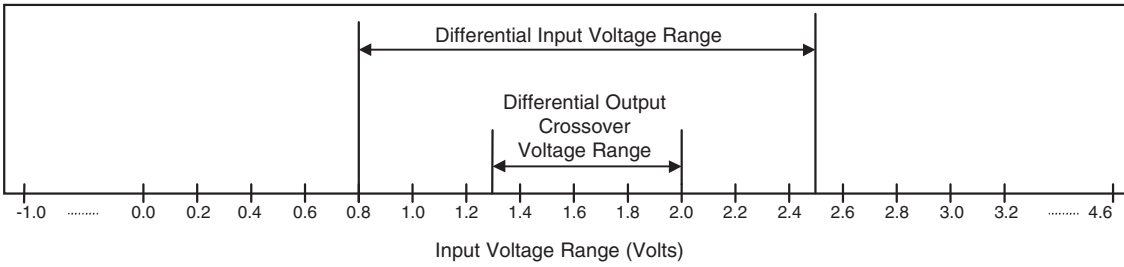


Figure 6-2. Full-speed Buffer V_{OH}/I_{OH} Characteristics for High-speed Capable Transceiver

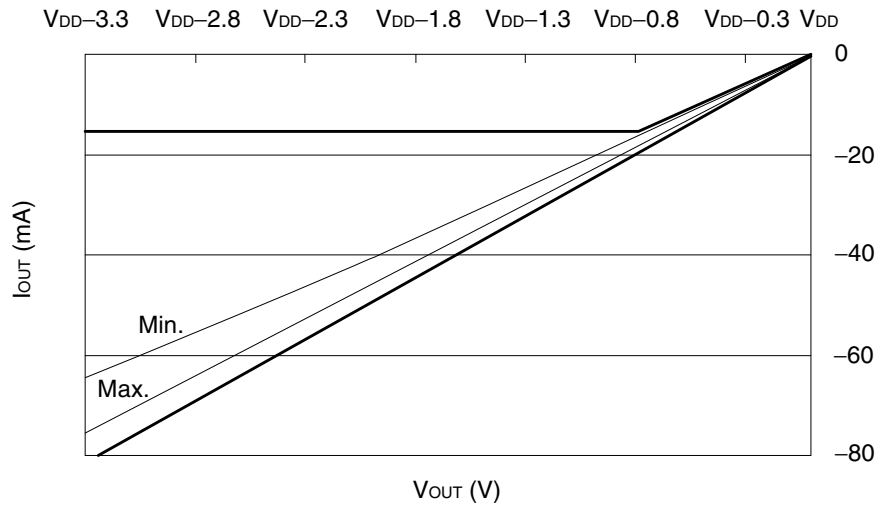


Figure 6-3. Full-speed Buffer V_{OL}/I_{OL} Characteristics for High-speed Capable Transceiver

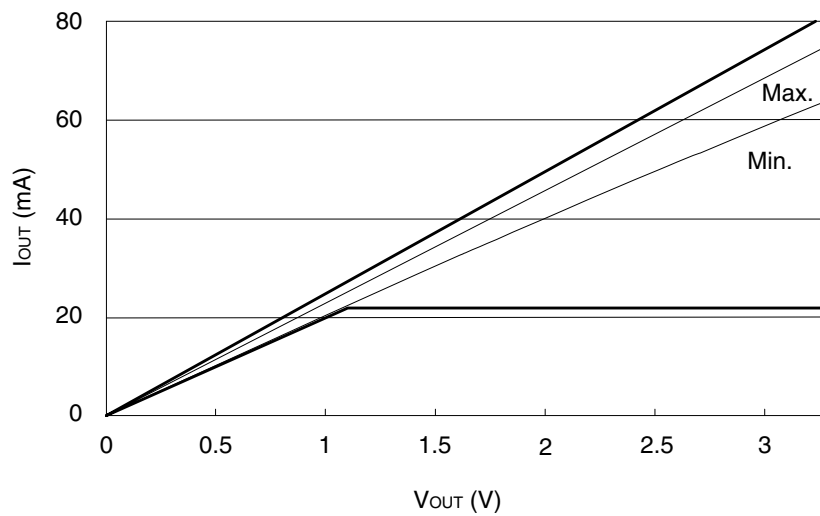


Figure 6-4. Receiver Sensitivity for Transceiver at DP/DM

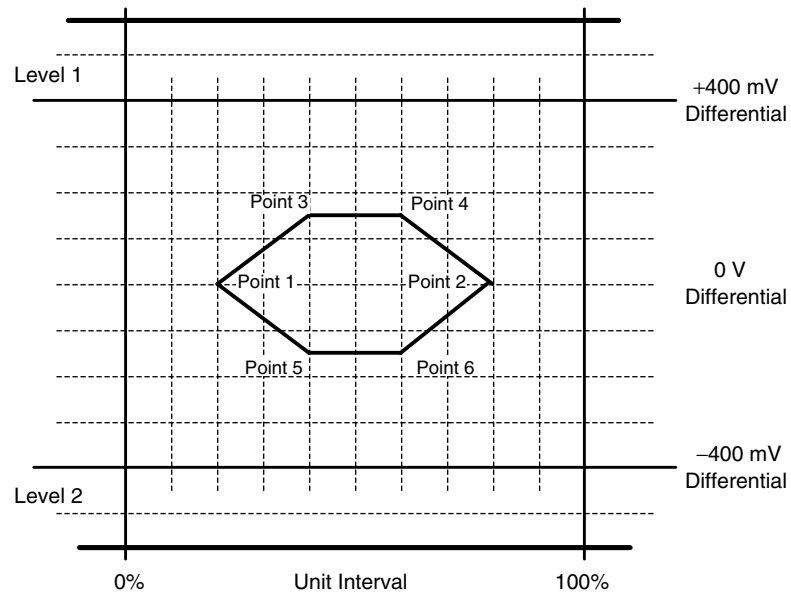
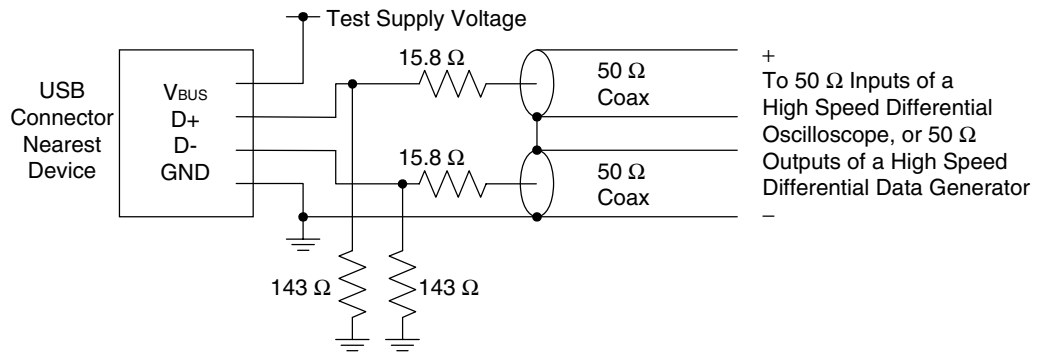


Figure 6-5. Receiver Measurement Fixtures



6.6 Power Consumption

Table 6-8. Power Consumption

Parameter	Symbol	Condition	Typ.	Unit
Power Consumption	P _{W-0}	The power consumption under the state without suspend. All the ports do not connect to any function. Note 1		
		Hub controller is operating at full-speed mode. Hub controller is operating at high-speed mode.	31 86	mA mA
	P _{W-2}	The power consumption under the state without suspend. The number of active ports is 2. Note 2		
		Hub controller is operating at full-speed mode. Hub controller is operating at high-speed mode.	36 120	mA mA
	P _{W-3}	The power consumption under the state without suspend. The number of active ports is 3. Note 2		
		Hub controller is operating at full-speed mode. Hub controller is operating at high-speed mode.	38 134	mA mA
	P _{W-4}	The power consumption under the state without suspend. The number of active ports is 4. Note 2		
		Hub controller is operating at full-speed mode. Hub controller is operating at high-speed mode.	41 149	mA mA
	P _{W-UNP}	The power consumption under unplug and the hub in idle state. Note 3	10	μA
	P _{W-S}	The power consumption under plug (V _{BUS} ON) and the hub in suspend state. Note 4	220	μA

- Notes**
1. Ports available but inactive or unplugged do not add to the power consumption.
 2. The power consumption depends on the number of ports available and actively operating.
 3. If the μ PD720114 is locally powered and the upstream facing port is unplugged, μ PD720114 goes into suspend state and downstream facing port V_{BUS} goes down.
 4. If the upstream V_{BUS} in OFF state, the power consumption is same as P_{W-UNP}.

6.7 AC Characteristics

AC characteristics are specified under following conditions: $V_{DD} = 3.14$ to 3.46 V, $T_A = 0$ to $+70$ °C

Table 6-9. Pin capacitance

Parameter	Symbol	Condition	Min.	Max.	Unit
Input capacitance	C_I	$V_{DD} = 0$ V, $T_A = 25$ °C $f_C = 1$ MHz Unmeasured pins returned to 0 V		6	pF
Output capacitance	C_O			6	pF
I/O capacitance	C_{IO}			6	pF

Table 6-10. System Clock Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock frequency	f_{CLK}	Crystal	–500 ppm	30	+500 ppm	MHz
Clock Duty cycle	t_{DUTY}		40	50	60	%

- Remarks**
1. Recommended accuracy of clock frequency is ± 100 ppm.
 2. Required accuracy of X'tal includes initial frequency accuracy, the spread of crystal capacitor loading, supply voltage, temperature, aging, etc.

Table 6-11. System Reset Signaling

Parameter	Symbol	Conditions	Min.	Max.	Unit
Reset active time (Figure 6-6)	t_{rst}		5		μ s

Figure 6-6. System Reset Timing

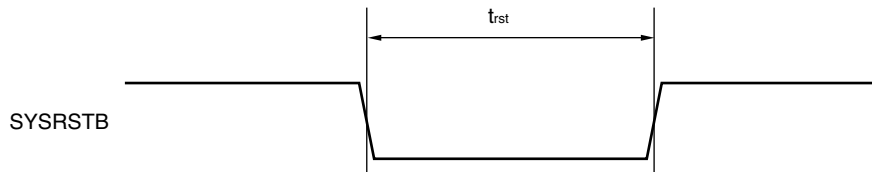
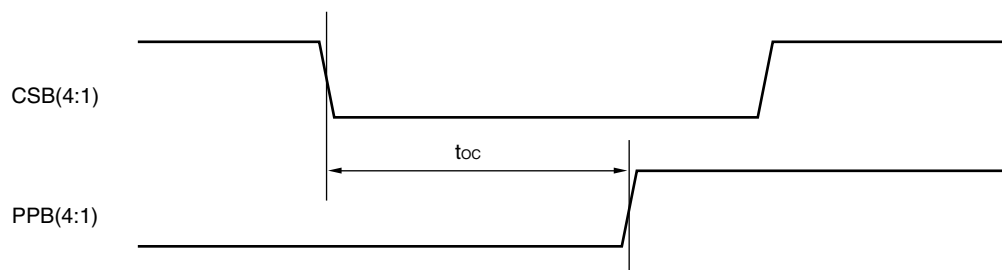
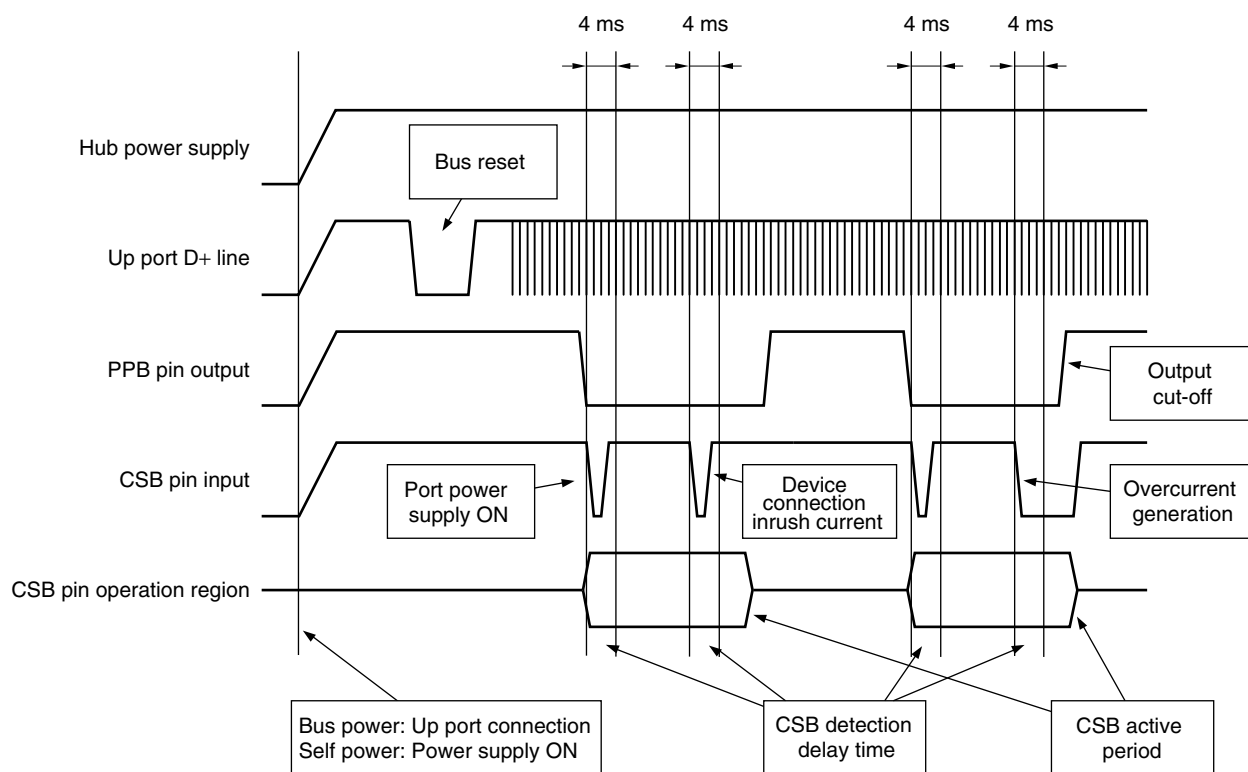


Table 6-12. AC Characteristics (Over-current Response Timing)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Over-current response time from CSB low to PPB high (Figure 6-7)	t_{oc}		4		5	ms

Figure 6-7. Over-current Response Timing**Figure 6-8. CSB/PPB Timing**

Remark The active period of the CSB pin is in effect only when the PPB pin is ON.
There is a delay time of approximately 4 ms duration at the CSB pin.

Table 6-13. AC Characteristics (USB Interface Block)

(1/4)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Low-speed Electrical Characteristics					
Rise time (10% to 90%)	t_{LR}	$C_L = 200 \text{ pF to } 600 \text{ pF}$	75	300	ns
Fall time (90% to 10%)	t_{LF}	$C_L = 200 \text{ pF to } 600 \text{ pF}$	75	300	ns
Differential rise and fall time matching	t_{LRFM}	(t_{LR}/t_{LF}) ^{Note}	80	125	%
Low-speed data rate	$t_{LDRATHS}$	Average bit rate	1.49925	1.50075	Mbps
Downstream facing port source jitter total (including frequency tolerance) (Figure 6-13):					
To next transition	t_{DDJ1}		-25	+25	ns
For paired transitions	t_{DDJ2}		-14	+14	ns
Downstream facing port differential receiver jitter total (including frequency tolerance) (Figure 6-15):					
To next transition	t_{UJR1}		-152	+152	ns
For paired transitions	t_{UJR2}		-200	+200	ns
Source SE0 interval of EOP (Figure 6-14)	t_{LEOPT}		1.25	1.5	μs
Receiver SE0 interval of EOP (Figure 6-14)	t_{LEOPR}		670		ns
Width of SE0 interval during differential transition	t_{LST}			210	ns
Hub differential data delay (Figure 6-11)	t_{LHDD}			300	ns
Hub differential driver jitter (including cable) (Figure 6-11):					
Downstream facing port					
To next transition	t_{LDHJ1}		-45	+45	ns
For paired transitions	t_{LDHJ2}		-15	+15	ns
Upstream facing port					
To next transition	t_{LUHJ1}		-45	+45	ns
For paired transitions	t_{LUHJ2}		-45	+45	ns
Data bit width distortion after SOP (Figure 6-11)	t_{LSOP}		-60	+60	ns
Hub EOP delay relative to t_{HDD} (Figure 6-12)	t_{LEOPD}		0	200	ns
Hub EOP output width skew (Figure 6-12)	t_{LHESK}		-300	+300	ns
Full-speed Electrical Characteristics					
Rise time (10% to 90%)	t_{FR}	$C_L = 50 \text{ pF},$ $R_S = 36 \Omega$	4	20	ns
Fall time (90% to 10%)	t_{FF}	$C_L = 50 \text{ pF},$ $R_S = 36 \Omega$	4	20	ns
Differential rise and fall time matching	t_{FRFM}	(t_{FR}/t_{FF})	90	111.11	%
Full-speed data rate	$t_{FDRATHS}$	Average bit rate	11.9940	12.0060	Mbps
Frame interval	t_{FRAME}		0.9995	1.0005	ms

Note Excluding the first transition from the Idle state.

(2/4)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Full-speed Electrical Characteristics (Continued)					
Consecutive frame interval jitter	t_{RFI}	No clock adjustment		42	ns
Source jitter total (including frequency tolerance) (Figure 6-13):		Note			
To next transition	t_{DJ1}		-3.5	+3.5	ns
For paired transitions	t_{DJ2}		-4.0	+4.0	ns
Source jitter for differential transition to SE0 transition (Figure 6-14)	t_{FDEOP}		-2	+5	ns
Receiver jitter (Figure 6-15):					
To Next Transition	t_{JR1}		-18.5	+18.5	ns
For Paired Transitions	t_{JR2}		-9	+9	ns
Source SE0 interval of EOP (Figure 6-14)	t_{FEOPT}		160	175	ns
Receiver SE0 interval of EOP (Figure 6-14)	t_{FEOPR}		82		ns
Width of SE0 interval during differential transition	t_{FST}			14	ns
Hub differential data delay (Figure 6-11)					
(with cable)	t_{HDD1}			70	ns
(without cable)	t_{HDD2}			44	ns
Hub differential driver jitter (including cable) (Figure 6-11):					
To next transition	t_{HDJ1}		-3	+3	ns
For paired transitions	t_{HDJ2}		-1	+1	ns
Data bit width distortion after SOP (Figure 6-11)	t_{FSOP}		-5	+5	ns
Hub EOP delay relative to t_{HDD} (Figure 6-12)	t_{FEOPD}		0	15	ns
Hub EOP output width skew (Figure 6-12)	t_{FHESK}		-15	+15	ns
High-speed Electrical Characteristics					
Rise time (10% to 90%)	t_{HSR}		500		ps
Fall time (90% to 10%)	t_{HSF}		500		ps
Driver waveform	See Figure 6-9 .				
High-speed data rate	t_{HSDRAT}		479.760	480.240	Mbps
Microframe interval	t_{HSFRAM}		124.9375	125.0625	μs
Consecutive microframe interval difference	t_{HSRFI}			4 high-speed	Bit times
Data source jitter	See Figure 6-9 .				
Receiver jitter tolerance	See Figure 6-4 .				
Hub data delay (without cable)	t_{HSHDD}			36 high-speed+4 ns	Bit times
Hub data jitter	See Figure 6-4 , Figure 6-9 .				
Hub delay variation range	t_{HSHDV}			5 high-speed	Bit times

Note Excluding the first transition from the Idle state.

Parameter	Symbol	Conditions	Min.	Max.	Unit
Hub Event Timings					
Time to detect a downstream facing port connect event (Figure 6-17): Awake hub Suspended hub	tDCNN		2.5	2000	μs
			2.5	12000	μs
Time to detect a disconnect event at a hub's downstream facing port (Figure 6-16)	tDDIS		2.0	2.5	μs
Duration of driving resume to a downstream port (only from a controlling hub)	tDRMDN		20		ms
Time from detecting downstream resume to rebroadcast	tURSM			1.0	ms
Duration of driving reset to a downstream facing port (Figure 6-18)	tDRST	Only for a SetPortFeature (PORT_RESET) request	10	20	ms
Time to detect a long K from upstream	tURLK		2.5	100	μs
Time to detect a long SE0 from upstream	tURLSE0		2.5	10000	μs
Duration of repeating SE0 upstream (for low-/full-speed repeater)	tURPSE0			23	FS Bit times
Inter-packet delay (for high-speed) of packets traveling in same direction	tHSIPDSD		88		Bit times
Inter-packet delay (for high-speed) of packets traveling in opposite direction	tHSIPDOD		8		Bit times
Inter-packet delay for device/root hub response with detachable cable for high-speed	tHSRSPID1			192	Bit times
Time of which a Chirp J or Chirp K must be continuously detected (filtered) by hub or device during Reset handshake	tFILT		2.5		μs
Time after end of device Chirp K by which hub must start driving first Chirp K in the hub's chirp sequence	tWTDCH			100	μs
Time for which each individual Chirp J or Chirp K in the chirp sequence is driven downstream by hub during reset	tDCHBIT		40	60	μs
Time before end of reset by which a hub must end its downstream chirp sequence	tDCHSE0		100	500	μs
Time from internal power good to device pulling D+ beyond V _{IHZ} (Figure 6-18)	tSIGATT			100	ms
Debounce interval provided by USB system software after attach (Figure 6-18)	tATTDB			100	ms
Maximum duration of suspend averaging interval	tSUSAVGI			1	s
Period of idle bus before device can initiate resume	tWTRSM		5		ms
Duration of driving resume upstream	tDRSMUP		1	15	ms

Parameter	Symbol	Conditions	Min.	Max.	Unit
Hub Event Timings (Continued)					
Resume recovery time	t _{RSRCY}	Remote-wakeup is enabled	10		ms
Time to detect a reset from upstream for non high-speed capable devices	t _{DETRST}		2.5	10000	μs
Reset recovery time (Figure 6-18)	t _{RSTRCY}			10	ms
Inter-packet delay for full-speed	t _{IPD}		2		Bit times
Inter-packet delay for device response with detachable cable for full-speed	t _{RSPID1}			6.5	Bit times
SetAddress() completion time	t _{DSETADDR}			50	ms
Time to complete standard request with no data	t _{DRQCPLTND}			50	ms
Time to deliver first and subsequent (except last) data for standard request	t _{DRETDATA1}			500	ms
Time to deliver last data for standard request	t _{DRETDATAN}			50	ms
Time for which a suspended hub will see a continuous SE0 on upstream before beginning the high-speed detection handshake	t _{FILTSE0}		2.5		μs
Time a hub operating in non-suspended full-speed will wait after start of SE0 on upstream before beginning the high-speed detection handshake	t _{WTRSTFS}		2.5	3000	ms
Time a hub operating in high-speed will wait after start of SE0 on upstream before reverting to full-speed	t _{WTREV}		3.0	3.125	ms
Time a hub will wait after reverting to full-speed before sampling the bus state on upstream and beginning the high-speed will wait after start of SE0 on upstream before reverting to full-speed	t _{WTRSTHS}		100	875	ms
Minimum duration of a Chirp K on upstream from a hub within the reset protocol	t _{UCH}		1.0		ms
Time after start of SE0 on upstream by which a hub will complete its Chirp K within the reset protocol	t _{UCHEND}			7.0	ms
Time between detection of downstream chip and entering high-speed state	t _{WTHS}			500	μs
Time after end of upstream Chirp at which hub reverts to full-speed default state if no downstream Chirp is detected	t _{WTFS}		1.0	2.5	ms

Figure 6-9. Transmit Waveform for Transceiver at DP/DM

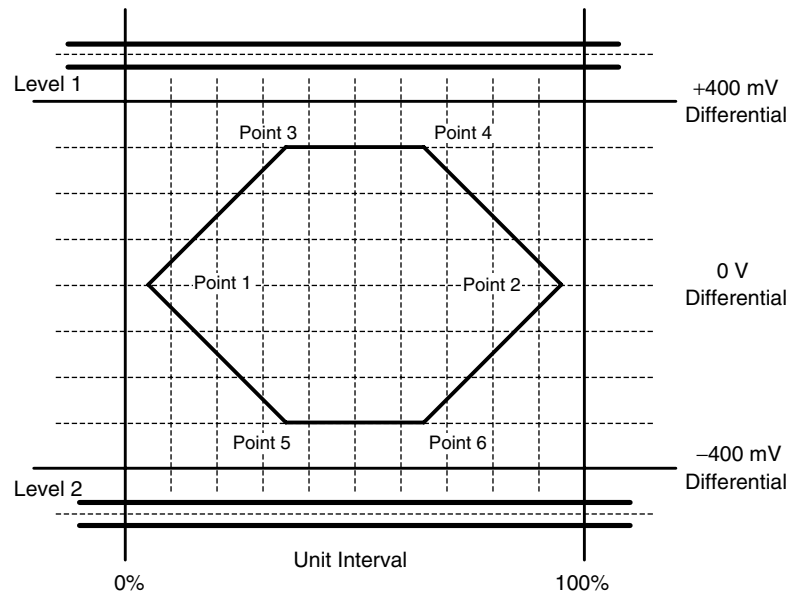
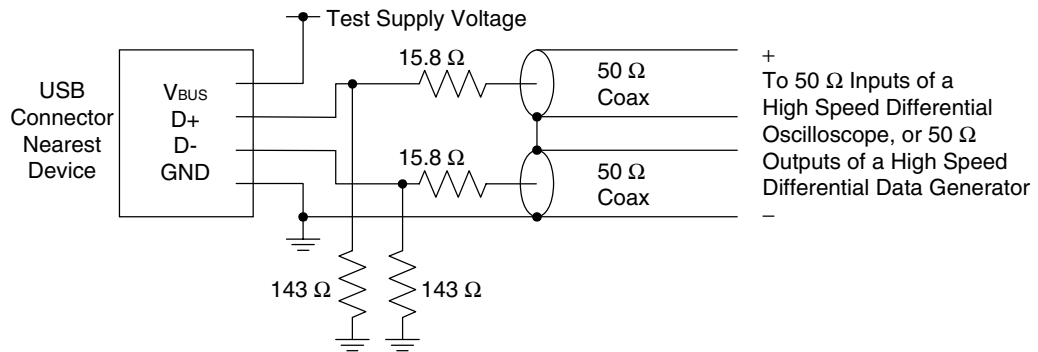
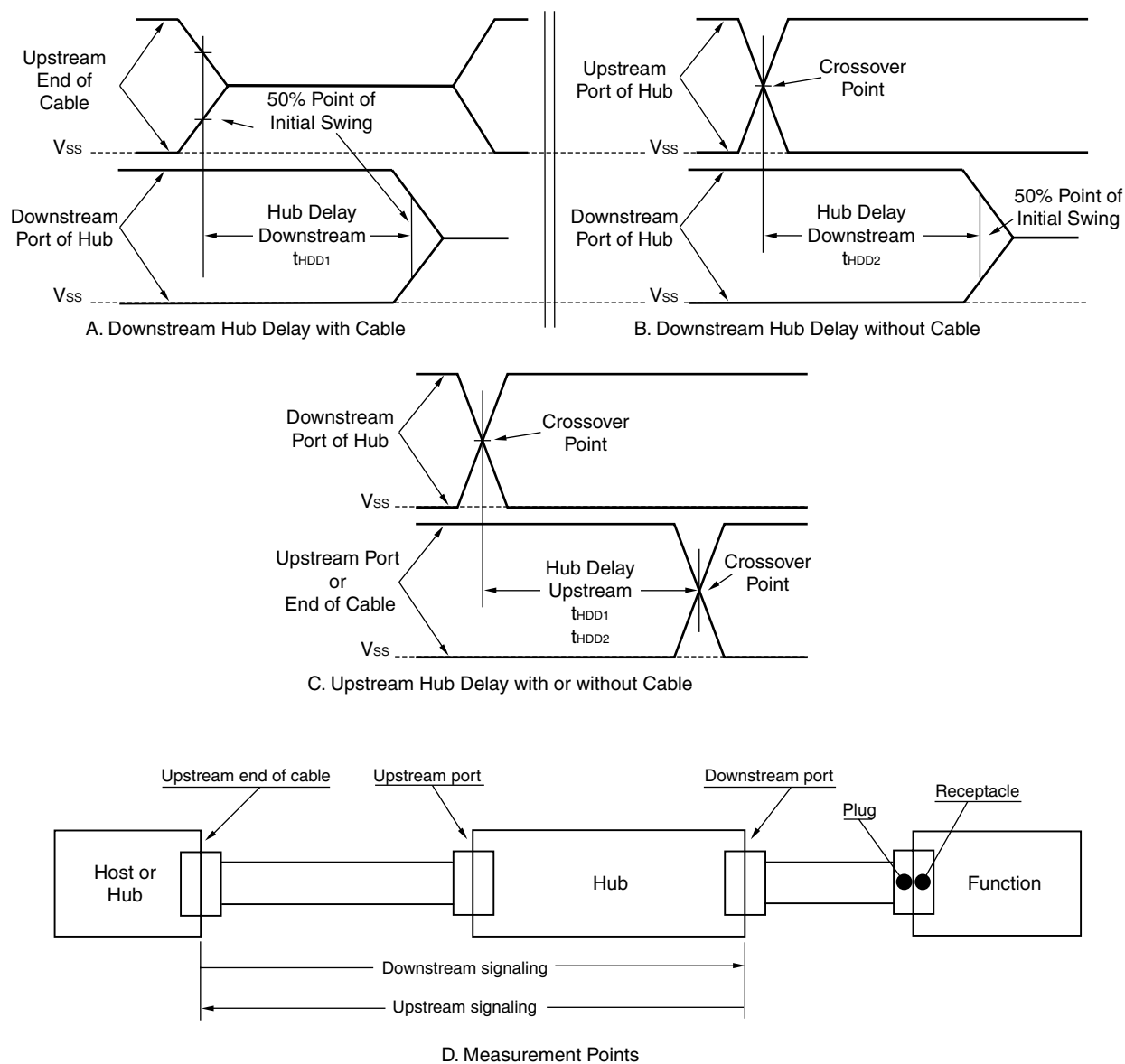


Figure 6-10. Transmitter Measurement Fixtures



6.8 Timing Diagram

Figure 6-11. Hub Differential Delay, Differential Jitter, and SOP Distortion



Hub Differential Jitter:

$$t_{HDJ1} = t_{HDDx}(J) - t_{HDDx}(K) \text{ or } t_{HDDx}(K) - t_{HDDx}(J) \quad \text{Consecutive Transitions}$$

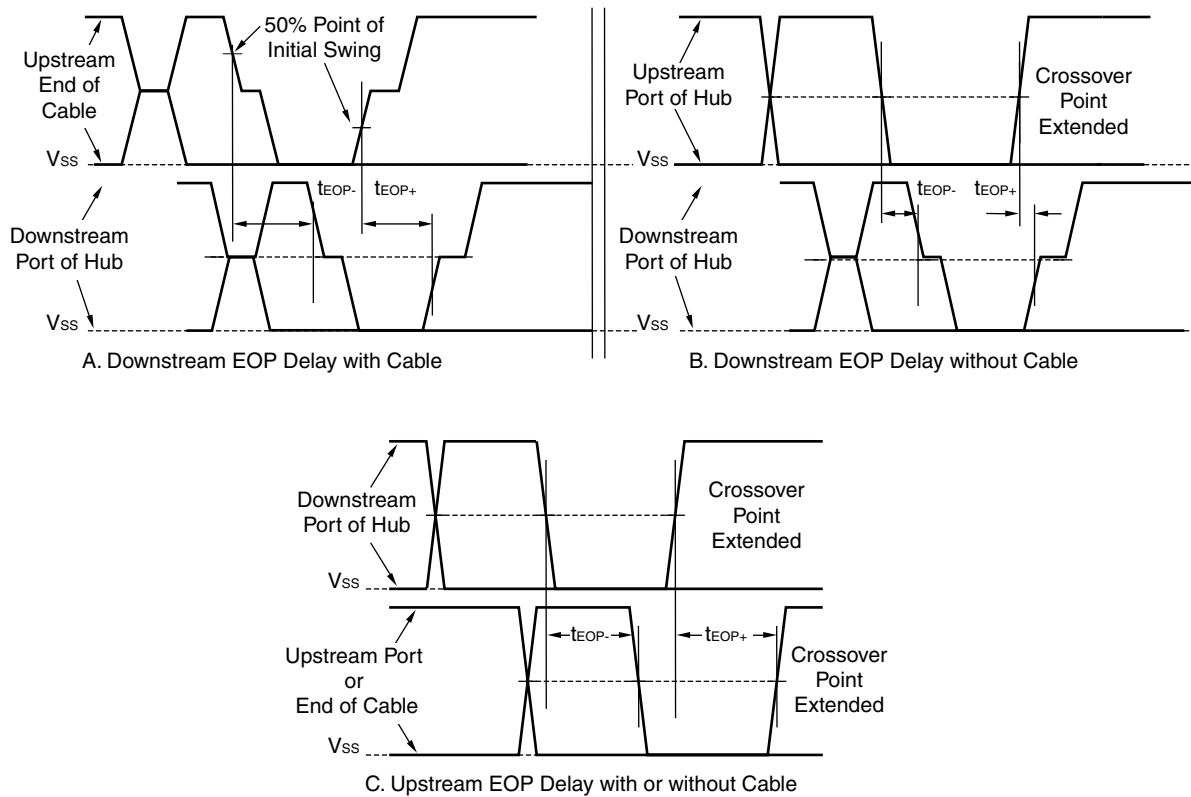
$$t_{HDJ2} = t_{HDDx}(J) - t_{HDDx}(J) \text{ or } t_{HDDx}(K) - t_{HDDx}(K) \quad \text{Paired Transitions}$$

Bit after SOP Width Distortion (same as data jitter for SOP and next J transition):

$$t_{FSOP} = t_{HDDx}(\text{next J}) - t_{HDDx}(\text{SOP})$$

Low-speed timings are determined in the same way for:

t_{LHDD} , t_{LDHJ1} , t_{LDJH2} , t_{LUHJ1} , t_{LUJH2} , and t_{LSOP}

Figure 6-12. Hub EOP Delay and EOP Skew**EOP Delay:**

$$t_{FEOPD} = t_{EOPy} - t_{HDDx}$$

(t_{EOPy} means that this equation applies to t_{EOP-} and t_{EOP+})

EOP Skew:

$$t_{FHESK} = t_{EOP+} - t_{EOP-}$$

Low-speed timings are determined in the same way for:

t_{LEOPD} and t_{LHESK}

Figure 6-13. USB Differential Data Jitter for Low-/full-speed

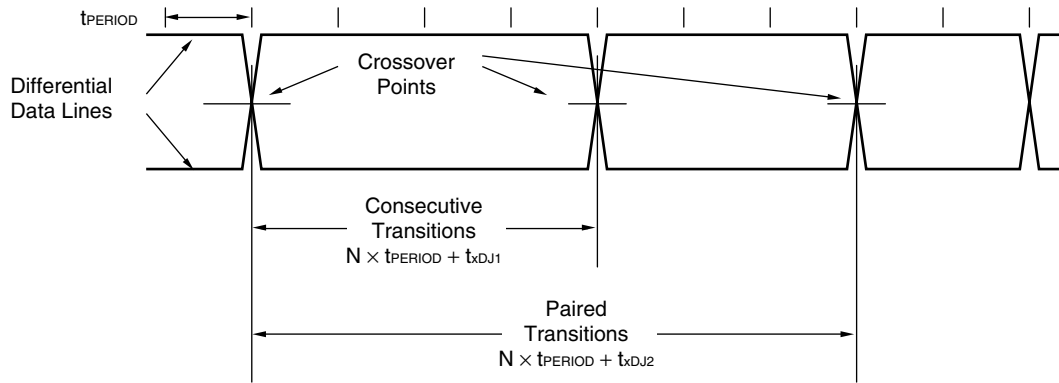


Figure 6-14. USB Differential-to-EOP Transition Skew and EOP Width for Low-/full-speed

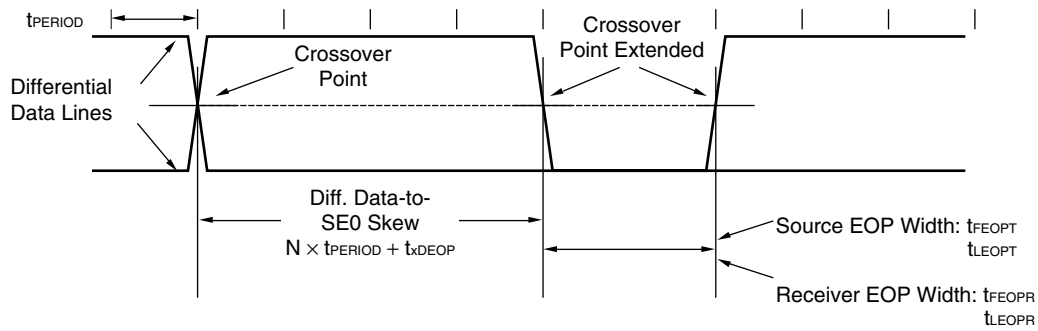


Figure 6-15. USB Receiver Jitter Tolerance for Low-/full-speed

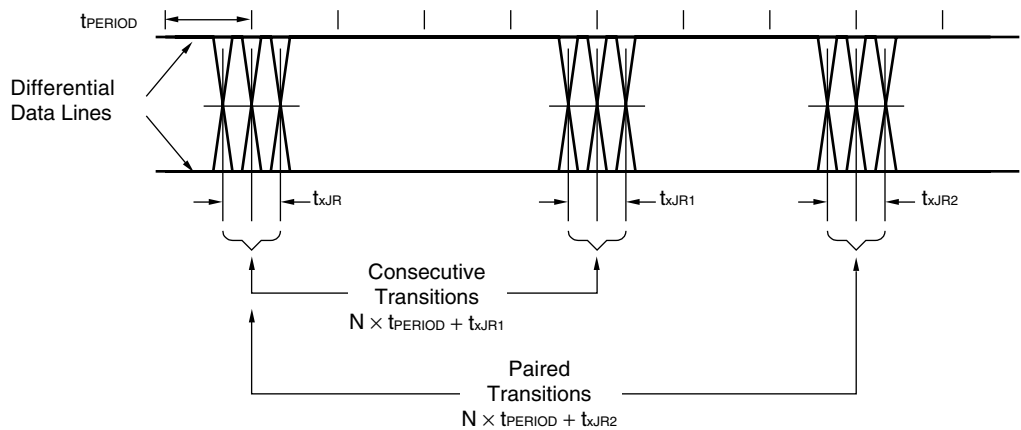


Figure 6-16. Low-/full-speed Disconnect Detection

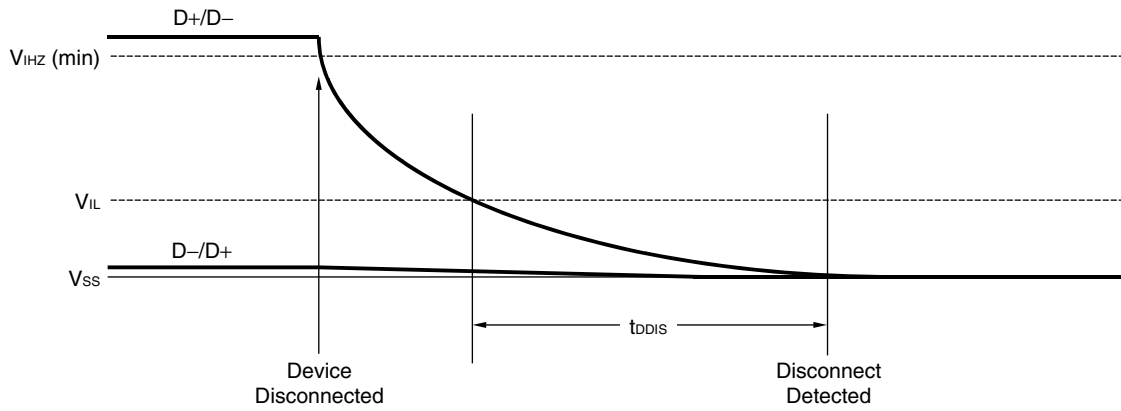


Figure 6-17. Full-/high-speed Device Connect Detection

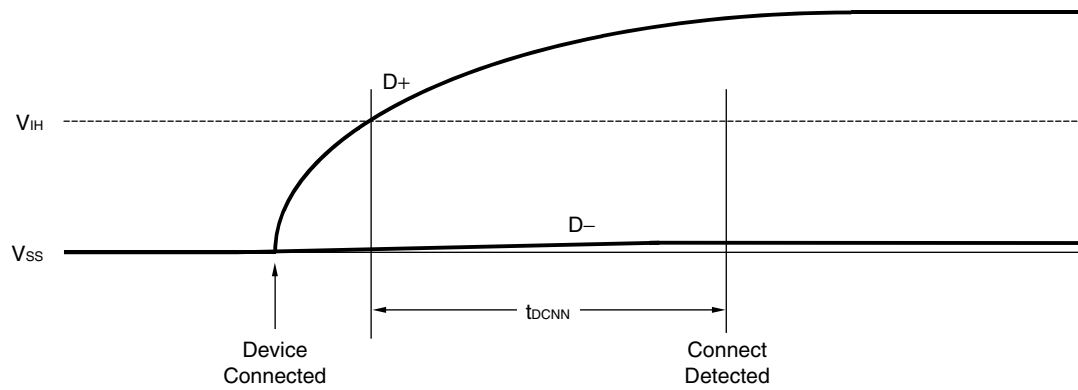
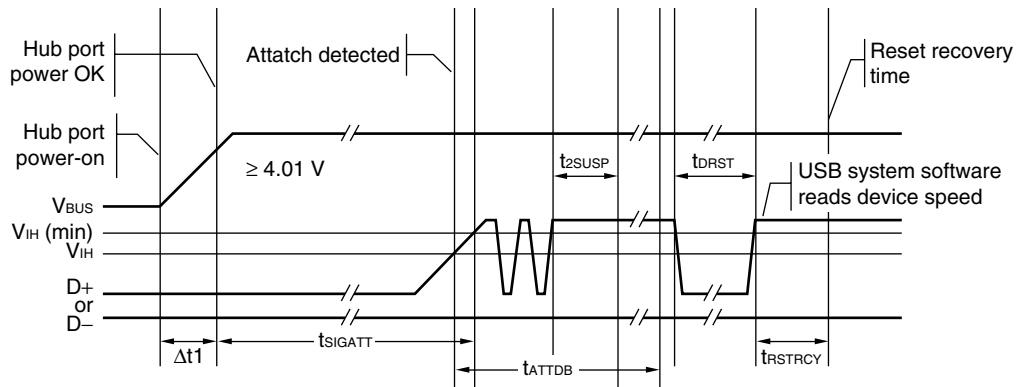


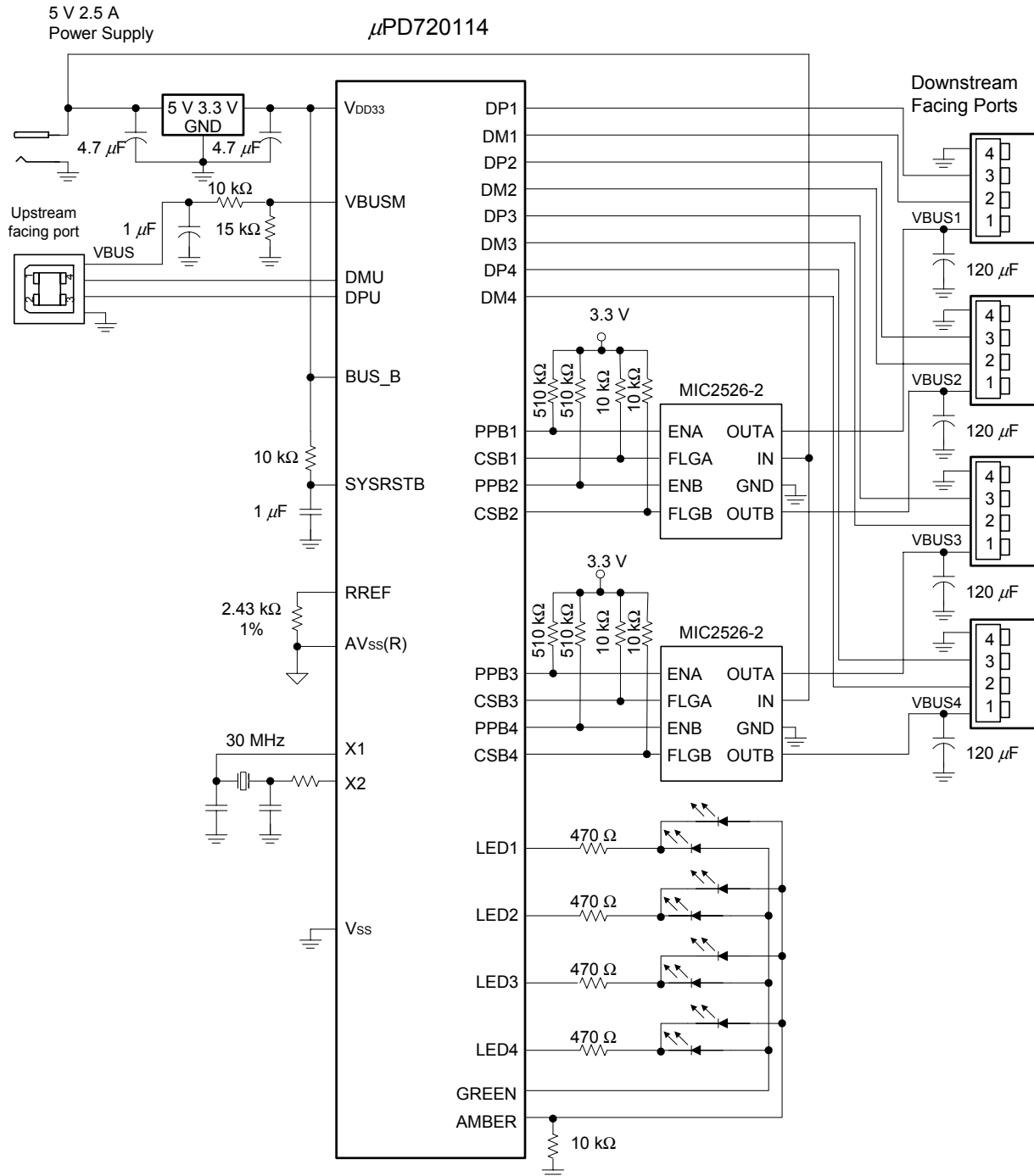
Figure 6-18. Power-on and Connection Events Timing



CHAPTER 7 APPLICATION INFORMATION

7.1 4 Port Self-powered Individual Port Power Management Hub

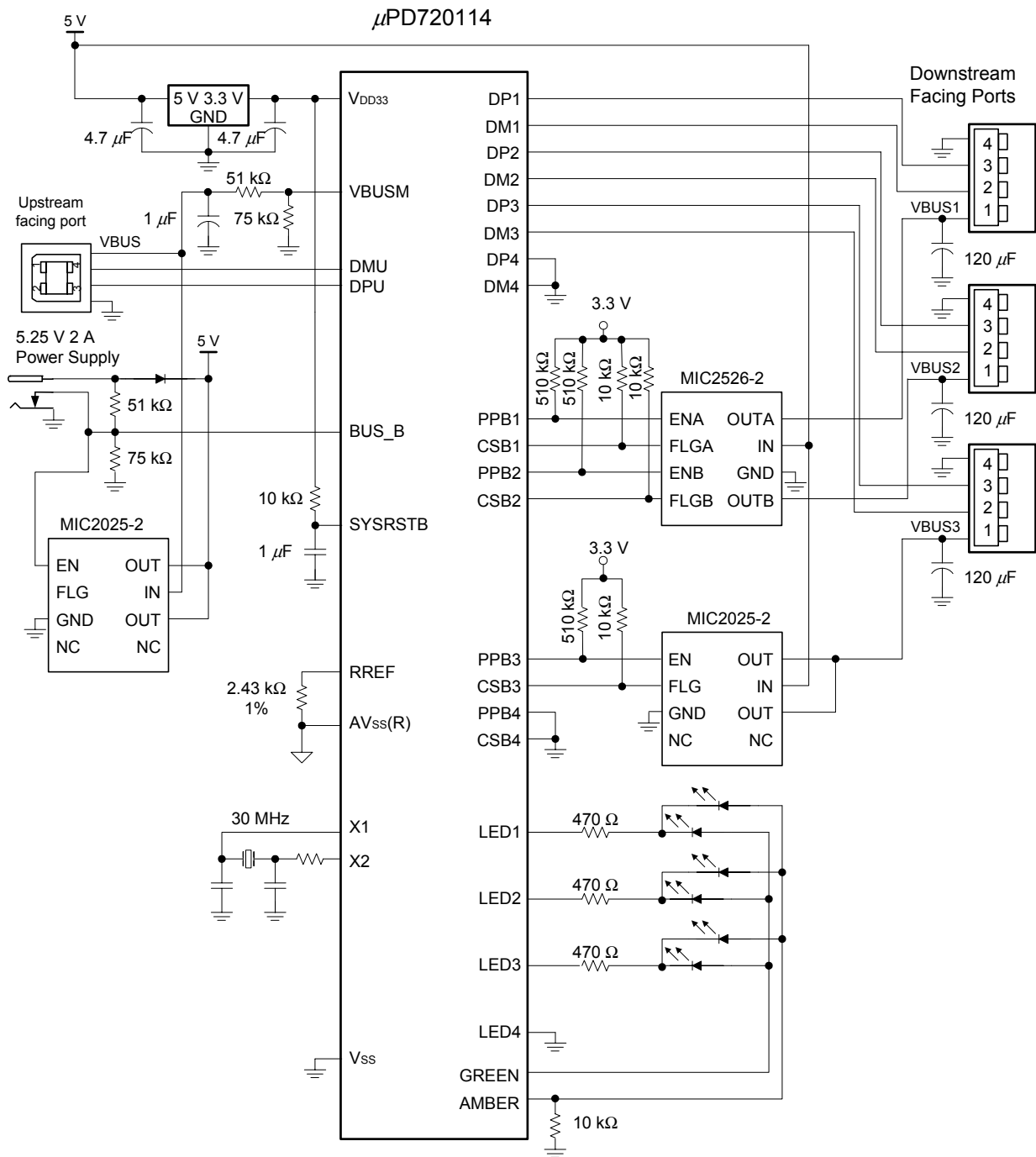
Figure 7-1. 4 Port Self-powered Individual Port Power Management Hub with LED Indicator Diagram



Remark PPB[4:1] should connect by 510 k Ω resistance to 3.3 V. CSB[4:1] should connect by 10 k Ω resistance to 3.3 V.

7.2 3 Port Bus/self-powered Individual Port Power Management Hub

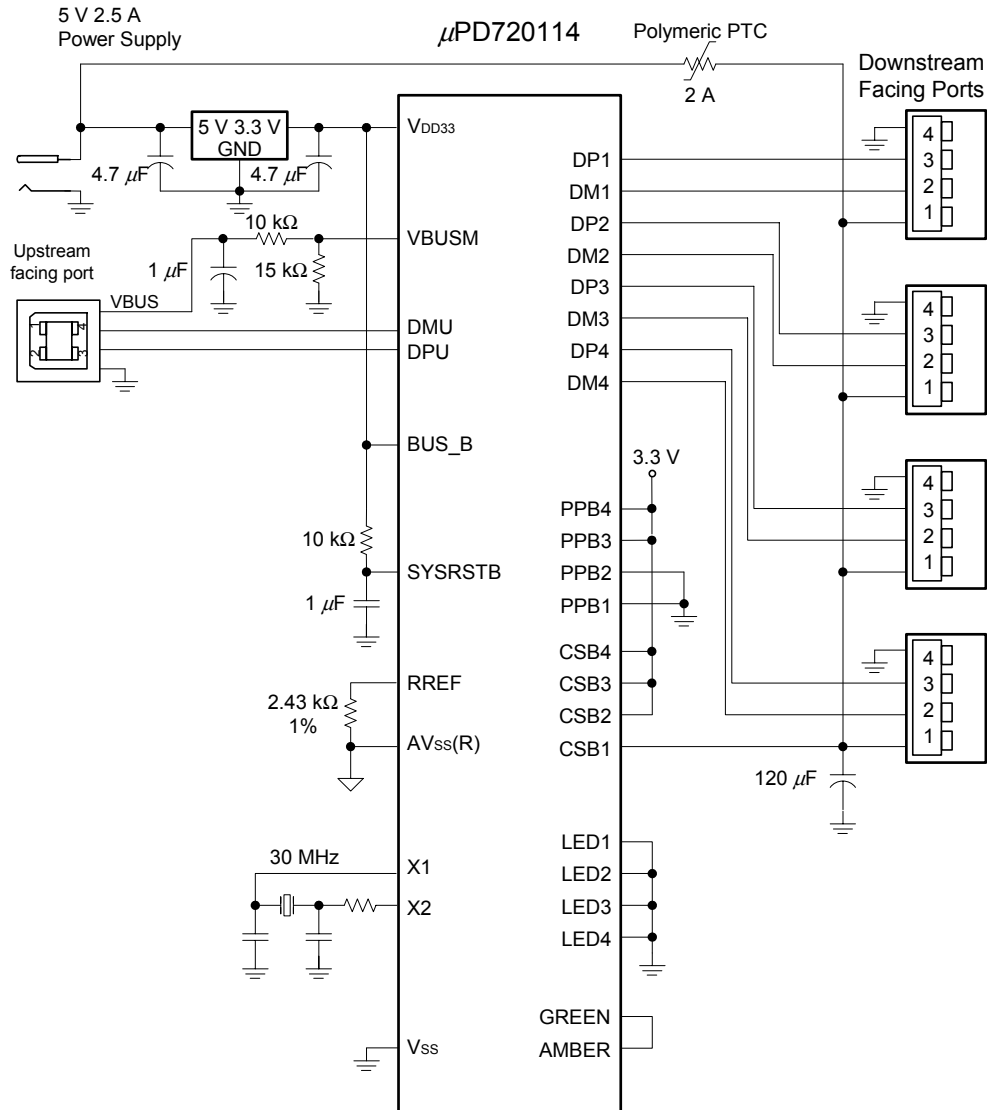
Figure 7-2. 3 Port Bus/self-powered Individual Port Power Management Hub Diagram



Remark PPB[3:1] should connect by 510 k Ω resistance to 3.3 V. CSB[3:1] should connect by 10 k Ω resistance to 3.3 V.

7.3 4 Port Self-powered Ganged Port Power Management Hub

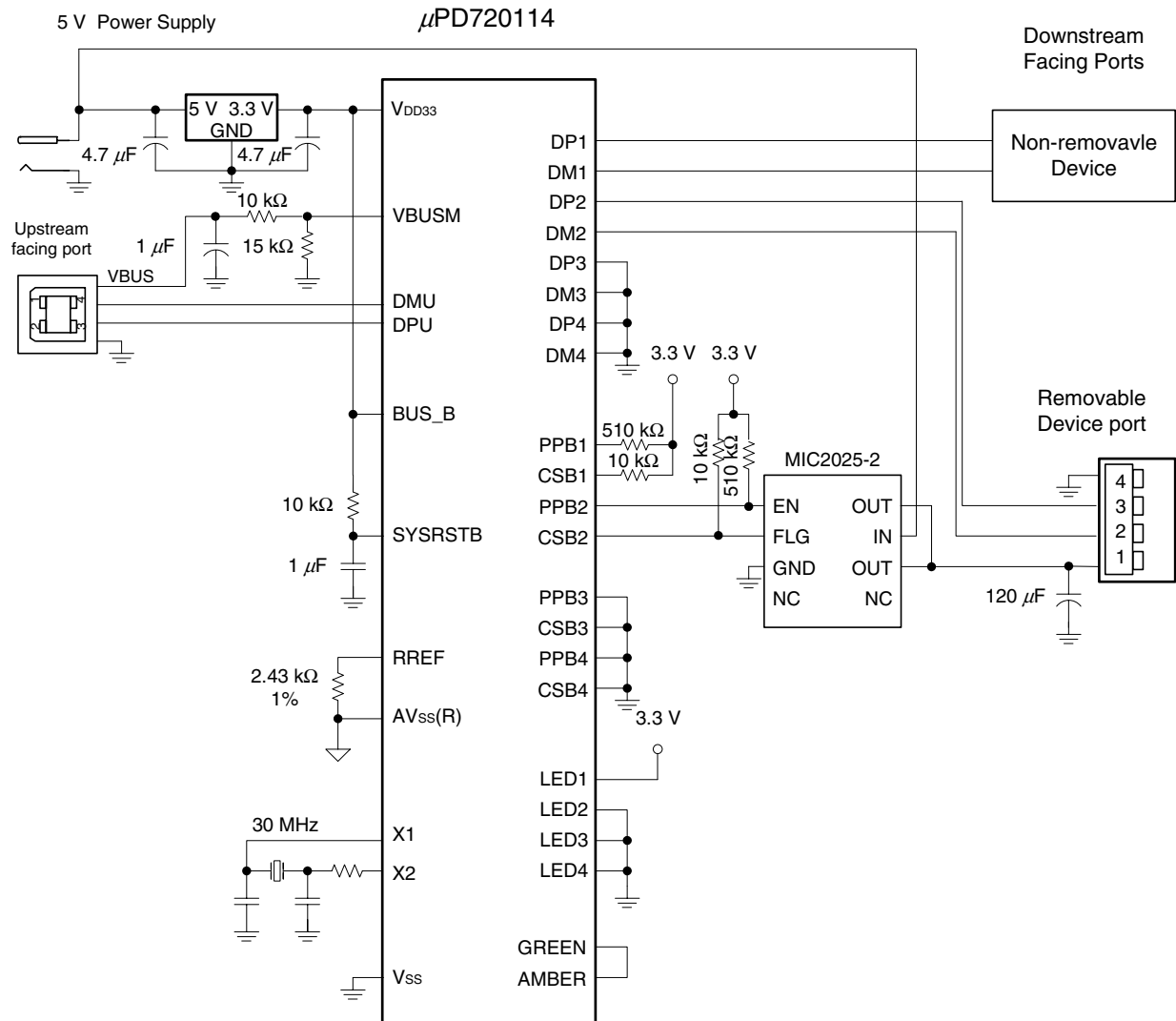
Figure 7-3. 4 Port Self-powered Ganged Port Power Management Hub without LED Indicator Diagram



Remark PPB1, PPB2 should connect to low when no power switch used.

7.4 2 Port Hub with One Embedded Device

Figure 7-4. 2 Port Hub with Embedded Device Diagram



Remark PPB[2:1] should connect by 510 k Ω resistance to 3.3 V. CSB[2:1] should connect by 10 k Ω resistance to 3.3 V, and PPB[4:3] should connect to low.

[MEMO]

[MEMO]

*For further information,
please contact:*

NEC Electronics Corporation
1753, Shimonumabe, Nakahara-ku,
Kawasaki, Kanagawa 211-8668,
Japan
Tel: 044-435-5111
<http://www.necel.com/>

[America]

NEC Electronics America, Inc.
2880 Scott Blvd.
Santa Clara, CA 95050-2554, U.S.A.
Tel: 408-588-6000
800-366-9782
<http://www.am.necel.com/>

[Europe]

NEC Electronics (Europe) GmbH
Arcadiastrasse 10
40472 Düsseldorf, Germany
Tel: 0211-65030
<http://www.eu.necel.com/>

Hanover Office

Podbielskistrasse 166 B
30177 Hannover
Tel: 0 511 33 40 2-0

Munich Office

Werner-Eckert-Strasse 9
81829 München
Tel: 0 89 92 10 03-0

Stuttgart Office

Industriestrasse 3
70565 Stuttgart
Tel: 0 711 99 01 0-0

United Kingdom Branch

Cygnus House, Sunrise Parkway
Linford Wood, Milton Keynes
MK14 6NP, U.K.
Tel: 01908-691-133

Succursale Française

9, rue Paul Dautier, B.P. 52
78142 Velizy-Villacoublay Cédex
France
Tel: 01-3067-5800

Sucursal en España

Juan Esplandiú, 15
28007 Madrid, Spain
Tel: 091-504-2787

Tyskland Filial

Täby Centrum
Entrance S (7th floor)
18322 Täby, Sweden
Tel: 08 638 72 00

Filiale Italiana

Via Fabio Filzi, 25/A
20124 Milano, Italy
Tel: 02-667541

Branch The Netherlands

Steijgerweg 6
5616 HS Eindhoven
The Netherlands
Tel: 040 265 40 10

[Asia & Oceania]

NEC Electronics (China) Co., Ltd

7th Floor, Quantum Plaza, No. 27 ZhiChunLu Haidian
District, Beijing 100083, P.R.China
Tel: 010-8235-1155
<http://www.cn.necel.com/>

Shanghai Branch

Room 2509-2510, Bank of China Tower,
200 Yincheng Road Central,
Pudong New Area, Shanghai, P.R.China P.C:200120
Tel:021-5888-5400
<http://www.cn.necel.com/>

Shenzhen Branch

Unit 01, 39/F, Excellence Times Square Building,
No. 4068 Yi Tian Road, Futian District, Shenzhen,
P.R.China P.C:518048
Tel:0755-8282-9800
<http://www.cn.necel.com/>

NEC Electronics Hong Kong Ltd.

Unit 1601-1613, 16/F., Tower 2, Grand Century Place,
193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: 2886-9318
<http://www.hk.necel.com/>

NEC Electronics Taiwan Ltd.

7F, No. 363 Fu Shing North Road
Taipei, Taiwan, R. O. C.
Tel: 02-8175-9600
<http://www.tw.necel.com/>

NEC Electronics Singapore Pte. Ltd.

238A Thomson Road,
#12-08 Novena Square,
Singapore 307684
Tel: 6253-8311
<http://www.sg.necel.com/>

NEC Electronics Korea Ltd.

11F., Samik Lavied'or Bldg., 720-2,
Yeoksam-Dong, Kangnam-Ku,
Seoul, 135-080, Korea
Tel: 02-558-3737
<http://www.kr.necel.com/>