AU6350-MGL

USB2.0 Hub-Reader Controller

Technical Reference Manual

Rev. 1.04

30 APR. 2009

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Revision History

Date	Revision	Description
Nov 2008	1.00	Official Release
Jan 2009	1.01	Remove “Table 5.6 Static characteristic : Digital pin”
Mar 2009	1.02	Modify Feature 1.2.
Mar 2009	1.03	Modify Pin Description
Apr 2009	1.04	Modify “Table 5.1 Absolute Maximum Ratings”

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1. Introduction

1.1 Description

AU6350-MGL is a single chip integrated USB2.0 hub and SD/MS card reader controller.

1.2 Features

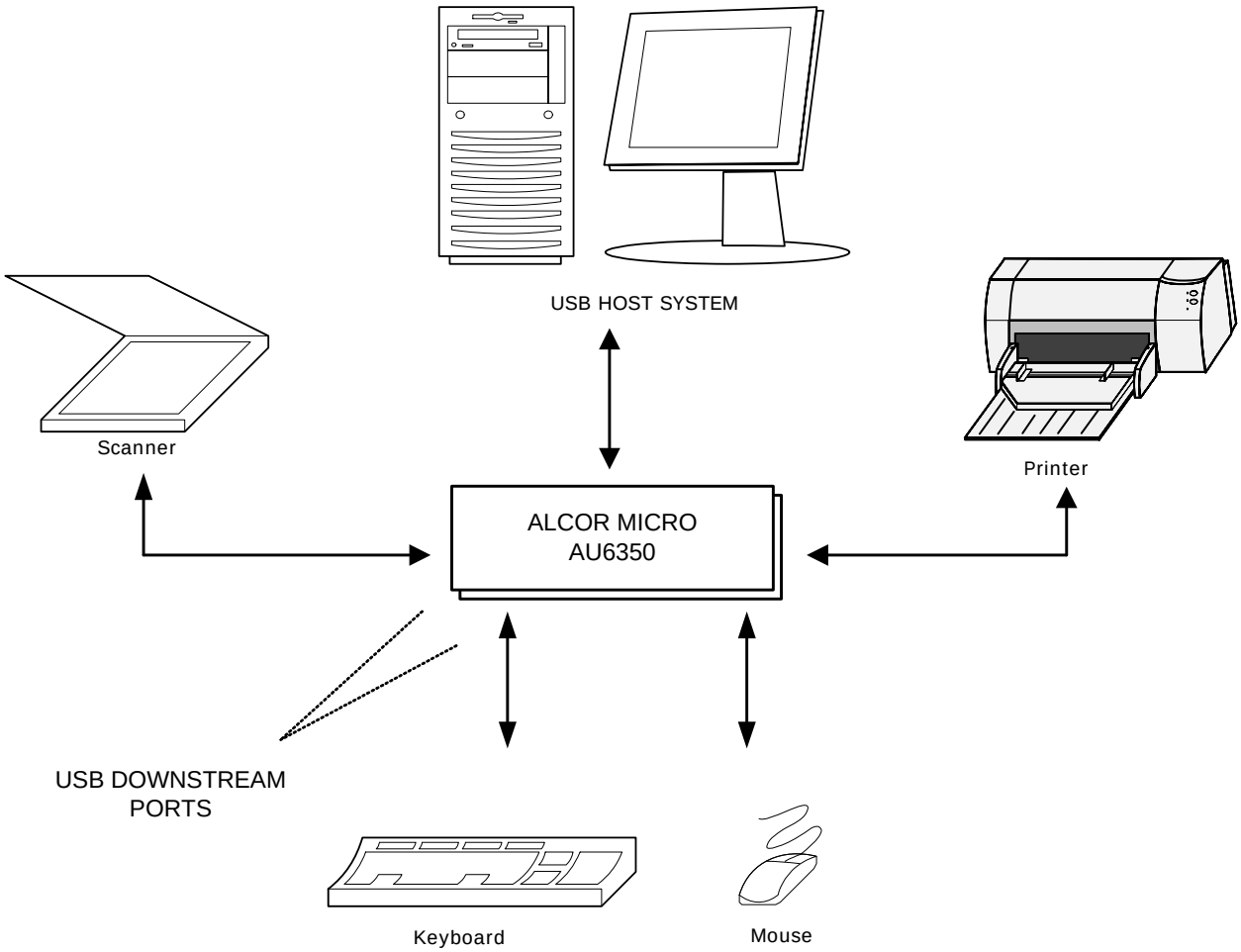
- HUB
  - Fully compliant with USB Hub Specification version 2.0 and is also backward compatible with USB Hub specification 1.1.
  - Supports three bus-powered/self-powered downstream ports.
  - Supports automatic switching between bus-power and self-power modes.
  - Cost effective design using one transaction translator for all downstream ports.
  - Extra low power consumption.
  - On chip internal pull-up and meets USB bus power regain emend pull down resistors for all data line.
  - Built-in USB 2.0 transceiver.
  - Supports gang modes of power management.
  - Built-in power switch control for over current sensing control.
  - Built-in 1.8V regulator for core logic.
  - Built-in 3.3V regulator
  - Embedded in PLL circuit for 12MHz operation precision.

- Card Reader
  - USB Device Class Definition for Mass Storage, Bulk-Transport V1.0
  - Support SD spec up to ver. 2.0 (SDHC).
  - Support MMC spec up to ver. 4.2.
  - Support MS spec up to ver. 1.43.
  - Support MSPRO spec up to ver. 1.03.
  - Compatible to MSPRO-HG spec up to ver. 1.01 with 4-bit data bus
  - Hardware DMA engine integrated for performance enhancement.
  - Work with default driver from Windows ME/2000/XP and Mac OS X; Windows 98/2000(SP1/SP2) and Mac OS 9 are supported by vendor driver from Alcor.
  - Ping-pong FIFO implementation for concurrent bus operation
  - Support multiple sectors transfer optimize performance
  - Support port-to-slot and read/write operation
  - Support Dynamic Icon Utility
  - Power switch integrated to reduce production BOM cost

2. Application Block Diagram

AU6350 is a single chip 3-port USB Hub-Reader controller. Its upstream port is connected to a USB Host system. The downstream ports can be used for a mouse, joystick, scanner, printer or other devices.

Figure 2.1 Block Diagram



3. Pin Assignment

AU6350-MGL is available in 48-pin LQFP package. Below diagram shows signal name of each pin and table in the following page describes each pin in detail.

Figure 3.1 AU6350-MGL Pin Assignment Diagram

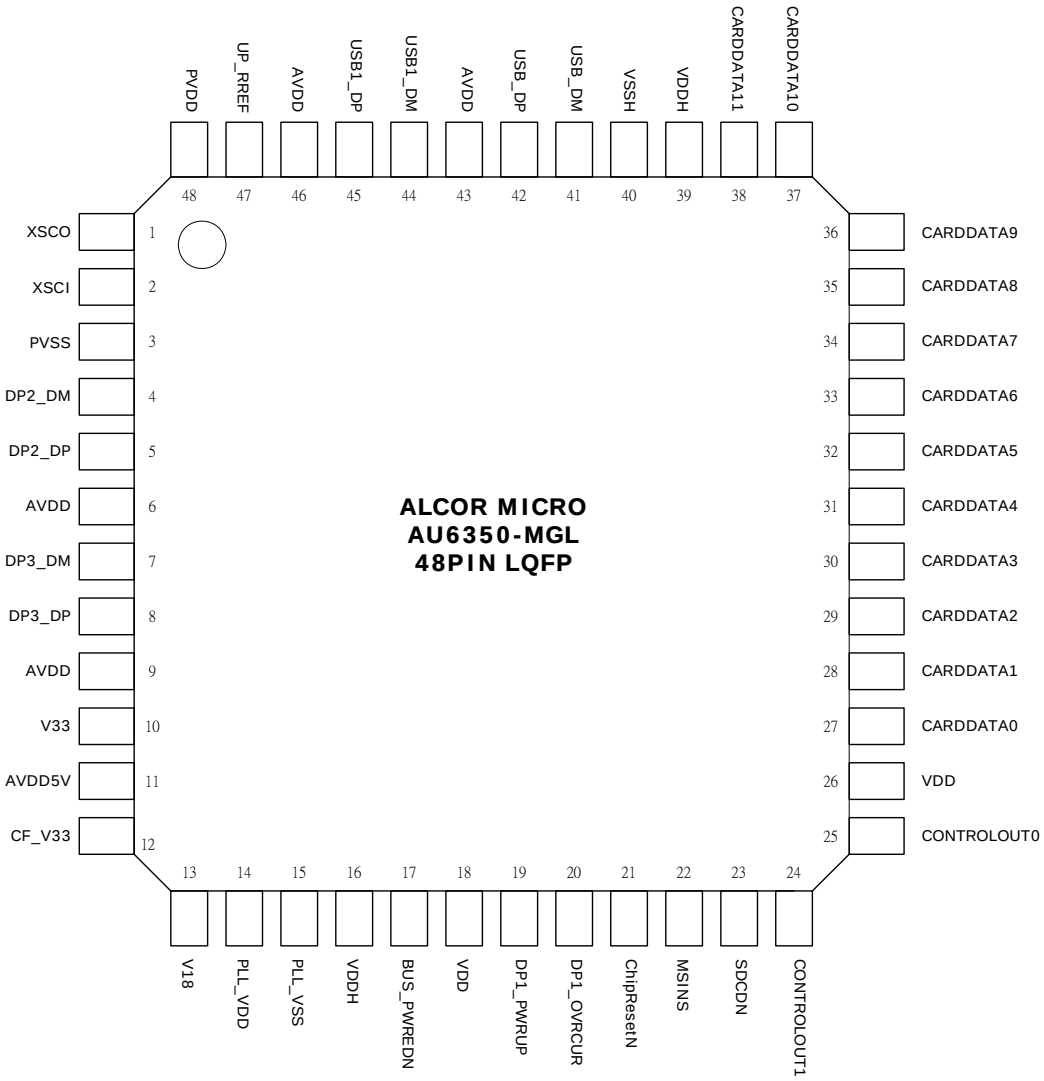


Table 3.1 AU6350-MGL Pin Descriptions

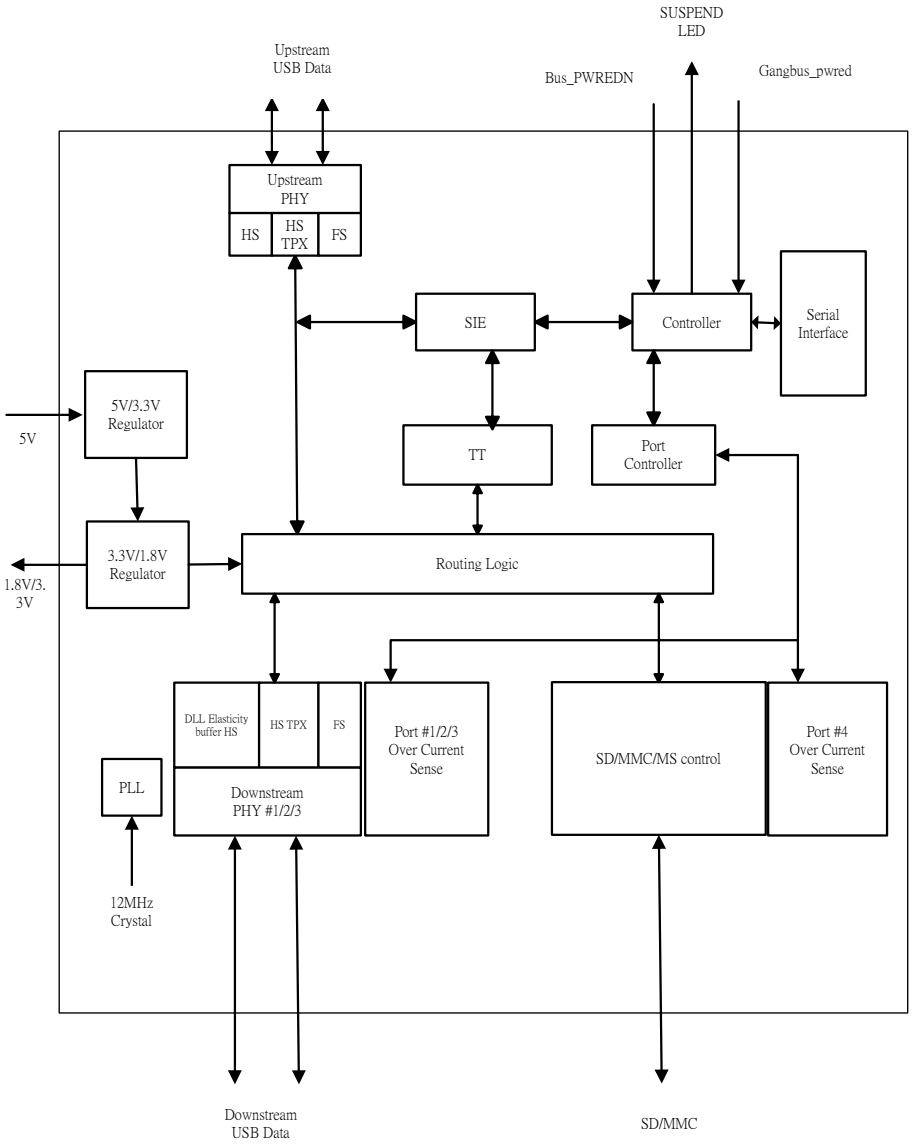
Pin #	Pin Name	I/O	Description
1	XSCO		12MHz crystal output
2	XSCI		12MHz crystal input
3	PVSS	GND	Ground
4	DP2_DM		Port2 USB bus
5	DP2_DP		Port2 USB bus
6	AVDD	PWR	3.3V power input
7	DP3_DM		Port3 USB bus
8	DP3_DP		Port3 USB bus
9	AVDD	PWR	3.3V power input
10	V33	PWR	Voltage regulator output 3.3V
11	AVDD5V	PWR	5V power input
12	CF_V33	PWR	card power 3.3V output
13	V18	PWR	1.8V power output
14	PLL_VDD	PWR	1.8V power input
15	PLL_VSS	GND	Ground
16	VDDH	PWR	3.3V power input
17	BUS_PWREDN	I	'1' = Self Powered '0' = Bus Powered
18	VDD	PWR	1.8V power input
19	DP1_PWRUP	O	Port1 PowerEnable '0' = power on '1' = power off
20	DP1_OVRCUR	I	Port 1 Overcurrent '0' = overcurrent '1' = not overcurrent
21	ChipResetN	I	0' = Reset '1' = Run
22	MSINS	I	MS card detect
23	SDCDN	I	SD card detect
24	CONTROLOUT1	O	MSCLK
25	CONTROLOUT0	O	SDCLK / MSBS
26	VDD	PWR	1.8V power input
27	CARDDATA0	IO	SDCMD / MSDAT0
28	CARDDATA1	IO	MSDAT1
29	CARDDATA2	IO	SDWP / MSDAT2
30	CARDDATA3	IO	MSDAT3
31	CARDDATA4	IO	SDDAT0 / MSDAT4
32	CARDDATA5	IO	SDDAT1 / MSDAT5
33	CARDDATA6	IO	SDDAT2 / MSDAT6

Pin #	Pin Name	I/O	Description
34	CARDDATA7	IO	SDDAT3 / MSDAT7
35	CARDDATA8	IO	SDDAT4
36	CARDDATA9	IO	SDDAT5
37	CARDDATA10	IO	SDDAT6
38	CARDDATA11	IO	SDDAT7
39	VDDH	PWR	3.3V power input
40	VSSH	GND	Ground
41	USB_DM		Upstream port USB bus
42	USB_DP		Upstream port USB bus
43	AVDD	PWR	3.3V power input
44	USB1_DM		Port1 USB bus
45	USB1_DP		Port1 USB bus
46	AVDD	PWR	3.3V power input
47	UP_RREF		1K 1% current reference resistor
48	PVDD	PWR	3.3V power input

4. System Architecture and Reference Design

4.1 AU6350 Block Diagram

Figure 4.1 AU6350-MGL Block Diagram



5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{5IN}	Power Supply	-1 to 6V	V
V_{DDH}	Power Supply	-0.3 to V_{DDH} +0.3	V
V_{IN}	Input Signal Voltage	-0.3 to 3.6	V
V_{OUT}	Output Signal Voltage	-0.3 to V_{DDH} +0.3	V
T_{STG}	Storage Temperature	-40 to 150	^{O}C

5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{5IN}	5V Power Supply	4.5	5.0	5.5	V
V_{DDH}	Power Supply	3.0	3.3	3.6	V
V_{DD}	Digital Supply	1.62	1.8	1.98	V
V_{IN}	Input Signal Voltage	0	3.3	3.6	V
T_{OPR}	Operating Temperature	0		85	^{O}C

5.3 General DC Characteristics

Table 5.3 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IN}	Input current	No pull-up or pull-down	-10	±1	10	μA
I_{OZ}	Tri-state leakage current		-10	±1	10	μA
C_{IN}	Input capacitance	Pad Limit		2.8		ρF
C_{OUT}	Output capacitance	Pad Limit		2.8		ρF
C_{BID}	Bi-directional buffer capacitance	Pad Limit		2.8		ρF

5.4 DC Electrical Characteristics of 3.3V I/O Cells

Table 5.4 DC Electrical Characteristics of 3.3V I/O Cells

SYMBOL	PARAMETER	CONDITIONS	Limits			UNIT
			MIN	TYP	MAX	
V_{D33P}	Power supply	3.3V I/O	3.0	3.3	3.6	V
V_{il}	Input low voltage	LVTTL			0.8	V
V_{ih}	Input high voltage		2.0			V
V_{ol}	Output low voltage	$\lvert I_{ol} \rvert$ =2~16mA			0.4	V
V_{oh}	Output high voltage	$\lvert I_{oh} \rvert$ =2~16mA	2.4			V
R_{pu}	Input pull-up resistance	PU=high, PD=low	55	75	110	KΩ
R_{pd}	Input pull-down resistance	PU=low, PD=high	40	75	150	KΩ
I_{in}	Input leakage current	V_{in}= V_{D33P} or 0	-10	±1	10	μA
I_{oz}	Tri-state output leakage current		-10	±1	10	μA

5.5 USB Transceiver Characteristics

Table 5.5 Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VD33P	Analog supply Voltage		3.0	3.3	3.6	V
VDD V18	Digital supply Voltage		1.62	1.8	1.98	V
I_{CC}	Operating supply current	High speed operating at 480 MHz			55	mA

Table 5.6 Static characteristic：Analog I/O pins（DP/DM）

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
USB2.0 Transceiver（HS）						
Input Levels（differential receiver）						
V_{HSDIFF}	High speed differential input sensitivity	$\lvert V_{I(DP)}-V_{I(DM)} \rvert$ measured at the connection as application circuit	300			mV
V_{HSCM}	High speed data signaling common mode voltage range		-50		500	mV
V_{HSSQ}	High speed squelch detection threshold	Squelch detected			100	mV
		No squelch detected	150			mV
V_{HSDSC}	High speed disconnection detection threshold	Disconnection detected	625			mV
		Disconnection not detected			525	mV
Output Levels						
V_{HSOI}	High speed idle level output voltage(differential)		-10		10	mV
V_{HSOL}	High speed low level output voltage(differential)		-10		10	mV
V_{HSOH}	High speed high level output voltage(differential)		-360		400	mV
V_{CHIRPJ}	Chirp-J output voltage（differential）		700		1100	mV
V_{CHIRPK}	Chirp-K output voltage（differential）		-900		-500	mV
Resistance						
R_{DRV}	Driver output impedance	Equivalent resistance used as internal chip only	3	6	9	Ω
		Overall resistance including external resistor	40.5	45	49.5	
Termination						
V_{TERM}	Termination voltage for pull-up resistor on pin RPU		3.0		3.6	V
USB1.1 Transceiver（FS/LS）						
Input Levels（differential receiver）						
V_{DI}	Differential input sensitivity	$\lvert V_{I(DP)}-V_{I(DM)} \rvert$	0.2			V
V_{CM}	Differential common mode voltage		0.8		2.5	V
Input Levels（single-ended receivers）						
V_{SE}	Single ended receiver threshold		0.8		2.0	V
Output levels						

V_{OL}	Low-level output voltage		0		0.3	V
V_{OH}	High-level output voltage		2.8		3.6	V

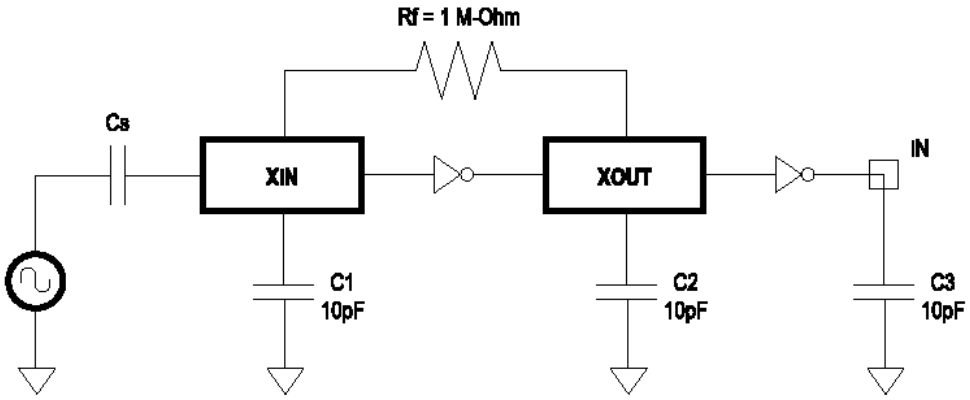
Table 5.7 Dynamic characteristic：Analog I/O pins（DP/DM）

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Driver Characteristics						
High-Speed Mode						
t_{HSR}	High-speed differential rise time		500			ps
t_{HSF}	High-speed differential fall time		500			ps
Full-Speed Mode						
t_{FR}	Rise time	CL=50pF；10 to 90% of $\lvert V_{OH}-V_{OL} \rvert$ ；	4		20	ns
t_{FF}	Fall time	CL=50pF；90 to 10% of $\lvert V_{OH}-V_{OL} \rvert$ ；	4		20	ns
t_{FRMA}	Differential rise/fall time matching（t_{FR} / t_{FF}）	Excluding the first transition from idle mode	90		110	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
Low-Speed Mode						
t_{LR}	Rise time	CL=200pF-600pF；10 to 90% of $\lvert V_{OH}-V_{OL} \rvert$ ；	75		300	ns
t_{LF}	Fall time	CL=200pF-600pF；90 to 10% of $\lvert V_{OH}-V_{OL} \rvert$ ；	75		300	ns
t_{LRMA}	Differential rise/fall time matching（t_{LR} / t_{LF}）	Excluding the first transition from idle mode	80		125	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
V_{OH}	High-level output voltage		2.8		3.6	V

5.6 Crystal Oscillator Circuit Setup for Characterization

The following setup was used to measure the open loop voltage gain for crystal oscillator circuits. The feedback resistor serves to bias the circuit at its quiescent operating point and the AC coupling capacitor, Cs, is much larger than C1 and C2.

Figure 5.1 Crystal Oscillator Circuit Setup for Characterization



5.7 Bus Timing / Electrical Characteristics

Table 5.8 DC Electrical Characteristics

Input Levels for Low-/Full –speed:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{IH}	High (Driven)	2.0		V
V_{IHZ}	High (floating)	2.7	3.6	V
V_{IL}	Low		0.8	V
V_{DI}	Differential Input Sensitivity	0.2		V
V_{CM}	Differential Common Mode Range	0.8	2.5	V

Input Levels for High –speed:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{HHSSQ}	High-speed squelch detection threshold (differential signal amplitude)	100	150	mV
V_{HSDSC}	High speed disconnect detection threshold (differential signal amplitude)	525	625	mV

Output Levels for Low-/Full-speed:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{OL}	Low	0.0	0.3	V
V_{OH}	High (driven)	2.8	3.6	V
V_{OSE1}	SE1	0.8		V
V_{CRS}	Output Signal Crossover Voltage	1.3	2.0	V

Output Levels for High –speed:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{HSOI}	High-speed idle level	-10	10	mV
V_{HSOH}	High-speed data signaling high	360	440	mV
V_{HSOL}	High-speed data signaling low	-10	10	mV
V_{CHIRPJ}	Chirp J level (differential voltage)	700	1100	mV
V_{CHIRPK}	Chirp K level (differential voltage)	-900	-500	mV

Terminations:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
R_{PU}	Bus Pull-up Resistor on Upstream Facing Port	1.425	1.575	kΩ
R_{PD}	Bus Pull-down Resistor on Upstream Facing Port	14.25	15.75	kΩ
Z_{INP}	Input impedance exclusive of pull-up/pull-down (for low-/full-speed)	300		kΩ
V_{TERM}	Termination voltage for upstream facing port pull-up (R_{PU})	3.0	3.6	V

Terminations in High-speed:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{HSTERM}	Termination voltage in high-speed	-10	10	mV

Table 5.9 High-speed Source Electrical Characteristics

Driver Characteristics:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
T_{HSR}	Rise Time (10%-90%)	500		ps
T_{HSF}	Fall Time (10%-90%)	500		ps
Z_{HSDRV}	Driver Output Resistance (which also serves as high-speed termination)	40.5	49.5	Ω

Clock Timings:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
T_{HSDRAT}	High-speed Data Rate	479.76	480.24	Mb/s
T_{HSFRAM}	Micorframe Interval	124.9375	125.0625	μs
T_{HSRFI}	Consecutive Microframe Interval Difference		4 high-speed bit times	

Table 5.10 Full-speed Source Electrical Characteristics

Driver Characteristics:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
T_{FR}	Rise Time	4	20	ns
T_{FF}	Fall Time	4	20	ns
T_{FRFM}	Differential Rise and Fall Time Matching	90	111.11	%
Z_{ZRV}	Driver Output Resistance for driver which is not high-speed capable	28	44	Ω

Clock Timings:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
$T_{FDRATHS}$	Full-speed Data Rate for hubs and devices which are high-speed capable	11.994	12.006	Mb/s
T_{FDRATE}	Full-speed Data Rate for devices which are not high-speed capable	11.970	12.030	Mb/s
T_{FRAME}	Frame interval	0.9995	1.0005	Ms
T_{RFI}	Consecutive Frame Interval Jitter		42	ns

Full-speed Data Timings:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
	Source Jitter Total(including frequency tolerance):			
T_{DJ1}	To Next Transition	-3.5	-3.5	ns
T_{DJ2}	For Paired Transitions	-4	-4	ns
T_{FDEOP}	Source Jitter for Differential Transition to SE0 Transition	-2	5	ns
	Receiver Jitter:			
T_{JR1}	To Next Transition	-18.5	-18.5	ns
T_{JR2}	For Paired Transitions	-9	-9	ns
T_{FEPPT}	Source SE0 interval of EOP	160	175	ns
T_{FEOPR}	Receiver SE0 interval of EOP	82		ns
T_{FST}	Width of SE0 interval during differential transition		14	ns

Table 5.11 Low-speed Source Electrical Characteristics

Driver Characteristics:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
T_{LR}	Rise Time	75	300	ns
T_{LF}	Fall Time	75	300	ns
T_{LRFM}	Differential Rise and Fall Time Matching	80	125	%
C_{LINUA}	Upstream Facing Port (w/cable, low-speed only)	200	450	pF

Clock Timings:

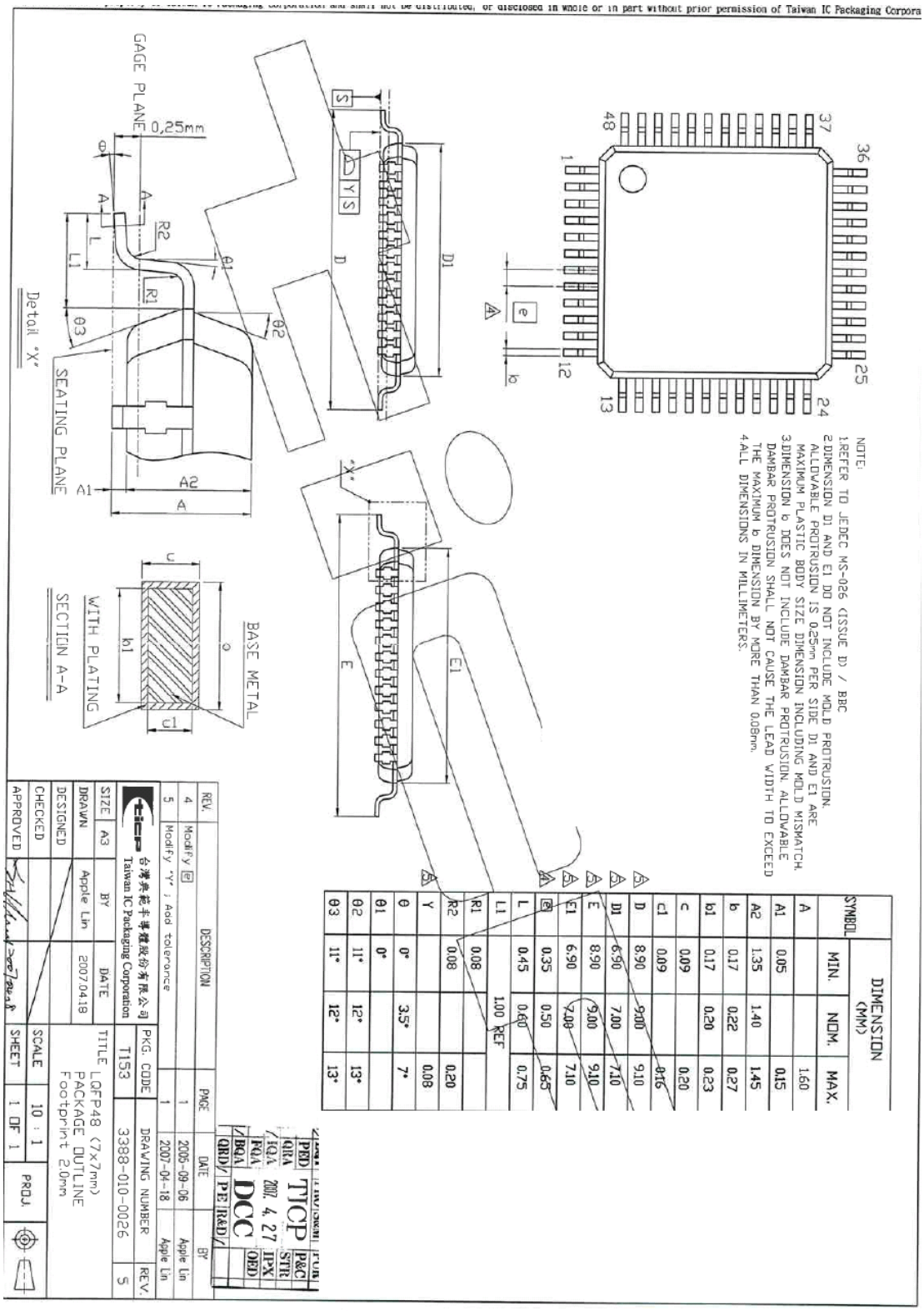
SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
$T_{LDRATHS}$	Low-speed Data Rate for hubs and devices which are high-speed capable	1.49925	1.50075	Mb/s
T_{LDRATE}	Low-speed Data Rate for devices which are not high-speed capable	1.4775	1.5225	Mb/s

Low-speed Data Timings:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
	Upstream facing port source Jitter Total(including frequency tolerance):			
T_{UDJ1}	To Next Transition	-95	95	ns
T_{UDJ2}	For Paired Transitions	-150	150	ns
T_{LDEOP}	Upstream facing port source Jitter for Differential Transition to SE0 Transition	-40	100	ns
	Upstream facing port differential Receiver Jitter:			
T_{DJR1}	To Next Transition	-75	75	ns
T_{DJR2}	For Paired Transitions	-45	45	ns
	Upstream facing port differential Receiver Jitter:			
T_{DDJ1}	To Next Transition	-25	25	ns
T_{DDJ2}	For Paired Transitions	-14	14	ns
	Downstream facing port Differential Receiver Jitter:			
T_{UJR1}	To Next Transition	-152	152	ns
T_{UJR2}	For Paired Transitions	-200	200	ns
T_{LEOPT}	Source SE0 interval of EOP	1.25	1.50	μs
T_{LEOPR}	Receiver SE0 interval of EOP	670		ns
T_{LST}	Width of SE0 interval during differential transition		210	ns

6. Mechanical Information

Figure 6.1 Mechanical Information Diagram



7. Abbreviations

In this chapter some of the terms and abbreviations used throughout the technical reference manual are listed as follows.

SIE	Serial Interface Engine
SD	Secure Digital
MMC	Multimedia Card
UTMI	USB Transceiver Macrocell Interface

About Alcor Micro, Corp.

Alcor Micro, Corp. designs, develops and markets highly integrated and advanced peripheral semiconductor, and software driver solutions for the personal computer and consumer electronics markets worldwide. We specialize in USB solutions and focus on emerging technology such as USB and IEEE 1394. The company offers a range of semiconductors including controllers for USB hub, integrated keyboard/USB hub and USB Flash memory card reader…etc. Alcor Micro, Corp. is based in Taipei, Taiwan, with sales offices in Taipei, Japan, Korea and California. Alcor Micro is distinguished by its ability to provide innovative solutions for spec-driven products. Innovations like single chip solutions for traditional multiple chip products and on-board voltage regulators enable the company to provide cost-efficiency solutions for the computer peripheral device OEM customers worldwide.