Lab Three Notes and Comments

Part 1:

Implementation of a simple gated RS latch. Tried both sets of code in the lab description. In both cases Quartus implemented the modules as four 4-LUTs, as expected. No issues encountered.

Part 2:

Implementation of a simple gated D latch. Modified the code from part 1 and encountered no issues.

Part 3:

Master-Slave D flip flop implemented with two instances of the module from part 2. No issues encountered.

Part 4:

Implemented the D latch with the code from part 2, and both the positive and negative edge triggered D flip flop with the code from part 3. Implemented inverted edge triggering by inverting the clock at the input. Attempted to implement as two separate flip flops, with edge triggering based on and **always @ (pos/negedge Clk)** but realized it could be more easily implemented in this way, and aware that can be posedge or negedge as needed for future modules.

Part 5:

Implemented a 16 bit wide memory register out of D flip flops, connecting the input switches to one set of seven segment displays, and the outputs of the flip flop outputs to the others. Modified the seven segment decoder from lab 2 to output in hex. No issues encountered.