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Part 1 –

Implemented an 8-bit accumulator adder by altering the high level behavioural code in the lab write up. Simulated the circuit to verify its operation. No issues encountered.

Part 2 –

Extended the circuit from part 1 to add subtraction functionality. No problems encountered.

Part 3 –

Based on the guideline of using high level behavioural descriptions, rather than low level logic asked for in the labs, used the same kind of module as in parts 1 & 2 to implement the multiplied. Simulated to verify its operation. No issues encountered.

Under these guidelines, the same code as in part one would be used for parts 4 and 5.

Total Logic Elements – 56
Fmax - Not reported and I can't figure out why, but using one of the Keys as the clock.