Lab Eight Notes and Comments:

Part 1 –

ramlpm.v created from IP library. No issues encountered.

Part 2 –

No issues encountered with realizing the 1-port memory on the DE2. Was able to verify could read/write to all 32 locations.

Part 3 –

No issues encountered with implementing the memory as a multi-dimensional array. The Quartus compiler used memory blocks as expected. Did not notice any differences between the circuits as inferred memory used the same memory blocks as before.

Part 4 –

I had a lot of trouble getting my head around the control inputs needed for the SRAM chip. Found a solution online at **https://github.com/BenBergman/AlteraDE2Labs_Verilog/blob/master/AlteraLab8/part4.v**, which was not copied directly, but solution of my problems with control inputs was heavily based on this code.

Part 5 –

No issues encountered with this problem. Was able to realize the 2-port memory on the DE2 and access all memory locations.

Part 6 –

No issues encountered with this problem. Was able to realize the 1-port memory on the DE2 and access all memory locations, both though direct inputs with the switches, etc, and through the In-System Memory Content Editor.

Part 7 -

Given the issues encountered in Part 4, implemented Ben Bergman's code found at **https://github.com/BenBergman/AlteraDE2Labs_Verilog/blob/master/AlteraLab8/part7.v**. I feel that I understand what changes I needed to make to implement Part 6 using the SRAM instead of memory blocks, but didn't feel like writing from scratch (or copy/paste from previous parts) and the solution from Ben works perfectly.