

Lab Nine Notes and Comments:

Part 1) Implementing a basic processor:

I had a lot of problems with getting this part of the lab complete. To be honest, used the skeleton from the lab description, however did not pay enough attention to how the registers were declared (e.g. `assign I = IR[1:3]`, and in the decoders, least-most significant, rather than most-least). Solution was heavily influenced by the solution available from Ben Bergman at https://github.com/BenBergman/AlteraDE2Labs_Verilog/tree/master/AlteraLab9, however his was based on an old version of the Altera Digital Logic labs, so could not be utilized directly, but did point out what I was misunderstanding about the way the registers were declared.

Once this was sorted, was able to solve other issues. Total time spent on this lab was > 4 hrs.

Part 2) Only issue encountered was not reading the lab write up completely and attempting to implement with a single clock driving both the processor and the memory, which did not work out at all. Instructions from memory need to be loaded in to the processor with vastly different timing to the internal functions of the processor. Otherwise, was a basic extension of part 1.