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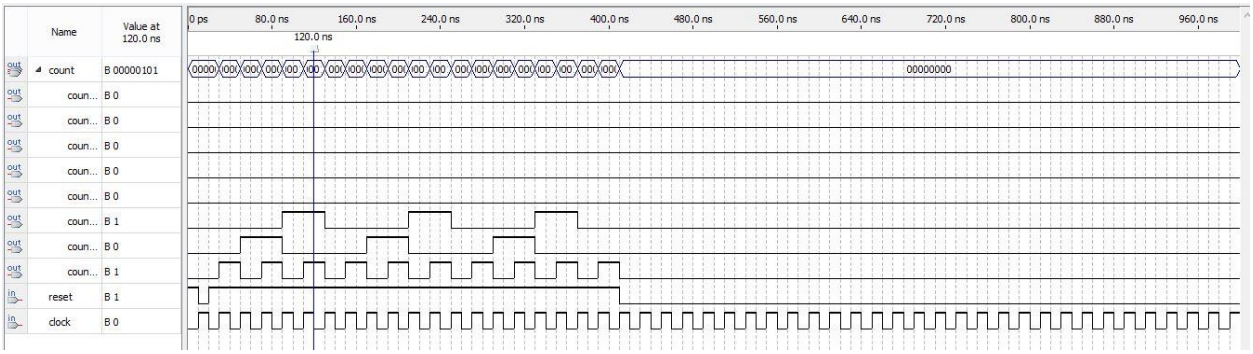
Lab Five Notes and Comments:

Part 1:
Implemented the code from the lab description. No issues encountered.
Simulation output:



Part 2:
Implemented the 3digit BCD counter as one module with, a 12-bit wide output, with a four bit counter for each of the BCD elements, using modulo 10 counters. No issues encountered.

Part 3:
Had no issue implementing the clock as three two digit BCD counters (modified from part 2), modulo 24, 60 and 60. Ran into significant trouble in getting the initial set time option. Spent several hours working on it, and finally added an enable from SW17 to stop the clock while setting the time.

Part 4:
Ran into significant issues in implementing this lab experiment. After several hours of working on this part, I found a 'solution' online from Ben Bergman, Altera DE2 labs_verilog. I could not figure out what was different from my code in the clocking. Both his an mine compiled, but **neither** had the desired behaviour when programmed to the board. I eventually was able to get this to work by modifying his clocking counter arrangements.

All told, I spent >3 hrs on parts 3 & 4.