ECE3750 Project Final Report

Joey's Juniors
12/8/2023

Team Member 1: Daniel Sarria

Team Member 2: Andrew Vithoulkas

Team Member 3: Joey Cohen

Team Member 4: John Skiles

Pledge:
On my honor as a student, I have neither given nor received unauthorized aid on this assignment/examination.

Team Member Responsibilities

Daniel Sarria - I played a comprehensive role in the development of the project, contributing to various aspects. I was actively involved in analytically determining the component values, ensuring the completeness of the parts list, and offering unique insights in the creation of the test plan. Taking a pivotal role in digital signal processing, I not only designed but analytically developed the Finite Impulse Response (FIR) filter kernels for the project. My analytical approach involved careful consideration of signal characteristics and precise calculations to optimize the filter's performance. Additionally, I wrote the necessary code to implement the FIR filter, specifically in generating the filtered EKG signal.

Andrew Vithoulkas - I played a part in all sections of this project, from initial design to finalized testing. In the design phase, I helped by sorting through all data sheets to ensure that we had chosen the values that worked according to the manufacturers. In this same sense, I aided in the math involved for all blocks of the circuit as well as writing the code for the anti-aliasing filters. My board was the one chosen for the final manufacturing board, meaning that my design ultimately was the most efficient with space and part placement. Through testing, I ensured that the output of all circuit components made sense as well as performing continuity checks on all elements. I recorded all measurements from the EKG and ensured that they got on the final report effectively.

Joey Cohen - My primary contribution involved calibrating the instrumentation amplifier. I focused on achieving the correct gain setting, essential for accurately amplifying heart signals. Additionally, I assisted in setting the voltage offset for the integrator, ensuring the output signal was centered at 1.65V. I worked with my groupmates to design the 4th-order Butterworth filter by selecting and testing two 2nd-order Sallen-Key filters to reduce noise and enhance signal quality. My role extended to adjusting the isolator's transfer gain, vital for ensuring clean signal transmission. I engaged in discussions with the teaching assistants during class to gain a better understanding of the specific topics within the project to allow my group and I to exceed the expectations of the EKG hardware. Overall, I was available to assist my group in any way they needed me and bounced around to various roles.

John Skiles - I provided general assistance to my group throughout the course of the project. I was particularly involved in the design of the isolator, analyzing datasheets to determine how to apply universal isolator schematics to the unique requirements of the EKG. I helped to develop the test plan, facilitating correspondence with instructors while team members were absent. I helped to test the board, providing and operating such equipment as the AD2 and multimeter during tests of continuity and power supply. I assisted in debugging the board, namely when challenges arose from the size of the gain resistor, and performed soldering when necessitated by this issue. To verify the overall functionality of the EKG, I submitted myself to the machine and gave unto it the beating of my own heart.

Section 1

Background

Embarking on the design of an Electrocardiogram (EKG), our approach is centered around the integration of key components to elevate signal quality and precision in cardiac electrical activity measurement. This comprehensive design incorporates instrumentation amplifiers, integrators, filters, isolators, analog-to-digital converters (ADCs), and digital signal processing (DSP) techniques. The primary objective is to synergize these elements, optimizing the EKG system for accurate, noise-resistant signal acquisition and advanced digital analysis. As a result, our design process consisted of implementing each component separately and unit testing each component to ensure the intended functionality.

Specifically, the use of an instrumentation amplifier is pivotal in our design as it allows two differential signals, originating from the electrodes placed on a person's skin to measure their heart’s electrical signal, to be accurately and precisely amplified. These differential signals represent the minute electrical potentials generated by the heart's activity. By employing differential amplification, the instrumentation amplifier not only magnifies these faint signals but also effectively cancels out common-mode noise, which is essential when dealing with the subtle electrical variations inherent in capturing the nuanced rhythms of the heart. We aimed for a gain of 1000 in order to achieve a peak-to-peak AC amplitude of 1.0 to 2.5V at the output. This ensures that the signal can be easily seen and is at a voltage level that is relevant for information capture. From here, the gain of the signal all the way to the output should be 1.

The use of an integrator plays a crucial role in aligning the output signal of the instrumentation amplifier with a specific voltage offset. This offset is set by the positive terminal of the integrator, serving as a standardized reference point for the amplified signal. This is due to the raw output not being centered at a convenient reference voltage, potentially containing DC components that need correction. The integrator will have a 1.65V DC input into its positive terminal. Therefore, the output signal of the instrumentation amplifier is expected to be centered at 1.65V.

The filtering stage is accomplished through the implementation of two 2nd-order low-pass Sallen-Key filters. These filters play a critical role in refining the EKG signal by selectively allowing lower-frequency components to pass through while attenuating

higher-frequency signals. The choice of Sallen-Key filters is deliberate, as they offer a balance between simplicity, performance, and versatility. Each 2nd order low-pass filter is designed to attenuate frequencies above a certain cutoff point, effectively removing high-frequency noise that may have been introduced during the signal acquisition process. By cascading two of these 2nd-order filters together, we create a 4th-order Butterworth filter, which acts as an antialiasing filter. This is crucial in analog-to-digital conversion, preventing aliasing that could distort the digital representation of the EKG signal. The filters were designed to attenuate a signal to -72 dB at 500 Hz. Additionally, the order of the Q values of each filter was important because designing a 4th order Butterworth filter requires the first stage of the filter to have a Q value of 0.5412 and the second stage of the filter to have a Q value of 1.3065. The values of the capacitors and resistors were designed using a simplification technique provided by Texas Instruments' Active Low-Pass Filter Design document in order to keep the gain to 1 in the passband.

Lastly, the isolator provides physical isolation between the input signal and the output signals of the overall circuit. It ensures that signals on one side of the isolator do not directly affect or interfere with the components on the other side. This allows us to transmit signals across the isolation barrier without introducing unwanted noise or distortion. This helps maintain the integrity of the output EKG signal. The isolator was designed to have a transfer gain bin between 1.297 and 1.456. The overall gain of input to the output of the isolator should be seen as 1.

Schematics

For the following sections, each circuit block description begins under the schematic image for the respective block.

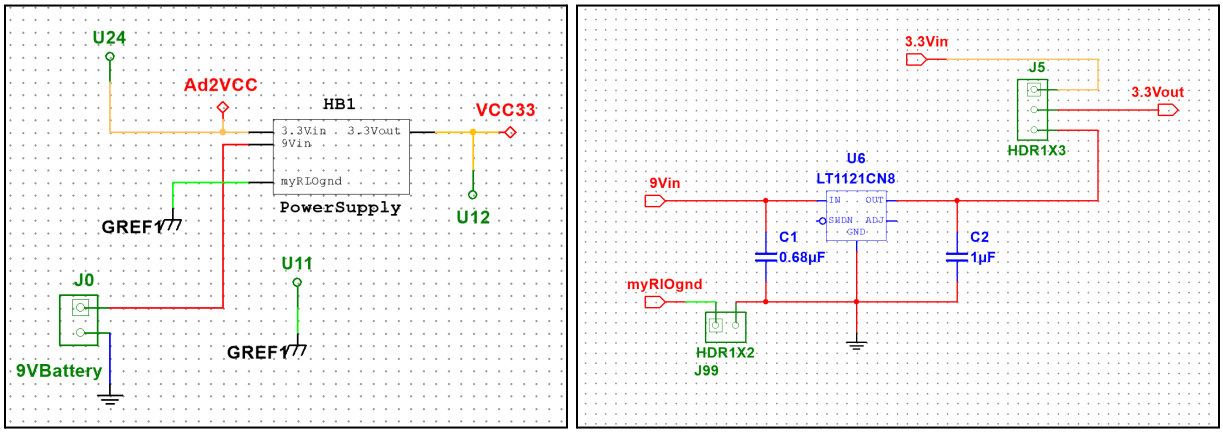

Fig 1. Power Supply Unit Schematic

The functionality of the power supply unit is to provide a 3.3V DC supply to the entire system. It can run by being powered either from the Analog-Discovery 2 (AD2) or from a 9V battery. The overall system works by taking in a 9V supply from the battery and running it through a voltage regulator, which steps down the voltage to 3.3V. C1 and C2 (seen above) act as bypass capacitors to ensure no AC signals get to the voltage regulator. Based on the datasheet for the LT1121CN8 voltage regulator, C2 was advised to be in the range of 0.68µF, whereas C1 was advised to be any value, as its purpose is to prevent oscillations. For this reason, 1µF was chosen. It is important to note that when a 9V battery is being used to power the system, J5 (seen in the right image above) must be shunted so that the output of the voltage regulator is directly connected to 3.3Vout. When the AD2 is being used to power the system, J5 must be shunted so that 3.3Vin is directly connected to 3.3Vout. The final part values are below.

$$C_1 = 0.68\mu F$$

$$C_2 = 1\mu F$$

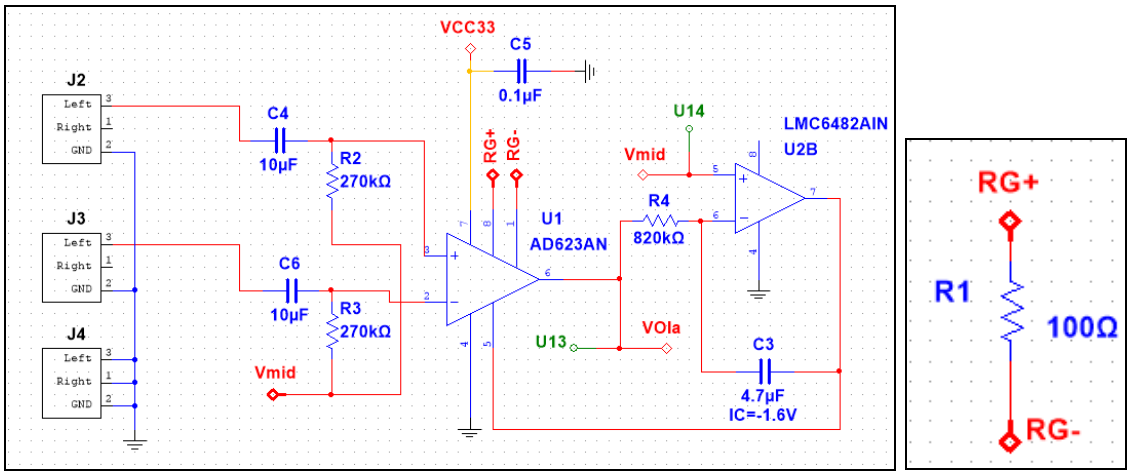

Fig 2. Instrumentation Amplifier (U1) and Integrator (U2B) Schematic

The next block of our EKG system is the instrumentation amplifier (in-amp, seen as U1 above) and integrator (U2B). The in-amp works by taking two inputs (seen as the nodes after C4 and C6, respectively) and provides an output that is a gained difference of the two inputs. In this way, it cancels out any signals common to the two signals. This is an incredibly important component in an EKG system, as the measurement that is being made is the electrical potential difference in one wrist versus the other (referenced to a third point, which for our case was the ankle, far away from other points). The electrical signals are very small, found to be going from -515µV to 583µV, which is why the gain resistor was chosen to be 100Ω (R1 above), as this results in a gain of 1000 from the in-amp. This means our signal has been multiplied to now have a peak-to-peak voltage of roughly 1V, meeting design specs. To ensure this value is within our power supply voltages, the integrator (U2B above) becomes crucial. When paired with the in-amp, the integrator's role is to center the in-amp output signal (VOIa above) around the integrator's positive terminal input, which in this case is Vmid. To this end, Vmid must be greater than 1V from 0V or 3.3V. If this is not the case, the output of the system will rail, meaning data will be lost.

The RC networks that take in each input (going into the in-amp) were calculated so that the corner frequency of the high pass filters occurred between 0.05Hz and 0.1Hz. It was also specified that the resistors of these networks had to be between 250k and 300kOhms, of which we only had access to one resistor value in between those (270kOhm, so it was just the choice of the capacitor to get our corner frequency at the correct location. The corner frequency was found by:

$$0.05Hz \leq \frac{1}{2\pi RC} \leq 0.1Hz$$

With the resistor value already set, it was easy to choose the capacitor to be 10μF. This led to our corner frequency to be at ~0.59Hz.

The integrator's values were found using the transfer function, which specified that R*C had to be between 1 and 10 (to satisfy the transfer function $H(s) = -\frac{1}{sRC}$). Our values were calculated to make the transfer function: $H(s) = -\frac{1}{3.854s}$, thus satisfying the design requirement. It can be noted that C5 is acting as a bypass capacitor, and for all of the other blocks in the circuit, 0.1μF was the selected value, as this provides sufficient aid for the signals we are dealing with.

C_3 = 4.7μF

C_4 = 10μF

C_5 = 0.1μF

C_6 = 10μF

R_1 = 100Ω

R_2 = 270kΩ

R_3 = 270kΩ

R_4 = 820kΩ

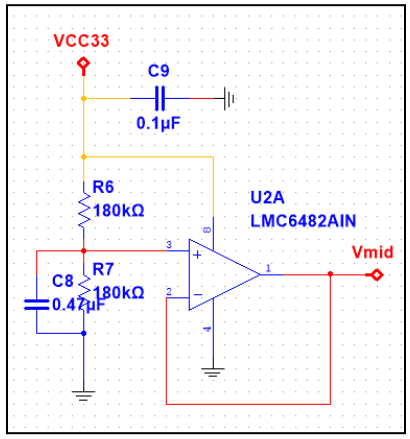

Fig 3. Vmid Design Schematic

The next block in our EKG system is designing Vmid, which determines where the output of our instrumentation amplifier (in-amp) is centered. This was designed so that Vmid was at half of the input voltage (as specified in the design requirements). This was chosen so that the output of our in-amp would not go over the max supply voltage (3.3V) or under the minimum (0V) for any op-amps. This was achieved by making R6 and R7 (as seen above) the same value. The voltage in between the resistors, which is the output of the op-amp can be found by using the following equation:

$$V_{mid} = V_{CC33}\left(\frac{R_7}{R_6+R_7}\right)$$

It can easily be seen that if the resistors are set to the same value, the output voltage of the circuit will be half of the input voltage. The resistor requirements were that the Thevenin equivalent voltage at the positive terminal had to be between 25k and 100kOhms. Not only this, but the corner frequency of the RC network had to be between 2Hz and 5Hz:

$$2Hz \leq \frac{1}{2\pi \cdot \frac{R_6 R_7}{R_6+R_7} \cdot C_8} \leq 5Hz$$

To satisfy this, the values in the image above were chosen, resulting in a corner frequency of 3.76Hz, which is within design specs. C9 is a bypass capacitor.

$C_8 = 0.47\mu F$

$C_9 = 0.1\mu F$

$R_6 = 180k\Omega$

$R_7 = 180k\Omega$

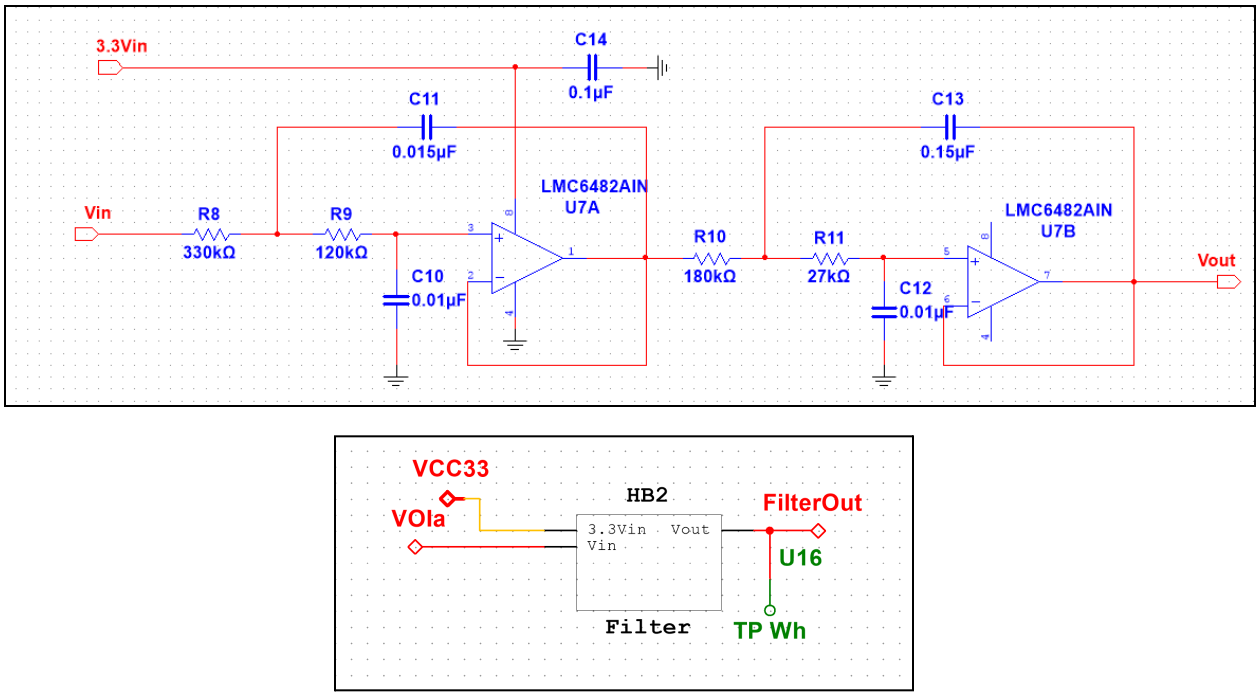

Fig 4a. Filter Design Schematic

The next section of our EKG circuit is the anti-aliasing filters. The filters take a power supply, previously set at 3.3V, and the output of the in-amp, as previously discussed. The criteria for designing the filter are as follows: a Butterworth filter with -72dB of attenuation at 500Hz. Texas Instruments provided a simplification that eased the value calculations and allowed the filters to have a gain of 1 in the passband, which meant that R8 (seen on the left filter) was a ratio to R9. The ratio is called m ($R_8 = mR_9$ *and* $R_{10} = mR_{11}$). The same went for the two capacitors, whose ratio is said to be n ($C_{11} = nC_{10}$ *and* $C_{13} = nC_{12}$). We can use these ratios to define our corner frequency and Q value:

$$f_c = \frac{1}{2\pi RC\sqrt{mn}}$$

Where R and C are R9 and C10 in the left filter and R11 and C12 in the right filter

$$Q = \frac{\sqrt{mn}}{m+1}$$

It should be noted that in order to make a 4th order Butterworth by cascading two-second order filters, the overall Q value should equal 0.707. The first filter should have a Q value of 0.5412 and the second filter should have a Q value of 1.3065. Cascaded, this will equal 0.707 (causing the corner frequency to be at -3dB from the passband). In order to calculate the correct

values, the corner frequency was first found by solving: $10^{\frac{-72}{80}} * 500Hz$ (to achieve at least -72dB at 500Hz). The transfer function for an individual 2nd order Sallen Key filter with a gain of 1 is as follows:

$$H(s) = \frac{1}{s^2(R_1R_2C_1C_2) + s(R_1C_1 + R_2C_1) + 1}$$

To get a 4th order filter response, the two transfer functions are multiplied. Combining the Q values, corner frequencies, transfer function, and a minimum resistance value of 10kOhms, a Python script was run using all of these requirements to calculate all values. Using the R and C values that we had access to, the first filter's Q value is 0.5427, the second filter's is 1.304, the first filter's corner frequency was 64.66Hz, and the second filter's is 58.95Hz. This meant that we were within a 5% tolerance once cascaded, which we interpreted as a design success. The component values of both filters are shown below with the python script on the next page:

$C_{10} = 0.01\mu F$

$C_{11} = 0.015\mu F$

$C_{12} = 0.01\mu F$

$C_{13} = 0.15\mu F$

$C_{14} = 0.1\mu F$

$R_8 = 330k\Omega$

$R_9 = 120k\Omega$

$R_{10} = 180k\Omega$

$R_{11} = 27k\Omega$

```python
import math

resistor_values_in_lab_kit = [10, 12, 15, 18, 22, 27, 33, 39, 47, 56, 68, 82,
100, 120, 150, 180, 220, 270, 330, 390, 470, 560, 680, 820,
1e3, 1.2e3, 1.5e3, 1.8e3, 2.2e3, 2.7e3, 3.3e3, 3.9e3, 4.7e3, 5.6e3, 6.8e3, 8.2e3,
10e3, 12e3, 15e3, 18e3, 22e3, 27e3, 33e3, 39e3, 47e3, 56e3, 68e3, 82e3,
100e3, 120e3, 150e3, 180e3, 220e3, 270e3, 330e3, 390e3, 470e3, 560e3, 680e3, 820e3, 1e6]

capacitor_values_in_lab_kit = [0.01e-6, 0.1e-6, 0.47e-6, 1e-6, 4.7e-6, 10e-6, 100e-6]

tolerance = 0
tolerance2 = 0
tolerance3 = 0
pi = 3.141592  # Corrected the value of pi
Q1 = 0.5412
Q2 = 1.3065
f = 1975j
h = -60

for R2 in resistor_values_in_lab_kit:
    for R3 in resistor_values_in_lab_kit:
        for C2 in capacitor_values_in_lab_kit:
            for C3 in capacitor_values_in_lab_kit:
                q = math.sqrt((R2 * C2) / (R3 * C3)) / ((R2/R3) + 1)
                if 0.50 < q < 0.55:
                    corn1 = 1 / (2 * math.pi * R3 * C3 * math.sqrt((R2 / R3) * (C2 / C3)))
                    if 0 < abs(corn1 - 351.3) < 10:
                        for R6 in resistor_values_in_lab_kit:
                            for R14 in resistor_values_in_lab_kit:
                                for C5 in capacitor_values_in_lab_kit:
                                    for C4 in capacitor_values_in_lab_kit:
                                        q2 = math.sqrt((R6 / R14) * (C4 / C5)) / ((R6 / R14) + 1)
                                        if 1.2 < q2 < 1.4:
                                            corn2 = 1 / (2 * math.pi * R14 * C5 * math.sqrt((R6 / R14)
* (C4 / C5)))

                                            if 0 < abs(corn2 - 351.3) < 10:


                                                trans = abs((1 / (  (f * 2*math.pi)**2 * (R2*R3*C2*C3)
+ (f*2*math.pi)*(R2*C3 + R3*C3) + 1  )) * (1 / ( (f * 2*math.pi)**2 * (R6*R14*C5*C4) + (f*2*math.pi)*
(R6*C5 + R14*C5) + 1 )))
                                                mag = 20*math.log10(trans)
                                                if -60 > mag > -62:
                                                    print(mag)
                                                    print("Q1: ", q)
                                                    print("Q2: ", q2)
                                                    print("R2: ", R2)
                                                    print("R3: ", R3)
                                                    print("C2: ", C2)
                                                    print("C3: ", C3)
                                                    print("R6: ", R6)
                                                    print("R14: ", R14)
                                                    print("C5: ", C5)
                                                    print("C4: ", C4)
                                                    print("corner1: ", corn1)
                                                    print("corner2: ", corn2)
                                                    print()
```

Fig 4b. Filter Python Script

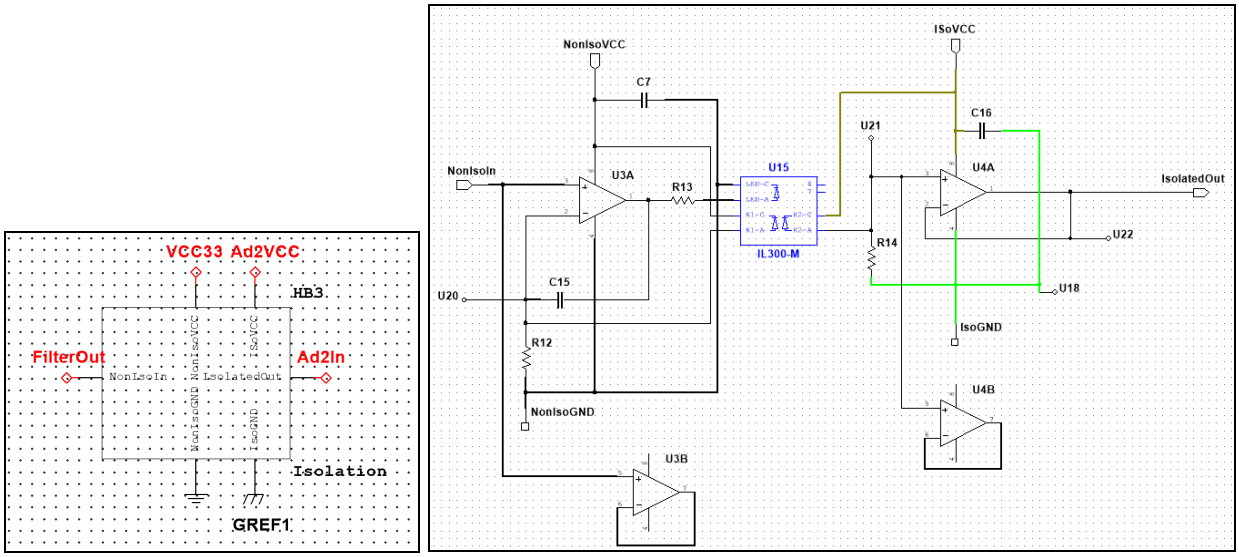

Fig 5. Isolator Schematic

The last section in the EKG design is the isolator. The purpose of the isolator is to physically separate one circuit from another while transferring electrical signals between them. It runs on one LED whose intensity is dependent on the current running through it. This light signal is picked up by a photodiode, which transfers the electrical signal to the other part of the circuit. Our isolator's input is the output of the filter, whose information is transferred to the output of the EKG as a whole. For this to work effectively, it must have two separate power sources: one that is not isolated, VCC33 from the battery, and one that has been isolated, 3.3V from the AD2. The gain of the isolator is ideally 1 in order to accurately transfer the electrical signal from one system to the other (ideally with no losses). It should be noted that the maximum output current from the op-amp feeding the isolator is 30mA. Using equations found in the isolator's data sheet:

$$Gain = K_3 \cdot \frac{R_2}{R_1}$$

$$K_1 = \frac{I_{P_1}}{I_f}$$

In order to choose the isolator design specs, we were first informed that it fell under the I Transfer Gain Bin for K3, meaning that our K3 has to be between 1.297 and 1.456. Using equations for K3 and K1 from the datasheet:

$$R_{12} = \frac{1.89V}{K_1 \cdot (30mA)}$$

$$1 = K_3 \cdot \frac{R_{14}}{R_{12}}$$

Resulting in values of 47kOhm and 33kOhm for R12 and R14 (above) respectively for a K3 value of 1.4242 and a K1 value of 0.0065. Using a 20mA current to be within spec (and not near the max current) for the LED, R13 could be calculated using a 0.5V voltage across it:

$$0.5V = (20mA)(R_{13})$$

Ideally, R_{13} would be 25Ω, however, we did not have access to this resistor. Instead, we had to use 27Ω, which slightly reduced the current through the diode but still kept it within spec. The capacitors were followed as required from the IL300 data sheet, as R12 was greater than 10kOhms.

$C_7 = 0.1\mu F$

$C_{15} = 680pF$

$C_{16} = 0.1\mu F$

$R_{12} = 47k\Omega$

$R_{13} = 27\Omega$

$R_{14} = 33k\Omega$

Multisim Simulations

Testing in Multisim, the EKG example data was used to ensure that all components were functioning correctly. Each component of the circuit was tested in the time domain, and frequency domain simulations were done as necessary.

First, the power supplies were set to 3.3V. The first test was at Vmid to ensure the overall output of the circuit would be centered at the correct location:

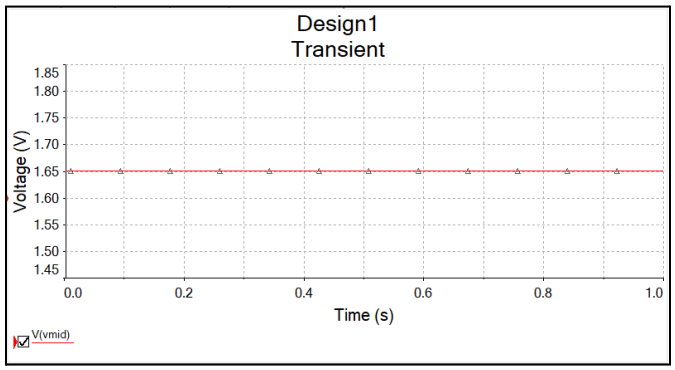

Fig 6. Vmid Simulation Output

The above image shows the output at Vmid and how it is centered at 1.65V. This proves that our circuit, having a peak-to-peak output from the in-amp at roughly 1V will be centered in our power supply voltages well and will not rail. The RC network in the Vmid configuration had to have a corner frequency between 2 and 5Hz. This was then simulated in Multisim:

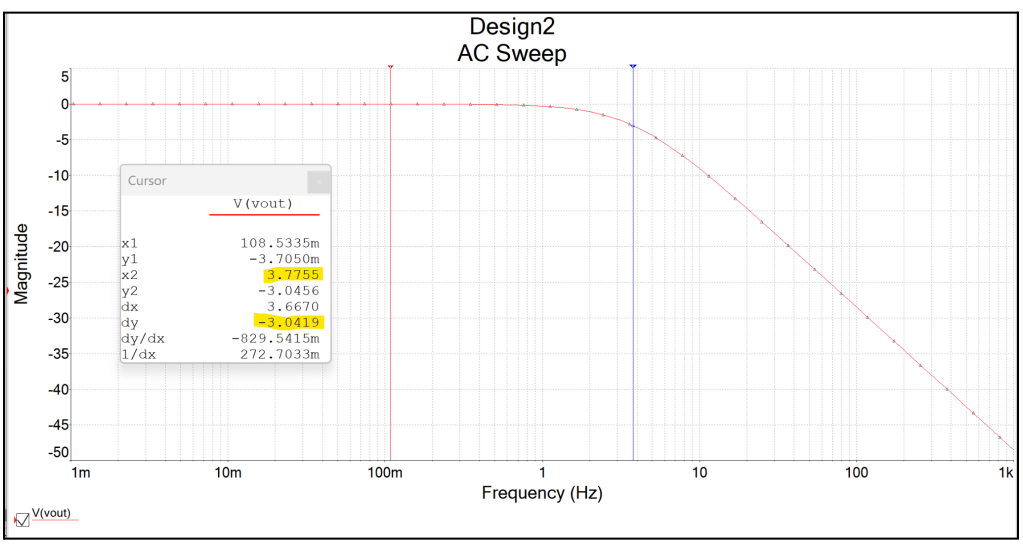

Fig 7. Vmid RC Network Frequency Response Simulation

The above image proves that the RC network fulfills design requirements, as the corner frequency is at 3.76Hz, just as analytically calculated. The next frequency domain simulation was run on the input RC network that feeds the in-amp:

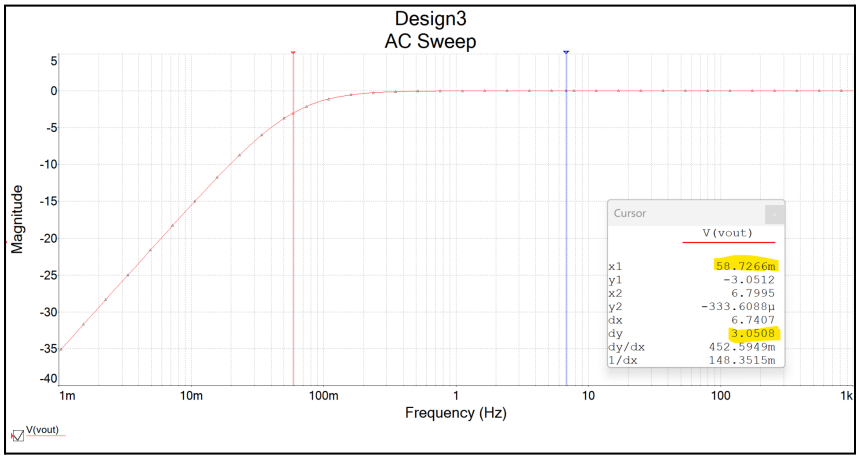

Fig 8. In-Amp RC Network Frequency Response Simulation

The image shows that our input RC networks meet the design criteria and the corner frequency is within the .05 and .1Hz requirements. The second RC network is identical, with the same output below:

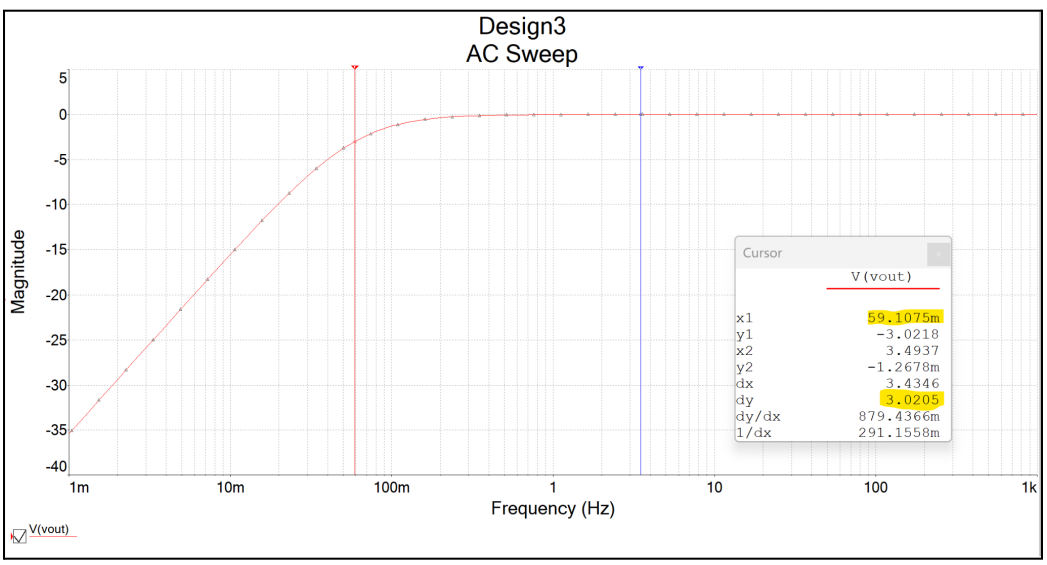

Fig 9. In-Amp Second RC Network

This proves that the RC network was configured correctly to design specs. The next simulation was run on the output of the instrumentation amplifier using the same example EKG data. It showed:

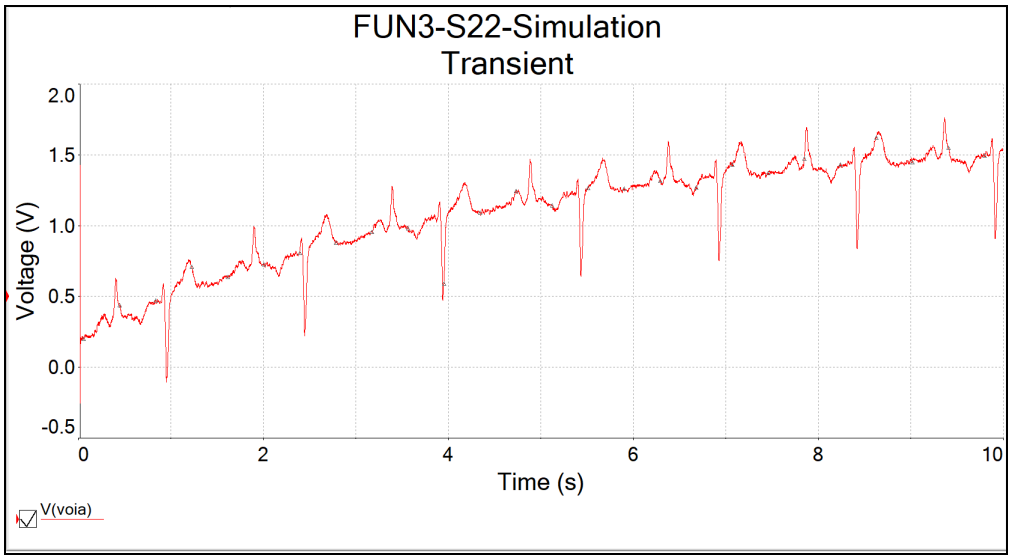

Fig 10. Example EKG Data In-Amp Output

The above image shows the output of the in-amp starting from T=0s. As you can see, the overall signal is going towards the Vmid, which is 1.65V. Below is further proof that this is happening.

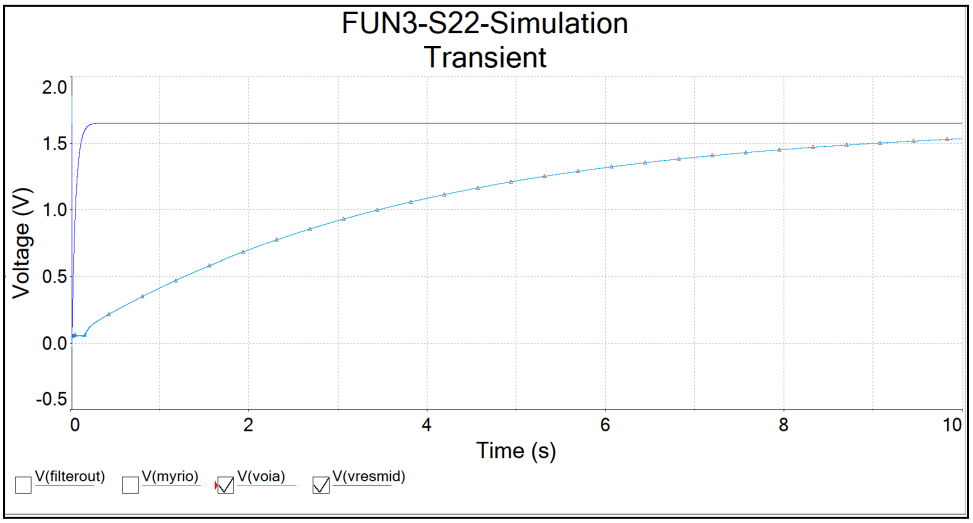

Fig 11. Identical Sinusoid In-Amp Inputs

This simulation result was acquired from sending in two identical sinusoids to the in-amp. The in-amp cancels out the same signals (which in this case is all of each signal) and centers it around Vmid. Voia, the curved line approaching Vmid, is the output of the in-amp. As you can see, the signal will follow this curve and will approach Vmid at 1.65V. This proves that our in-amp is working correctly as well as our integrator and Vmid are centering the signal

correctly. The next test run was a frequency response on the filters to ensure that they were built correctly and that their purpose in anti-aliasing would be successful:

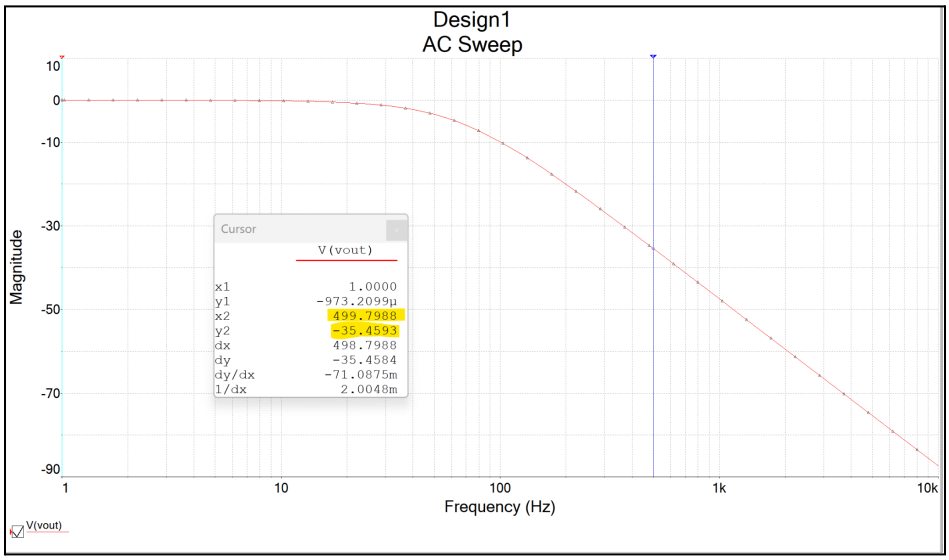

Fig 12. First Filter Frequency Response

The above image is the frequency response of just the first filter (lower Q value of 0.5427). As you can see, the filter begins its curve down earlier and does not have any peaking in the frequency domain. It achieves -35dB of attenuation at 500Hz, which is promising for the cascading of two filters to complete design requirements.

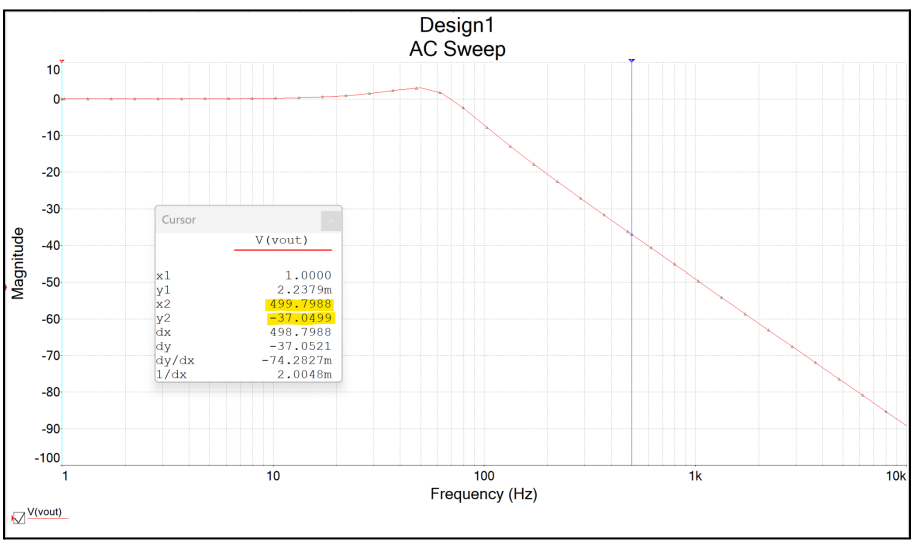

Fig 13. Second Filter Frequency Response

The above output is from the second filter (the higher Q value of 1.304). As you can see, it represents this well, as it has peaked in the frequency domain from such a high Q value. This

filter has -37dB of attenuation at 500Hz, which should cascade well with the first to achieve -72dB.

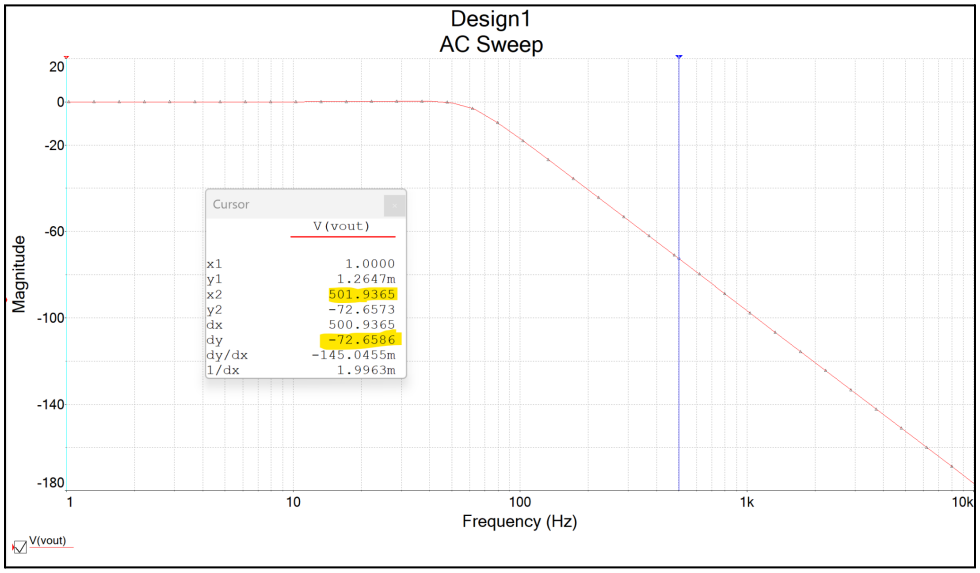

Fig 14. Cascaded Filter Frequency Response

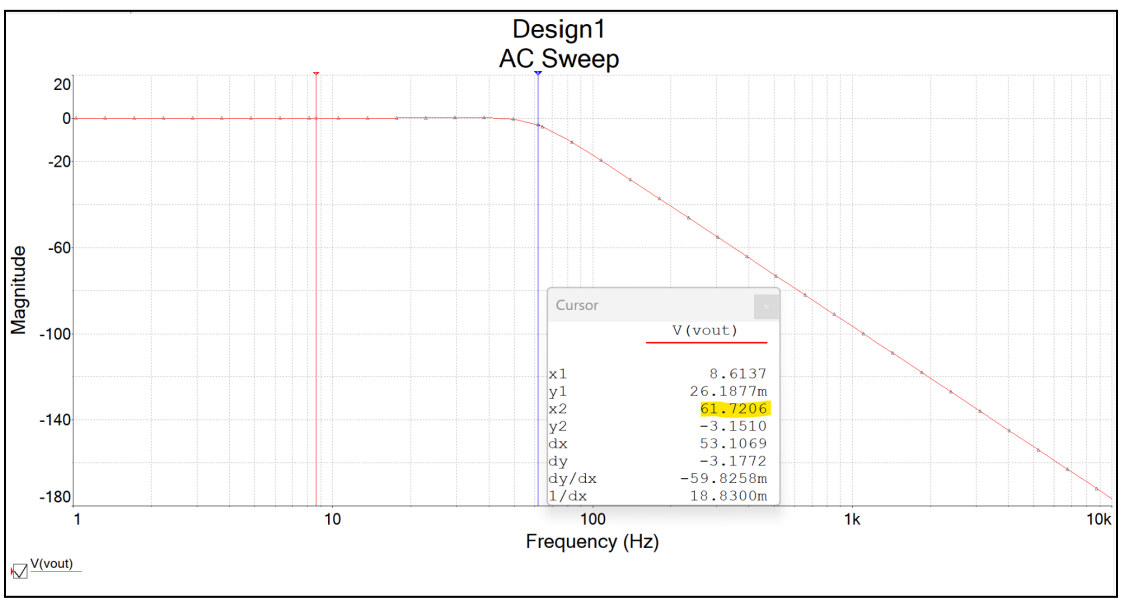

Fig 15. Cascaded Filter Corner Frequency

The above images show the overall filter frequency response. As you can see, it completes the required -72dB of attenuation at 500Hz and has a corner frequency of ~62dB, matching our analytical calculations. This will prove to be effective in anti-aliasing, as the purpose of this filter is to remove aliasing artifacts when going to the ADC.

The time domain output of our filters was simulated to be as follows:

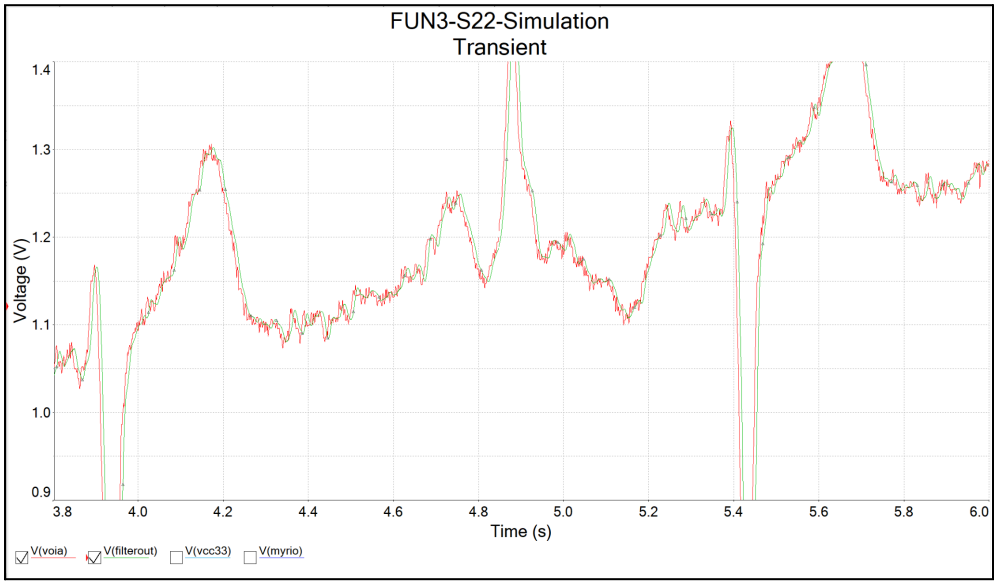

Fig 16. Time Domain Output of Filter Network

In the above image, the green is the output of the filter and the red is the output of the in-amp. The purpose of the filter is anti-aliasing, but here shows the effects it has on the actual data. High frequencies above our corner frequency are heavily attenuated, so a slightly smoother version of the input is what is seen at the output. Other than this, unity gain should be achieved. The output of the filters in the time domain at full scale is as follows:

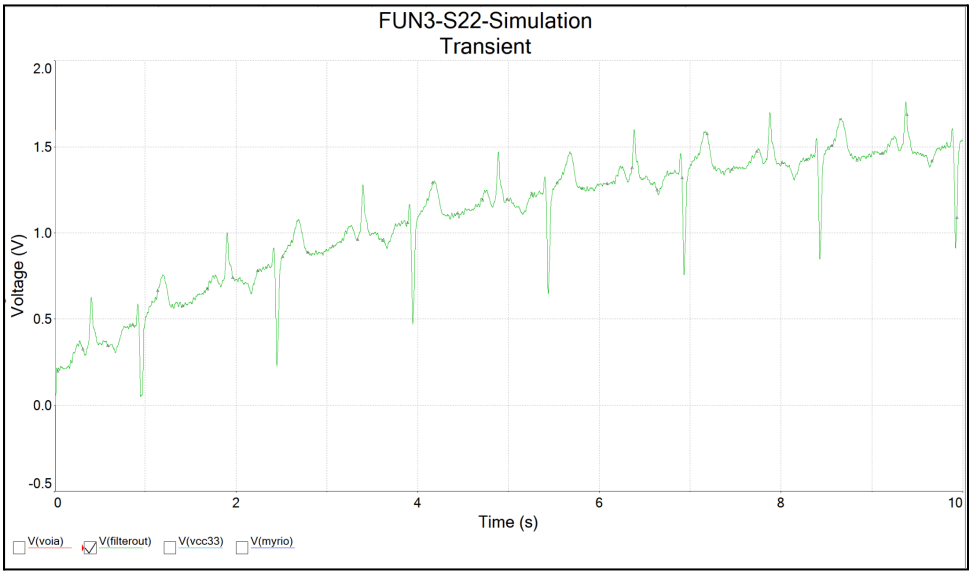

Fig 17. Time Domain Output

As for the isolator, the important quality is that the gain should be equal to 1. Running the output of the filters as input to the isolator:

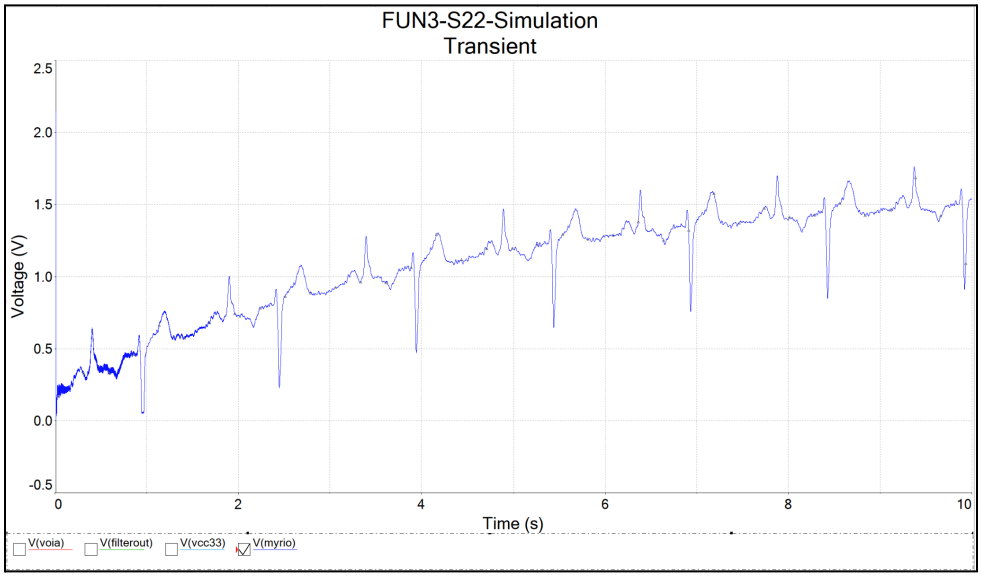

Fig 18. Isolator Output

This proves that the isolator is operating with a gain of 1, as this is identical to the output of our filters. Now, we have verified that our values meet all design specifications and at this point are ready for board assembly.

Layout

The silkscreen layer of our final EKG board with reference designators moved inside the component for easier understanding is as below:

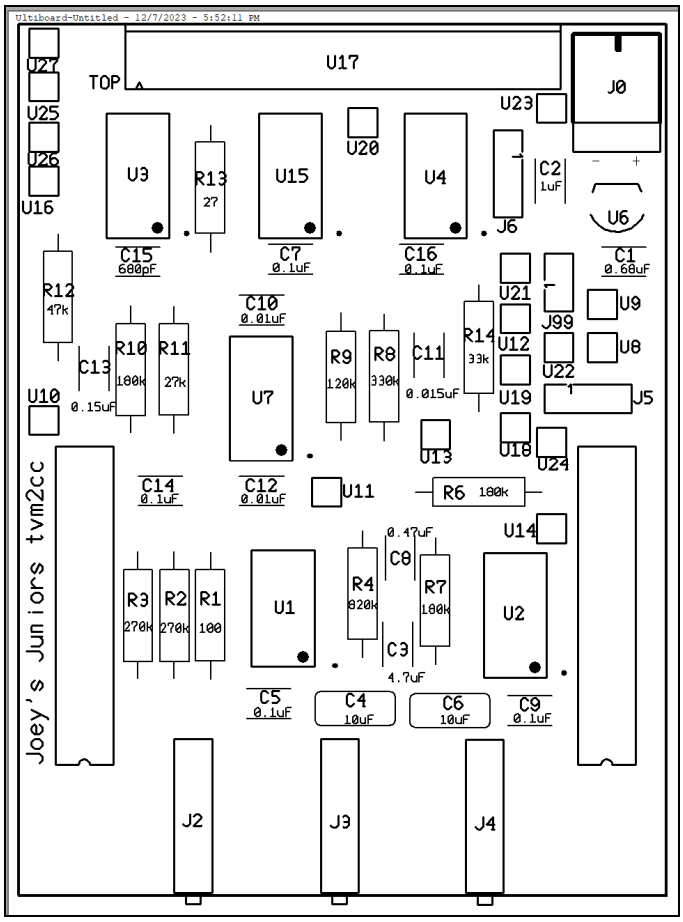

Fig 19. Ultiboard Silkscreen Design Layout

This image shows some of the design strategies. Bypass capacitors were all placed near their respective chips, and the overall flow of the designed circuit was kept. This means that starting with the input jacks (J2, J3, and J4 at the bottom), the next nearest thing is the in-amp (U1) and related components. Next to this is U2, which functions as Vmid control and the integrator, both of which are crucial to U1's operation. After this is U7 (in the middle of the board), which is the filter. This is fed by the in-amp and goes to the isolator, which is U15. The isolator has two chips that help its control, which are U3 and U4. As you can see above, this flow is kept on the board to ensure that traces are kept at a reasonable length. All related components (resistors and capacitors) are near the chips that they work with as well to ensure that the overall design is kept as simple as possible. The placement of power (U6 and J0) was not as important,

as it was going to be fed everywhere. Because of this, it was placed in the most convenient spot to not interfere with space constraints.

The board's copper layers are printed as below:

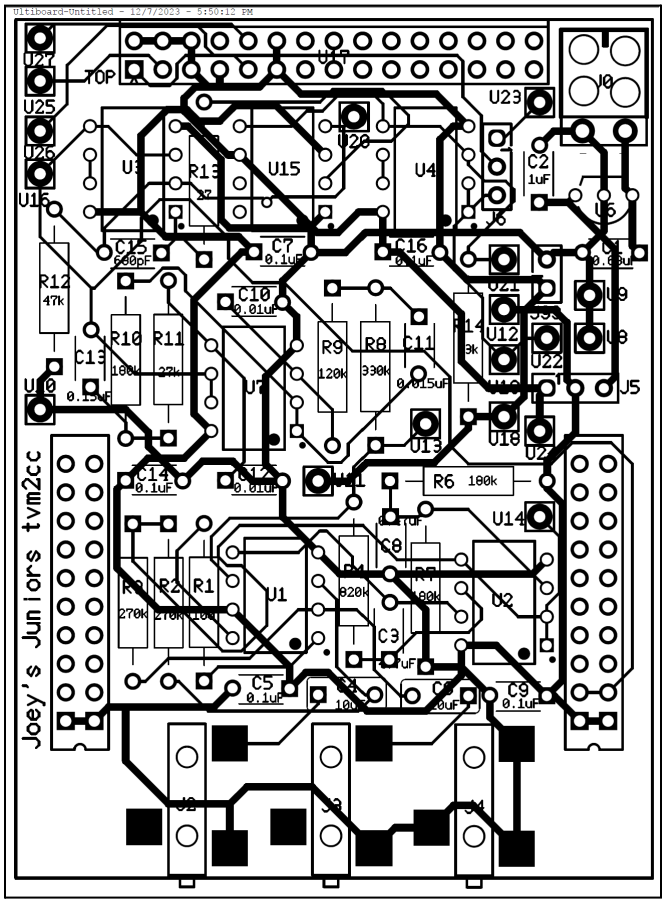

Fig 20. Ultiboard Copper Layers

As you can see from the copper layers, the power (thickest lines) was prioritized in the routing process. This ensured that there were no extra issues from interference or the power channels acting as an antenna (picking up extra noise) while the circuit was running. After this, the routing became very easy, as components were all placed near each other on the board.

The CAM file generation was the next step in the manufacturing process. A DRC and netlist as well as a connectivity check was run on Ultiboard to ensure there were no issues with connectivity or routing placement. The Ultiboard file was exported as a Gerber file and was run through a "Cam File Renamer" software to further personalize our design files. These newly renamed files were sent to "Freedfm.com," and with some small specification instructions from our instructor, the design board was sent off to be checked for any design problems. The report

came back clean the first time, and we were ready to move on with our design project. The only issue we ran into was an incorrect file name, which we changed and tested again, coming through with no showstoppers again. We were then ready to send the board design to WWW for manufacturing.

Section 2

Assembly and Testing

When testing our board after assembly, it was very important to test each “block” (as outlined in Schematics) independently of each other to ensure each piece was functioning correctly. Before this, connectivity checks were done with a multimeter at each node of the circuit to ensure all pieces were installed correctly. No problems were found. We were not given a battery to start, so we provided power to the board ourselves by supplying a 3.3V DC supply from the AD2, which was connected to U12 (VCC33) and U24 (AD2VCC). This ensured that all chips of the circuit were receiving the correct voltage before we could test our power supply (as we didn’t have a battery yet). The first component to be tested was Voltage Mid.

The purpose of Vmid testing was to ensure that the correct DC input was being sent to the non-inverting input of the integrating amplifier, which essentially centers our in-amp output around this voltage to stay in range. In our case, it was expected to be 1.65V, as this is half of the input voltage. This was tested at test point U14.

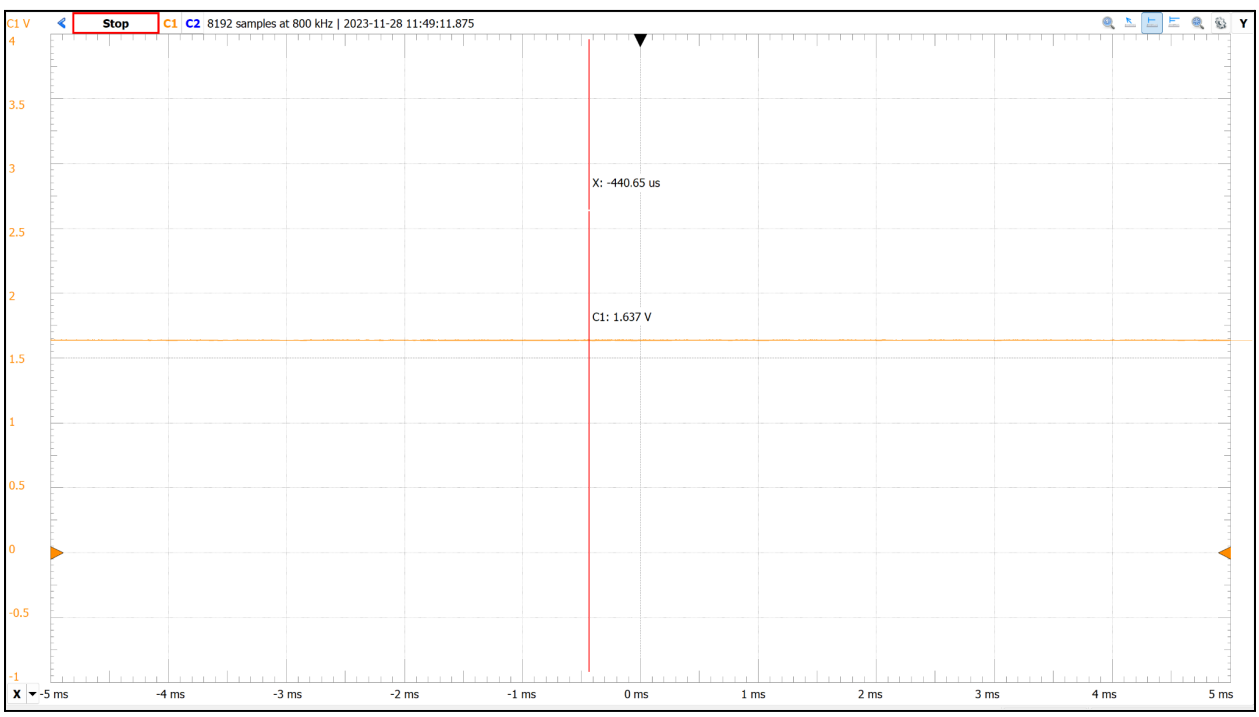

Fig 21. Vmid Output

As you can see from this image, Vmid was recorded at 1.637V, which is well within a 5% tolerance. This difference is most likely due to the resistor values not exactly matching. Regardless, this will work well for our EKG system.

Now that Vmid has been verified, the Instrumentation Amplifier and Integrator were checked, as they were next in the circuit. When testing U1, the first step was to clip the gain resistor (R1). This instrumentation amplifier model has a gain of 1 when the gain resistance goes to infinity. We tested this part of the circuit with R1 clipped. For testing, two 0.5V amplitude sinusoids were input at J2 and J3 180 degrees out of phase. The expected output was a 1V amplitude sinusoid centered around the integrator and Vmid (1.65V, checked by testing U14). Because of part tolerances, an output of 0.9-1.1V (~2V peak-to-peak) centered at 1.65V was expected. The input test is below:

Fig 22. Out of Phase Sinusoid In-Amp Inputs

And the output is seen at:

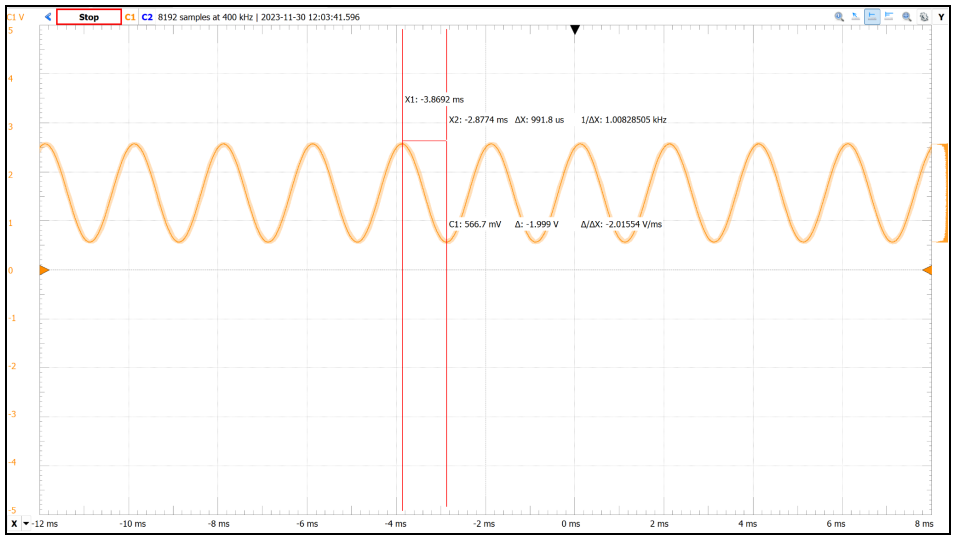

Fig 23. In-Amp Output

We ended up seeing a near-perfect amplification of the difference in frequencies. Instead of a peak-to-peak of 2V, we saw 1.999V, well within tolerance. The output was centered at 1.65V, proving that our integrator was functioning correctly. This pretty much perfectly matched our Multisim tests (seeing the correct gain). R1 was then soldered back on and then we were on our way. The next step in the EKG circuit was validating the anti-aliasing filters.

When testing the filters, U16 was tested with a signal source at U13, verifying that both filters cascaded met the requirements. At this point, we had verified that our Op-Amps were operating within range (it was expected not to rail). We had to add a 1.65V DC offset into the input of our filter, as we saw it railing initially (the input was a sinusoid that was not within 0-3.3V, causing it to rail). The output of the overall filter is below:

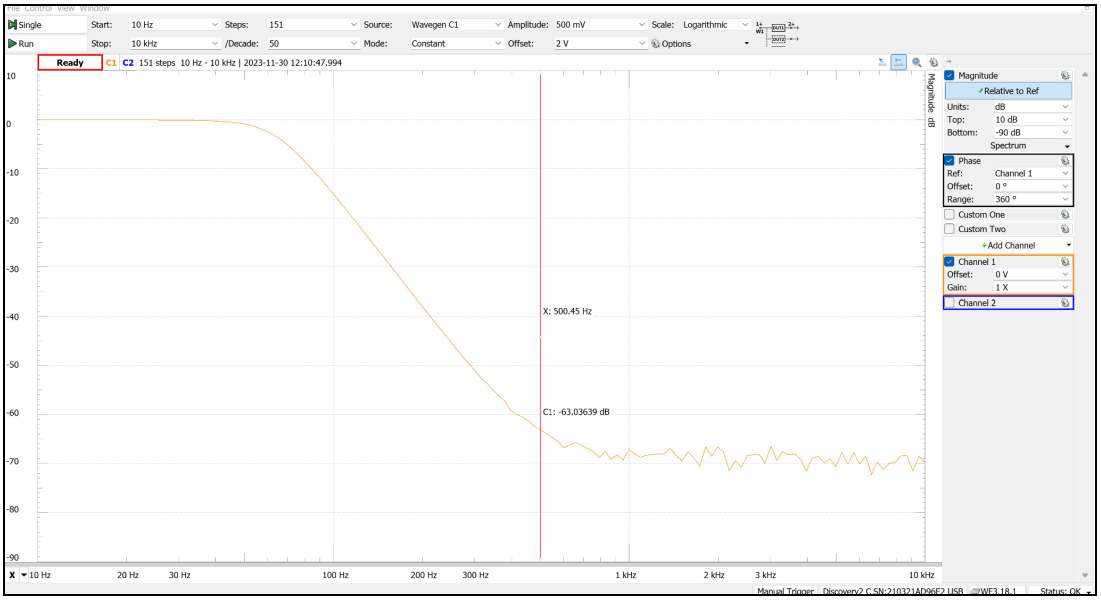

Fig 24. 4th Order Butterworth Filter Frequency Response

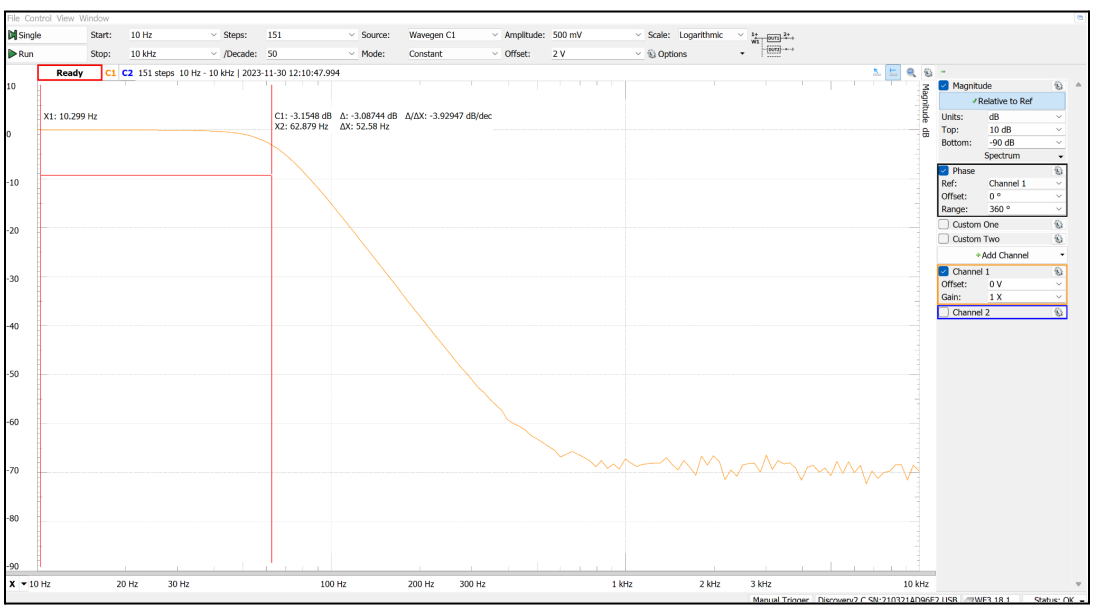

Fig 25. 4th Order Butterworth Filter Corner Frequency

Overall, it can be seen that the filters approach the design criteria of -72dB of attenuation at 500Hz. The best we saw was -62dB, but after discussing with our instructors, it was concluded that the in-amp models used did not handle that low of gain well, and this was verified as a completion of the design requirements. It would have been nice to see the full attenuation, however, the component quality did not help in this. At this point, the circuit all the way through the filters had been verified to meet design specs, so all that was left was the isolator.

The isolator's input was tested at U16 and the output at U19 (at J6). The isolator as a circuit was tested by sending a small input waveform (within the bounds of NonIsoVCC, ISoVCC, and ground) into U16 and recording the output at U19. The isolator was expected (ideally) to have unity gain, however, a tolerance of around 0.9-1.1 gain was expected from component tolerances. After this, the isolator was tested in series with the rest of the circuit with the sample input. When testing with the entire circuit with the example EKG data, the input to the isolator (in the time domain) was found to be as follows:

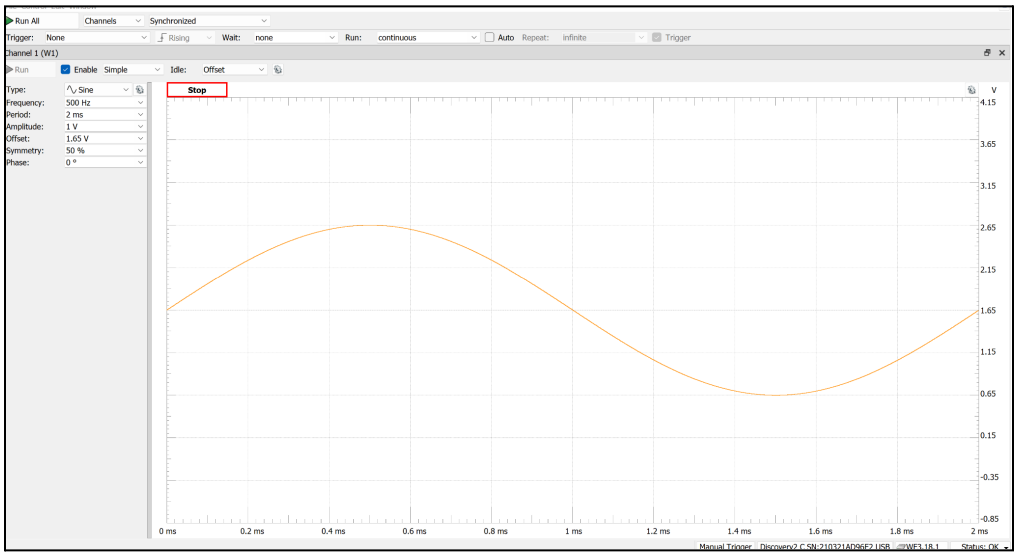

Fig 26. Isolator Input of 1V Amplitude Sinusoid

With an output of:

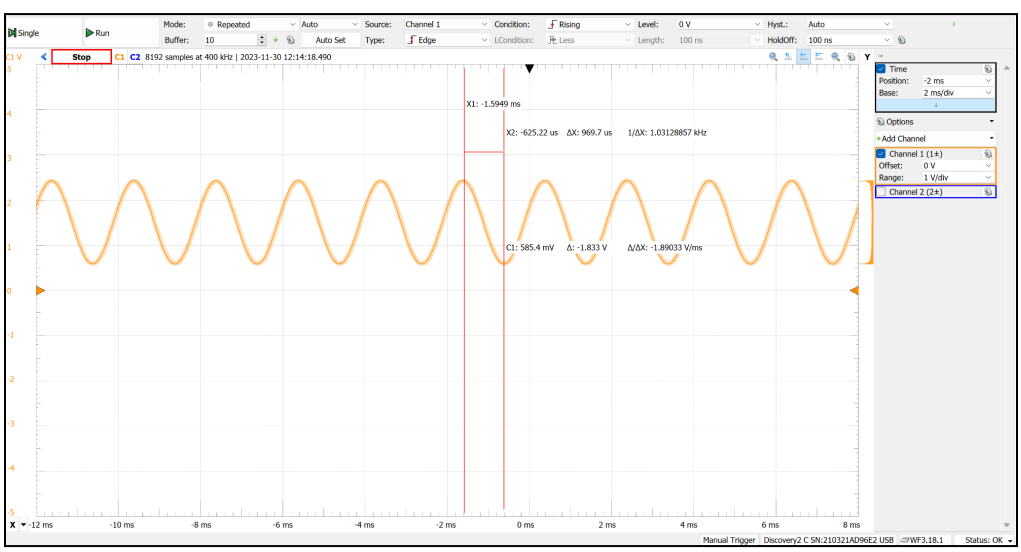

Fig 27. Isolator Output Showing Gain of 0.9165

This output shows a peak-to-peak of 1.833V, meaning an amplitude of 0.9165V. This was within our 10% expected error. It would have been nice to see a gain of closer to 1 (instead of 0.9165), however, the found gain will suffice for the purpose of our project. It is possible that certain component choices due to limited selection caused this. After all of this was verified, we were ready to send in a voltage at the input and record an overall output. To do this, the example EKG data given to us in Multisim was converted to a CSV, which was then sent as an input to the J2 input. J1 was set to ground to ensure that that signal (which looked like a heartbeat at this point, no in-amp operation was needed now) would go straight through the in-amp to the filters. The input looked like this:

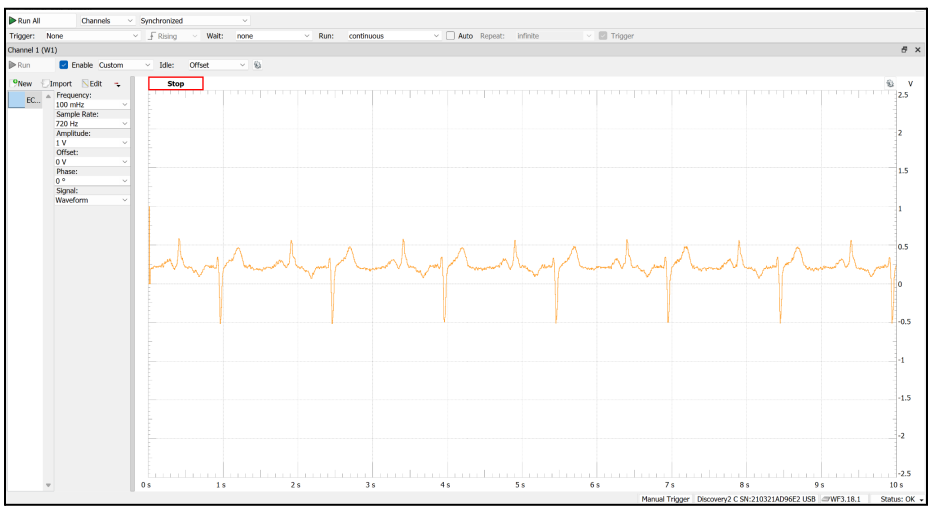

Fig 28. Example EKG Data Input to In-Amp

Which resulted in an output after the isolator of:

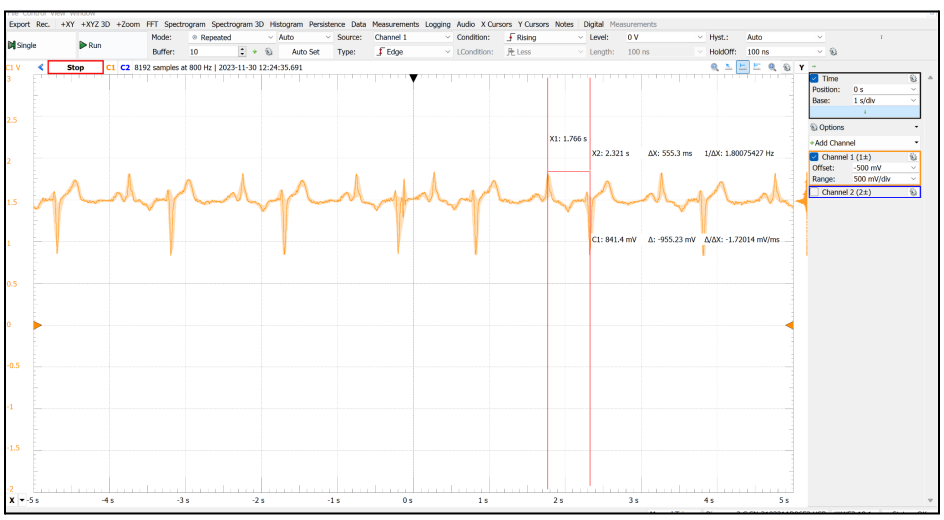

Fig 29. Total EKG Output From Example Input

The peak-to-peak measured in at 955.23mV, which was extremely close to the 1V desired peak-to-peak. We attributed this difference to the isolator's lower-than-desired gain. J1 and J2 were flipped, to which we expected the same result but upside-down. The following output was recorded:

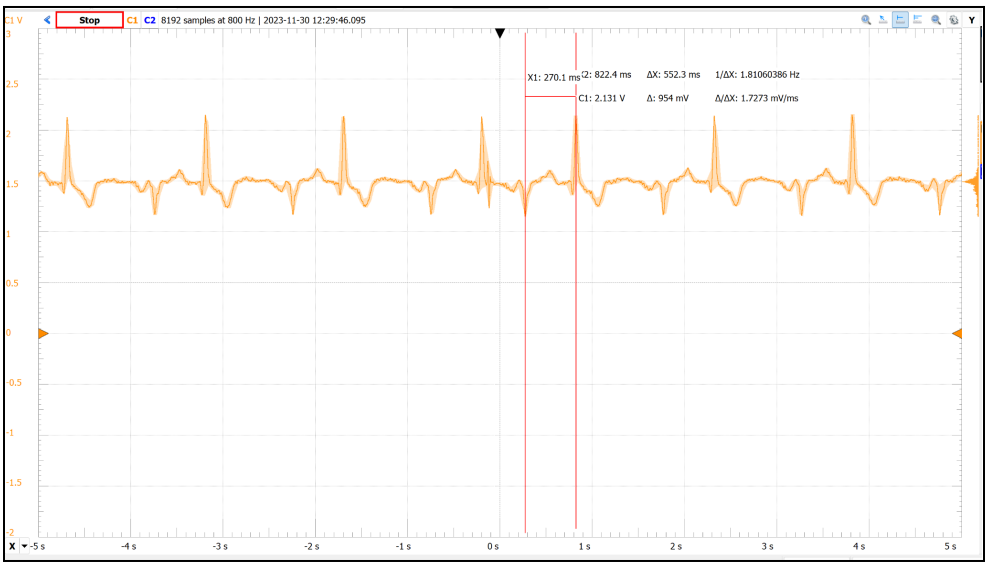

Fig 30. Flipped Input to In-Amp Using Example EKG Data

This exactly matched what we wanted to get, as all that we did was switch which references the in-amp took. Our output compared to our input:

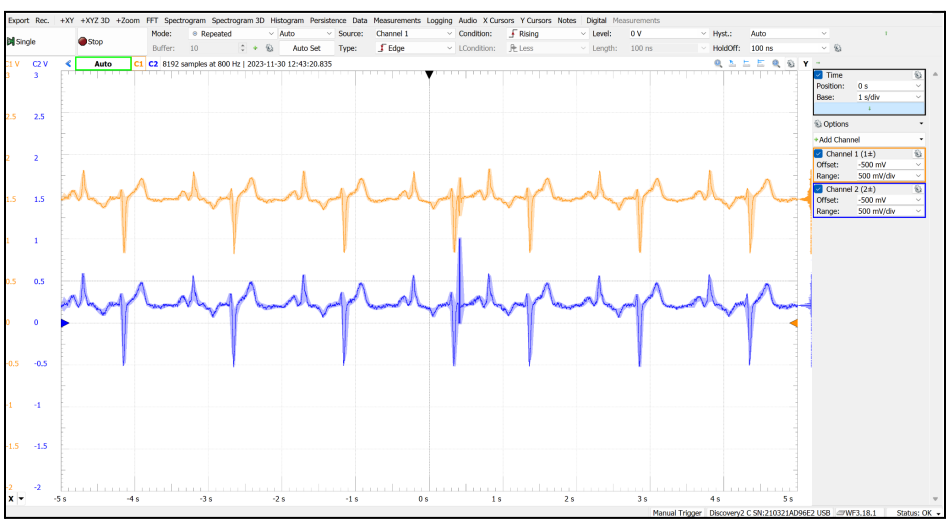

Fig 31. Example EKG Data Input (Blue) vs Output (Orange)

This output (Orange) makes sense, as it is now roughly centered around 1.65V. The actual value was found to be much lower than 1.65V, which was again related to the low gain from the isolator. Because of this, this differed from our Multisim expected value that looked like:

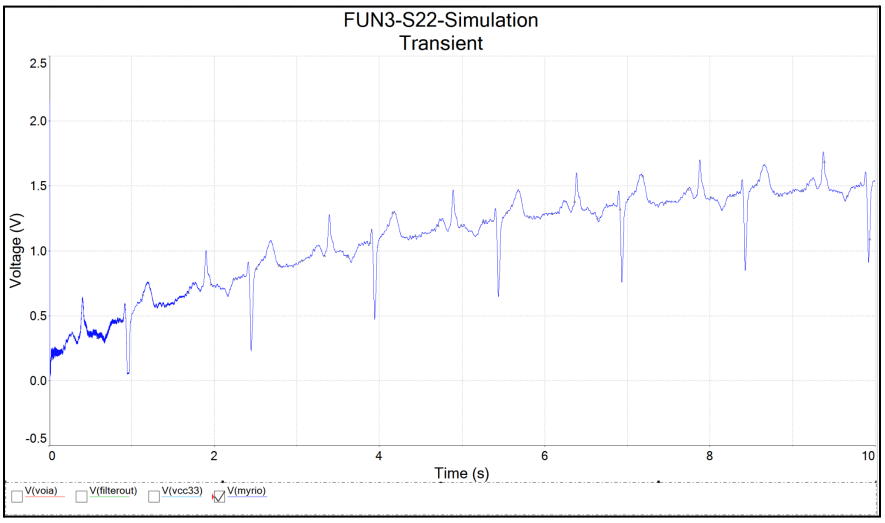

Fig 32. Multisim Expected Output

The Multisim value has a peak-to-peak of right at 1V and is perfectly centered around 1.65V. Our real output had less gain and because of this was centered lower.

Now that we had successfully passed a signal through the entire circuit, it was time to check our power supply so that it could run on battery power. Testing the power supply initially consisted of having a supply voltage check. The jumper at J99 was disconnected, as we now had to separate the isolated ground, and the bottom two pins of J5 were connected to ensure the output of the voltage regulator was feeding the circuit. This went extremely well and a multimeter measured 3.29V at the output of the voltage regulator as well as the VCC pin of all chips. This verified that we were ready to test with leads. One electrode was on each of the test subject's wrist (which were connected to J2 and J3 respectively), with a third connected far away on the subject's ankle. J6 was also jumpered to ensure that the output of the EKG could be read by the AD2. The experimental setup here is below in the next section of the document.

Images

As previously stated, when testing our board (as seen below), our 3.3V inputs were set by the AD2 and connected to U24 and U12, both 3.3V inputs. The grounds from the AD2 were connected to U11 and U10. This resulted in all of the above images of each step in our testing process.

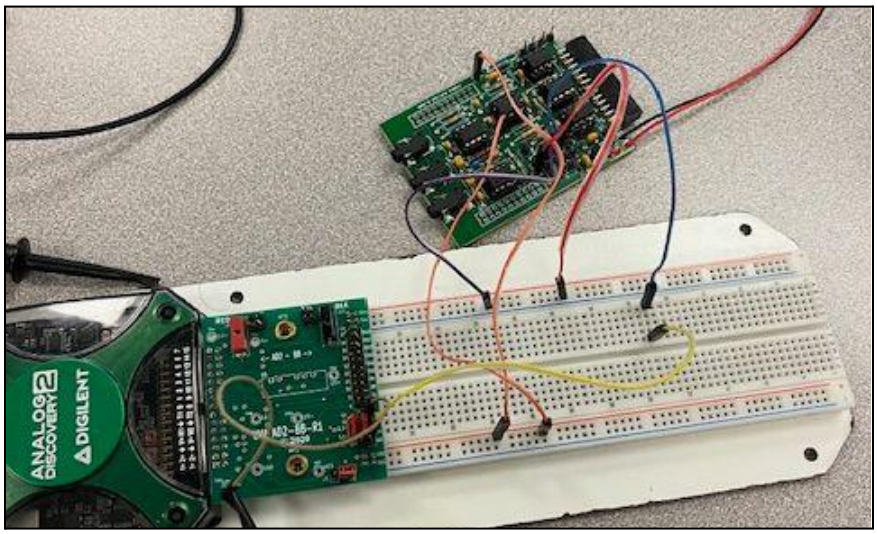

Fig 33. Experimental Setup Before Battery Power Supply

When taking the EKG of a test subject, leads were set on either of the subject's wrists and connected to J2 and J3, with a third lead connected to the subject's ankle to provide a ground reference that was far away from the other leads. Connection to the subject looked like this:

Fig 34. Leads on Test Subject

These were connected (left to right above) to J4, J3, and J2. Our board during testing is shown below:

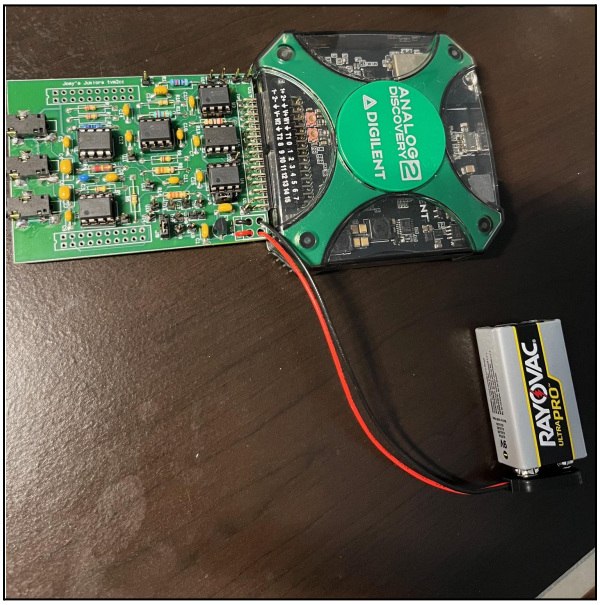

Fig 35. EKG Circuit Powered by Battery for Testing

J5 and J6 were jumpered in order to power the EKG by battery as well as reading the output from the AD2. Leads connecting to the test subject's wrists were connected to the top input pins (J2 and J3) and the ankle's lead (ground) was connected to the bottom input pin, J4. The battery was connected and the AD2 was wired from a USB cable. Our board (front and back) after manufacturing is below:

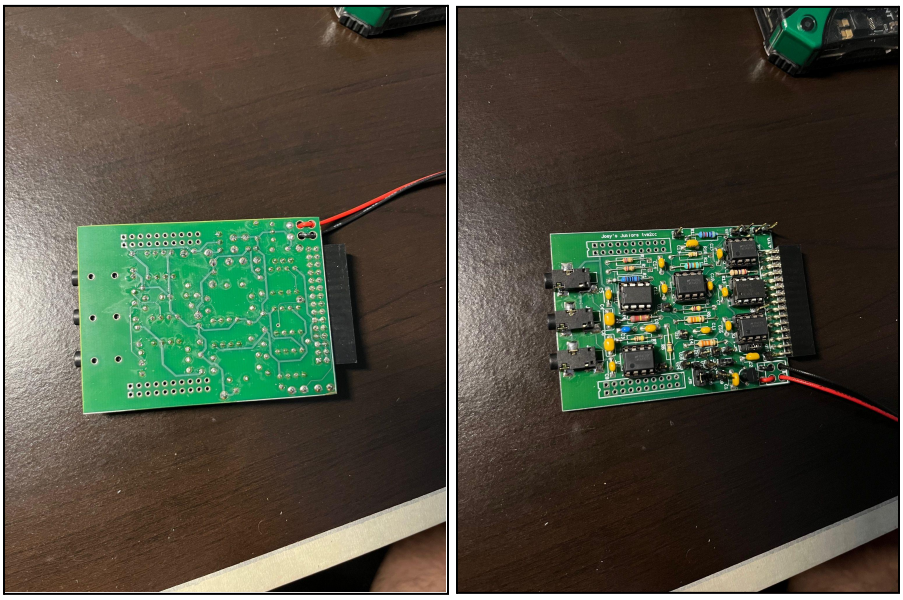

Fig 36. Front and Back of Manufactured EKG Board

The board looked great, and after putting on all chips, the continuity tests proved that it was manufactured correctly. Once our tests were run and we were able to attempt to take the EKG of a test subject, we attached the leads and applied the oscilloscope feature on Waveforms:

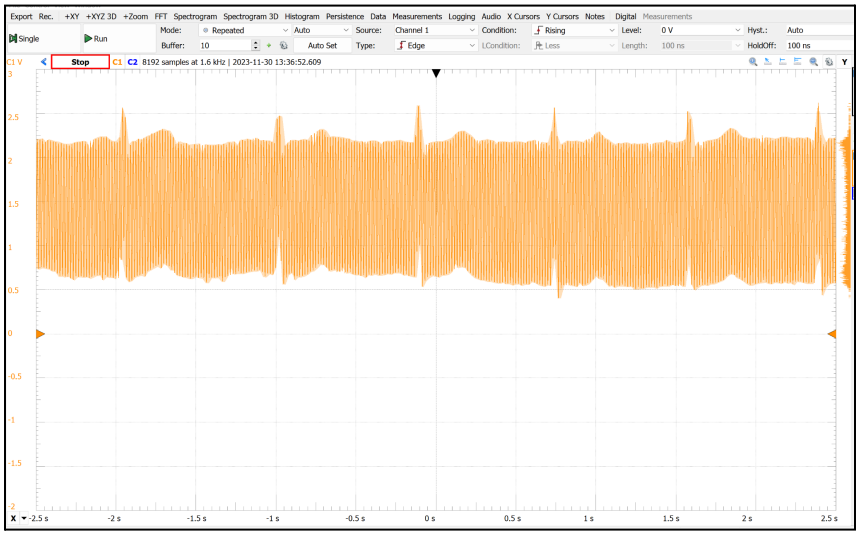

Fig 37. Test Subject EKG Experimental Output

At first, we thought this was bad data, as it just looked like extreme noise. However, with further inspection, our group noted that there were spikes at roughly once a second, matching a near 60 bpm heart rate, which is very normal for a human being at rest. This made us believe that we were on the right track, and once we realized that everything in between was 60-cycle interference caused by power lines and other electrical signals in the room operating at 60Hz, we understood that we could run the output data through an FIR filter to eliminate the 60Hz noise and its harmonics from power lines in the room. This is done below, in the next section of the document.

Data Capture

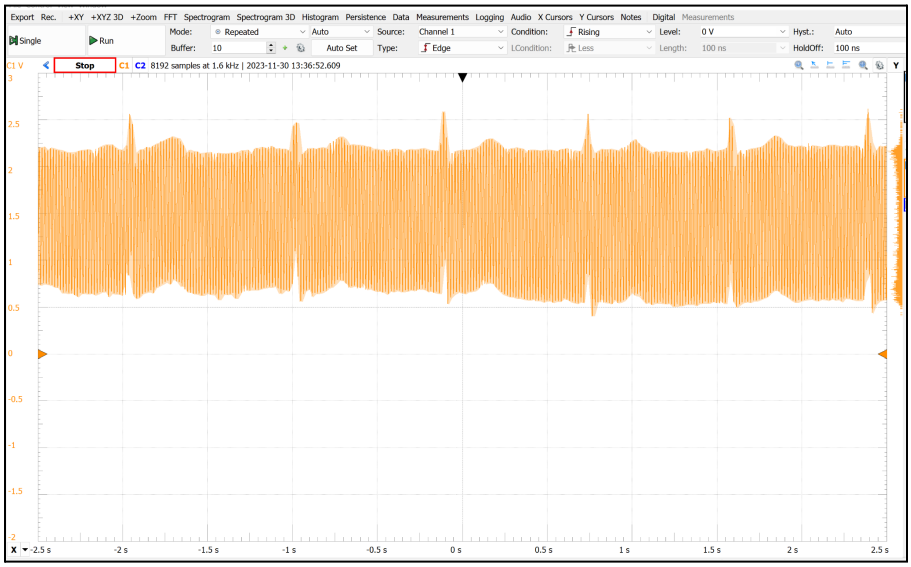

Fig 38. Experimental Output of EKG

After capturing the raw EKG data from the AD2, we needed to design an FIR filter that eliminated the 60 Hz interference within the signal. First, we needed to create the kernels of our filter. Knowing that we needed a null at 60 Hz and having a sampling frequency of 1600 Hz, the following analytical calculations were used to calculate the kernels of the FIR filter:

$$\frac{2\pi\times 60}{1600} = \frac{3\pi}{40} = \Omega$$

$$\frac{3\pi}{40} = \frac{2\pi\times n}{N}$$

Number of values in kernel: $\frac{f_s}{f_c} = \frac{1600}{60} = 26.67$

Coefficients of the kernel: $\frac{f_c}{f_s} = \frac{60}{1600} = \frac{3}{80}$

Now we clearly cannot have a kernel with a fractional number of array elements. As a result, we developed two kernels, one with 26 values and one with 27 values. In order to find the corresponding corner frequencies for each kernel, the following calculations were performed:

$$\frac{1600}{f_{C1}} = 26$$

$$f_{C1} = 61.54\ Hz$$

$$\frac{1600}{f_{C2}} = 27$$

$$f_{C2} = 59.26\ Hz$$

As a result, we developed two kernels for the filter:

Kernel 1: 26 values of $\frac{3}{80}$ at a corner frequency of 61.54 Hz

Kernel 2: 27 values of $\frac{3}{80}$ at a corner frequency of 59.26 Hz

Then, we convolved both kernels to obtain a combined kernel. Lastly, using the combined kernel, we convolved the raw EKG data with the combined kernel to remove the 60 Hz interference to produce clear EKG data. The following Python code (Fig. 39) to convolve the kernels, filtered EKG results (Fig. 40), and the frequency response of the FIR filter (Fig. 41) are shown below respectively. As you can see, Fig. 40 shows a near-perfect removal of the 60-cycle interference. This looks like a true EKG output.

```python
import numpy as np
import matplotlib.pyplot as plt

import csv

sampling_rate = 1600  # samples/s
corner_frequency_one = 59.26  # 27 hz
corner_frequency_two = 61.54 # 26 hz

csv_file_path = 'C:/Users/maste/Downloads/john.csv' # Change path file to your specific directory

csv_data = []
time_array = []

with open(csv_file_path, 'r') as file:
    # Create a CSV reader object
    csv_reader = csv.reader(file)

    for row in csv_reader: # data values
        second_column_value = float(row[1])  # Assuming the values are numeric
        csv_data.append(second_column_value)


def calculate_z(omega, n):
    z = np.exp(-1j * omega * n)
    return z

kernel_one = []
num_values_kernel_one = sampling_rate / corner_frequency_two
kernel_one_values = corner_frequency_two / sampling_rate

for i in range(26):
    kernel_one.append(kernel_one_values)

kernel_two = []
num_values_kernel_two = sampling_rate / corner_frequency_one
kernel_two_values = corner_frequency_one / sampling_rate

for i in range(27):
    kernel_two.append(kernel_two_values)

print(kernel_one)
print(kernel_two)

combined_kernel = np.convolve(kernel_one, kernel_two) # in frequency domain

final_result = np.convolve(combined_kernel, csv_data)

time_array = np.linspace(-2.56, 2.56, 8243)

print("Length of Data: ", len(final_result))
print("Length of Time: ", len(time_array))

plt.plot(time_array, final_result)
plt.title('EKG Results')
plt.xlim(-2.54, 2.54)
plt.ylim(1.25,2)
plt.xlabel('Time (s)')
plt.ylabel('Voltage (V)')
plt.grid(True)
plt.show()

frequency = np.arange(0, np.pi, np.pi / 1024)

n = len(combined_kernel)
transfer_function_array = []

for freq in frequency:
    transfer_function_sum = 0
    for value in range(0, n):
        z = calculate_z(freq, value)
        transfer_function_sum += combined_kernel[value] * z
    transfer_function_array.append(transfer_function_sum)

transfer_function_array = 20 * np.log10(transfer_function_array)

plt.plot(frequency / np.pi, transfer_function_array)
plt.xlim(0, 1)
plt.title('Frequency Response')
plt.xlabel('Fractions of Capital Omega')
plt.ylabel('Magnitude (dB)')
plt.grid(True)
plt.show()
```

Fig 39. FIR Filter Script

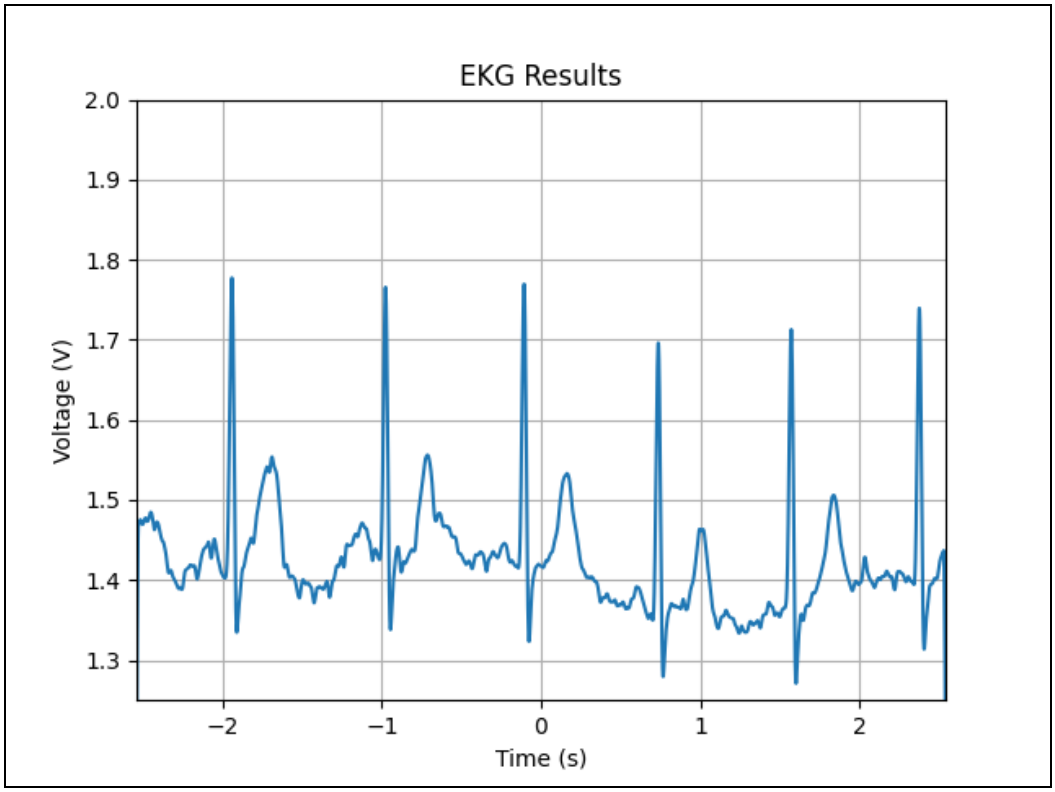

Fig 40. Total Output of EKG after FIR Filter to Eliminate Noise

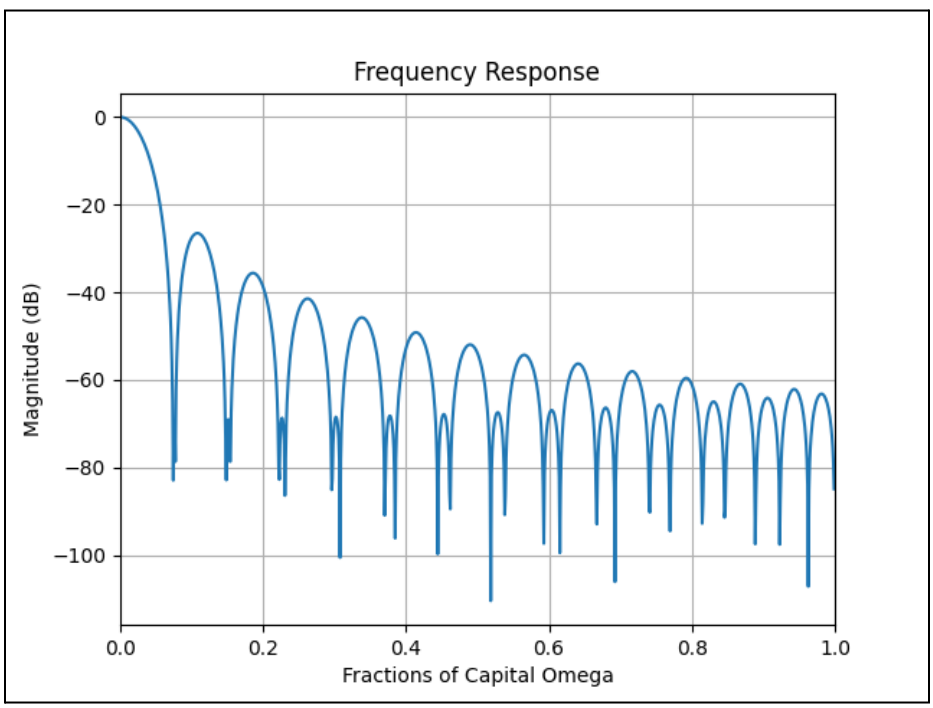

Fig 41. FIR Filter Frequency Response

Conclusions

Summary

The purpose of this project was to use circuit components and designs that we had learned in class and that are readily used in the real world and apply them to create an Electrocardiogram. We did this using the combination of an instrumentation amplifier, integrator, Butterworth filters (using the Sallen Key configuration with op-amps), an isolator, and a voltage regulator. In our design process, we started with the input RC networks that would feed the in-amp. We had to meet the design specs of a filter corner frequency and minimum resistance, which we did using previously acquired knowledge in our FUN classes. We then moved on to designing the gain resistor for the in-amp. After reviewing the peak-to-peak of the example data, we used 100Ω resistors to achieve a gain of 1000, putting our peak-to-peak near 1V, as requested by design specs. We then designed the integrator, which had a transfer function requirement. We found the transfer function by hand and changed the resistor and capacitor value in order to meet design specs. It was then that we had to design Vmid, which is where our circuit output would be centered around. We knew it had to be half of our supply voltage, and this paired with a resistance and corner frequency requirement meant we could derive the transfer function by hand and move forward with designing the resistor and capacitor values. As for the antialiasing filters, most of the work for this design was done in a previous homework assignment. Using the transfer function of the filters and a required corner frequency, we were able to meet the requirements of -72dB of attenuation at 500Hz using simplification strategies by Texas Instruments as well as a minimum resistance. Our isolator design was relatively straightforward, as we were given the isolator's transfer gain bin, allowing for the design of resistor and capacitor values to be relatively straightforward. Throughout the design process, the chips' data sheets by their manufacturer proved to be the most helpful resource. Although time-consuming, all suggestions and design considerations were able to be found.

When building the circuit on Ultiboard, the major design consideration was to apply circuit elements in the order they were as the circuit moved signals forward. First, the in-amp and integrator were placed, then the filter, then the isolator and related components. Power was routed to all components first, and since all elements were already near each other in the circuit,

routing one to another became very straightforward. All bypass capacitors were placed near their respective chips in order to reduce noise and ensure they could function correctly.

The Ultiboard file was sent to WWW for manufacturing along with design instruction documents to ensure it was manufactured correctly. The board was shipped to school and we were able to test. Each circuit component was continuity checked using a multimeter and was then tested using signals that would ensure we knew if it was functioning correctly. Vmid was first tested to ensure we saw 1.65V, meaning our circuit's output would be centered around there. For the in-amp, the gain resistor was removed (resulting in a gain of 1) and two input waveforms were sent out of phase, noting that the output should be the difference between the two. Having the output seen as centered around 1.65V proved that our integrator was also functioning correctly. The filters were tested in the frequency domain, ensuring that we matched design specs. The isolator was next to be tested, and this was sent a sinusoid, noting that the expected value was a sinusoid with a gain of 1 (an identical signal). This was where our largest discrepancy was, as we saw a gain of slightly over 0.9. However, we decided as a group that this would be okay for the purpose of our project, as our output would not rail and all of the signal would still make it to the output. We could then test our power supply by adding jumpers to the correct pins and then attaching the battery. Once we verified that all components were receiving the correct voltage, we could conclude that the power supply was working and we could then test our design in real life. We used a group member as a test subject and applied leads to both of his wrists and one on his ankle, acting as a ground reference point. The EKG was attached to the AD2, which received power from a USB connection to the computer and could also display the output in Waveforms. The leads were attached to a headphone jack input, and the output was recorded on a group member's computer. The output was heavily affected by 60-cycle interference from power sources and electrical signals all around the test room, so the output was taken as a CSV file and run through an FIR filter using the information we received in lecture. This completely eliminated the 60-cycle interference, resulting in an EKG output as we expected it. At this point, the project was finished.

Future Improvement

In the future, the main focus of this project should definitely be kept. It was an extremely valuable experience for our entire group that we were able to design such a complex system from nothing, referencing data sheets and class lectures in order to correctly design it. However, our group felt as though we could not focus on the project as much as we needed. We were pressed for time with other assignments from this class and others. It is possible that if the due dates were spread out more (for example instead of all part values due at once, each circuit block's values were due at separate times throughout the semester). This would help by letting us apply what we learned right when we learned it in class to ensure that we could reinforce our knowledge. Other than this, the project testing and verification went surprisingly smoothly for our group, and the EKG as a whole was a success.