ISA bus

File: ECBbus.kicad_sch

Decoder

File: Decoder.kicad_sch

MMU four

File: MMU-4.kicad_sch

RTC

File: RTC.kicad_sch

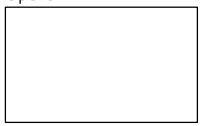
Power

File: Power.kicad_sch

CPU 6502

File: cpu-6502.kicad_sch

Spare

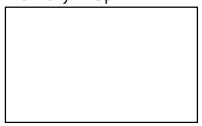


File: Spare.kicad_sch

ACIA

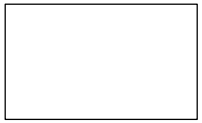
File: ACIA.kicad_sch

Memory Map



File: memory-map.kicad_sch

IO



File: IO.kicad_sch

Reset

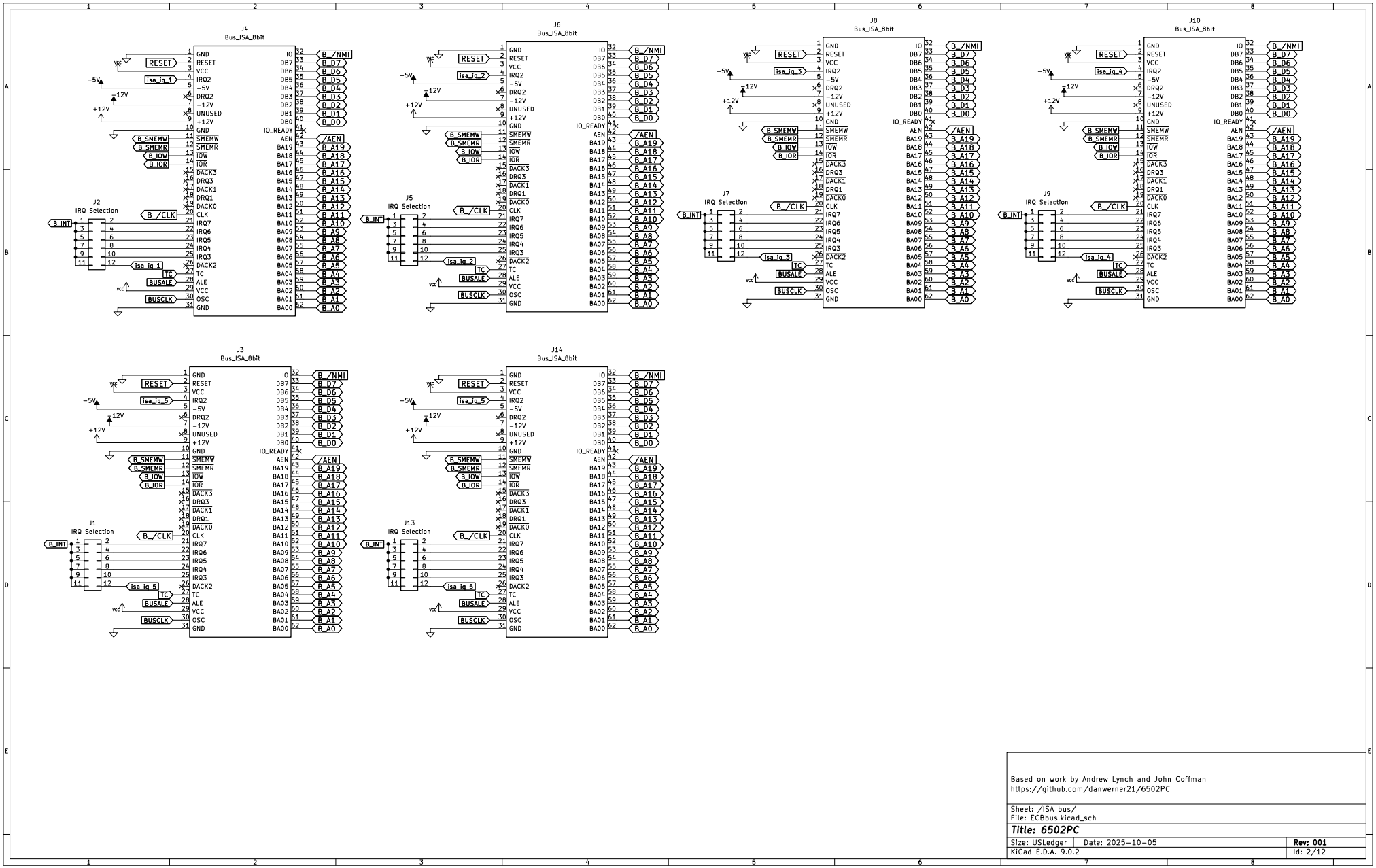
File: Reset.kicad_sch

Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6502PC

Sheet: /
File: 6502PC-6U.kicad_sch

Title: 6502PC

Size: A	Date: 2025-10-05	**Rev: 001**
KiCad E.D.A. 9.0.2		Id: 1/12

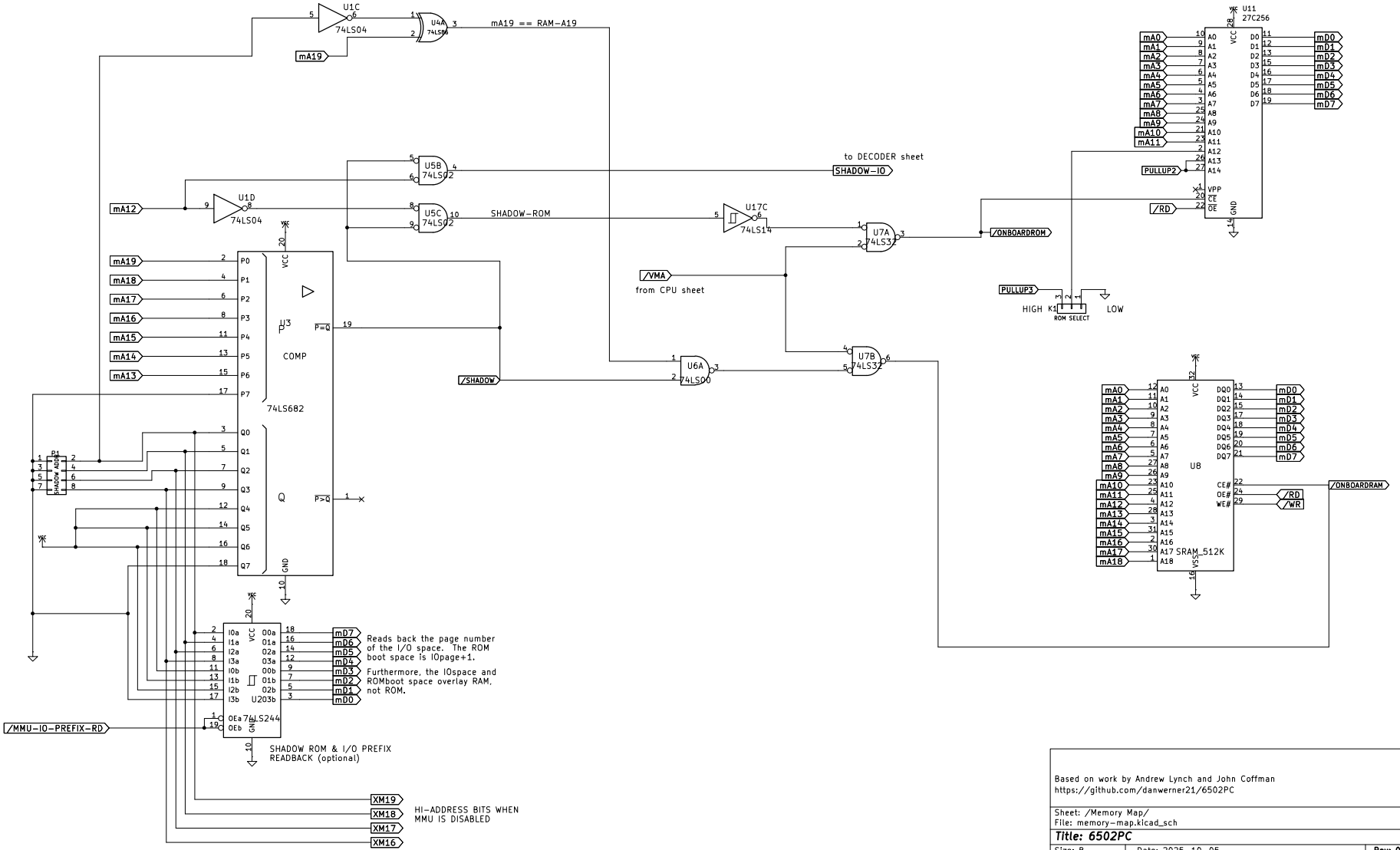


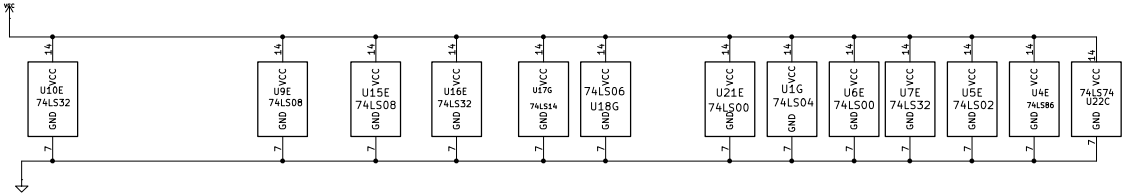
Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6502PC

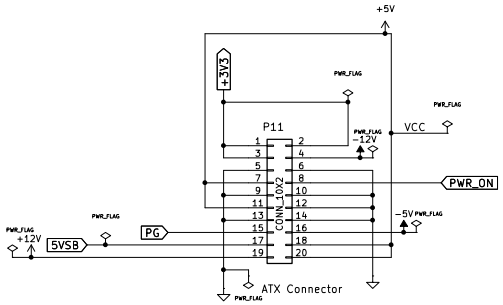
Sheet: /ISA bus/
File: ECBbus.kicad_sch

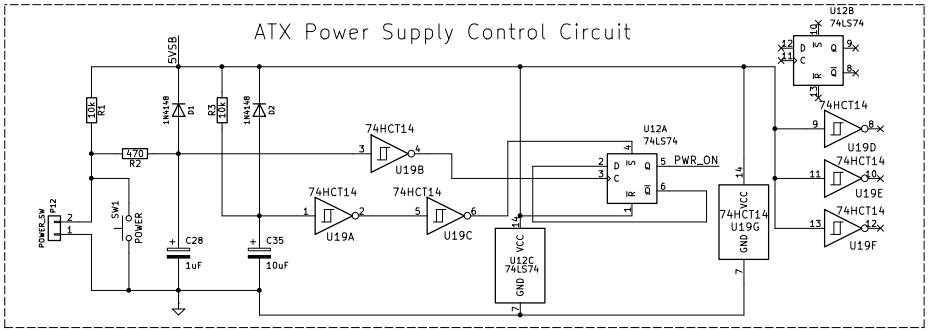
Title: 6502PC

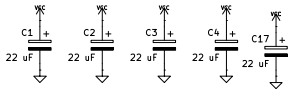
Size: USLedger | Date: 2025-10-05 | **Rev: 001**
KiCad E.D.A. 9.0.2 | Id: 2/12


U1C
74LS04
U4A
74LS86
mA19 == RAM-A19
mA19
U5B
74LS02
to DECODER sheet
SHADOW-IO
mA12
U1D
74LS04
U5C
74LS02
SHADOW-ROM
U17C
74LS14
U7A
74LS32
/ONBOARDROM
/VMA
from CPU sheet
PULLUP3
HIGH
K1
ROM SELECT
LOW
U11
27C256
PULLUP2
/RD
mA0
mA1
mA2
mA3
mA4
mA5
mA6
mA7
mA8
mA9
mA10
mA11
mD0
mD1
mD2
mD3
mD4
mD5
mD6
mD7
U3
74LS682
COMP
P0
P1
P2
P3
P4
P5
P6
P7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
P=Q
SHADOW ADD
/SHADOW
U6A
74LS00
U7B
74LS32
U8
SRAM_512K
CE#
OE#
WE#
/WR
/ONBOARDRAM
U2
74LS244
/MMU-IO-PREFIX-RD
Reads back the page number of the I/O space. The ROM boot space is IOpage+1.
Furthermore, the IOspace and ROMboot space overlay RAM, not ROM.
SHADOW ROM & I/O PREFIX READBACK (optional)
XM19
XM18
XM17
XM16
HI-ADDRESS BITS WHEN MMU IS DISABLED
Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6502PC
Sheet: /Memory Map/
File: memory-map.kicad_sch
Title: 6502PC
Size: B
Date: 2025-10-05
Rev: 001
KiCad E.D.A. 9.0.2
Id: 4/12

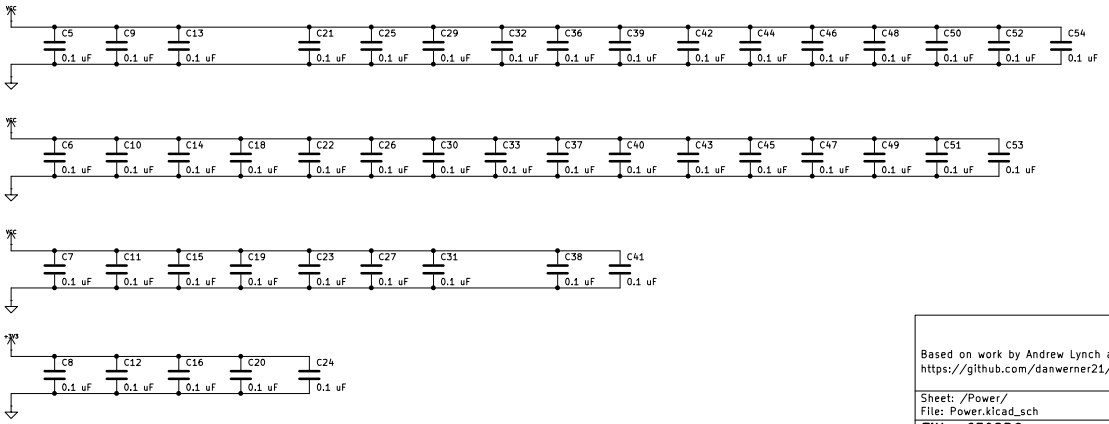


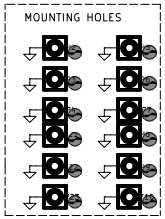






BYPASS CAPACITORS





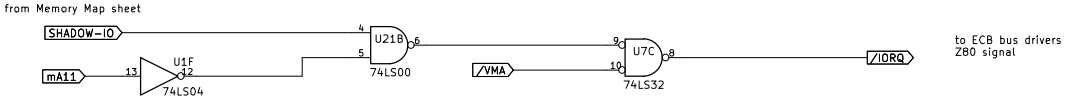
Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6502PC

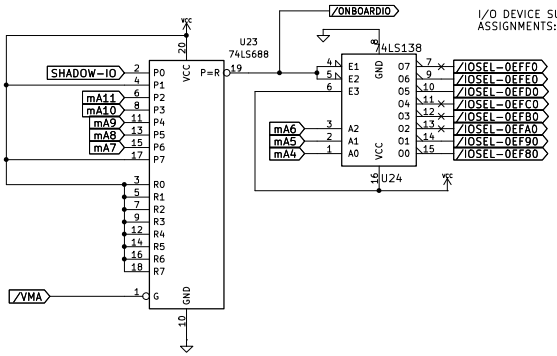
Sheet: /Power/
File: Power.kicad_sch

Title: 6502PC

Size: B	Date: 2025-10-05	Rev: 001
KiCad E.D.A. 9.0.2		Id: 6/12

HIGHEST LEVEL I/O ADDRESS DECODE





I/O DEVICE SUBSYSTEM ADDRESS ASSIGNMENTS:

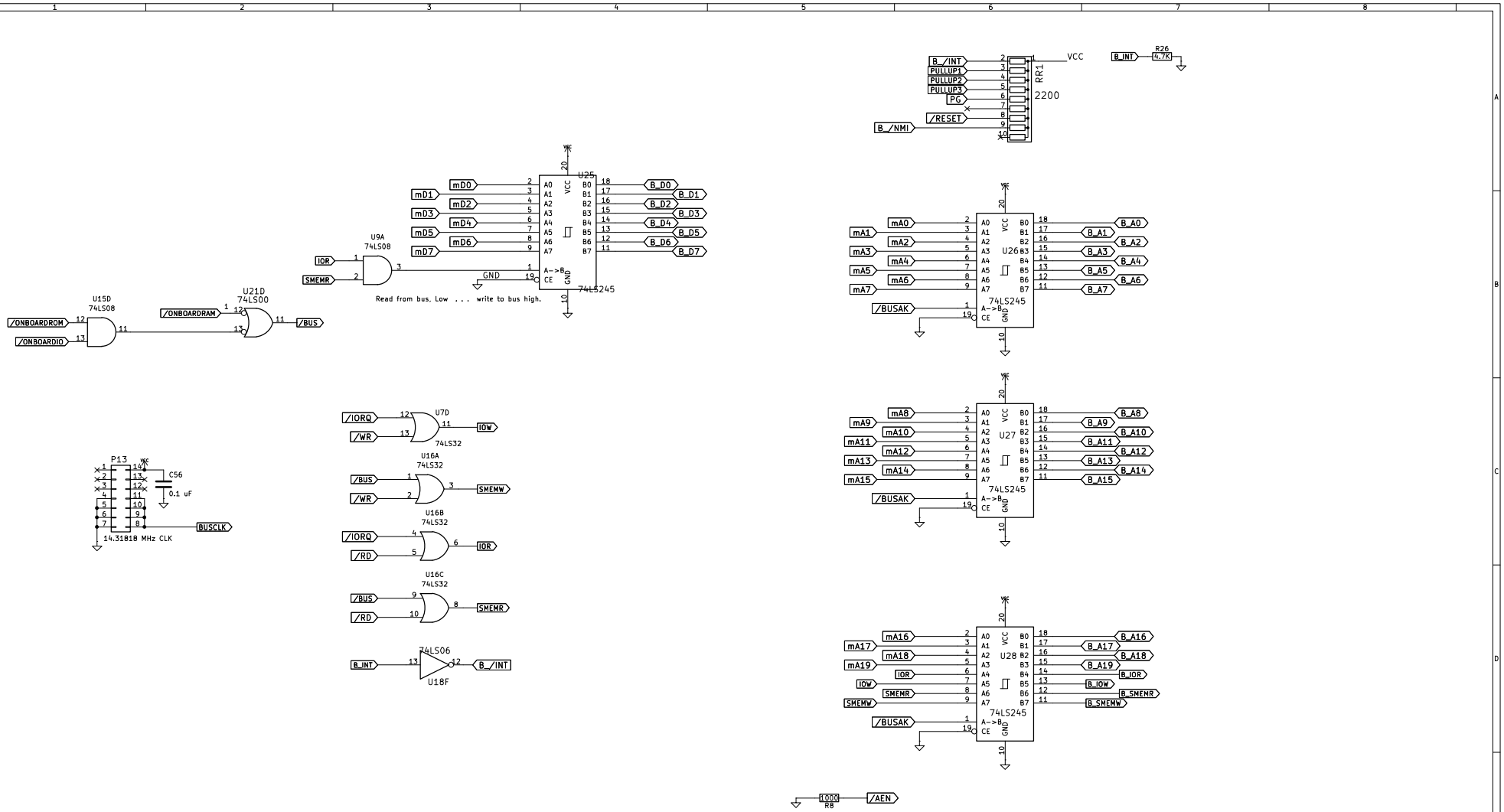
$EFF0 – $EFFF	available
$EFE0 – $EFEF	MMU Registers (3)
$EFD0 – $EFDF	MMU Task Map (16)
$EFC0 – $EFCF	available
$EFB0 – $EFBF	available
$EFA0 – $EFAF	available
$EF90 – $EF9F	RTC (16)
$EF80 – $EF8F	ACIA (4)

Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6502PC

Sheet: /Decoder/
File: Decoder.kicad_sch

Title: 6502PC

Size: B	Date: 2025-10-05	**Rev: 001**
KiCad E.D.A. 9.0.2		Id: 7/12



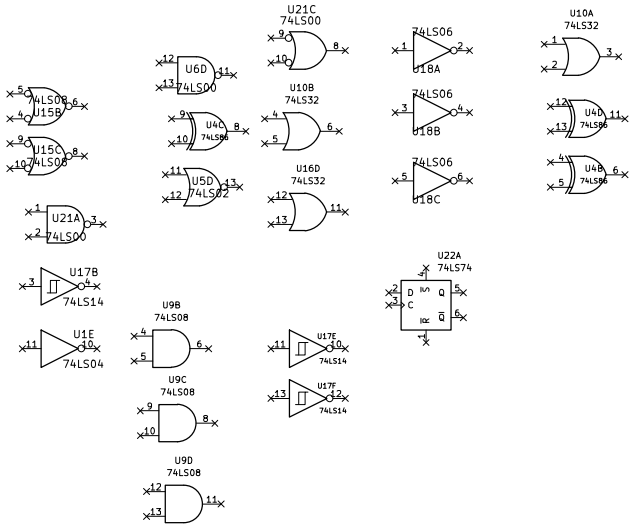
Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6502PC

Sheet: /IO/
File: IO.kicad_sch

Title: 6502PC

Size: B	Date: 2025-10-05	**Rev: 001**
KiCad E.D.A. 9.0.2		Id: 8/12

SPARE

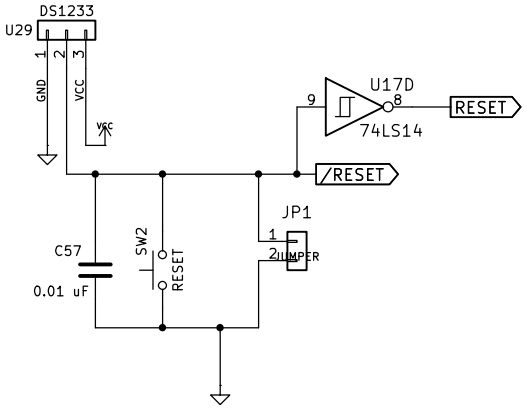


Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6502PC

Sheet: /Spare/
File: Spare.kicad_sch

Title: 6502PC

Size: B	Date: 2025-10-05	**Rev: 001**
KiCad E.D.A. 9.0.2		Id: 9/12

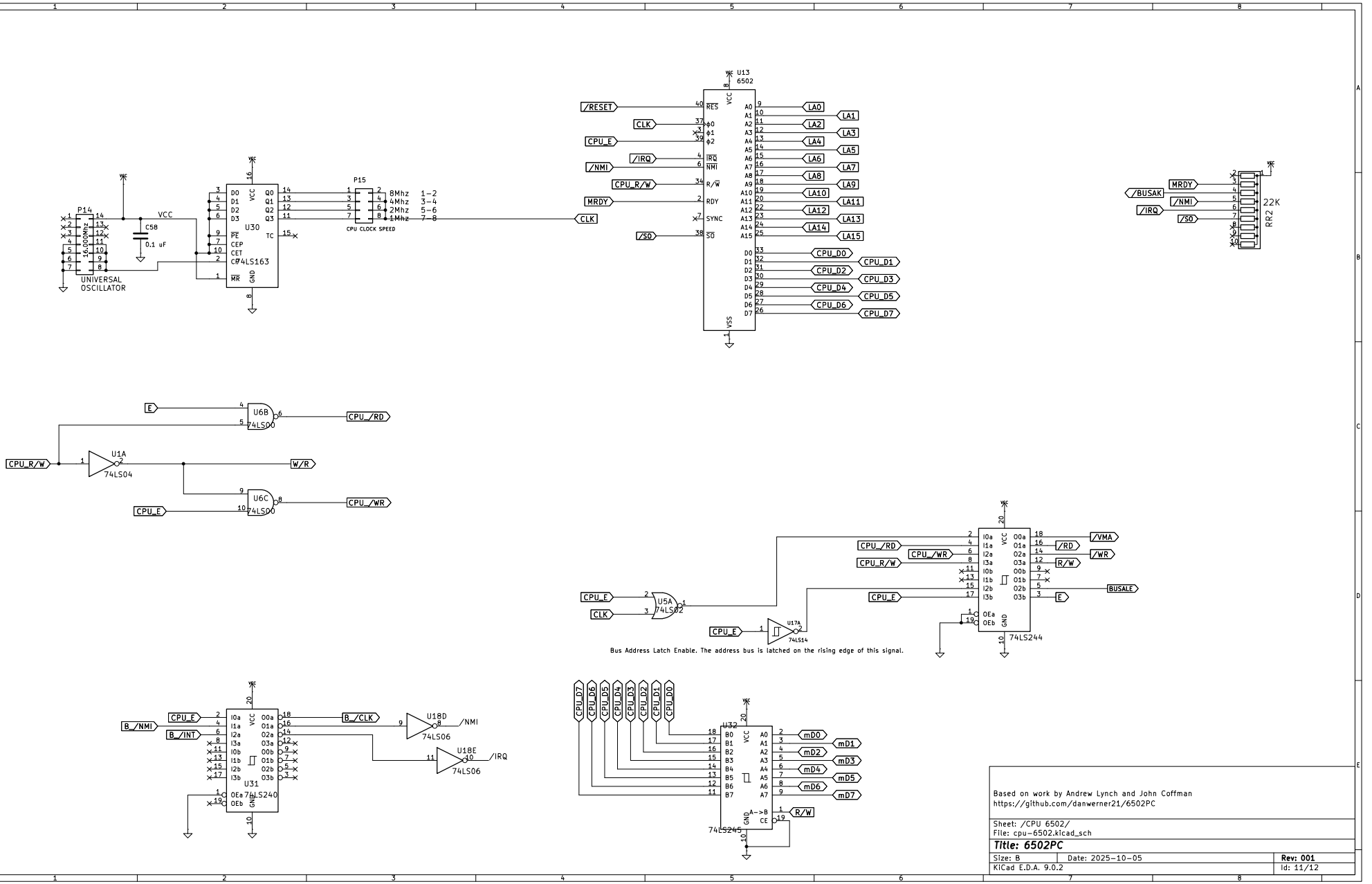


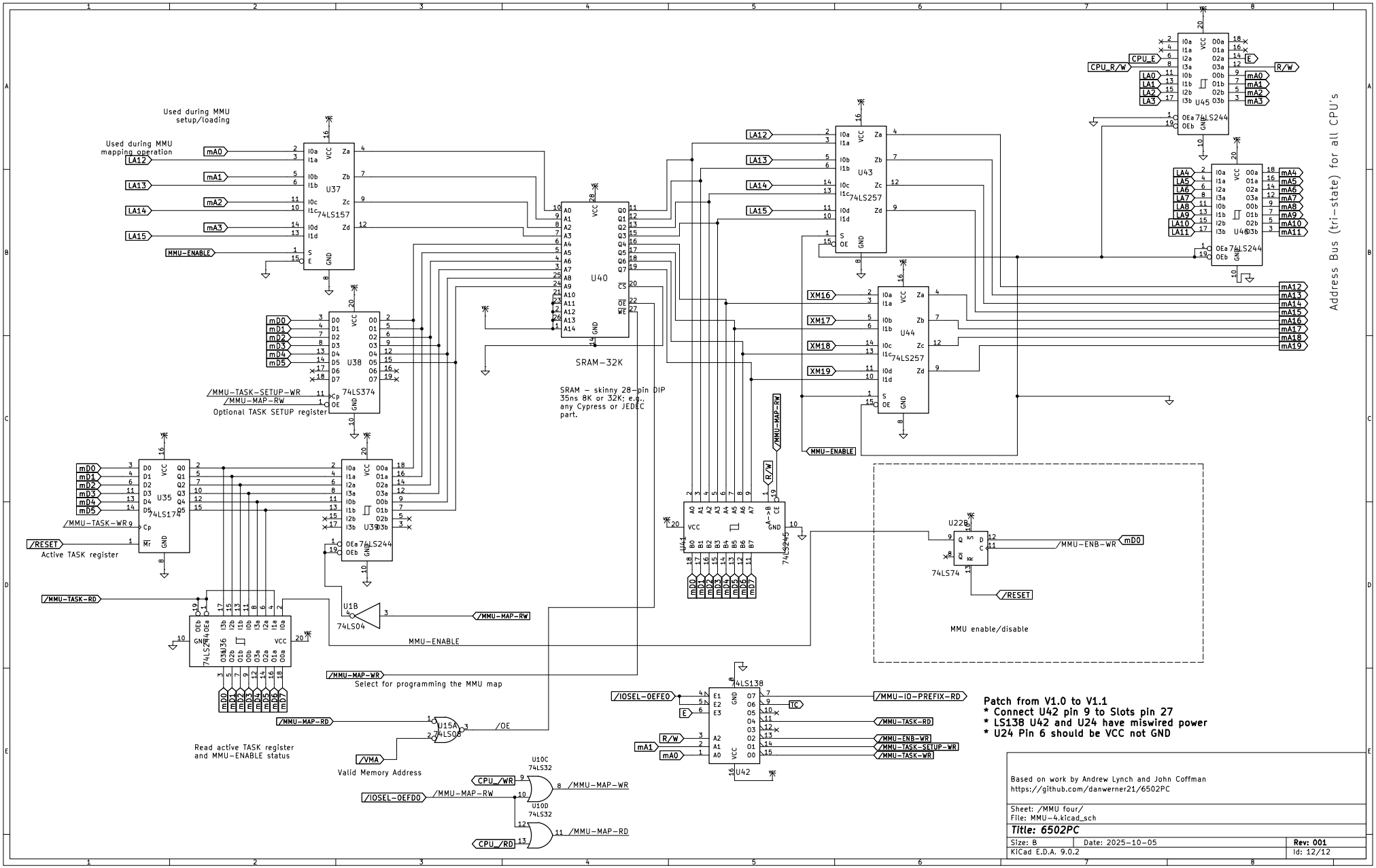
Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6502PC

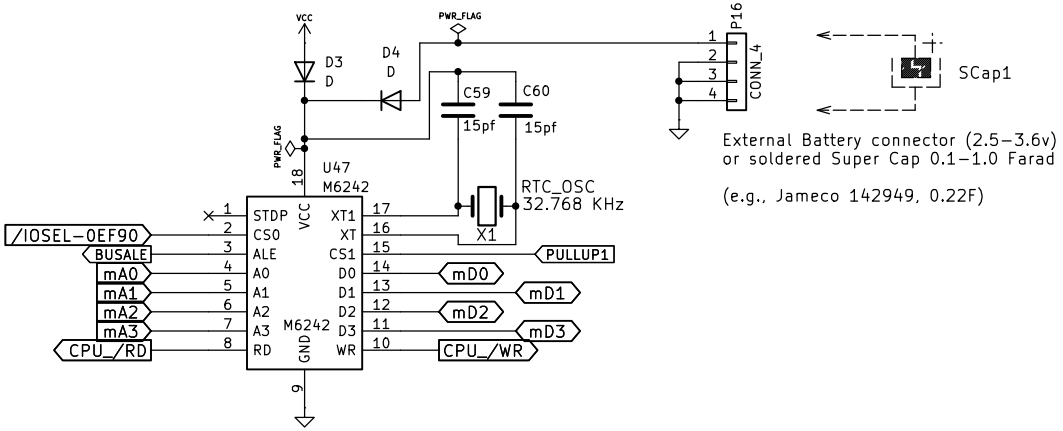
Sheet: /Reset/
File: Reset.kicad_sch

Title: 6502PC

Size: A	Date: 2025-10-05	**Rev: 001**
KiCad E.D.A. 9.0.2		Id: 10/12


P14
16.000MHz
VCC
C58
0.1 uF
UNIVERSAL
OSCILLATOR
U30
74LS163
P15
8Mhz 1-2
4Mhz 3-4
2Mhz 5-6
1Mhz 7-8
CPU CLOCK SPEED
U13
6502
/RESET
CLK
CPU_E
/NMI
/IRQ
CPU_R/W
MRDY
/SO
LA0
LA1
LA2
LA3
LA4
LA5
LA6
LA7
LA8
LA9
LA10
LA11
LA12
LA13
LA14
LA15
CPU_D0
CPU_D1
CPU_D2
CPU_D3
CPU_D4
CPU_D5
CPU_D6
CPU_D7
MRDY
/BUSAK
/NMI
/IRQ
/SO
22K
RR2
E
U6B
74LS00
CPU_/RD
CPU_R/W
U1A
74LS04
W/R
U6C
74LS00
CPU_/WR
CPU_E
U5A
74LS02
CLK
U17A
74LS14
Bus Address Latch Enable. The address bus is latched on the rising edge of this signal.
CPU_/RD
CPU_/WR
CPU_R/W
CPU_E
/VMA
/RD
/WR
R/W
BUSALE
E
74LS244
B_/NMI
B_/INT
B_/CLK
U18D
74LS06
NMI
U18E
74LS06
IRQ
U31
74LS240
CPU_D7
CPU_D6
CPU_D5
CPU_D4
CPU_D3
CPU_D2
CPU_D1
CPU_D0
U32
74LS245
mD0
mD1
mD2
mD3
mD4
mD5
mD6
mD7
R/W
A->B
Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6502PC
Sheet: /CPU 6502/
File: cpu-6502.kicad_sch
Title: 6502PC
Size: B
Date: 2025-10-05
Rev: 001
KiCad E.D.A. 9.0.2
Id: 11/12


Used during MMU setup/loading
Used during MMU mapping operation
U37
74LS157
mA0
mA1
mA2
mA3
LA12
LA13
LA14
LA15
MMU-ENABLE
U38
74LS374
mD0
mD1
mD2
mD3
mD4
mD5
/MMU-TASK-SETUP-WR
/MMU-MAP-RW
Optional TASK SETUP register
U40
SRAM-32K
SRAM – skinny 28-pin DIP
35ns 8K or 32K; e.g.,
any Cypress or JEDEC
part.
U43
74LS257
U44
74LS257
XM16
XM17
XM18
XM19
U45
74LS244
CPU_E
CPU_R/W
LA0
LA1
LA2
LA3
E
R/W
U46
74LS244
LA4
LA5
LA6
LA7
LA8
LA9
LA10
LA11
mA4
mA5
mA6
mA7
mA8
mA9
mA10
mA11
mA12
mA13
mA14
mA15
mA16
mA17
mA18
mA19
Address Bus (tri-state) for all CPU's
U35
74LS174
/MMU-TASK-WR
/RESET
Active TASK register
U39
74LS244
/MMU-TASK-RD
U36
74LS244
U1B
74LS04
/MMU-MAP-RW
MMU-ENABLE
/MMU-MAP-WR
Select for programming the MMU map
U44
74LS245
R/W
U22B
74LS74
/MMU-ENB-WR
MMU enable/disable
/MMU-MAP-RD
U15A
74LS08
/OE
/VMA
Valid Memory Address
Read active TASK register
and MMU-ENABLE status
U10C
74LS32
U10D
74LS32
CPU_/WR
CPU_/RD
/IOSEL-OEFD0
/MMU-MAP-WR
/MMU-MAP-RD
U42
74LS138
/IOSEL-OEFE0
/MMU-IO-PREFIX-RD
/MMU-TASK-RD
/MMU-ENB-WR
/MMU-TASK-SETUP-WR
/MMU-TASK-WR
TC
Patch from V1.0 to V1.1
* Connect U42 pin 9 to Slots pin 27
* LS138 U42 and U24 have miswired power
* U24 Pin 6 should be VCC not GND
Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6502PC
Sheet: /MMU four/
File: MMU-4.kicad_sch
Title: 6502PC
Size: B
Date: 2025-10-05
Rev: 001
KiCad E.D.A. 9.0.2
Id: 12/12

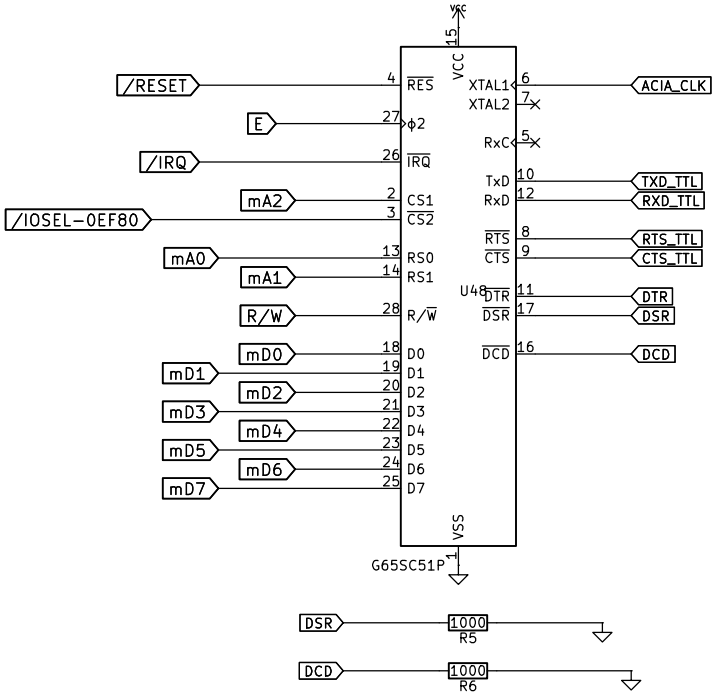


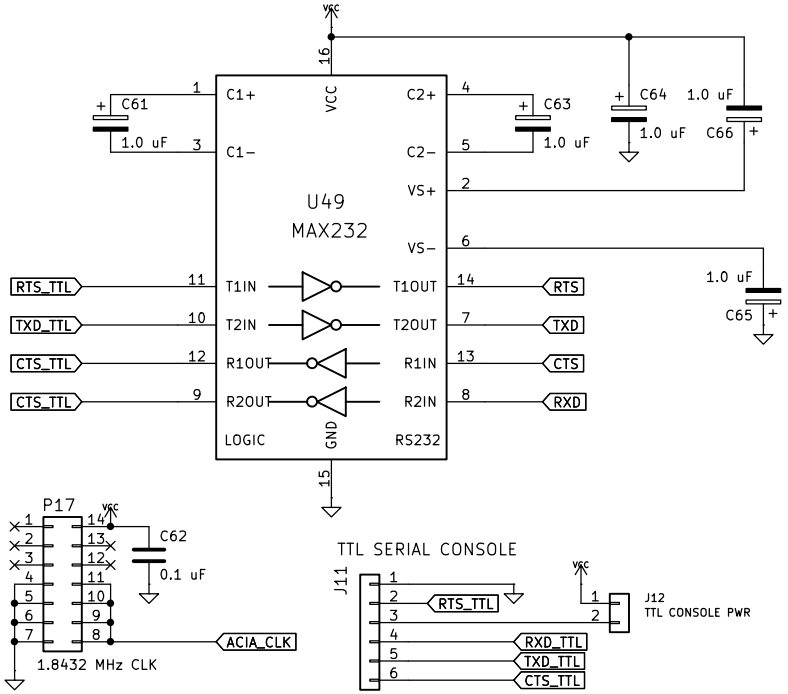
Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6502PC

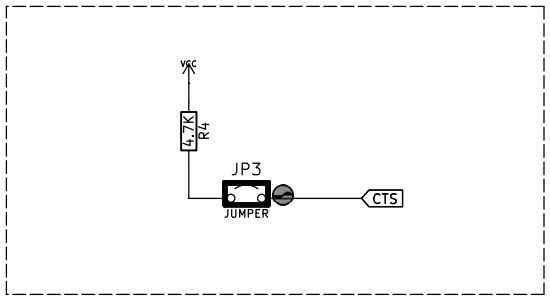
Sheet: /RTC/
File: RTC.kicad_sch

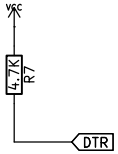
Title: 6502PC

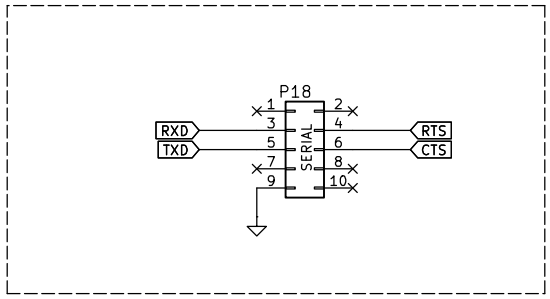
Size: A	Date: 2025–10–05	**Rev: 001**
KiCad E.D.A. 9.0.2		Id: 13/12











CTS is an inverted signal on the RS-232 port. So it is really /CTS. To assert the signal, it must be tied to SPACE, which is a + RS-232 voltage. (MARK, or true, is a - RS-232 voltage.)

Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6502PC

Sheet: /ACIA/
File: ACIA.kicad_sch

Title: 6502PC

Size: A	Date: 2025-10-05	**Rev: 001**
KiCad E.D.A. 9.0.2		Id: 14/12