ISA bus

File: ECBbus.kicad_sch

Decoder

File: Decoder.kicad_sch

MMU four

File: MMU-4.kicad_sch

RTC

File: RTC.kicad_sch

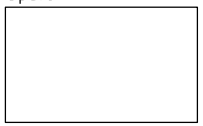
Power

File: Power.kicad_sch

CPU 6809

File: cpu-6809.kicad_sch

Spare

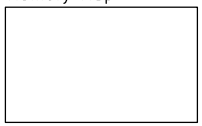


File: Spare.kicad_sch

ACIA

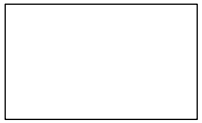
File: ACIA.kicad_sch

Memory Map



File: memory-map.kicad_sch

IO



File: IO.kicad_sch

Reset

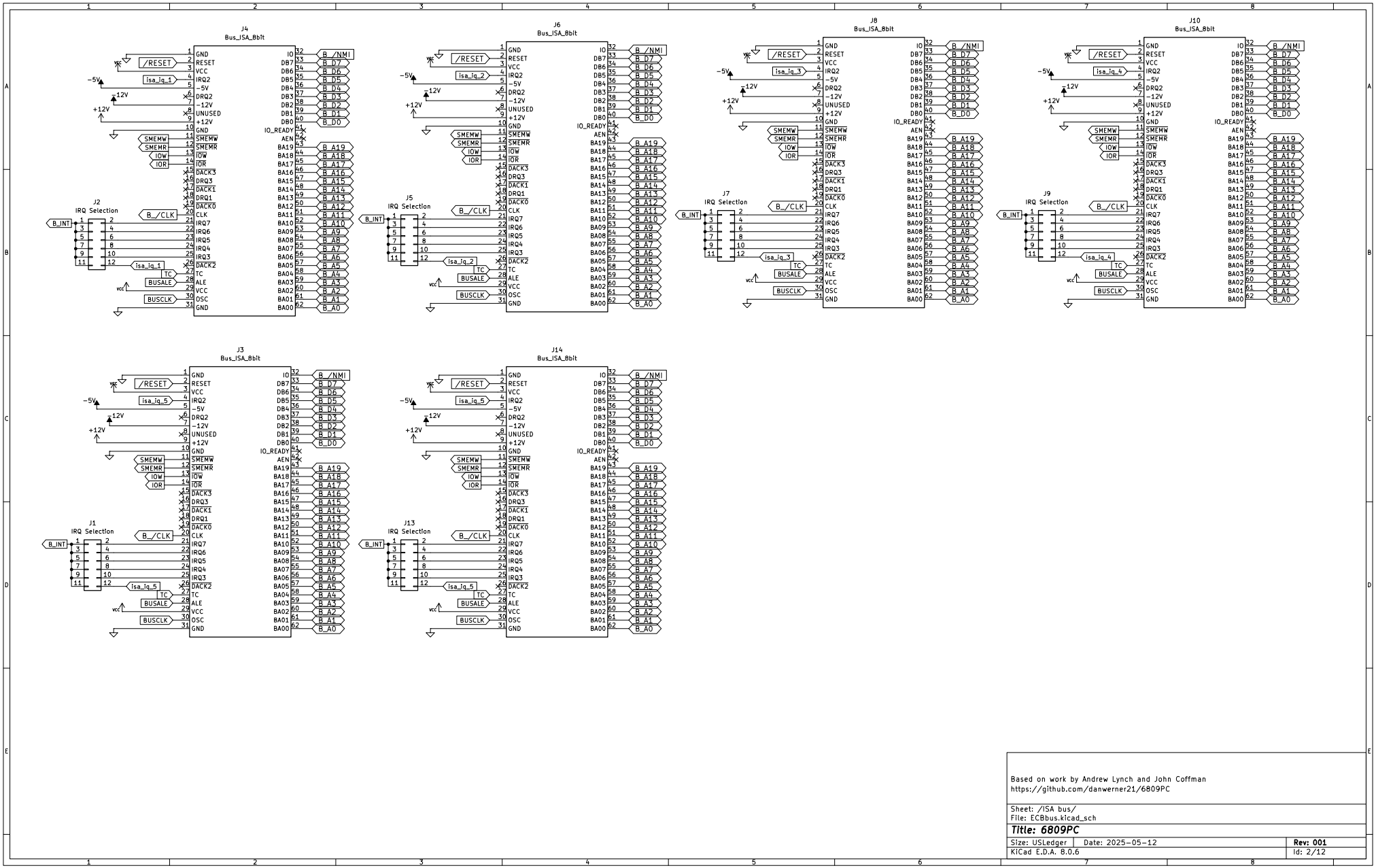
File: Reset.kicad_sch

Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

Sheet: /
File: 6809PC-6U.kicad_sch

Title: 6809PC

Size: A	Date: 2025-05-12	**Rev: 001**
KiCad E.D.A. 8.0.6		Id: 1/12

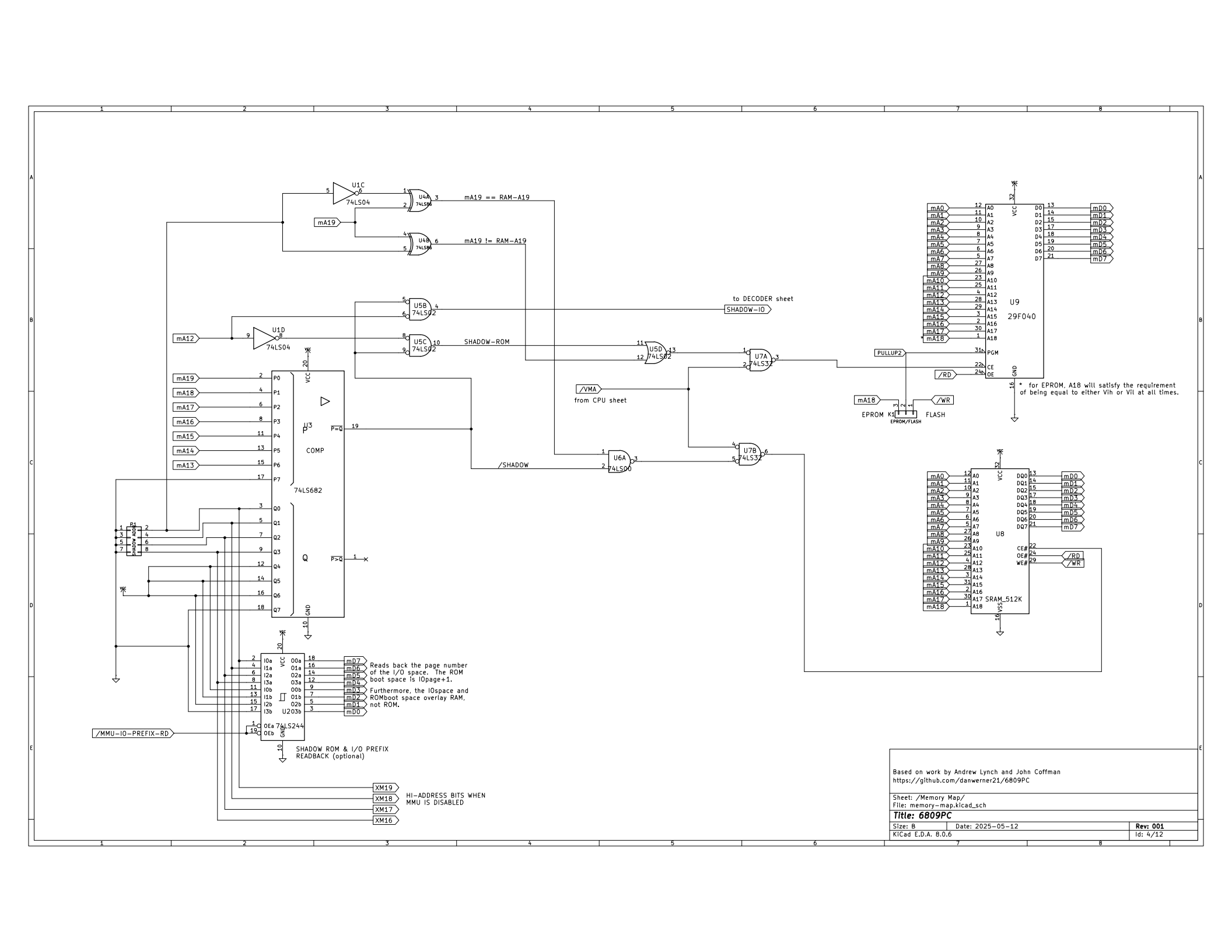


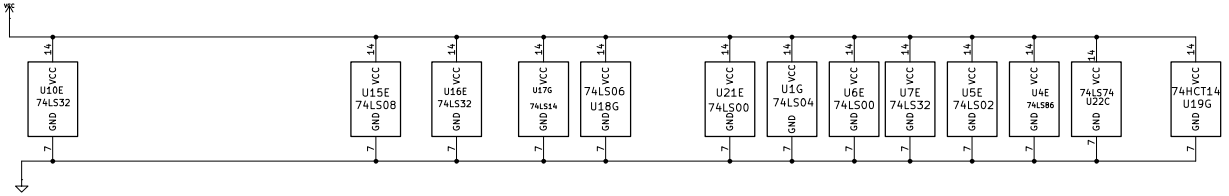
Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

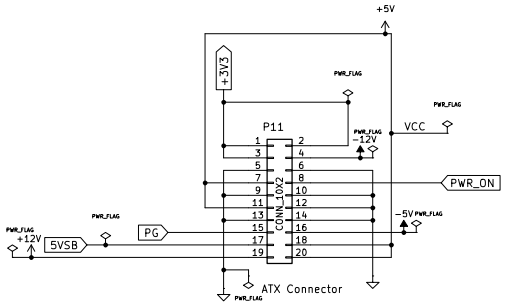
Sheet: /ISA bus/
File: ECBbus.kicad_sch

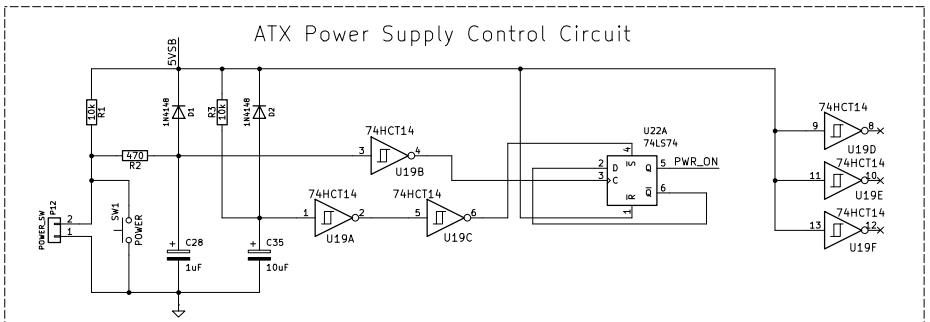
Title: 6809PC

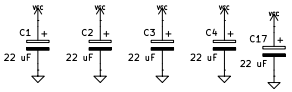
Size: USLedger	Date: 2025-05-12	Rev: 001
KiCad E.D.A. 8.0.6		Id: 2/12


U1C
74LS04
U4A
74LS86
mA19 == RAM-A19
mA19
U4B
74LS86
mA19 != RAM-A19
U5B
74LS02
to DECODER sheet
SHADOW-IO
mA12
U1D
74LS04
U5C
74LS02
SHADOW-ROM
U5D
74LS02
U7A
74LS32
/VMA
from CPU sheet
U6A
74LS00
U7B
74LS32
/SHADOW
U3
COMP
74LS682
P=Q
SHADOW ADDR
U2O3b
74LS244
/MMU-IO-PREFIX-RD
SHADOW ROM & I/O PREFIX
READBACK (optional)
Reads back the page number
of the I/O space. The ROM
boot space is IOpage+1.
Furthermore, the IOspace and
ROMboot space overlay RAM,
not ROM.
XM19
XM18
XM17
XM16
HI-ADDRESS BITS WHEN
MMU IS DISABLED
U9
29F040
PULLUP2
/RD
/WR
EPROM
FLASH
EPROM/FLASH
* for EPROM, A18 will satisfy the requirement
of being equal to either Vih or Vil at all times.
U8
SRAM_512K
Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC
Sheet: /Memory Map/
File: memory-map.kicad_sch
Title: 6809PC
Size: B
Date: 2025-05-12
Rev: 001
KiCad E.D.A. 8.0.6
Id: 4/12

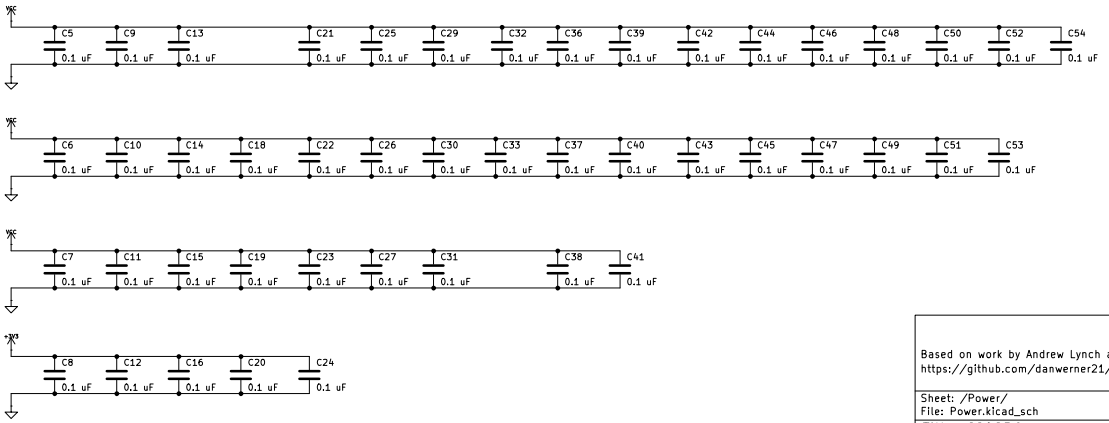


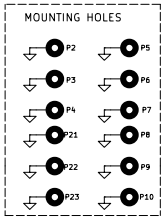






BYPASS CAPACITORS





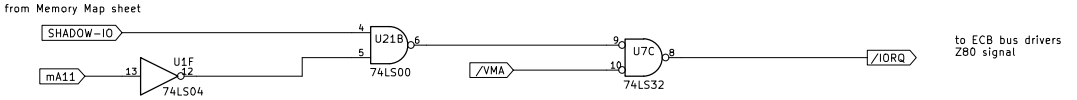
Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

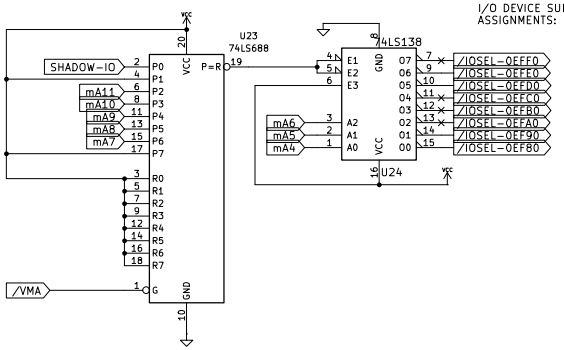
Sheet: /Power/
File: Power.kicad_sch

Title: 6809PC

Size: B	Date: 2025-05-12	**Rev: 001**
KiCad E.D.A. 8.0.6		Id: 6/12

HIGHEST LEVEL I/O ADDRESS DECODE





I/O DEVICE SUBSYSTEM ADDRESS ASSIGNMENTS:

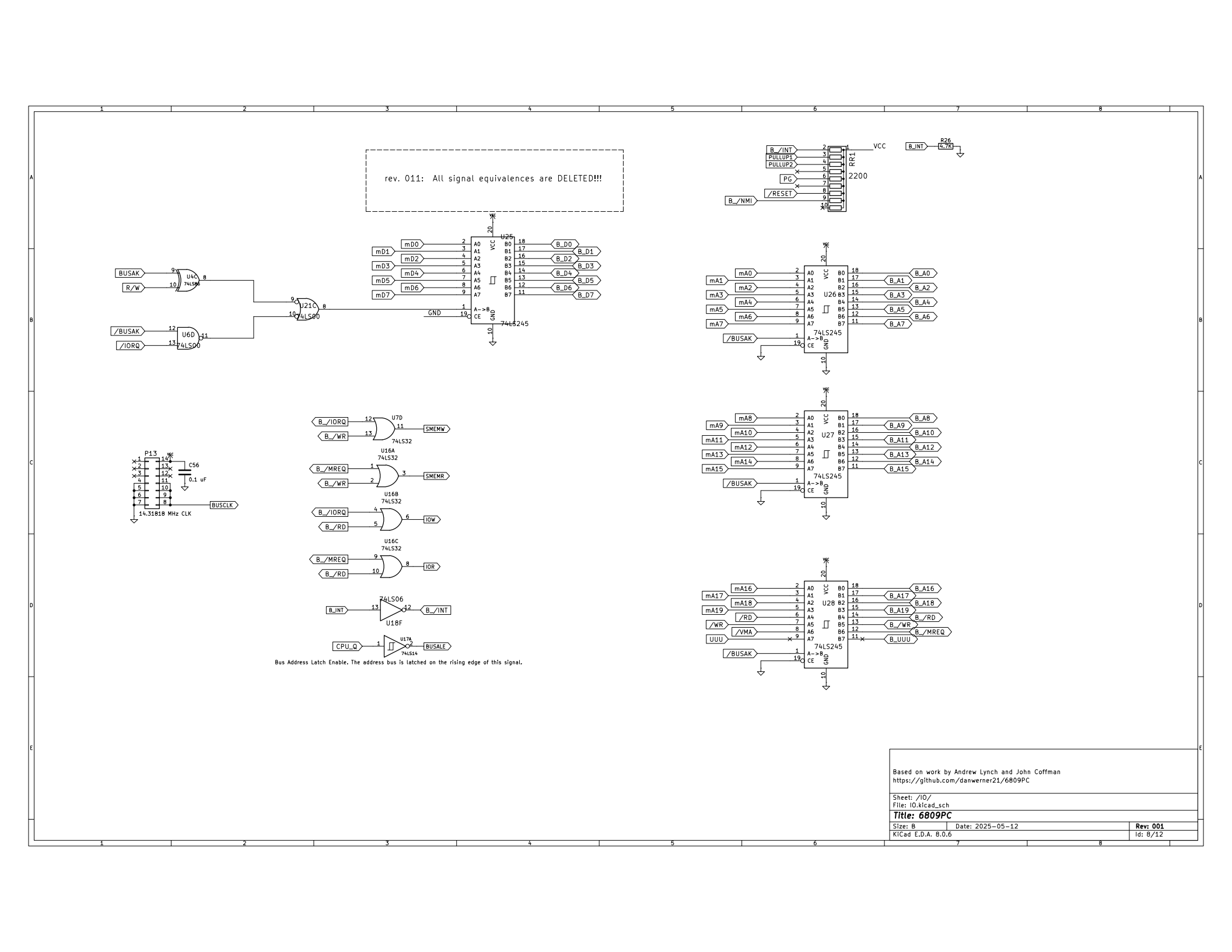
$EFF0 – $EFFF	available
$EFE0 – $EFEF	MMU Registers (3)
$EFD0 – $EFDF	MMU Task Map (16)
$EFC0 – $EFCF	available
$EFB0 – $EFBF	available
$EFA0 – $EFAF	available
$EF90 – $EF9F	RTC (16)
$EF80 – $EF8F	ACIA (4)

Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

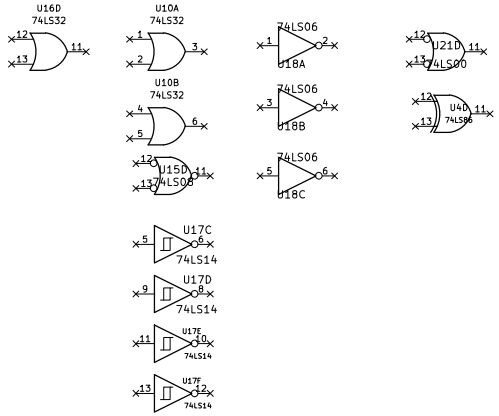
Sheet: /Decoder/
File: Decoder.kicad_sch

Title: 6809PC

Size: B	Date: 2025-05-12	**Rev: 001**
KiCad E.D.A. 8.0.6		Id: 7/12


rev. 011: All signal equivalences are DELETED!!!
B_/INT
PULLUP1
PULLUP2
PG
/RESET
B_/NMI
RR1
2200
VCC
B_INT
R26
4.7K
BUSAK
R/W
U4C
74LS86
U21C
74LS00
/BUSAK
/IORQ
U6D
74LS00
mD0
mD1
mD2
mD3
mD4
mD5
mD6
mD7
U25
74LS245
B_D0
B_D1
B_D2
B_D3
B_D4
B_D5
B_D6
B_D7
GND
mA0
mA1
mA2
mA3
mA4
mA5
mA6
mA7
/BUSAK
U26
74LS245
B_A0
B_A1
B_A2
B_A3
B_A4
B_A5
B_A6
B_A7
mA8
mA9
mA10
mA11
mA12
mA13
mA14
mA15
/BUSAK
U27
74LS245
B_A8
B_A9
B_A10
B_A11
B_A12
B_A13
B_A14
B_A15
mA16
mA17
mA18
mA19
/RD
/WR
/VMA
UUU
/BUSAK
U28
74LS245
B_A16
B_A17
B_A18
B_A19
B_/RD
B_/WR
B_/MREQ
B_UUU
P13
C56
0.1 uF
14.31818 MHz CLK
BUSCLK
B_/IORQ
B_/WR
U7D
74LS32
SMEMW
B_/MREQ
B_/WR
U16A
74LS32
SMEMR
B_/IORQ
B_/RD
U16B
74LS32
IOW
B_/MREQ
B_/RD
U16C
74LS32
IOR
B_INT
74LS06
U18F
B_/INT
CPU_Q
U17A
74LS14
BUSALE
Bus Address Latch Enable. The address bus is latched on the rising edge of this signal.
Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC
Sheet: /IO/
File: IO.kicad_sch
Title: 6809PC
Size: B
Date: 2025-05-12
Rev: 001
KiCad E.D.A. 8.0.6
Id: 8/12

SPARE

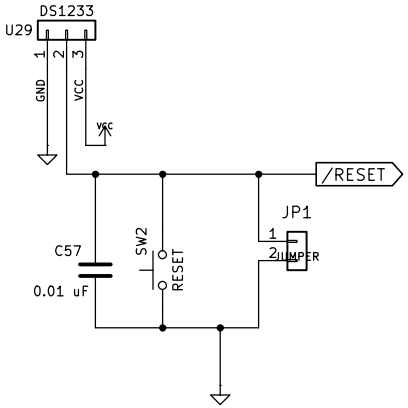


Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

Sheet: /Spare/
File: Spare.kicad_sch

Title: 6809PC

Size: B	Date: 2025-05-12	**Rev: 001**
KiCad E.D.A. 8.0.6		Id: 9/12

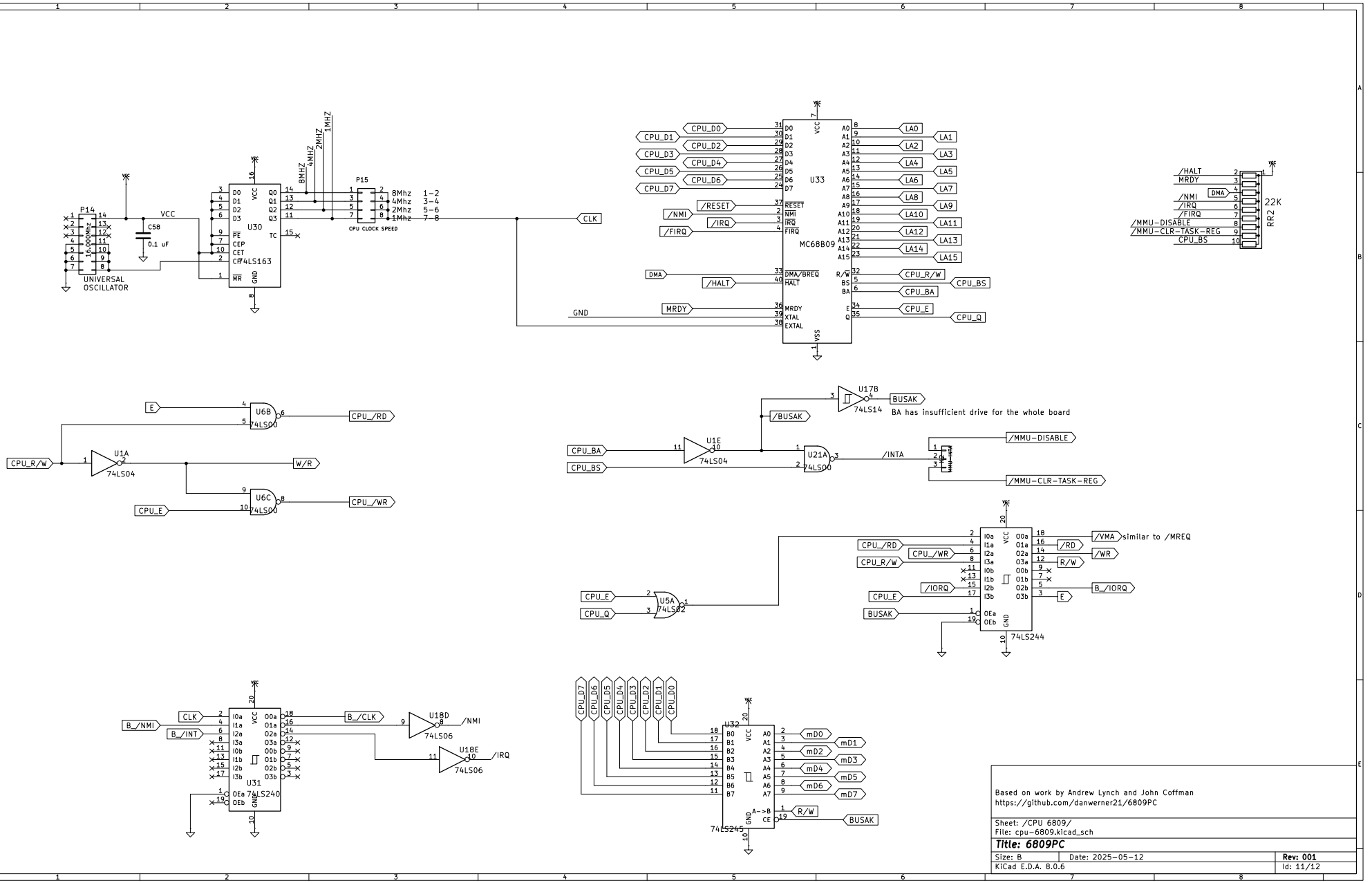


Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

Sheet: /Reset/
File: Reset.kicad_sch

Title: 6809PC

Size: A	Date: 2025-05-12	**Rev: 001**
KiCad E.D.A. 8.0.6		Id: 10/12

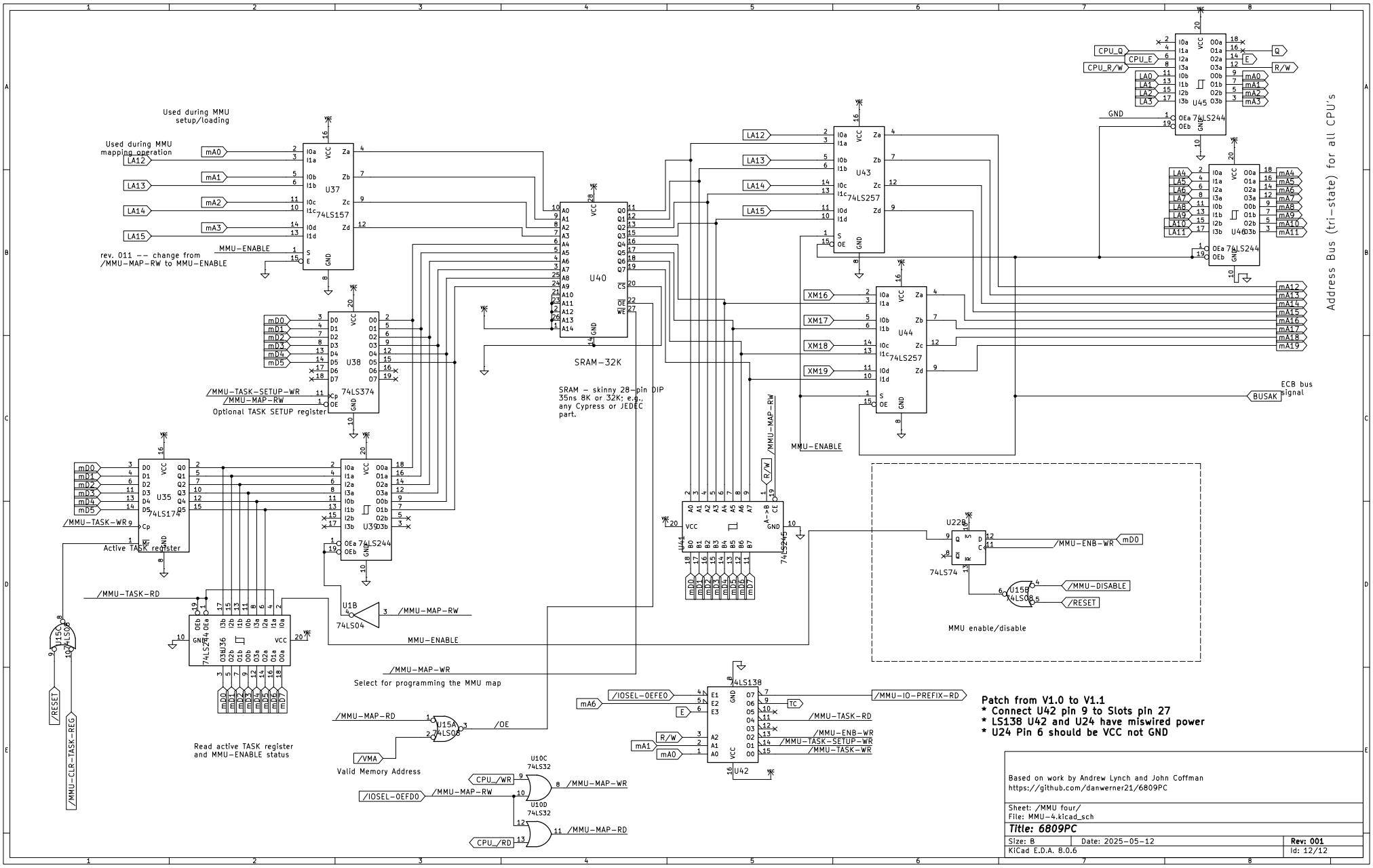


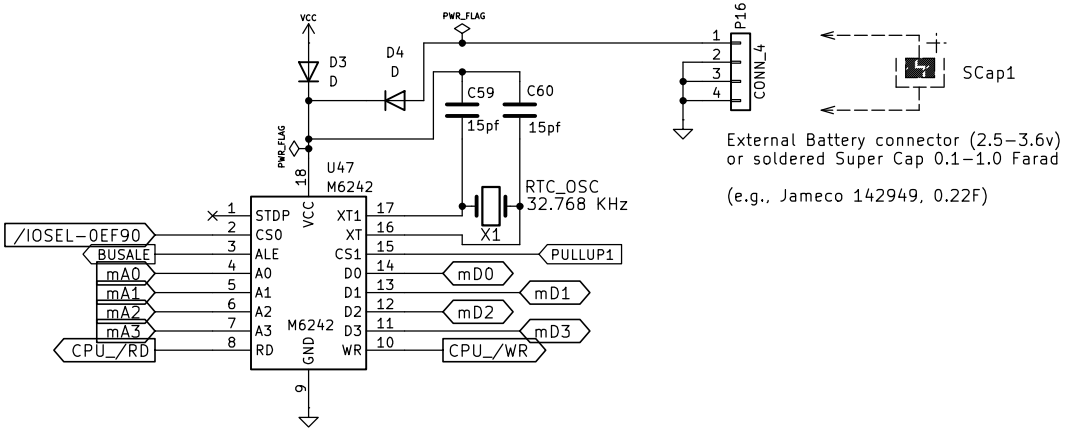
Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

Sheet: /CPU 6809/
File: cpu-6809.kicad_sch

Title: 6809PC

Size: B	Date: 2025-05-12	**Rev: 001**
KiCad E.D.A. 8.0.6		Id: 11/12


Used during MMU setup/loading
Used during MMU mapping operation
rev. 011 -- change from /MMU-MAP-RW to MMU-ENABLE
SRAM-32K
SRAM - skinny 28-pin DIP 35ns 8K or 32K; e.g., any Cypress or JEDEC part.
Optional TASK SETUP register
Active TASK register
Read active TASK register and MMU-ENABLE status
Select for programming the MMU map
Valid Memory Address
MMU enable/disable
ECB bus signal
Address Bus (tri-state) for all CPU's
Patch from V1.0 to V1.1
* Connect U42 pin 9 to Slots pin 27
* LS138 U42 and U24 have miswired power
* U24 Pin 6 should be VCC not GND
Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC
Sheet: /MMU four/
File: MMU-4.kicad_sch
Title: 6809PC
Size: B
Date: 2025-05-12
Rev: 001
KiCad E.D.A. 8.0.6
Id: 12/12

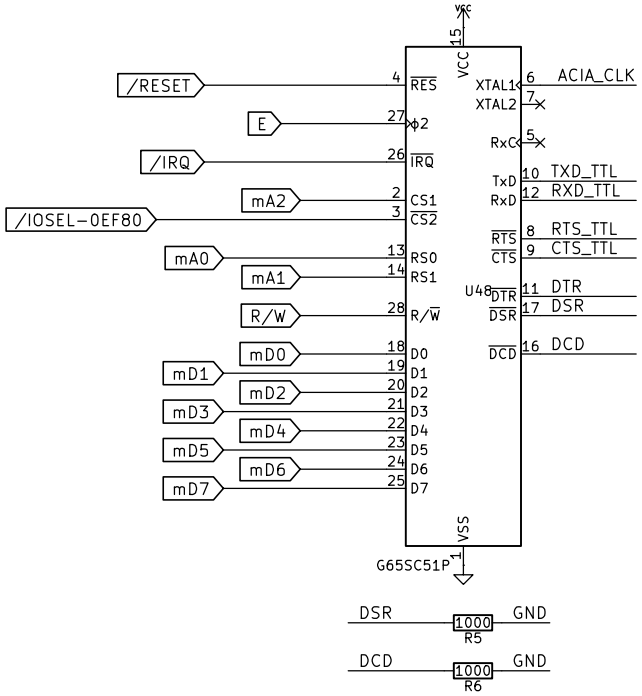


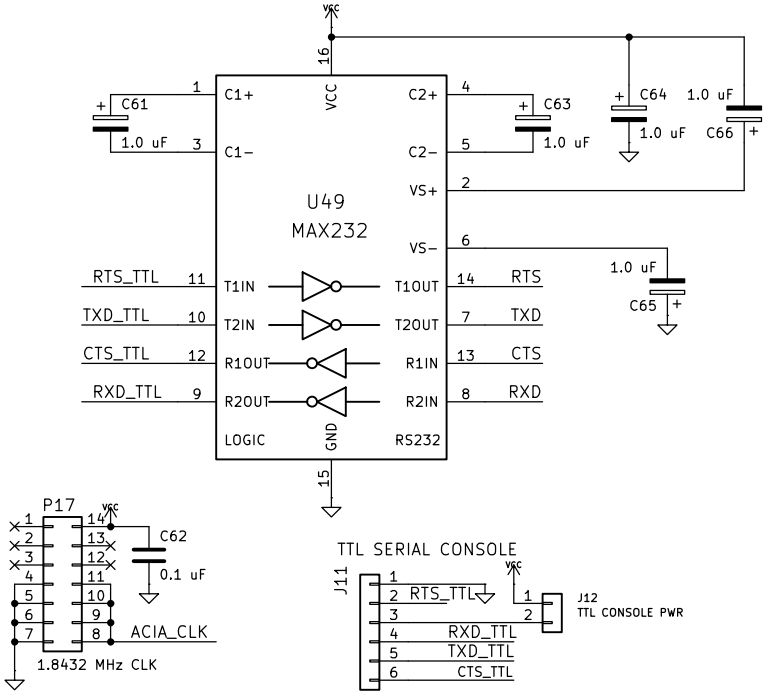
Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

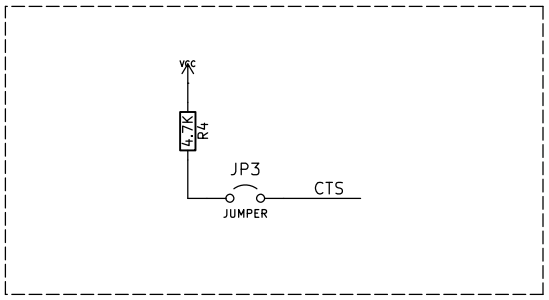
Sheet: /RTC/
File: RTC.kicad_sch

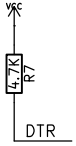
Title: 6809PC

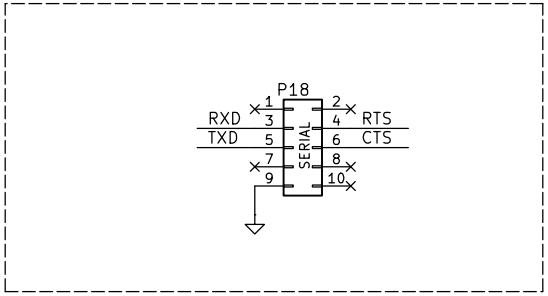
Size: A	Date: 2025–05–12	**Rev: 001**
KiCad E.D.A. 8.0.6		Id: 13/12











CTS is an inverted signal on the RS-232 port. So it is really /CTS. To assert the signal, it must be tied to SPACE, which is a + RS-232 voltage. (MARK, or true, is a - RS-232 voltage.)

Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

Sheet: /ACIA/
File: ACIA.kicad_sch

Title: 6809PC

Size: A	Date: 2025-05-12	**Rev: 001**
KiCad E.D.A. 8.0.6		Id: 14/12