ISA bus

File: ECBbus.kicad_sch

Decoder

File: Decoder.kicad_sch

MMU four

File: MMU-4.kicad_sch

RTC

File: RTC.kicad_sch

Power

File: Power.kicad_sch

CPU 6809

File: cpu-6809.kicad_sch

Spare

File: Spare.kicad_sch

ACIA

File: ACIA.kicad_sch

Memory Map

File: memory-map.kicad_sch

IO

File: IO.kicad_sch

Reset

File: Reset.kicad_sch

Sheet: /
File: 6809PC-6U.kicad_sch

Title: 6809PC

Size: A	Date: 2025-06-20	Rev: 004
KiCad E.D.A. 8.0.6		Id: 1/12

U1C 74LS04
U4A 74LS86
mA19 == RAM-A19
mA19

U5B 74LS02
to DECODER sheet
SHADOW-IO

mA12
U1D 74LS04
U5C 74LS02
SHADOW-ROM
U17C 74LS14
U7A 74LS32
/ONBOARDROM

U11 27C256
mA0 A0 D0 mD0
mA1 A1 D1 mD1
mA2 A2 D2 mD2
mA3 A3 D3 mD3
mA4 A4 D4 mD4
mA5 A5 D5 mD5
mA6 A6 D6 mD6
mA7 A7 D7 mD7
mA8 A8
mA9 A9
mA10 A10
mA11 A11
A12
A13
PULLUP2 A14
VPP
/RD CE
OE GND

mA19 P0
mA18 P1
mA17 P2
mA16 P3
U3
mA15 P4
mA14 P5
mA13 P6
P7
COMP

/VMA
from CPU sheet

74LS682

PULLUP3
HIGH K1 LOW
ROM SELECT

P=Q 19

/SHADOW
U6A 74LS00
U7B 74LS32

P1 SHADOW ADDR
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q
P>Q

U8 SRAM_512K
mA0 A0 DQ0 mD0
mA1 A1 DQ1 mD1
mA2 A2 DQ2 mD2
mA3 A3 DQ3 mD3
mA4 A4 DQ4 mD4
mA5 A5 DQ5 mD5
mA6 A6 DQ6 mD6
mA7 A7 DQ7 mD7
mA8 A8
mA9 A9
mA10 A10
mA11 A11
mA12 A12
mA13 A13
mA14 A14
mA15 A15
mA16 A16
mA17 A17 CE# /RD
mA18 A18 OE# /ONBOARDRAM
WE# /WR
VSS

I0a O0a mD7
I1a O1a mD6   Reads back the page number
I2a O2a mD5   of the I/O space. The ROM
I3a O3a mD4   boot space is IOpage+1.
I0b O0b mD3
I1b O1b mD2   Furthermore, the IOspace and
I2b O2b mD1   ROMboot space overlay RAM,
I3b O3b mD0   not ROM.
U203b

/MMU-IO-PREFIX-RD
OEa 74LS244
OEb

SHADOW ROM & I/O PREFIX
READBACK (optional)

XM19
XM18   HI-ADDRESS BITS WHEN
XM17   MMU IS DISABLED
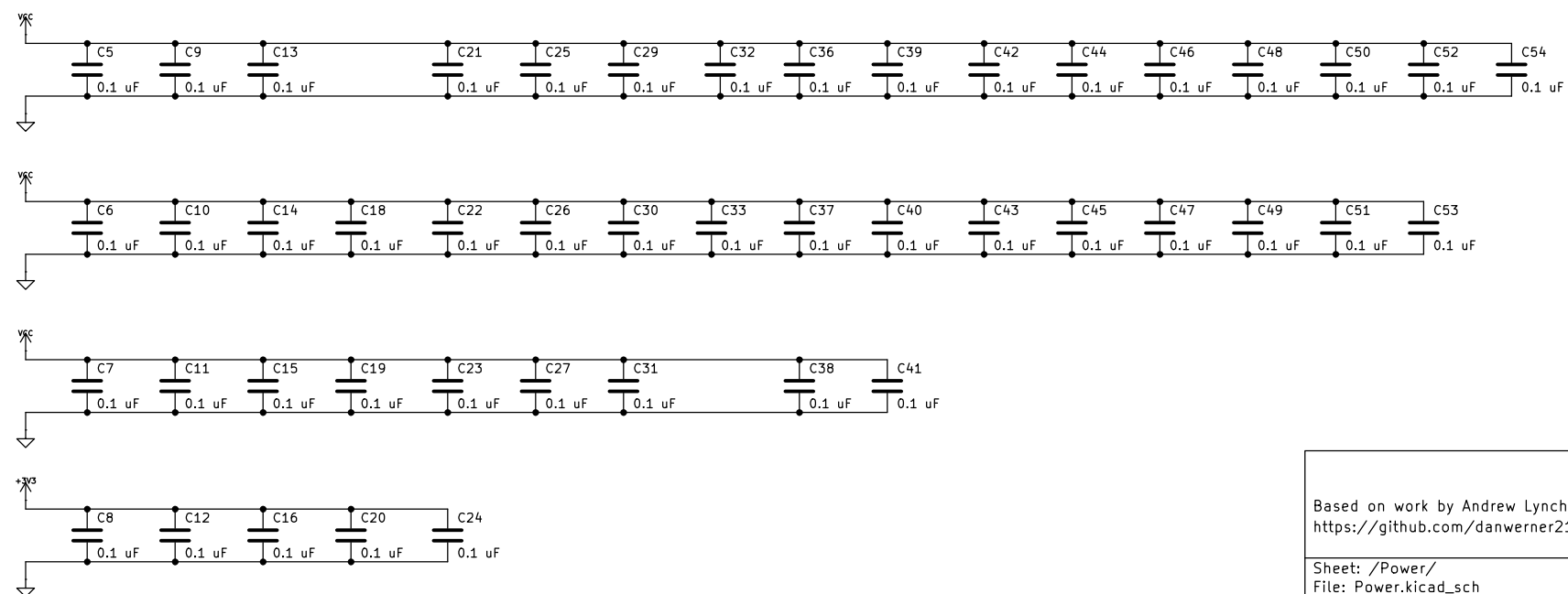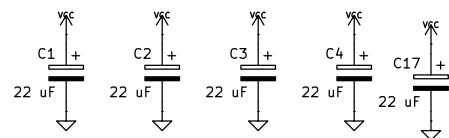XM16

Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

Sheet: /Memory Map/
File: memory-map.kicad_sch
Title: 6809PC
Size: B   Date: 2025-06-20   Rev: 004
KiCad E.D.A. 8.0.6   Id: 4/12

VCC

| U10E 74LS32 | U9E 74LS08 | U15E 74LS08 | U16E 74LS32 | U17G 74LS14 | 74LS06 U18G | U21E 74LS00 | U1G 74LS04 | U6E 74LS00 | U7E 74LS32 | U5E 74LS02 | U4E 74LS86 | 74LS74 U22C |

ATX Power Supply Control Circuit

U12B 74LS74

P11
CONN_10X2

1	2
3	4
5	6
7	8
9	10
11	12
13	14
15	16
17	18
19	20

+3V3

PWR_FLAG

PWR_FLAG
VCC

+5V

PWR_FLAG
-12V

PWR_ON

-5V PWR_FLAG

PWR_FLAG   PWR_FLAG
+12V   5VSB   PG

ATX Connector
PWR_FLAG

5VSB

10k R1
1N4148 D1
R3 10k
1N4148 D2

470 R2

POWER_SW P12
SW1
POWER

74HCT14
U19B

74HCT14
U19A

74HCT14
U19C

U12A
74LS74

PWR_ON

U12C
74LS74

74HCT14
U19G

74HCT14
U19D

74HCT14
U19E

74HCT14
U19F

+ C28
1uF

+ C35
10uF

BYPASS CAPACITORS

VCC

| C5 | C9 | C13 | C21 | C25 | C29 | C32 | C36 | C39 | C42 | C44 | C46 | C48 | C50 | C52 | C54 |
| 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF |

VCC

| C6 | C10 | C14 | C18 | C22 | C26 | C30 | C33 | C37 | C40 | C43 | C45 | C47 | C49 | C51 | C53 |
| 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF |

VCC

| C7 | C11 | C15 | C19 | C23 | C27 | C31 | C38 | C41 |
| 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF |

MOUNTING HOLES

P2	P5
P3	P6
P4	P7
P21	P8
P22	P9
P23	P10

| C1 22 uF | C2 22 uF | C3 22 uF | C4 22 uF | C17 22 uF |

+3V3

| C8 | C12 | C16 | C20 | C24 |
| 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF | 0.1 uF |

Sheet: /Power/
File: Power.kicad_sch
Title: 6809PC
Size: B   Date: 2025-06-20   Rev: 004
KiCad E.D.A. 8.0.6   Id: 6/12

HIGHEST LEVEL I/O ADDRESS DECODE

from Memory Map sheet

SHADOW-IO

mA11   13   U1F 12   74LS04

4   U21B 6   74LS00
5

/VMA   9   U7C 8   74LS32
10

/IORQ

to ECB bus drivers
Z80 signal

/ONBOARDIO

U23
74LS688

SHADOW-IO   2   P0
4   P1
mA11   6   P2
mA10   8   P3
mA9   11   P4
mA8   13   P5
mA7   15   P6
17   P7

VCC   20

P=R   19

3   R0
5   R1
7   R2
9   R3
12   R4
14   R5
16   R6
18   R7

/VMA   1   G

GND   10

74LS138

4   E1
5   E2
6   E3

mA6   3   A2
mA5   2   A1
mA4   1   A0

GND   8

O7   7   /IOSEL-0EFF0
O6   9   /IOSEL-0EFE0
O5   10   /IOSEL-0EFD0
O4   11   /IOSEL-0EFC0
O3   12   /IOSEL-0EFB0
O2   13   /IOSEL-0EFA0
O1   14   /IOSEL-0EF90
O0   15   /IOSEL-0EF80

VCC

16   U24

I/O DEVICE SUBSYSTEM ADDRESS
ASSIGNMENTS:

Range	Assignment
$EFF0 – $EFFF	available
$EFE0 – $EFEF	MMU Registers (3)
$EFD0 – $EFDF	MMU Task Map (16)
$EFC0 – $EFCF	available
$EFB0 – $EFBF	available
$EFA0 – $EFAF	available
$EF90 – $EF9F	RTC (16)
$EF80 – $EF8F	ACIA (4)

Sheet: /Decoder/
File: Decoder.kicad_sch

Title: 6809PC

Size: B   Date: 2025-06-20   **Rev: 004**
KiCad E.D.A. 8.0.6   Id: 7/12

This schematic sheet contains the following labels and component designators:

Top right connector (RR1, 2200):
- B_/INT — pin 2, 1 — VCC
- PULLUP1 — pin 3
- PULLUP2 — pin 4
- PULLUP3 — pin 5
- PG — pin 6
- 7
- /RESET — pin 8
- B_/NMI — pin 9
- 10
- R26 4.7K — B_INT

U25 74LS245:
- mD0 (A0, pin 2) — B0 (pin 18) — B_D0
- mD1 (A1, pin 3) — B1 (pin 17) — B_D1
- mD2 (A2, pin 4) — B2 (pin 16) — B_D2
- mD3 (A3, pin 5) — B3 (pin 15) — B_D3
- mD4 (A4, pin 6) — B4 (pin 14) — B_D4
- mD5 (A5, pin 7) — B5 (pin 13) — B_D5
- mD6 (A6, pin 8) — B6 (pin 12) — B_D6
- mD7 (A7, pin 9) — B7 (pin 11) — B_D7
- A->B (pin 1), CE (pin 19), GND (pin 10), VCC (pin 20)
- Read from bus, Low . . . write to bus high.

U9A 74LS08:
- IOR (pin 1), SMEMR (pin 2) — GND (pin 3)

U15D 74LS08:
- /ONBOARDROM (pin 12), /ONBOARDIO (pin 13) — pin 11

U21D 74LS00:
- /ONBOARDRAM (pin 12), pin 13 — /BUS (pin 11)

U7D 74LS32:
- /IORQ (pin 12), /WR (pin 13) — IOW (pin 11)

U16A 74LS32:
- /BUS (pin 1), /WR (pin 2) — SMEMW (pin 3)

U16B 74LS32:
- /IORQ (pin 4), /RD (pin 5) — IOR (pin 6)

U16C 74LS32:
- /BUS (pin 9), /RD (pin 10) — SMEMR (pin 8)

U18F 74LS06:
- B_INT (pin 13) — B_/INT (pin 12)

P13 / C56 0.1 uF:
- BUSCLK
- 14.31818 MHz CLK

U26 74LS245:
- mA0 (A0, pin 2) — B0 (pin 18) — B_A0
- mA1 (A1, pin 3) — B1 (pin 17) — B_A1
- mA2 (A2, pin 4) — B2 (pin 16) — B_A2
- mA3 (A3, pin 5) — B3 (pin 15) — B_A3
- mA4 (A4, pin 6) — B4 (pin 14) — B_A4
- mA5 (A5, pin 7) — B5 (pin 13) — B_A5
- mA6 (A6, pin 8) — B6 (pin 12) — B_A6
- mA7 (A7, pin 9) — B7 (pin 11) — B_A7
- /BUSAK — A->B (pin 1), CE (pin 19), GND (pin 10)

U27 74LS245:
- mA8 (A0, pin 2) — B0 (pin 18) — B_A8
- mA9 (A1, pin 3) — B1 (pin 17) — B_A9
- mA10 (A2, pin 4) — B2 (pin 16) — B_A10
- mA11 (A3, pin 5) — B3 (pin 15) — B_A11
- mA12 (A4, pin 6) — B4 (pin 14) — B_A12
- mA13 (A5, pin 7) — B5 (pin 13) — B_A13
- mA14 (A6, pin 8) — B6 (pin 12) — B_A14
- mA15 (A7, pin 9) — B7 (pin 11) — B_A15
- /BUSAK — A->B (pin 1), CE (pin 19), GND (pin 10)

U28 74LS245:
- mA16 (A0, pin 2) — B0 (pin 18) — B_A16
- mA17 (A1, pin 3) — B1 (pin 17) — B_A17
- mA18 (A2, pin 4) — B2 (pin 16) — B_A18
- mA19 (A3, pin 5) — B3 (pin 15) — B_A19
- IOR (A4, pin 6) — B4 (pin 14) — B_IOR
- IOW (A5, pin 7) — B5 (pin 13) — B_IOW
- SMEMR (A6, pin 8) — B6 (pin 12) — B_SMEMR
- SMEMW (A7, pin 9) — B7 (pin 11) — B_SMEMW
- /BUSAK — A->B (pin 1), CE (pin 19), GND (pin 10)

Bottom:
- 1000 R8 — /AEN

SPARE

U21C
74LS00

U6D
74LS00
12
13
11

U10B
74LS32
9
10
8
U4C
74LS86

U5D
74LS02
11
12
13

U16D
74LS32
12
13
11

74LS06
1
2
U18A

74LS06
3
4
U18B

74LS06
5
6
U18C

U10A
74LS32
1
2
3

U4D
74LS86
12
13
11

U4B
74LS86
4
5
6

U9B
74LS08
4
5
6

U9C
74LS08
9
10
8

U9D
74LS08
12
13
11

U17E
74LS14
11
10

U17F
74LS14
13
12

U22A
74LS74
D
C
Q
Q

Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

Sheet: /Spare/
File: Spare.kicad_sch

Title: 6809PC

Size: B   Date: 2025-06-20   Rev: 004
KiCad E.D.A. 8.0.6   Id: 9/12

DS1233

U29

GND 1
VCC 2
     3

VCC

U17D
9   8
74LS14   RESET

/RESET

C57

SW2

RESET

JP1
1
2 JUMPER

0.01 uF

Sheet: /Reset/
File: Reset.kicad_sch

Title: 6809PC

| Size: A | Date: 2025-06-20 | **Rev: 004** |
| KiCad E.D.A. 8.0.6 | | Id: 10/12 |

Sheet: /CPU 6809/
File: cpu-6809.kicad_sch

Title: 6809PC

Size: B | Date: 2025-06-20 | Rev: 004
KiCad E.D.A. 8.0.6 | | Id: 11/12

CPU_D0
CPU_D1
CPU_D2
CPU_D3
CPU_D4
CPU_D5
CPU_D6
CPU_D7

/RESET
/NMI
/IRQ
/FIRQ

DMA
/HALT
MRDY
GND

MC68B09
U33

LA0
LA1
LA2
LA3
LA4
LA5
LA6
LA7
LA8
LA9
LA10
LA11
LA12
LA13
LA14
LA15

CPU_R/W
CPU_BS
CPU_BA
CPU_E
CPU_Q

CLK

UNIVERSAL
OSCILLATOR
P14
16.000Mhz
VCC
C58
0.1 uF

U30
74LS163

P15
CPU CLOCK SPEED

8Mhz 1-2
4Mhz 3-4
2Mhz 5-6
1Mhz 7-8

8MHZ
4MHZ
2MHZ
1MHZ

/HALT
MRDY
/NMI
/IRQ
/FIRQ
/MMU-DISABLE
/MMU-CLR-TASK-REG
CPU_BS
22K
RR2
DMA

U17B
74LS14
BUSAK
/BUSAK

BA has insufficient drive for the whole board

E
U6B
74LS00
CPU_/RD

CPU_R/W
U1A
74LS04
W/R

CPU_E
U6C
74LS00
CPU_/WR

CPU_BA
CPU_BS
U1E
74LS04
U21A
74LS00
/INTA

/MMU-DISABLE
/MMU-CLR-TASK-REG

CPU_/RD
CPU_/WR
CPU_R/W

CPU_E
CPU_Q
U5A
74LS02

CPU_Q
U17A
74LS14

BUSAK

U-74LS244
/VMA
/RD
/WR
R/W
BUSALE
E

Bus Address Latch Enable. The address bus is latched on the rising edge of this signal.

B_/NMI
CPU_E
B_/INT

U18D
74LS06
B_/CLK
/NMI

U18E
74LS06
/IRQ

U31
74LS240

CPU_D7
CPU_D6
CPU_D5
CPU_D4
CPU_D3
CPU_D2
CPU_D1
CPU_D0

U32
74LS245

mD0
mD1
mD2
mD3
mD4
mD5
mD6
mD7

R/W
BUSAK

Address Bus (tri-state) for all CPU's

Used during MMU
setup/loading

Used during MMU
mapping operation

rev. 011 -- change from
/MMU-MAP-RW to MMU-ENABLE

U37 74LS157

U38 74LS374

Optional TASK SETUP register

U40 SRAM-32K

SRAM - skinny 28-pin DIP
35ns 8K or 32K; e.g.,
any Cypress or JEDEC
part.

U43 74LS257

U44 74LS257

ECB bus
signal
BUSAK

MMU-ENABLE

U45 74LS244

U46 74LS244

CPU_Q
CPU_E
CPU_R/W

Q
E
R/W

U35 74LS174

Active TASK register

U39 74LS244

U1B 74LS04   /MMU-MAP-RW

/MMU-TASK-RD

U24 74LS245

U34 74LS244

Read active TASK register
and MMU-ENABLE status

MMU-ENABLE

/MMU-MAP-WR

Select for programming the MMU map

/MMU-MAP-RD
/OE

U15B 74LS02

/VMA

/MMU-ENB-WR   mD0

U22B 74LS74

U15B 74LS08   /MMU-DISABLE
/RESET

MMU enable/disable

U42 74LS138

IOSEL-0EFE0
E

TC

/MMU-IO-PREFIX-RD
/MMU-TASK-RD
/MMU-ENB-WR
/MMU-TASK-SETUP-WR
/MMU-TASK-WR

R/W
mA1
mA0

/RESET

/MMU-CLR-TASK-REG

U15C 74LS08

Patch from V1.0 to V1.1
* Connect U42 pin 9 to Slots pin 27
* LS138 U42 and U24 have miswired power
* U24 Pin 6 should be VCC not GND

U10C 74LS32
CPU_/WR
/MMU-MAP-WR

U10D 74LS32
IOSEL-0EFD0   /MMU-MAP-RW
/MMU-MAP-RD

CPU_/RD

VCC

D3
D

D4
D

PWR_FLAG

P16

CONN_4

1
2
3
4

SCap1

C59
15pf

C60
15pf

PWR_FLAG

External Battery connector (2.5–3.6v)
or soldered Super Cap 0.1–1.0 Farad

(e.g., Jameco 142949, 0.22F)

U47
M6242

RTC_OSC
32.768 KHz

X1

/IOSEL-0EF90

BUSALE

mA0
mA1
mA2
mA3

CPU_/RD

1 STDP   VCC 18
2 CS0   XT1 17
3 ALE   XT 16
4 A0   CS1 15
5 A1   D0 14
6 A2   D1 13
7 A3   D2 12
8 RD   D3 11
9 GND   WR 10

M6242

PULLUP1

mD0
mD1
mD2
mD3

CPU_/WR

Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

Sheet: /RTC/
File: RTC.kicad_sch

Title: **6809PC**

| Size: A | Date: 2025–06–20 | Rev: 004 |
| KiCad E.D.A. 8.0.6 | | Id: 13/12 |

CTS is an inverted signal on the RS-232 port. So it is
really /CTS. To assert the signal, it must be tied to
SPACE, which is a + RS-232 voltage. (MARK, or
true, is a - RS-232 voltage.)

TTL SERIAL CONSOLE

1.8432 MHz CLK

Sheet: /ACIA/
File: ACIA.kicad_sch

Title: *6809PC*

Size: A	Date: 2025-06-20	Rev: 004
KiCad E.D.A. 8.0.6		Id: 14/12