ISA bus

File: ECBbus.kicad_sch

Decoder

File: Decoder.kicad_sch

MMU four

File: MMU-4.kicad_sch

RTC

File: RTC.kicad_sch

Power

File: Power.kicad_sch

CPU 6809

File: cpu-6809.kicad_sch

Spare

File: Spare.kicad_sch

ACIA

File: ACIA.kicad_sch

Memory Map

File: memory-map.kicad_sch

IO

File: IO.kicad_sch

Reset

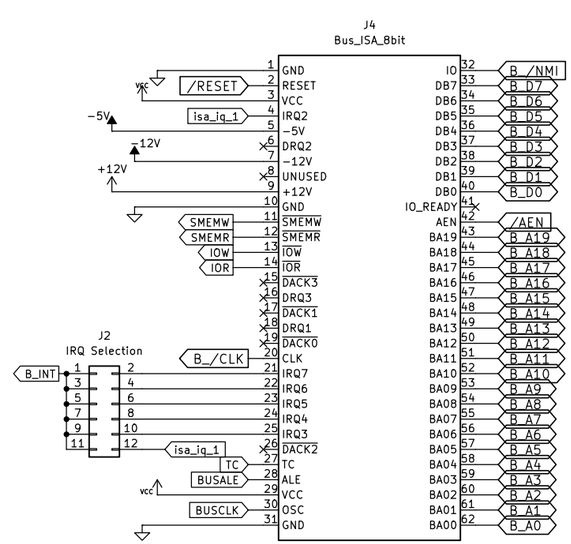
File: Reset.kicad_sch

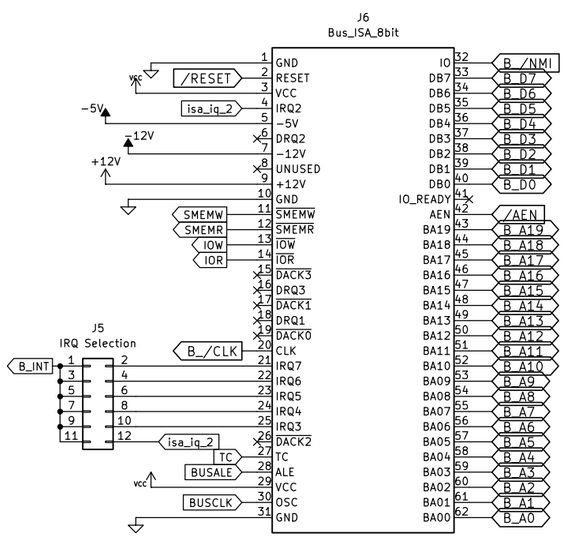
Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

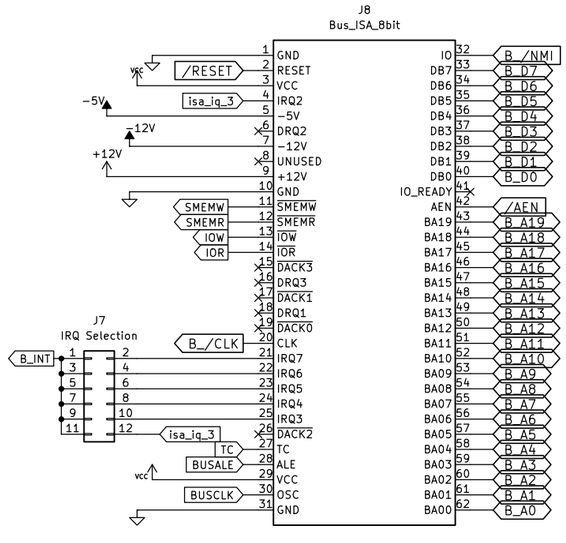
Sheet: /
File: 6809PC-6U.kicad_sch

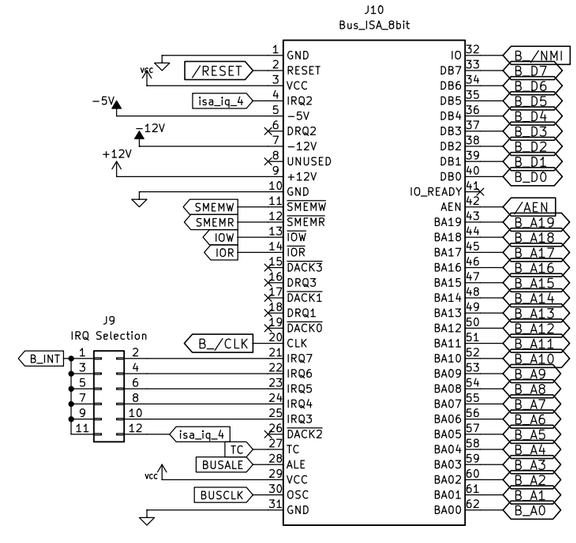
Title: 6809PC

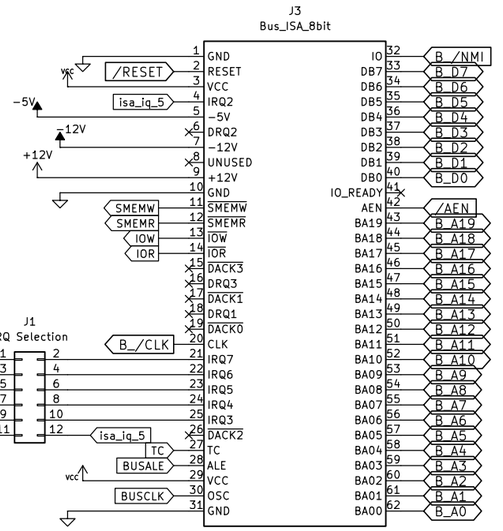
Size: A	Date: 2025-05-17	**Rev: 002**
KiCad E.D.A. 8.0.6		Id: 1/12

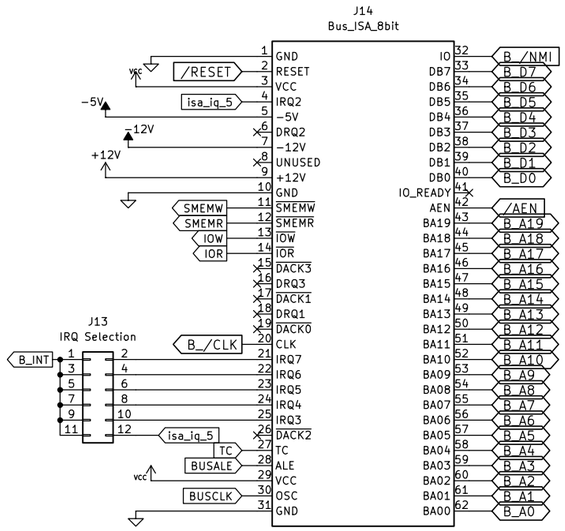


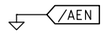












Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

Sheet: /ISA bus/
File: ECBbus.kicad_sch

Title: 6809PC

Size: USLedger	Date: 2025-05-17	**Rev: 002**
KiCad E.D.A. 8.0.6		Id: 2/12

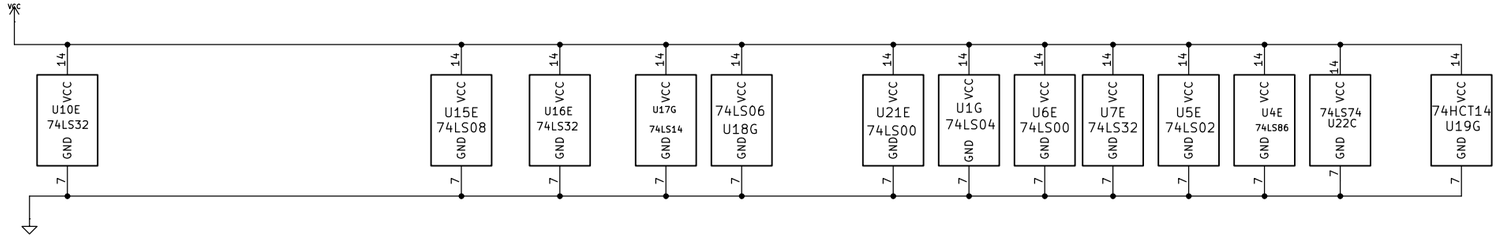
U1C
74LS04
U4A
74LS86
mA19 == RAM-A19
mA19
U1D
74LS04
mA12
U5B
74LS02
U5C
74LS02
SHADOW-ROM
to DECODER sheet
SHADOW-IO
U7A
74LS32
/VMA
from CPU sheet
U6A
74LS00
U7B
74LS32
/SHADOW
U9
27C64
mA0
mA1
mA2
mA3
mA4
mA5
mA6
mA7
mA8
mA9
mA10
mA11
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
VCC
D0
D1
D2
D3
D4
D5
D6
D7
mD0
mD1
mD2
mD3
mD4
mD5
mD6
mD7
PULLUP2
PGM
VPP
CE
OE
/RD
GND
PULLUP3
HIGH
K1
LOW
ROM SELECT
U3
COMP
74LS682
P
Q
P=Q
P>Q
VCC
GND
mA19
mA18
mA17
mA16
mA15
mA14
mA13
P0
P1
P2
P3
P4
P5
P6
P7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
P4
SHADOW ADD
U2
74LS244
I0a
I1a
I2a
I3a
I0b
I1b
I2b
I3b
O0a
O1a
O2a
O3a
O0b
O1b
O2b
O3b
OEa
OEb
/MMU-IO-PREFIX-RD
Reads back the page number of the I/O space. The ROM boot space is IOpage+1.
Furthermore, the IOspace and ROMboot space overlay RAM, not ROM.
SHADOW ROM & I/O PREFIX READBACK (optional)
XM19
XM18
XM17
XM16
HI-ADDRESS BITS WHEN MMU IS DISABLED
U8
SRAM_512K
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
CE#
OE#
WE#
/WR
VSS

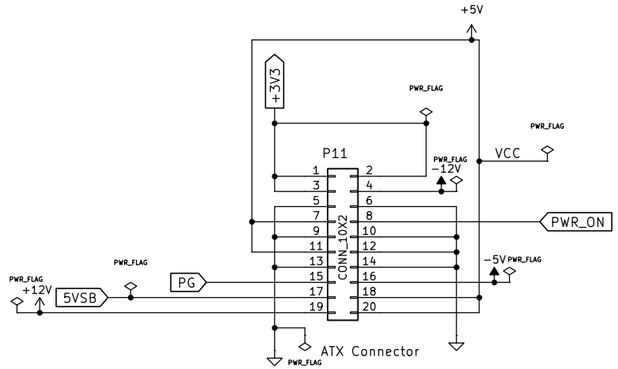
Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

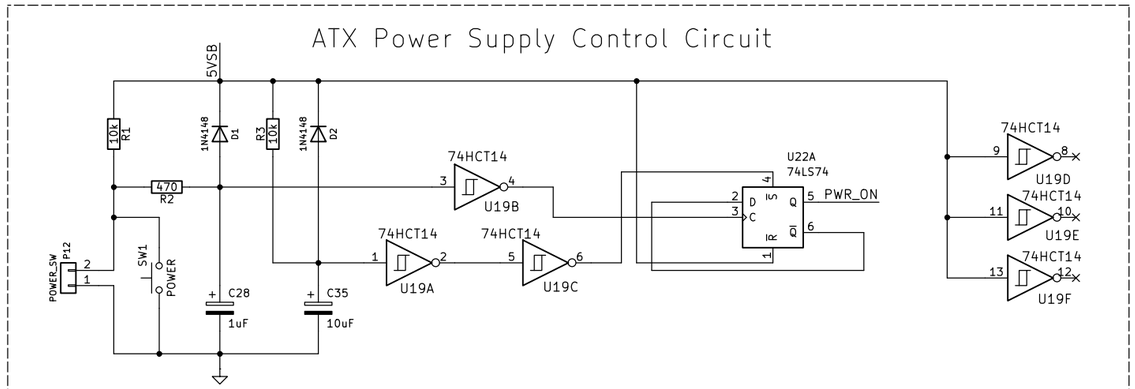
Sheet: /Memory Map/
File: memory-map.kicad_sch

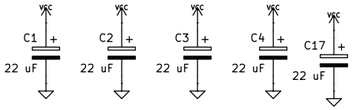
Title: 6809PC

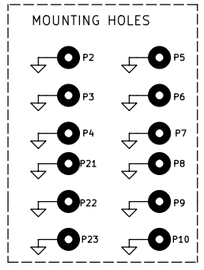
Size: B | Date: 2025-05-17 | **Rev: 002**
KiCad E.D.A. 8.0.6 | Id: 4/12



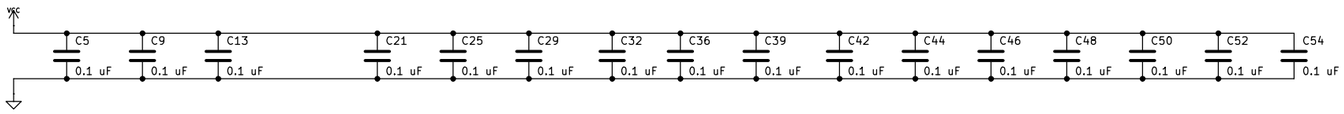


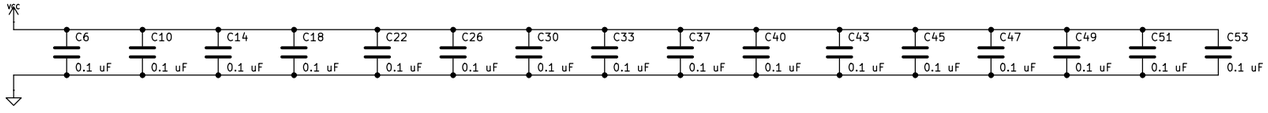


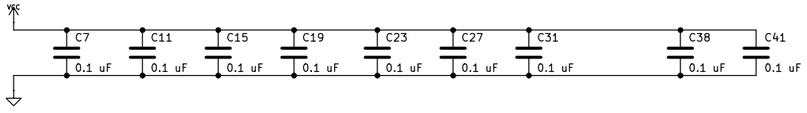


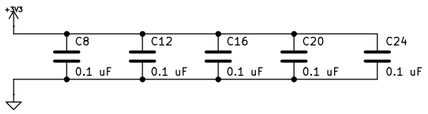


BYPASS CAPACITORS









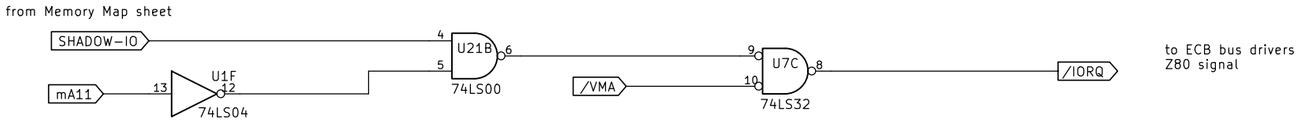
Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

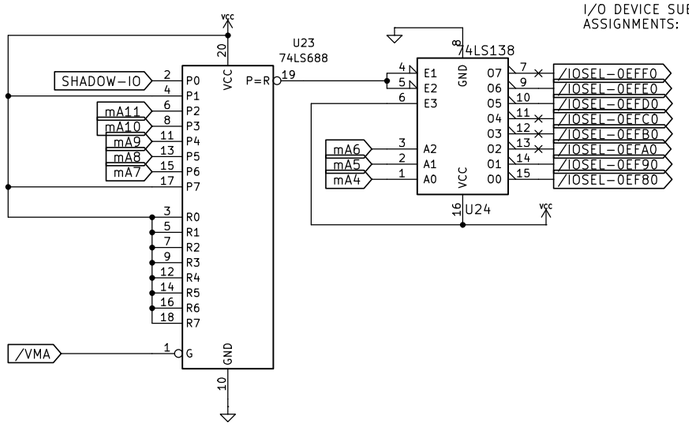
Sheet: /Power/
File: Power.kicad_sch

Title: 6809PC

Size: B	Date: 2025-05-17	**Rev: 002**
KiCad E.D.A. 8.0.6		Id: 6/12

HIGHEST LEVEL I/O ADDRESS DECODE





I/O DEVICE SUBSYSTEM ADDRESS ASSIGNMENTS:

$EFF0 – $EFFF	available	
$EFE0 – $EFEF	MMU Registers (3)	
$EFD0 – $EFDF	MMU Task Map (16)	
$EFC0 – $EFCF	available	
$EFB0 – $EFBF	available	
$EFA0 – $EFAF	available	
$EF90 – $EF9F	RTC (16)	
$EF80 – $EF8F	ACIA (4)	

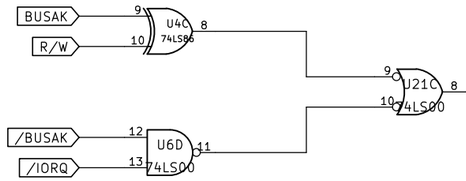
Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

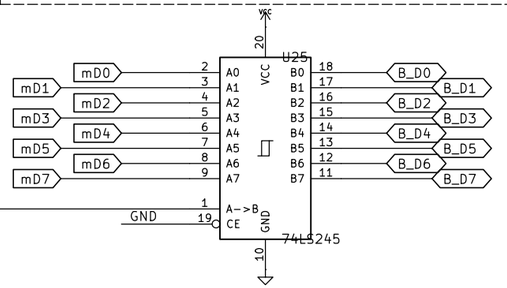
Sheet: /Decoder/
File: Decoder.kicad_sch

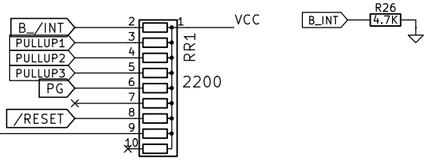
Title: 6809PC

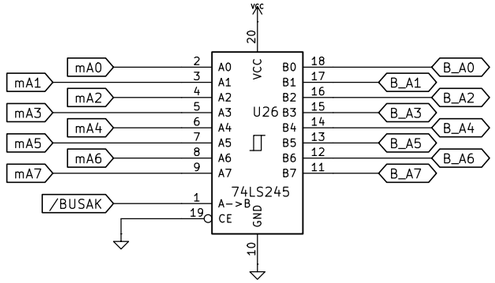
Size: B	Date: 2025-05-17	**Rev: 002**
KiCad E.D.A. 8.0.6		Id: 7/12

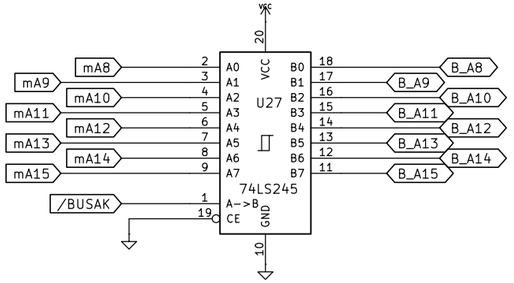
rev. 011: All signal equivalences are DELETED!!!

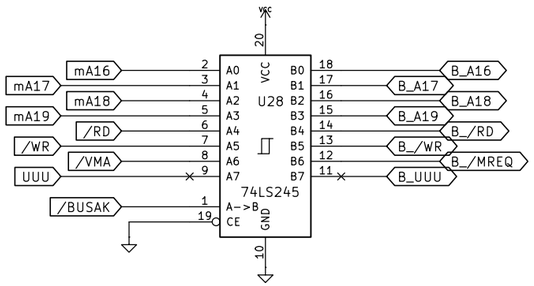


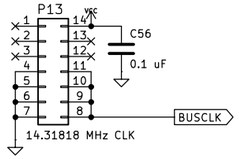


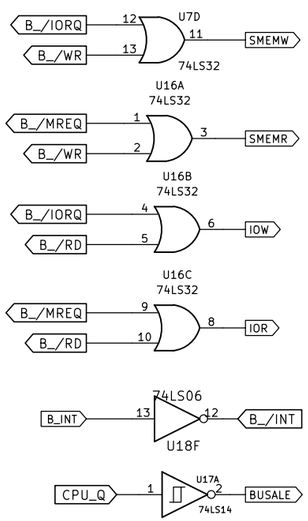












Bus Address Latch Enable. The address bus is latched on the rising edge of this signal.

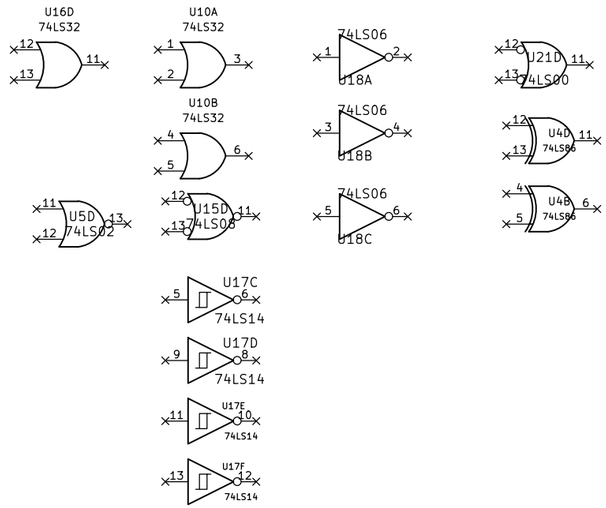
Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

Sheet: /IO/
File: IO.kicad_sch

Title: 6809PC

Size: B	Date: 2025-05-17	**Rev: 002**
KiCad E.D.A. 8.0.6		Id: 8/12

SPARE



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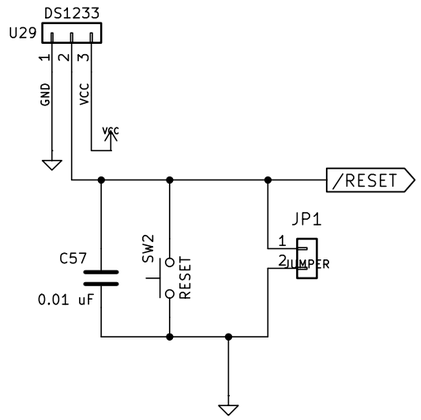
Sheet: /Spare/
File: Spare.kicad_sch

Title: 6809PC

Size: B	Date: 2025-05-17	**Rev: 002**
KiCad E.D.A. 8.0.6		Id: 9/12

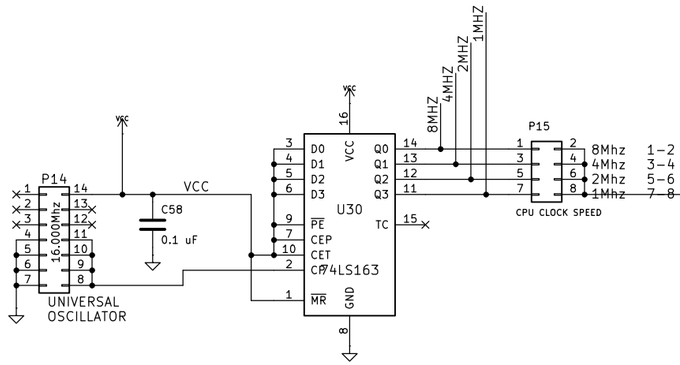


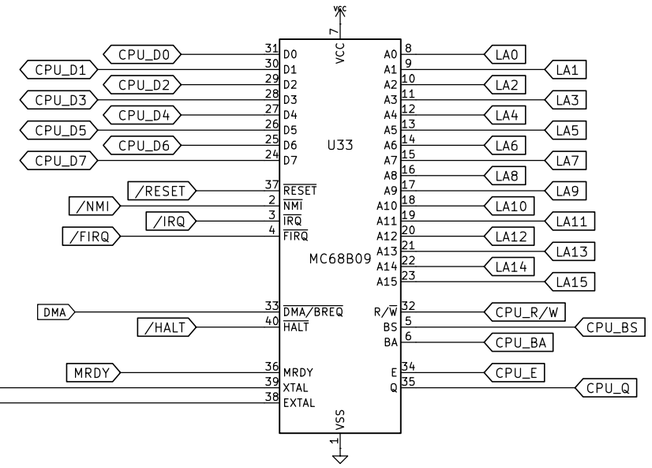
Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

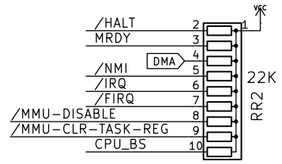
Sheet: /Reset/
File: Reset.kicad_sch

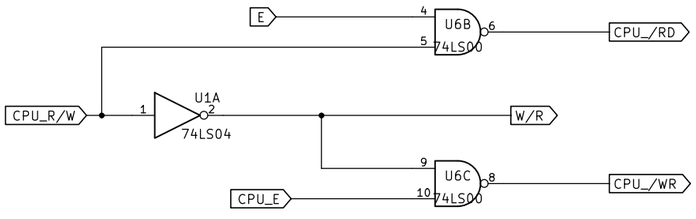
Title: 6809PC

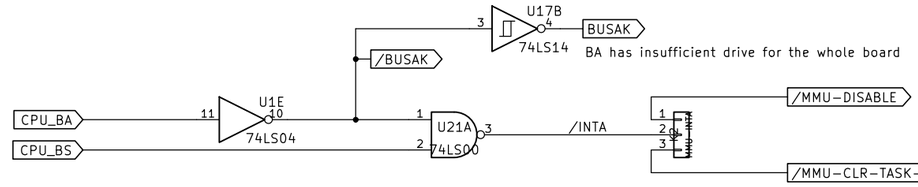
Size: A	Date: 2025-05-17	**Rev: 002**
KiCad E.D.A. 8.0.6		Id: 10/12

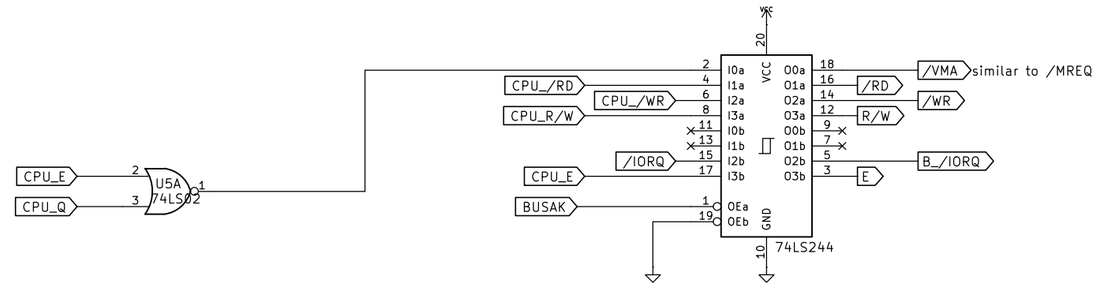


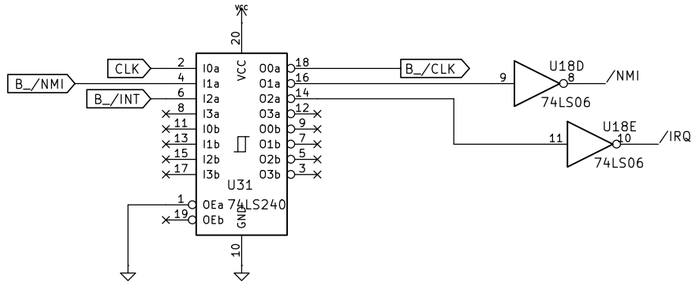


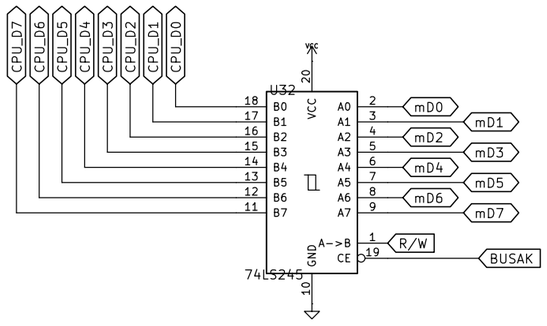












Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

Sheet: /CPU 6809/
File: cpu-6809.kicad_sch

Title: 6809PC

Size: B	Date: 2025-05-17	**Rev: 002**
KiCad E.D.A. 8.0.6		Id: 11/12

Used during MMU setup/loading

Used during MMU mapping operation

rev. 011 -- change from /MMU-MAP-RW to MMU-ENABLE

Optional TASK SETUP register

Active TASK register

Read active TASK register and MMU-ENABLE status

SRAM-32K

SRAM - skinny 28-pin DIP 35ns 8K or 32K; e.g., any Cypress or JEDEC part.

Select for programming the MMU map

Valid Memory Address

MMU enable/disable

ECB bus signal

Address Bus (tri-state) for all CPU's

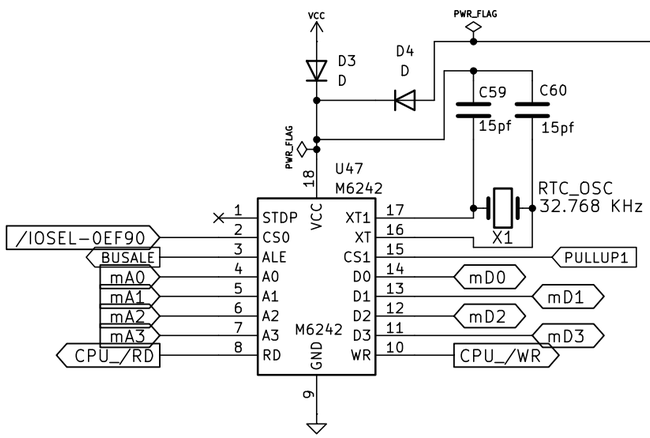
Patch from V1.0 to V1.1
*** Connect U42 pin 9 to Slots pin 27**
*** LS138 U42 and U24 have miswired power**
*** U24 Pin 6 should be VCC not GND**

Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

Sheet: /MMU four/
File: MMU-4.kicad_sch

Title: 6809PC

Size: B	Date: 2025-05-17	**Rev: 002**
KiCad E.D.A. 8.0.6		Id: 12/12



Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

Sheet: /RTC/
File: RTC.kicad_sch

Title: 6809PC

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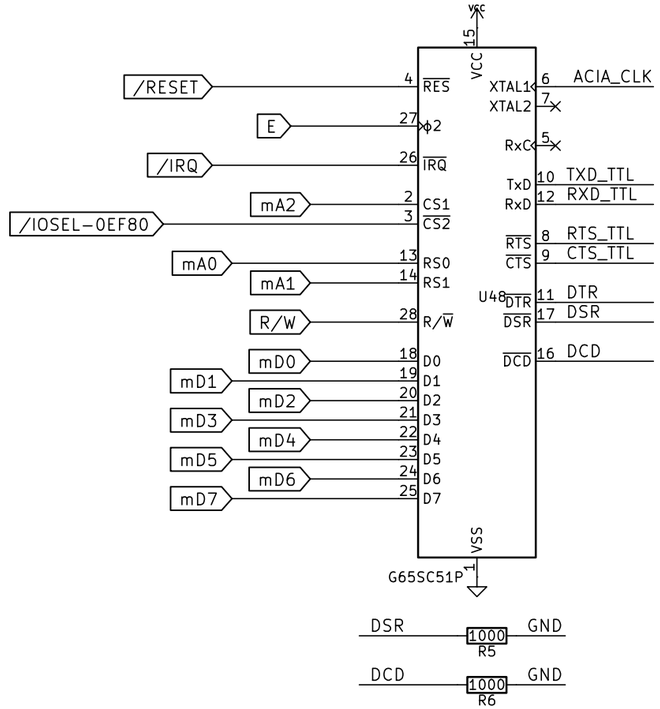

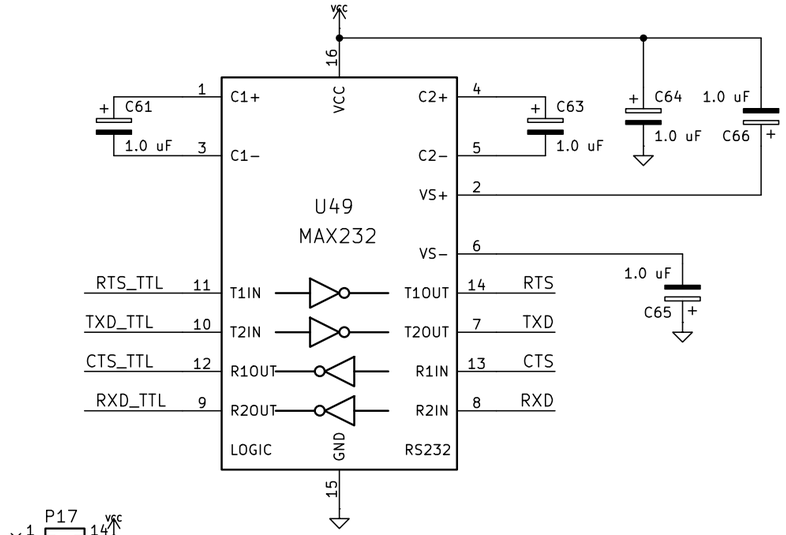

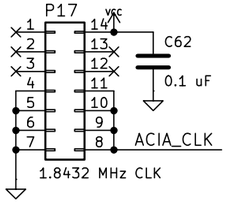

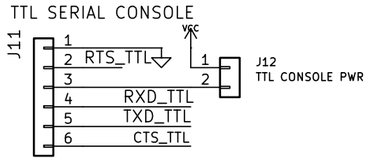

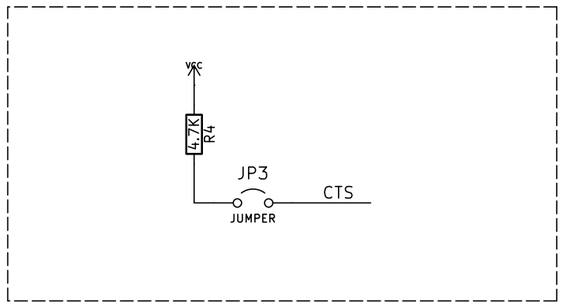

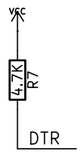

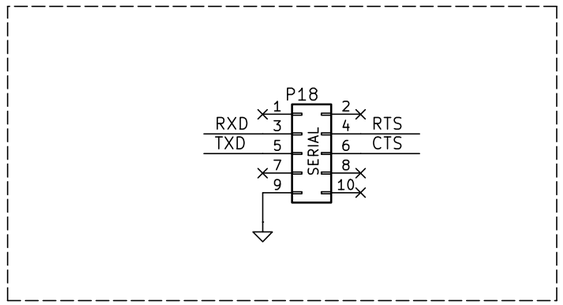

CTS is an inverted signal on the RS−232 port. So it is really /CTS. To assert the signal, it must be tied to SPACE, which is a + RS−232 voltage. (MARK, or true, is a − RS−232 voltage.)

Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

Sheet: /ACIA/
File: ACIA.kicad_sch

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