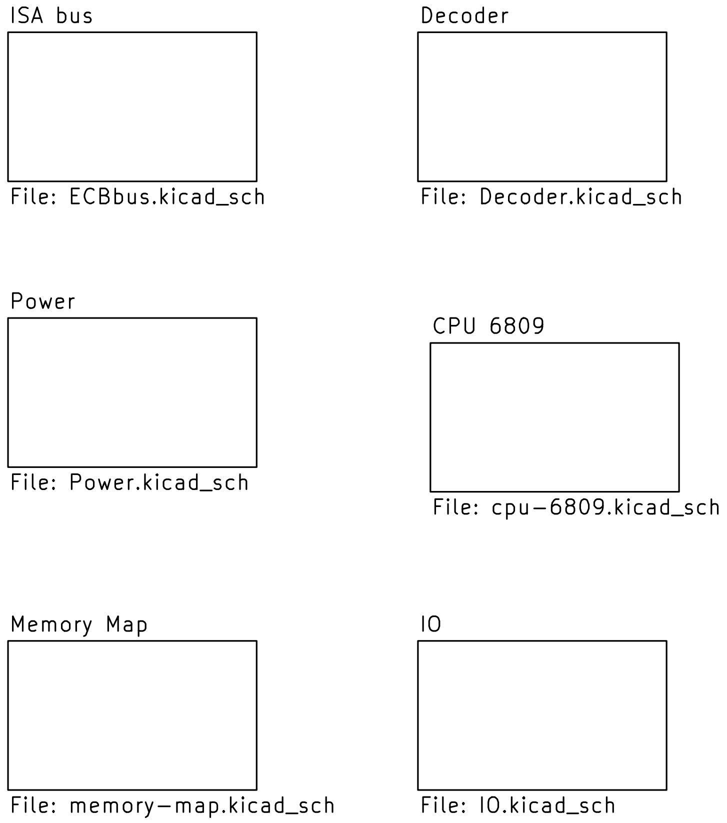
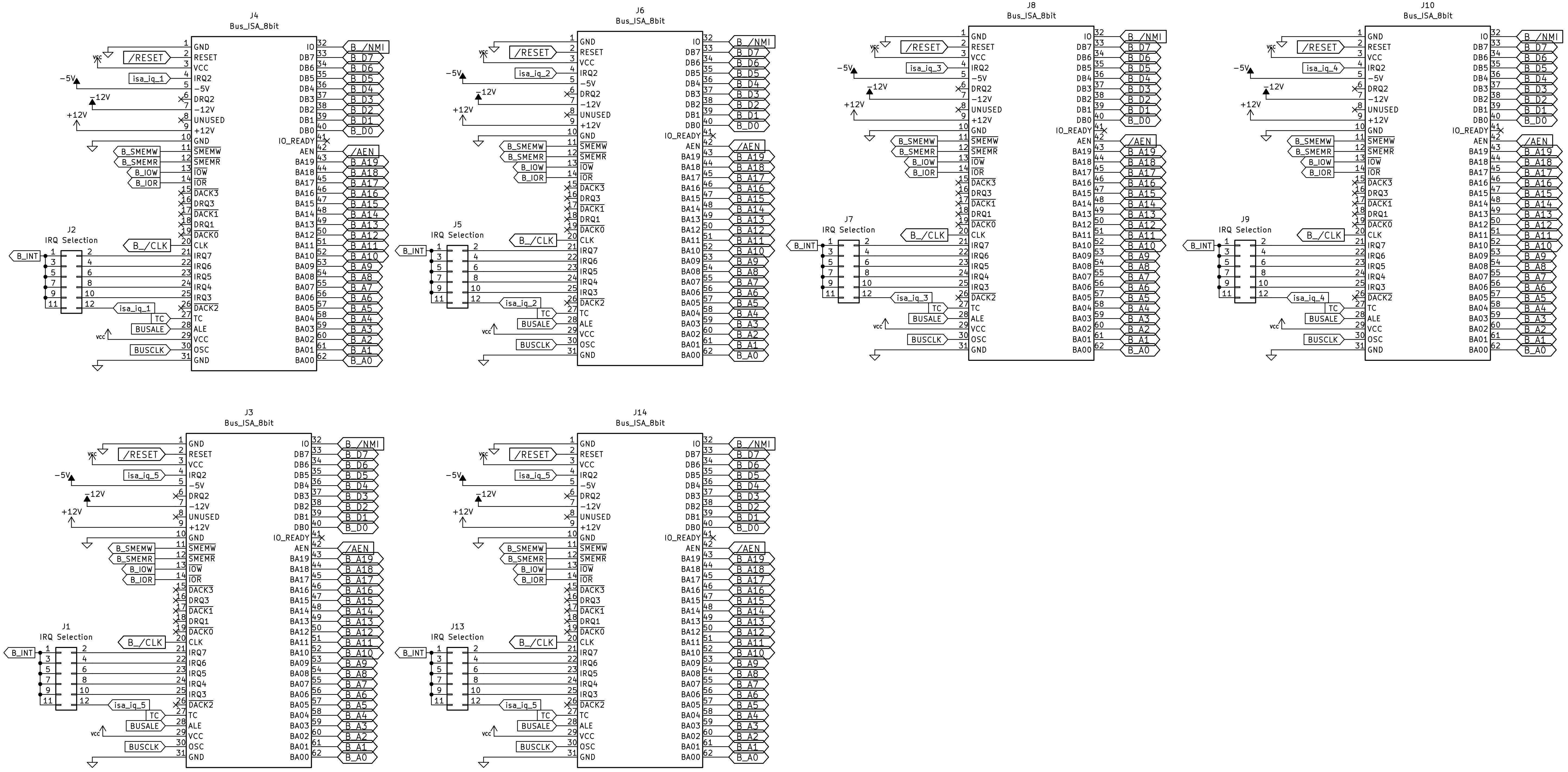

ISA bus
File: ECBbus.kicad_sch
Decoder
File: Decoder.kicad_sch
MMU four
File: MMU-4.kicad_sch
RTC
File: RTC.kicad_sch
Power
File: Power.kicad_sch
CPU 6809
File: cpu-6809.kicad_sch
Spare
File: Spare.kicad_sch
ACIA
File: ACIA.kicad_sch
Memory Map
File: memory-map.kicad_sch
IO
File: IO.kicad_sch
Reset
File: Reset.kicad_sch

Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

Sheet: /
File: 6809PC-6U.kicad_sch

Title: 6809PC

Size: A
Date: 2025-05-17
Rev: 002
KiCad E.D.A. 8.0.6
Id: 1/12

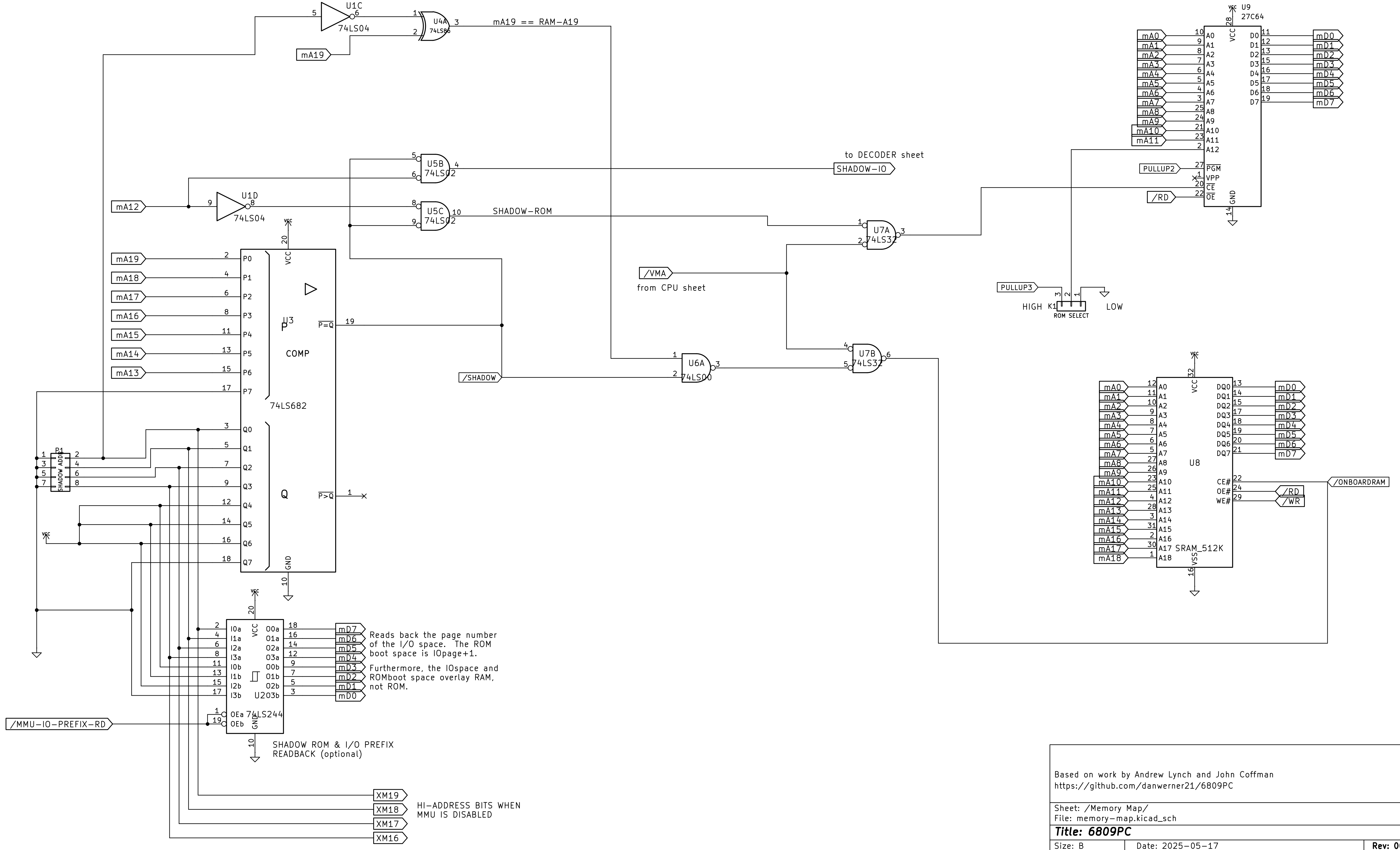

J4
Bus_ISA_8bit
J6
Bus_ISA_8bit
J8
Bus_ISA_8bit
J10
Bus_ISA_8bit
J3
Bus_ISA_8bit
J14
Bus_ISA_8bit
J2
IRQ Selection
J5
IRQ Selection
J7
IRQ Selection
J9
IRQ Selection
J1
IRQ Selection
J13
IRQ Selection
GND
RESET
VCC
IRQ2
-5V
DRQ2
-12V
UNUSED
+12V
SMEMW
SMEMR
IOW
IOR
DACK3
DRQ3
DACK1
DRQ1
DACK0
CLK
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
DACK2
TC
ALE
OSC
IO
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
IO_READY
AEN
BA19
BA18
BA17
BA16
BA15
BA14
BA13
BA12
BA11
BA10
BA09
BA08
BA07
BA06
BA05
BA04
BA03
BA02
BA01
BA00
/RESET
isa_iq_1
isa_iq_2
isa_iq_3
isa_iq_4
isa_iq_5
B_SMEMW
B_SMEMR
B_IOW
B_IOR
B_/CLK
B_INT
BUSALE
BUSCLK
B_/NMI
B_D7
B_D6
B_D5
B_D4
B_D3
B_D2
B_D1
B_D0
/AEN
B_A19
B_A18
B_A17
B_A16
B_A15
B_A14
B_A13
B_A12
B_A11
B_A10
B_A9
B_A8
B_A7
B_A6
B_A5
B_A4
B_A3
B_A2
B_A1
B_A0
VCC
-5V
-12V
+12V

Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

Sheet: /ISA bus/
File: ECBbus.kicad_sch

Title: 6809PC

Size: USLedger | Date: 2025-05-17 | **Rev: 002**
KiCad E.D.A. 8.0.6 | Id: 2/12


U1C
74LS04
U4A
74LS86
mA19
U5B
74LS02
U1D
74LS04
mA12
U5C
74LS02
SHADOW-IO
U7A
74LS32
/VMA
mA19
mA18
mA17
mA16
mA15
mA14
mA13
P0
P1
P2
P3
P4
P5
P6
P7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
VCC
GND
U3
P
COMP
Q
74LS682
P=Q
P>Q
/SHADOW
U6A
74LS00
U7B
74LS32
P1
SHADOW ADDR
U203
74LS244
I0a
I1a
I2a
I3a
I0b
I1b
I2b
I3b
O0a
O1a
O2a
O3a
O0b
O1b
O2b
O3b
OEa
OEb
mD7
mD6
mD5
mD4
mD3
mD2
mD1
mD0
/MMU-IO-PREFIX-RD
XM19
XM18
XM17
XM16
U9
27C64
mA0
mA1
mA2
mA3
mA4
mA5
mA6
mA7
mA8
mA9
mA10
mA11
PULLUP2
/RD
PGM
VPP
CE
OE
PULLUP3
HIGH
K1
ROM SELECT
LOW
U8
SRAM_512K
mA18
CE#
OE#
WE#
/ONBOARDRAM
/RD
/WR
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
VSS

mA19 == RAM-A19

to DECODER sheet

SHADOW-ROM

from CPU sheet

Reads back the page number
of the I/O space. The ROM
boot space is IOpage+1.

Furthermore, the IOspace and
ROMboot space overlay RAM,
not ROM.

SHADOW ROM & I/O PREFIX
READBACK (optional)

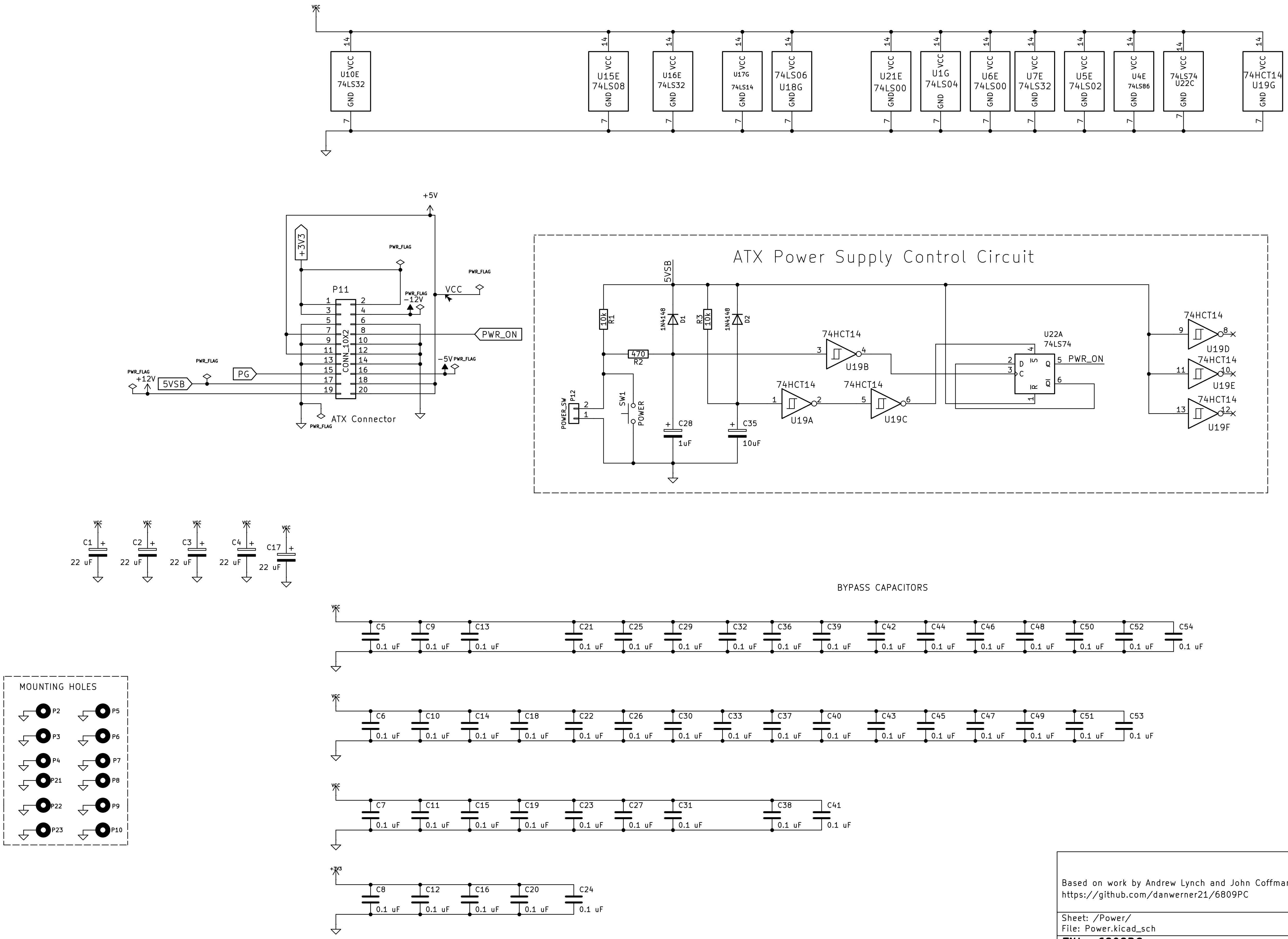
HI-ADDRESS BITS WHEN
MMU IS DISABLED

Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

Sheet: /Memory Map/
File: memory-map.kicad_sch

Title: 6809PC

Size: B	Date: 2025-05-17	Rev: 002
KiCad E.D.A. 8.0.6		Id: 4/12

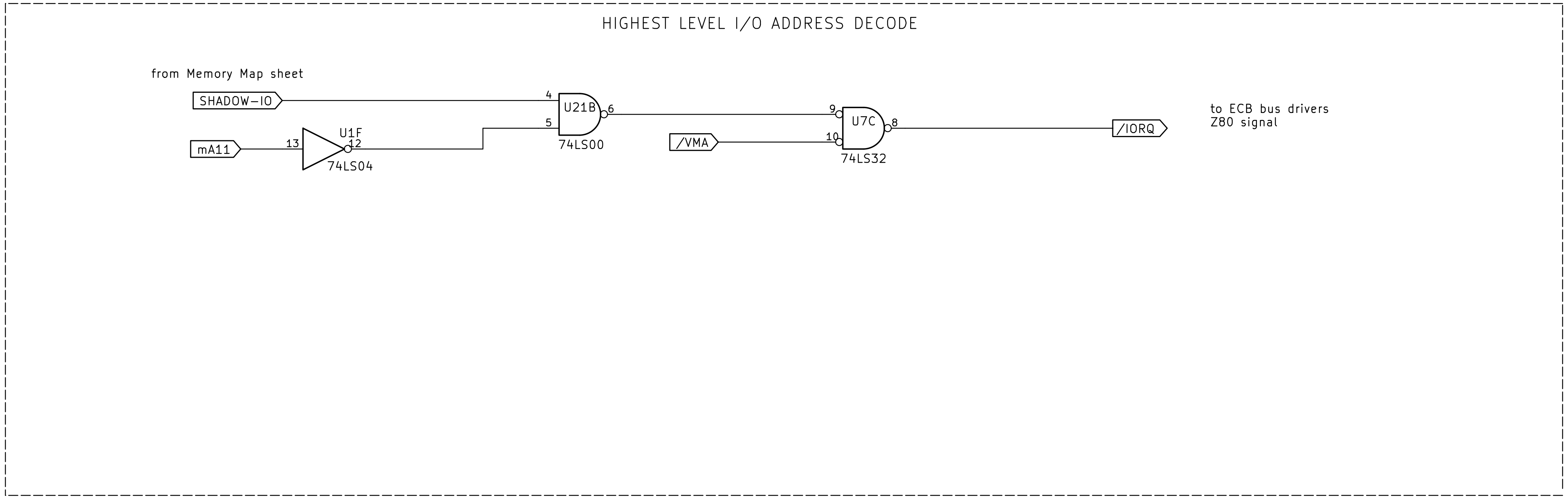

VCC
U10E
74LS32
U15E
74LS08
U16E
74LS32
U17G
74LS14
74LS06
U18G
U21E
74LS00
U1G
74LS04
U6E
74LS00
U7E
74LS32
U5E
74LS02
U4E
74LS86
74LS74
U22C
74HCT14
U19G
14
7
GND
+5V
+3V3
PWR_FLAG
P11
CONN_10X2
-12V
-5V
+12V
5VSB
PG
PWR_ON
ATX Connector
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
ATX Power Supply Control Circuit
5VSB
R1
10k
1N4148
D1
R3
10k
D2
470
R2
POWER_SW
P12
SW1
POWER
C28
1uF
C35
10uF
74HCT14
U19A
U19B
U19C
U22A
74LS74
D
C
S
Q
R
PWR_ON
U19D
U19E
U19F
C1
C2
C3
C4
C17
22 uF
BYPASS CAPACITORS
C5
C9
C13
C21
C25
C29
C32
C36
C39
C42
C44
C46
C48
C50
C52
C54
C6
C10
C14
C18
C22
C26
C30
C33
C37
C40
C43
C45
C47
C49
C51
C53
C7
C11
C15
C19
C23
C27
C31
C38
C41
C8
C12
C16
C20
C24
0.1 uF
MOUNTING HOLES
P2
P3
P4
P21
P22
P23
P5
P6
P7
P8
P9
P10

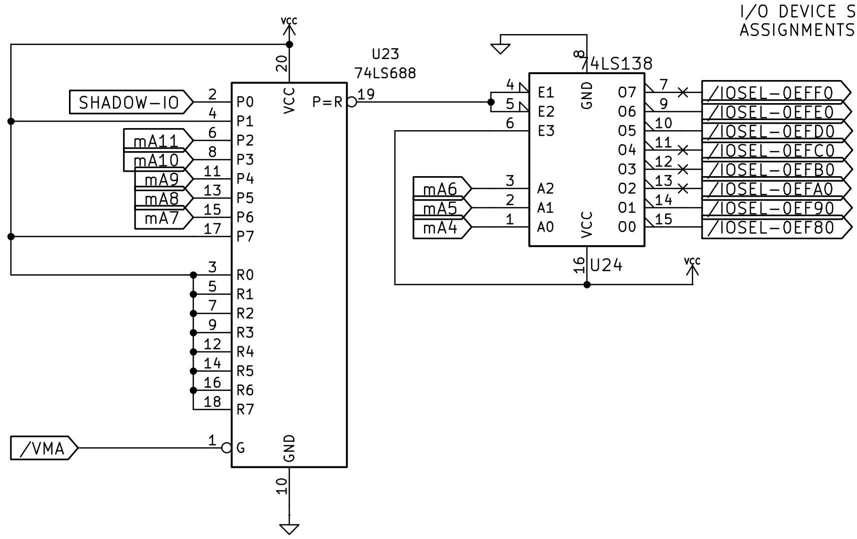
Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

Sheet: /Power/
File: Power.kicad_sch

Title: 6809PC

Size: B
Date: 2025-05-17
Rev: 002
KiCad E.D.A. 8.0.6
Id: 6/12


HIGHEST LEVEL I/O ADDRESS DECODE
from Memory Map sheet
SHADOW-IO
mA11
13
U1F
12
74LS04
4
5
U21B
6
74LS00
/VMA
9
10
U7C
8
74LS32
/IORQ
to ECB bus drivers
Z80 signal


U23
74LS688
VCC
20
SHADOW-IO
2 P0
4 P1
mA11 6 P2
mA10 8 P3
mA9 11 P4
mA8 13 P5
mA7 15 P6
17 P7
3 R0
5 R1
7 R2
9 R3
12 R4
14 R5
16 R6
18 R7
/VMA
1 G
GND
10
P=R 19
74LS138
8
GND
4 E1
5 E2
6 E3
mA6 3 A2
mA5 2 A1
mA4 1 A0
VCC
16
U24
O7 7 /IOSEL-0EFF0
O6 9 /IOSEL-0EFE0
O5 10 /IOSEL-0EFD0
O4 11 /IOSEL-0EFC0
O3 12 /IOSEL-0EFB0
O2 13 /IOSEL-0EFA0
O1 14 /IOSEL-0EF90
O0 15 /IOSEL-0EF80

I/O DEVICE SUBSYSTEM ADDRESS
ASSIGNMENTS:

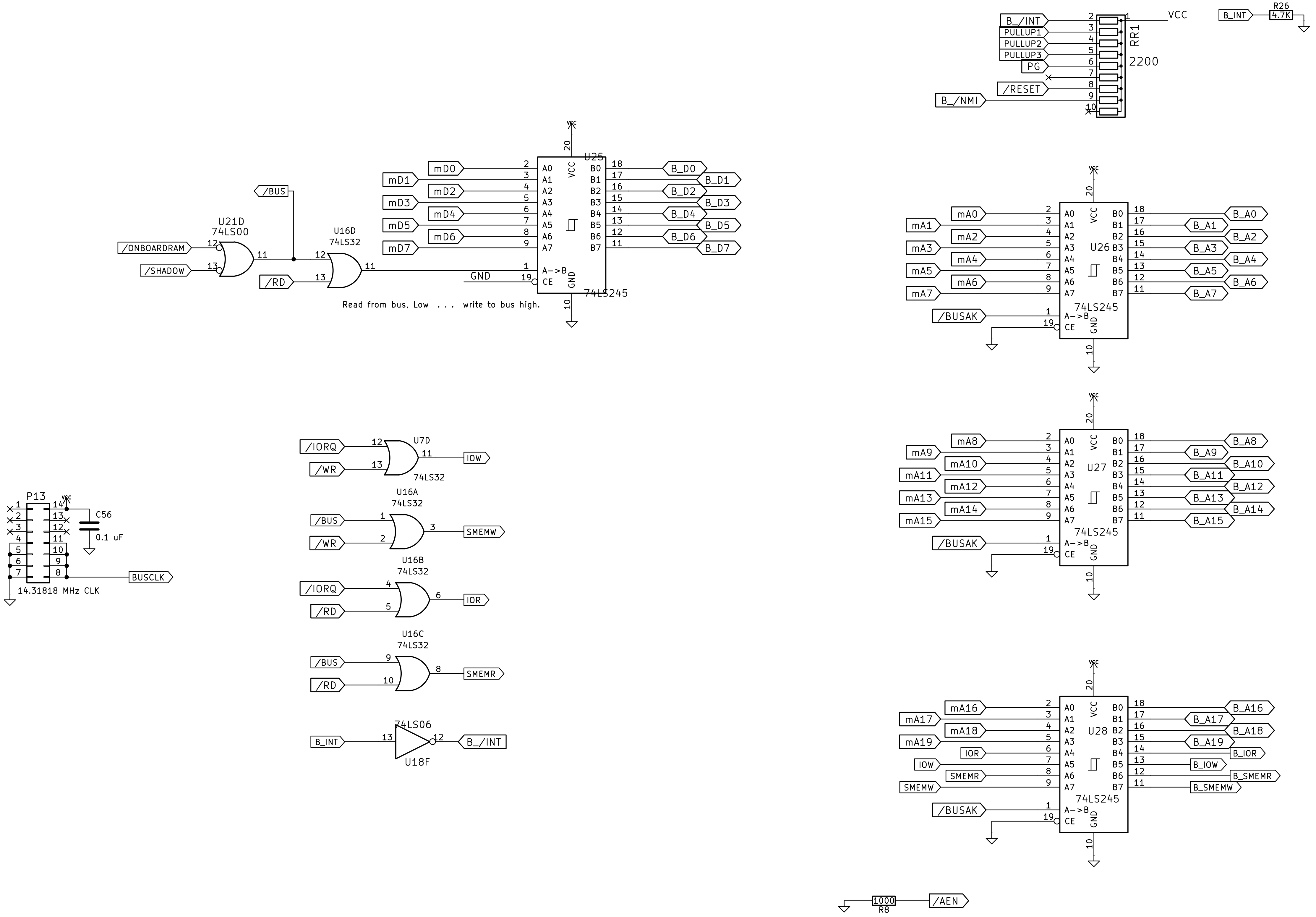
$EFF0 – $EFFF	available
$EFE0 – $EFEF	MMU Registers (3)
$EFD0 – $EFDF	MMU Task Map (16)
$EFC0 – $EFCF	available
$EFB0 – $EFBF	available
$EFA0 – $EFAF	available
$EF90 – $EF9F	RTC (16)
$EF80 – $EF8F	ACIA (4)

Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

Sheet: /Decoder/
File: Decoder.kicad_sch

Title: 6809PC

Size: B | Date: 2025-05-17 | **Rev: 002**
KiCad E.D.A. 8.0.6 | Id: 7/12



B_/INT
PULLUP1
PULLUP2
PULLUP3
PG
/RESET
B_/NMI
RR1
2200
VCC
B_INT
R26
4.7K
/BUS
U21D
74LS00
/ONBOARDRAM
/SHADOW
U16D
74LS32
/RD
mD0
mD1
mD2
mD3
mD4
mD5
mD6
mD7
U25
74LS245
B_D0
B_D1
B_D2
B_D3
B_D4
B_D5
B_D6
B_D7
GND
Read from bus, Low . . . write to bus high.
mA0
mA1
mA2
mA3
mA4
mA5
mA6
mA7
U26
74LS245
/BUSAK
B_A0
B_A1
B_A2
B_A3
B_A4
B_A5
B_A6
B_A7
/IORQ
/WR
U7D
74LS32
IOW
U16A
74LS32
/BUS
SMEMW
U16B
74LS32
IOR
U16C
74LS32
SMEMR
74LS06
B_INT
B_/INT
U18F
P13
C56
0.1 uF
BUSCLK
14.31818 MHz CLK
mA8
mA9
mA10
mA11
mA12
mA13
mA14
mA15
U27
74LS245
B_A8
B_A9
B_A10
B_A11
B_A12
B_A13
B_A14
B_A15
mA16
mA17
mA18
mA19
IOR
IOW
SMEMR
SMEMW
U28
74LS245
B_A16
B_A17
B_A18
B_A19
B_IOR
B_IOW
B_SMEMR
B_SMEMW
1000
R8
/AEN

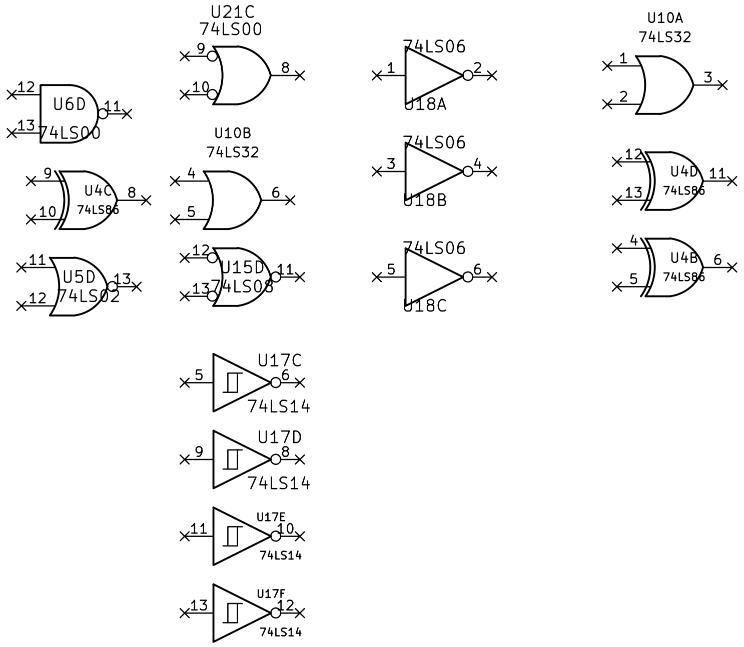
Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

Sheet: /IO/
File: IO.kicad_sch

Title: 6809PC

Size: B
Date: 2025-05-17
Rev: 002
KiCad E.D.A. 8.0.6
Id: 8/12

SPARE

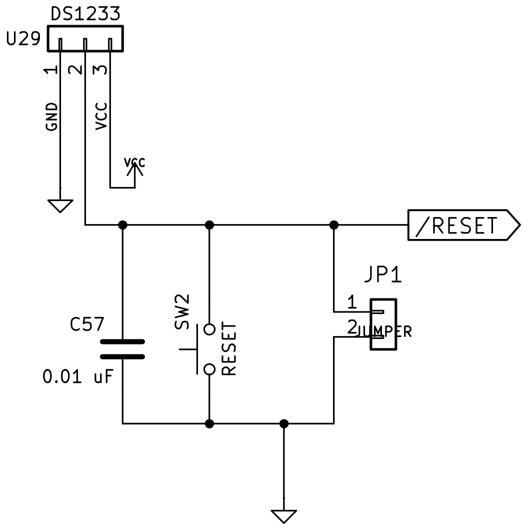

U21C
74LS00
U6D
74LS00
U10B
74LS32
U4C
74LS86
U15D
74LS08
U5D
74LS02
U18A
74LS06
U18B
74LS06
U18C
74LS06
U10A
74LS32
U4D
74LS86
U4B
74LS86
U17C
74LS14
U17D
74LS14
U17E
74LS14
U17F
74LS14

Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

Sheet: /Spare/
File: Spare.kicad_sch

Title: 6809PC

Size: B	Date: 2025-05-17	**Rev: 002**
KiCad E.D.A. 8.0.6		Id: 9/12

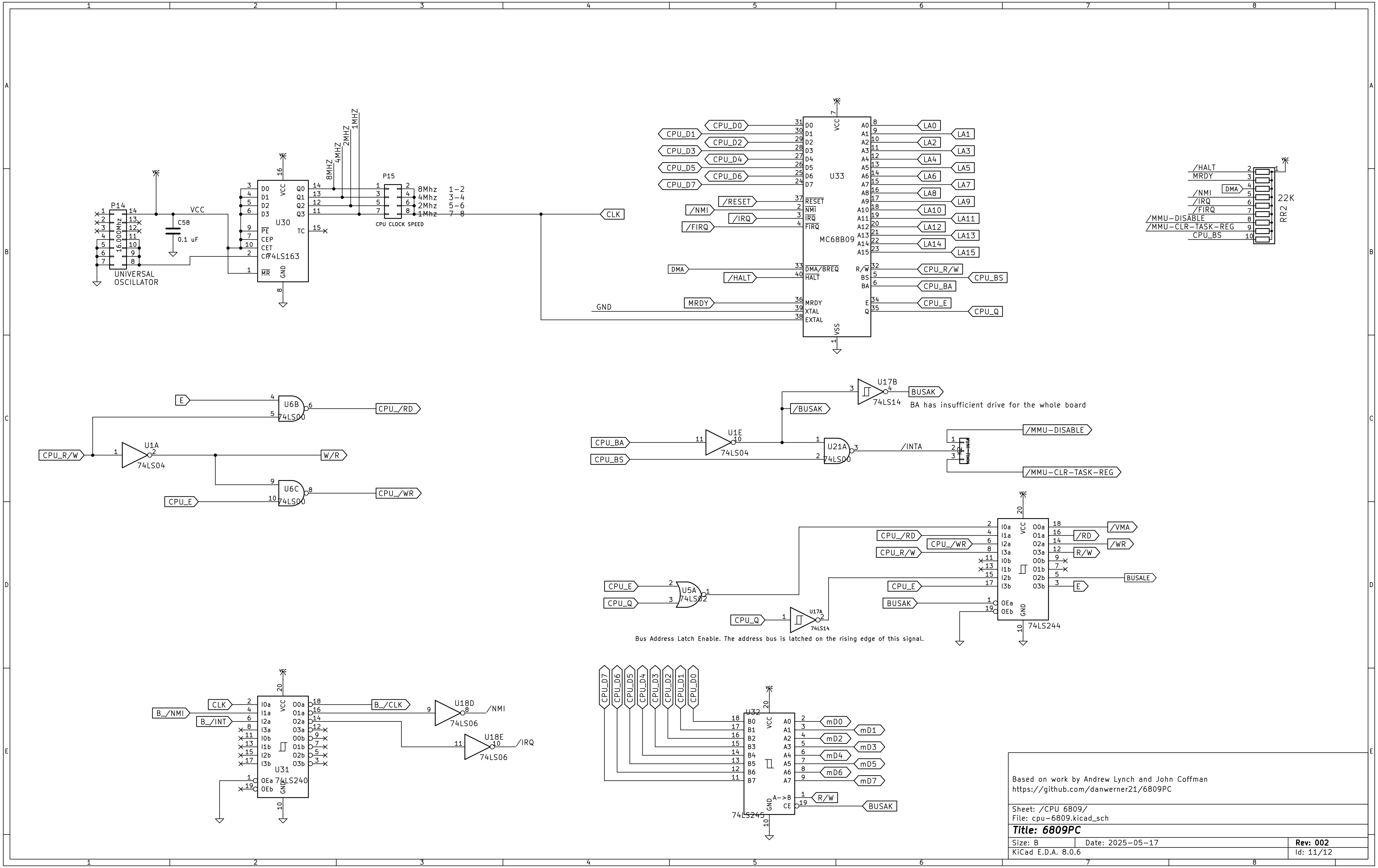

DS1233
U29
1
2
3
GND
VCC
VCC
/RESET
JP1
1
2
JUMPER
C57
0.01 uF
SW2
RESET

Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

Sheet: /Reset/
File: Reset.kicad_sch

Title: 6809PC

Size: A
Date: 2025-05-17
Rev: 002
KiCad E.D.A. 8.0.6
Id: 10/12

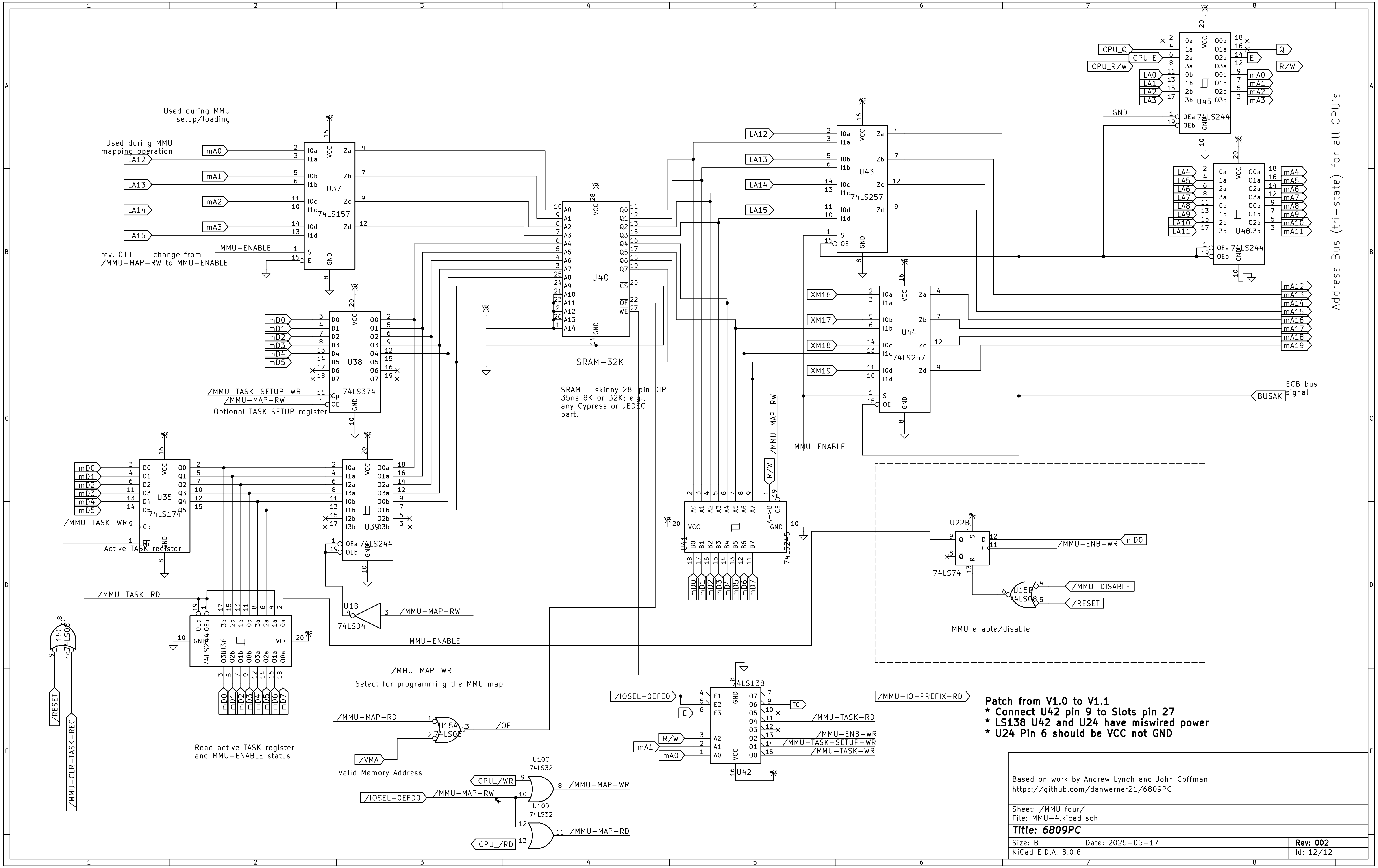

P14
UNIVERSAL
OSCILLATOR
16.000Mhz
C58
0.1 uF
VCC
U30
74LS163
D0
D1
D2
D3
PE
CEP
CET
CP
MR
Q0
Q1
Q2
Q3
TC
GND
8MHZ
4MHZ
2MHZ
1MHZ
P15
8Mhz 1-2
4Mhz 3-4
2Mhz 5-6
1Mhz 7 8
CPU CLOCK SPEED
CLK
GND
U33
MC68B09
CPU_D0
CPU_D1
CPU_D2
CPU_D3
CPU_D4
CPU_D5
CPU_D6
CPU_D7
/RESET
/NMI
/IRQ
/FIRQ
DMA
/HALT
MRDY
XTAL
EXTAL
DMA/BREQ
LA0
LA1
LA2
LA3
LA4
LA5
LA6
LA7
LA8
LA9
LA10
LA11
LA12
LA13
LA14
LA15
CPU_R/W
CPU_BS
CPU_BA
CPU_E
CPU_Q
VCC
VSS
RR2
22K
/HALT
MRDY
DMA
/NMI
/IRQ
/FIRQ
/MMU-DISABLE
/MMU-CLR-TASK-REG
CPU_BS
E
U6B
74LS00
CPU_/RD
CPU_R/W
U1A
74LS04
W/R
U6C
74LS00
CPU_E
CPU_/WR
U17B
74LS14
BUSAK
BA has insufficient drive for the whole board
/BUSAK
CPU_BA
U1E
74LS04
U21A
74LS00
CPU_BS
/INTA
/MMU-DISABLE
/MMU-CLR-TASK-REG
74LS244
CPU_/RD
CPU_/WR
CPU_R/W
CPU_E
BUSAK
/VMA
/RD
/WR
R/W
BUSALE
E
U5A
74LS02
CPU_E
CPU_Q
U17A
74LS14
CPU_Q
Bus Address Latch Enable. The address bus is latched on the rising edge of this signal.
U31
74LS240
CLK
B_/NMI
B_/INT
B_/CLK
U18D
74LS06
/NMI
U18E
74LS06
/IRQ
CPU_D7
CPU_D6
CPU_D5
CPU_D4
CPU_D3
CPU_D2
CPU_D1
CPU_D0
U32
74LS245
mD0
mD1
mD2
mD3
mD4
mD5
mD6
mD7
A->B
CE
R/W
BUSAK

Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

Sheet: /CPU 6809/
File: cpu-6809.kicad_sch

Title: 6809PC

Size: B
Date: 2025-05-17
Rev: 002
KiCad E.D.A. 8.0.6
Id: 11/12


Used during MMU setup/loading
Used during MMU mapping operation
rev. 011 -- change from /MMU-MAP-RW to MMU-ENABLE
MMU-ENABLE
U37
74LS157
mA0
mA1
mA2
mA3
LA12
LA13
LA14
LA15
U40
SRAM-32K
SRAM - skinny 28-pin DIP 35ns 8K or 32K; e.g., any Cypress or JEDEC part.
U38
74LS374
mD0
mD1
mD2
mD3
mD4
mD5
/MMU-TASK-SETUP-WR
/MMU-MAP-RW
Optional TASK SETUP register
U35
74LS174
/MMU-TASK-WR
Active TASK register
U39
74LS244
U1B
74LS04
/MMU-MAP-RW
/MMU-TASK-RD
U36
74LS244
Read active TASK register and MMU-ENABLE status
U15C
74LS08
/RESET
/MMU-CLR-TASK-REG
/MMU-MAP-WR
Select for programming the MMU map
/MMU-MAP-RD
U15A
74LS08
/OE
/VMA
Valid Memory Address
U10C
74LS32
U10D
74LS32
CPU_/WR
CPU_/RD
/IOSEL-0EFD0
/MMU-MAP-RW
/MMU-MAP-WR
/MMU-MAP-RD
U41
74LS245
R/W
/MMU-MAP-RW
U42
74LS138
/IOSEL-0EFE0
E
R/W
mA1
mA0
/MMU-IO-PREFIX-RD
TC
/MMU-TASK-RD
/MMU-ENB-WR
/MMU-TASK-SETUP-WR
/MMU-TASK-WR
U22B
74LS74
/MMU-ENB-WR
mD0
U15B
74LS08
/MMU-DISABLE
/RESET
MMU enable/disable
U43
74LS257
U44
74LS257
XM16
XM17
XM18
XM19
MMU-ENABLE
BUSAK
ECB bus signal
U45
74LS244
CPU_Q
CPU_E
CPU_R/W
Q
E
R/W
LA0
LA1
LA2
LA3
GND
U46
74LS244
LA4
LA5
LA6
LA7
LA8
LA9
LA10
LA11
mA4
mA5
mA6
mA7
mA8
mA9
mA10
mA11
mA12
mA13
mA14
mA15
mA16
mA17
mA18
mA19
Address Bus (tri-state) for all CPU's

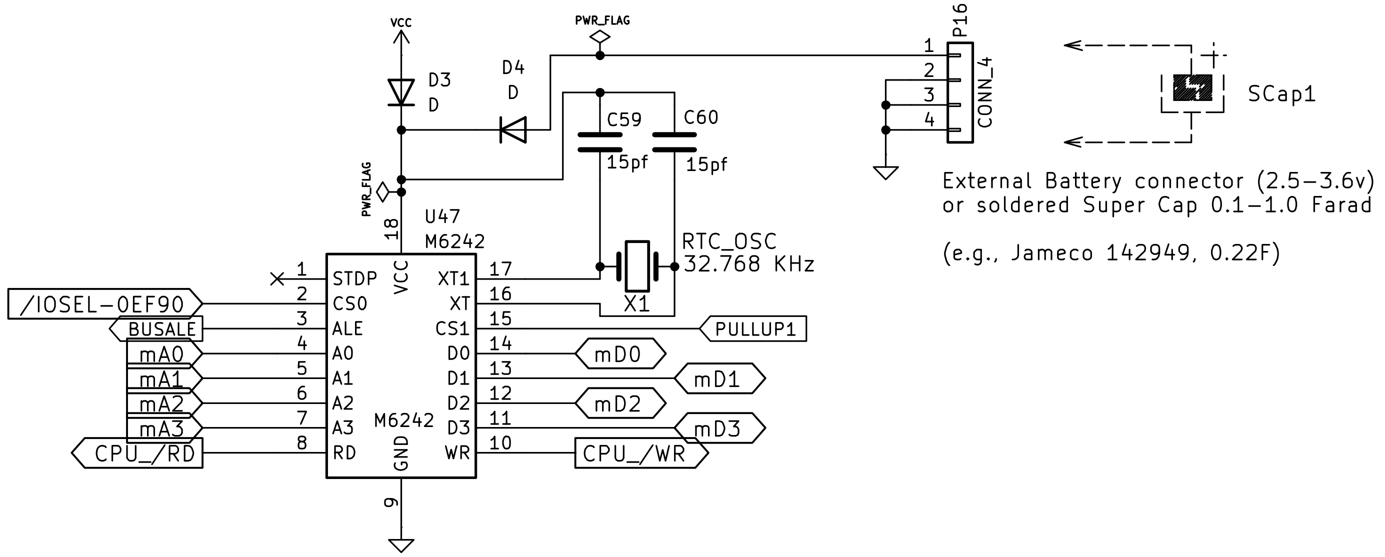
Patch from V1.0 to V1.1
*** Connect U42 pin 9 to Slots pin 27**
*** LS138 U42 and U24 have miswired power**
*** U24 Pin 6 should be VCC not GND**

Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

Sheet: /MMU four/
File: MMU-4.kicad_sch

Title: 6809PC

Size: B	Date: 2025-05-17	**Rev: 002**
KiCad E.D.A. 8.0.6		Id: 12/12


VCC
D3
D
D4
D
PWR_FLAG
PWR_FLAG
P16
1
2
3
4
CONN_4
SCap1
C59
15pf
C60
15pf
18
U47
M6242
RTC_OSC
32.768 KHz
X1
1 STDP
2 CS0
3 ALE
4 A0
5 A1
6 A2
7 A3
8 RD
VCC
GND
9
M6242
17 XT1
16 XT
15 CS1
14 D0
13 D1
12 D2
11 D3
10 WR
/IOSEL-0EF90
BUSALE
mA0
mA1
mA2
mA3
CPU_/RD
PULLUP1
mD0
mD1
mD2
mD3
CPU_/WR

External Battery connector (2.5-3.6v)
or soldered Super Cap 0.1-1.0 Farad

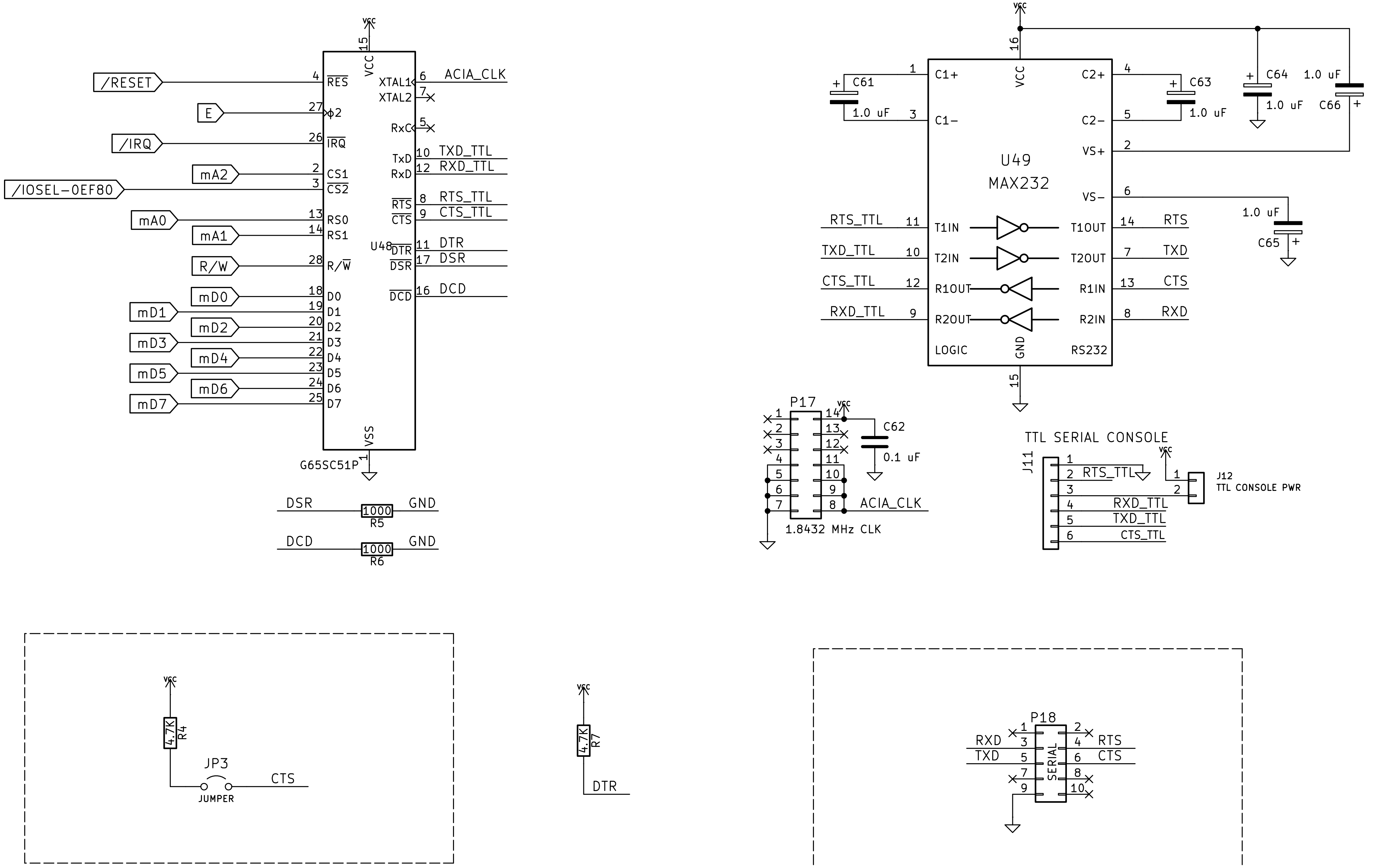
(e.g., Jameco 142949, 0.22F)

Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

Sheet: /RTC/
File: RTC.kicad_sch

Title: 6809PC

Size: A	Date: 2025-05-17	**Rev: 002**
KiCad E.D.A. 8.0.6		Id: 13/12


/RESET
E
/IRQ
mA2
/IOSEL-0EF80
mA0
mA1
R/W
mD0
mD1
mD2
mD3
mD4
mD5
mD6
mD7
RES
ϕ2
IRQ
CS1
CS2
RS0
RS1
R/W
D0
D1
D2
D3
D4
D5
D6
D7
VCC
VSS
U48
G65SC51P
XTAL1
XTAL2
RxC
TxD
RxD
RTS
CTS
DTR
DSR
DCD
ACIA_CLK
TXD_TTL
RXD_TTL
RTS_TTL
CTS_TTL
DTR
DSR
DCD
R5 1000
R6 1000
GND
U49
MAX232
C1+
C1-
C2+
C2-
VS+
VS-
T1IN
T2IN
R1OUT
R2OUT
T1OUT
T2OUT
R1IN
R2IN
LOGIC
GND
RS232
C61 1.0 uF
C63 1.0 uF
C64 1.0 uF
C66 1.0 uF
C65 1.0 uF
RTS
TXD
CTS
RXD
P17
C62 0.1 uF
1.8432 MHz CLK
TTL SERIAL CONSOLE
J11
J12
TTL CONSOLE PWR
VCC
R4 4.7K
JP3
JUMPER
R7 4.7K
P18
SERIAL

CTS is an inverted signal on the RS-232 port. So it is really /CTS. To assert the signal, it must be tied to SPACE, which is a + RS-232 voltage. (MARK, or true, is a - RS-232 voltage.)

Based on work by Andrew Lynch and John Coffman
https://github.com/danwerner21/6809PC

Sheet: /ACIA/
File: ACIA.kicad_sch

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