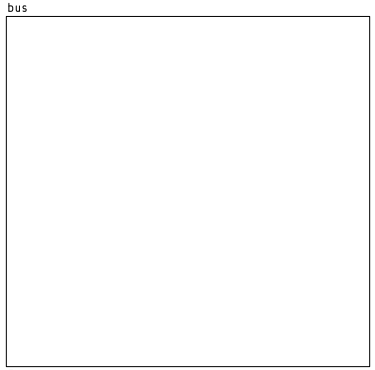
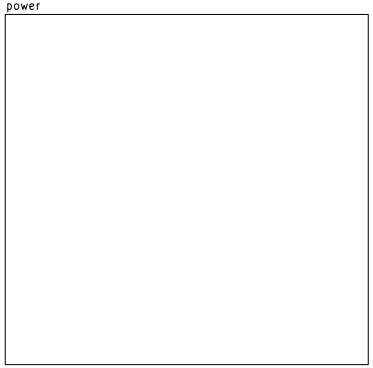
bus



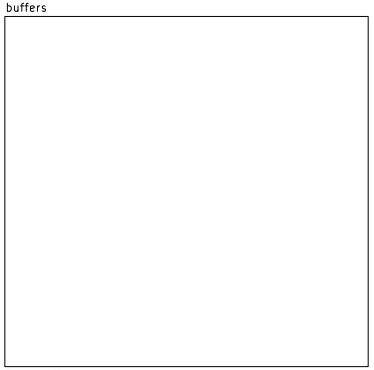
File: bus.kicad_sch

power



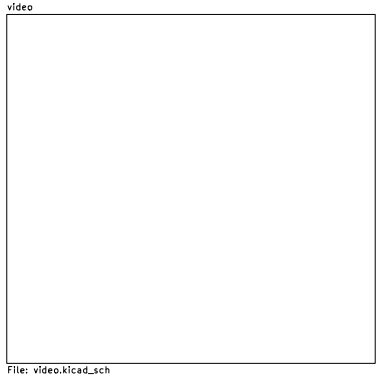
File: power.kicad_sch

buffers



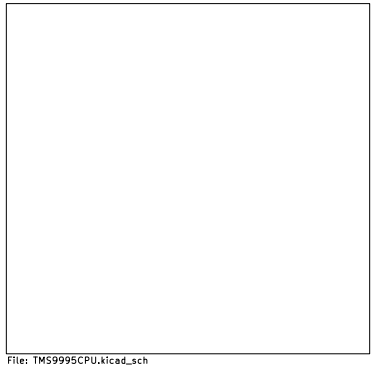
File: buffers.kicad_sch

video



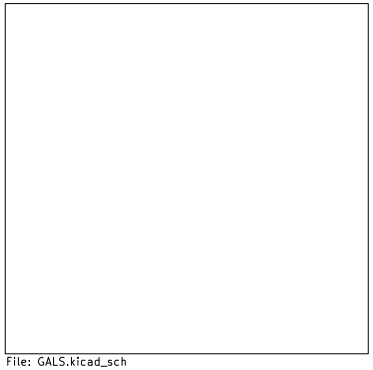
File: video.kicad_sch

TMS9995CPU



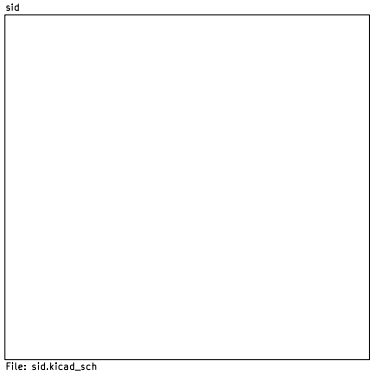
File: TMS9995CPU.kicad_sch

GALS



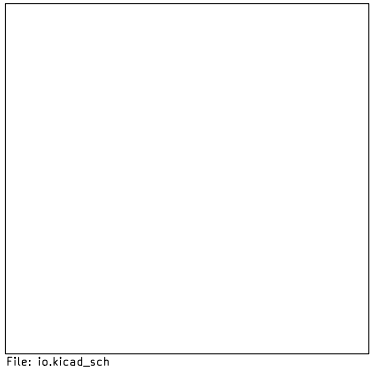
File: GALS.kicad_sch

sid



File: sid.kicad_sch

IO

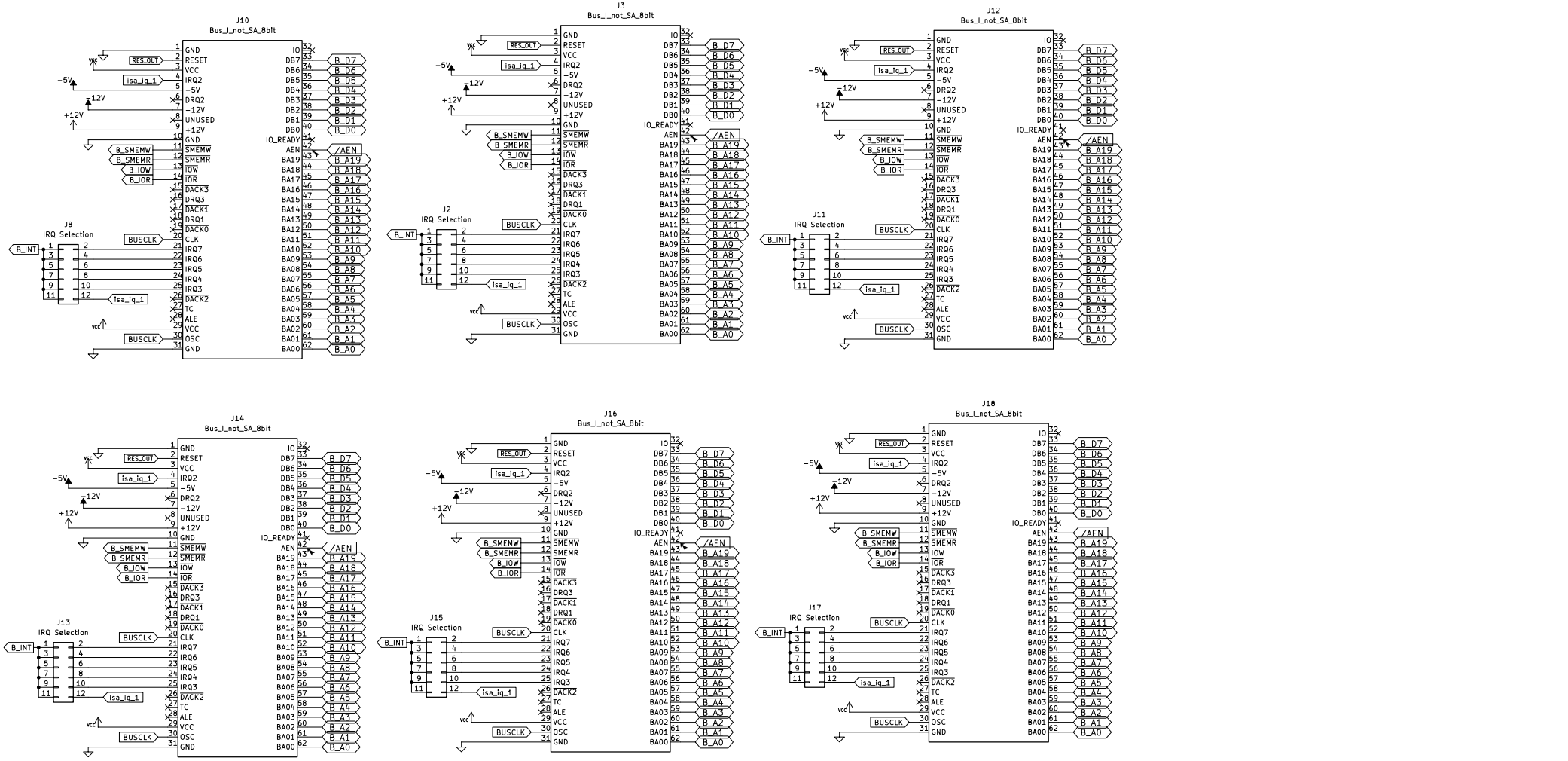


File: io.kicad_sch

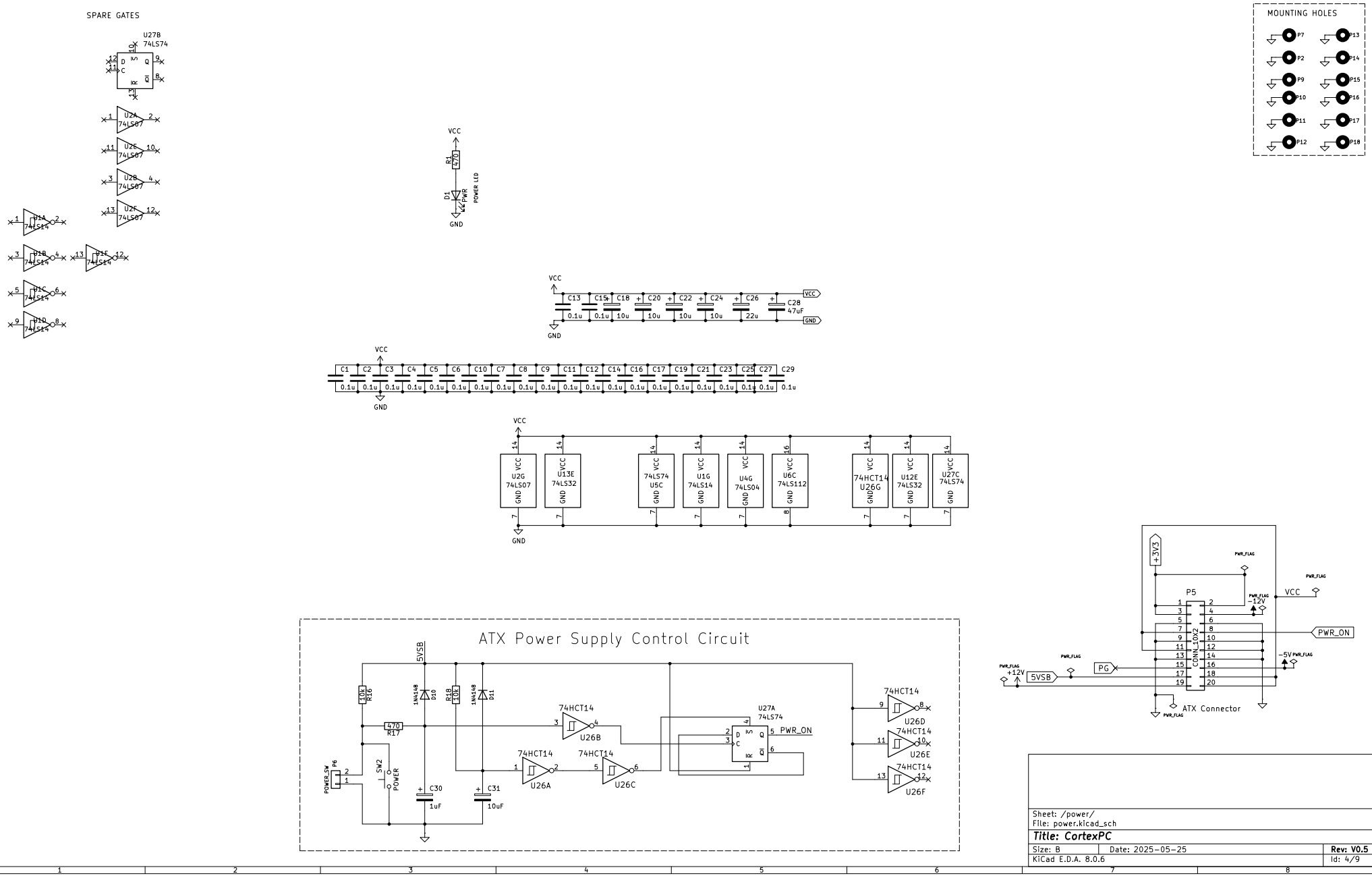
Sheet: /
File: CortexPC.kicad_sch

Title: CortexPC

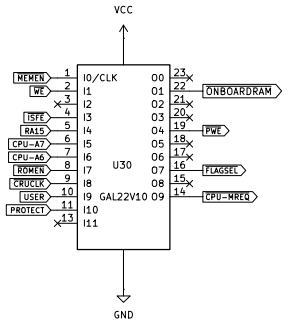
Size: B	Date: 2025-05-25	**Rev: V0.5**
KiCad E.D.A. 8.0.6		Id: 1/9



Sheet: /bus/	
File: bus.kicad_sch	
Title: CortexPC	
Size: B	Date: 2025-05-25
KiCad E.D.A. 8.0.6	Id: 2/9
	Rev: V0.5


SPARE GATES
U27B
74LS74
U2A
74LS07
U2E
74LS07
U2B
74LS07
U2F
74LS07
U14A
74LS14
U14B
74LS14
U14F
74LS14
U14C
74LS14
U14D
74LS14
MOUNTING HOLES
P7
P2
P9
P10
P11
P12
P13
P14
P15
P16
P17
P18
VCC
R4
470
D1
PWR
POWER LED
GND
C13
C15
C18
C20
C22
C24
C26
C28
0.1u
10u
22u
47uF
C1
C2
C3
C4
C5
C6
C10
C7
C8
C9
C11
C12
C14
C16
C17
C19
C21
C23
C25
C27
C29
U2G
74LS07
U13E
74LS32
74LS74
U5C
U1G
74LS14
U4G
74LS04
U6C
74LS112
74HCT14
U26G
U12E
74LS32
U27C
74LS74
ATX Power Supply Control Circuit
5VSB
R16
10k
470
R17
1N4148
D10
R18
D11
74HCT14
U26B
U26A
U26C
U27A
74LS74
PWR_ON
U26D
U26E
U26F
POWER_SW
P6
SW2
POWER
C30
1uF
C31
10uF
+3V3
PWR_FLAG
P5
CONN_10X2
VCC
-12V
-5V
PG
+12V
ATX Connector
Sheet: /power/
File: power.kicad_sch
Title: CortexPC
Size: B
Date: 2025-05-25
Rev: V0.5
KiCad E.D.A. 8.0.6
Id: 4/9

TMS9995 MEM GAL22V10



Equation ('+' is 'OR', '*' is 'AND')

$=\overline{MEMEN}+(!\overline{ROMEN}*!RA15*\overline{WE})\ +\ (!\overline{ISFE}\ *\ RA15)$

$=\overline{WE}+(PROTECT*USER)$

$=\overline{CRUCLK}+\overline{ISFE}+RA15+CPU-A7+!CPU-A6$

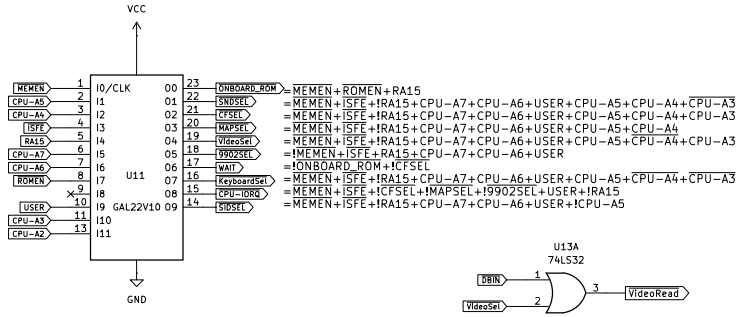
$=(!\overline{ISFE}\ *\ RA15)+\overline{OFFBOARD\_MEM}$

The memory map is shown in the table below.

Memory Address	Mapped To
>0000 – >7FFF	ROM when enabled, otherwise RAM
>8000 – >EFFF	RAM
>F000 – >F0FB	TMS 9995 internal RAM
>F0FC – >F0FF	RAM
>FE00 – >FE03	CF card ATA registers
>FE10 – >FE13	SOUND
>FE20 – >FE23	VIDEO
>FE30 – >FE33	KEYBOARD
>FE40 – >FE4F	Memory mapper registers 0–15
>FE60 – >FE7F	SID registers 0–31
>FE80 – >FEBF	Offboard IO (ports $80–$FF)
>FFF0 – >FFF9	RAM
>FFFA – >FFFF	TMS 9995 internal RAM

CRU Address	Mapped To
>0000 – >003F	TMS 9902 registers
>0040 – >007F	Control signal latch (further details here)
	(Plus processor internal CRU bits)

TMS9995 IO GAL22V10



$=\overline{MEMEN}+\overline{ROMEN}+RA15$

$=\overline{MEMEN}+\overline{ISFE}+!RA15+CPU-A7+CPU-A6+USER+CPU-A5+CPU-A4+\overline{CPU-A3}$

$=\overline{MEMEN}+\overline{ISFE}+!RA15+CPU-A7+CPU-A6+USER+CPU-A5+CPU-A4+CPU-A3$

$=\overline{MEMEN}+\overline{ISFE}+!RA15+CPU-A7+CPU-A6+USER+CPU-A5+\overline{CPU-A4}$

$=\overline{MEMEN}+\overline{ISFE}+!RA15+CPU-A7+CPU-A6+USER+CPU-A5+\overline{CPU-A4}+CPU-A3$

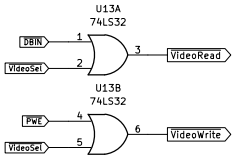
$=!\overline{MEMEN}+\overline{ISFE}+RA15+CPU-A7+CPU-A6+USER$

$=!\overline{ONBOARD\_ROM}+!\overline{CFSEL}$

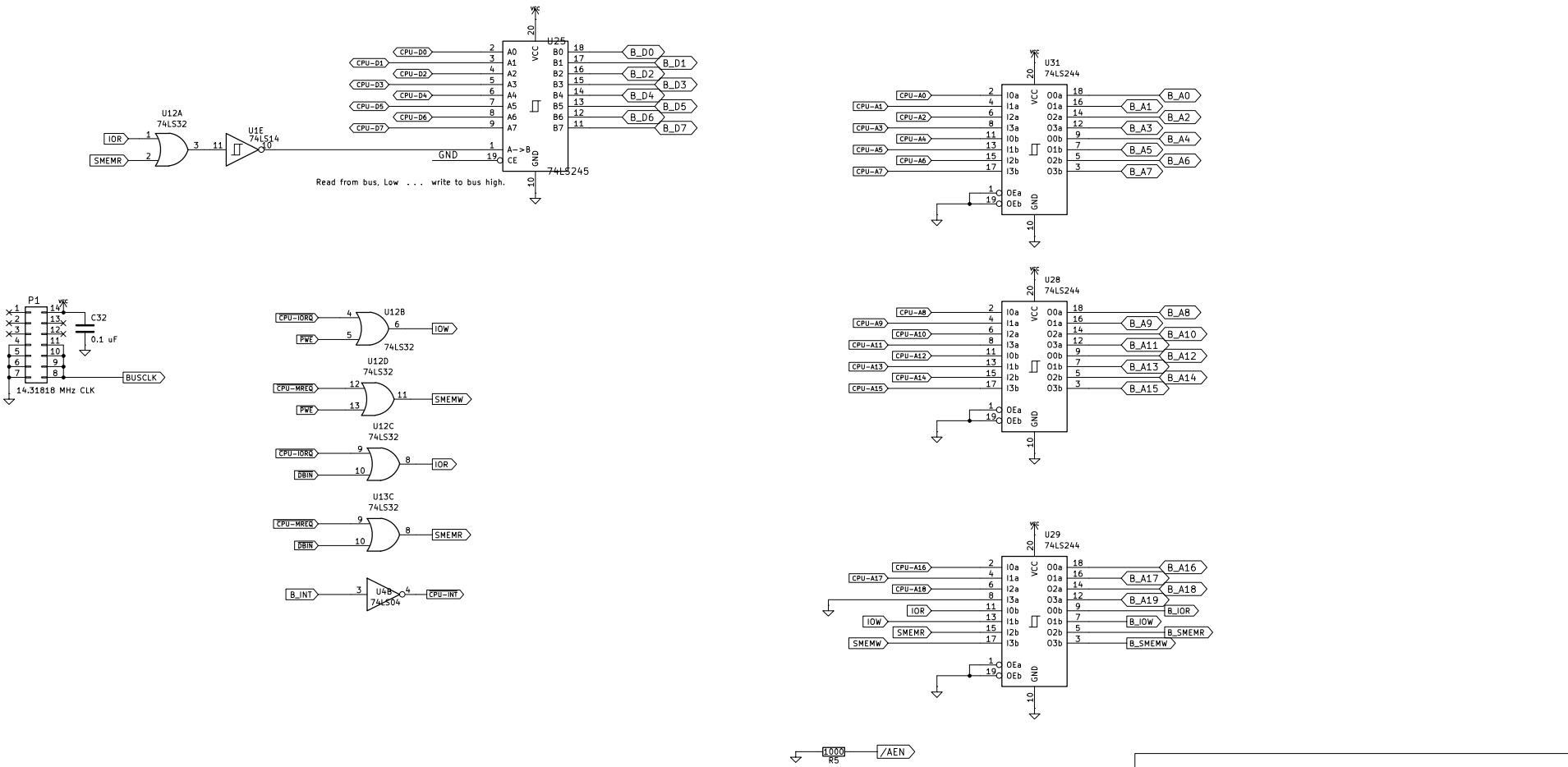
$=\overline{MEMEN}+\overline{ISFE}+!RA15+CPU-A7+CPU-A6+USER+CPU-A5+\overline{CPU-A4}+\overline{CPU-A3}$

$=\overline{MEMEN}+\overline{ISFE}+!\overline{CFSEL}+!MAPSEL+!9902SEL+USER+!RA15$

$=\overline{MEMEN}+\overline{ISFE}+!RA15+CPU-A7+CPU-A6+USER+!CPU-A5$

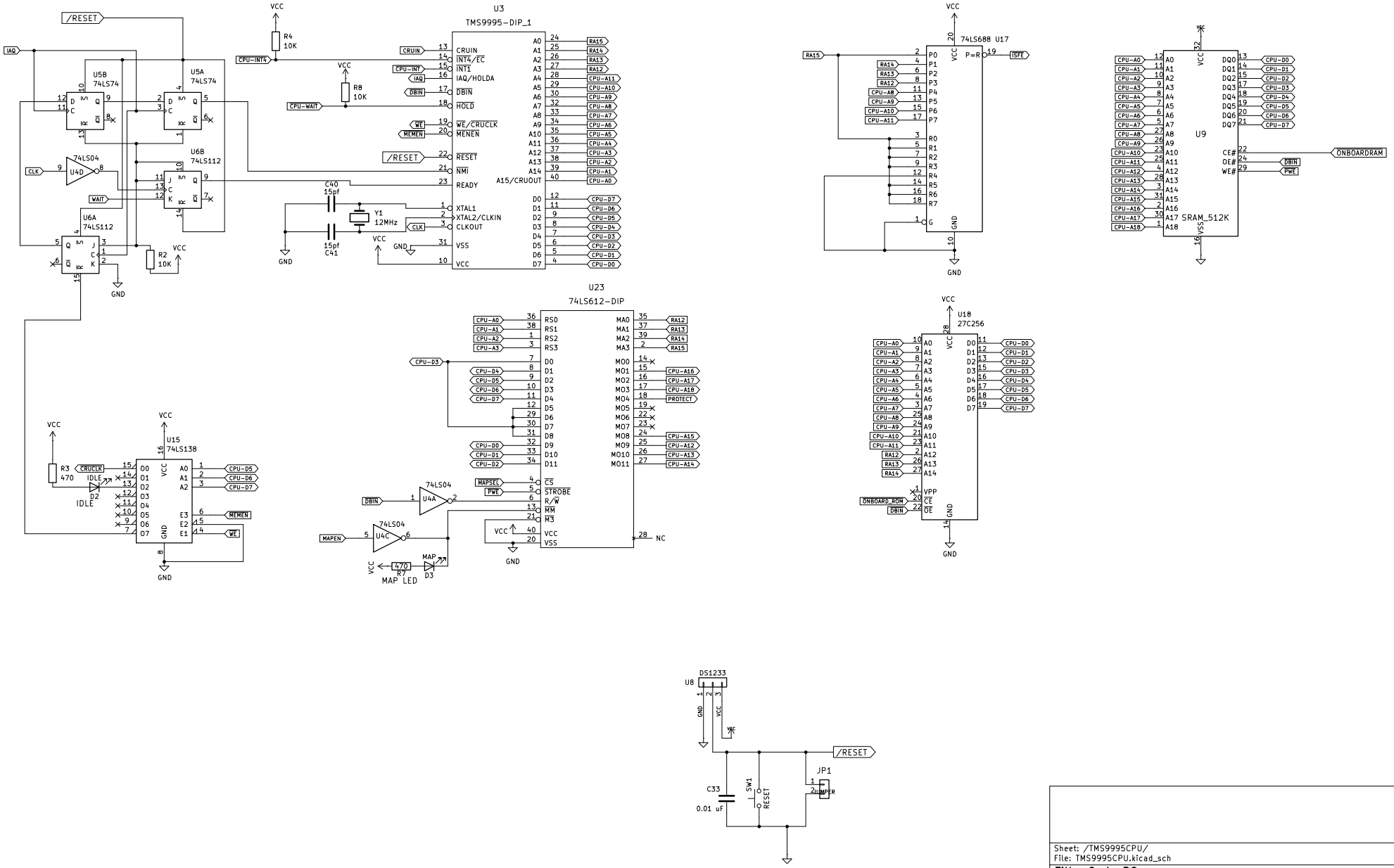


Sheet: /GALS/		
File: GALS.kicad_sch		
Title: CortexPC		
Size: B	Date: 2025-05-25	**Rev: V0.5**
KiCad E.D.A. 8.0.6		Id: 5/9

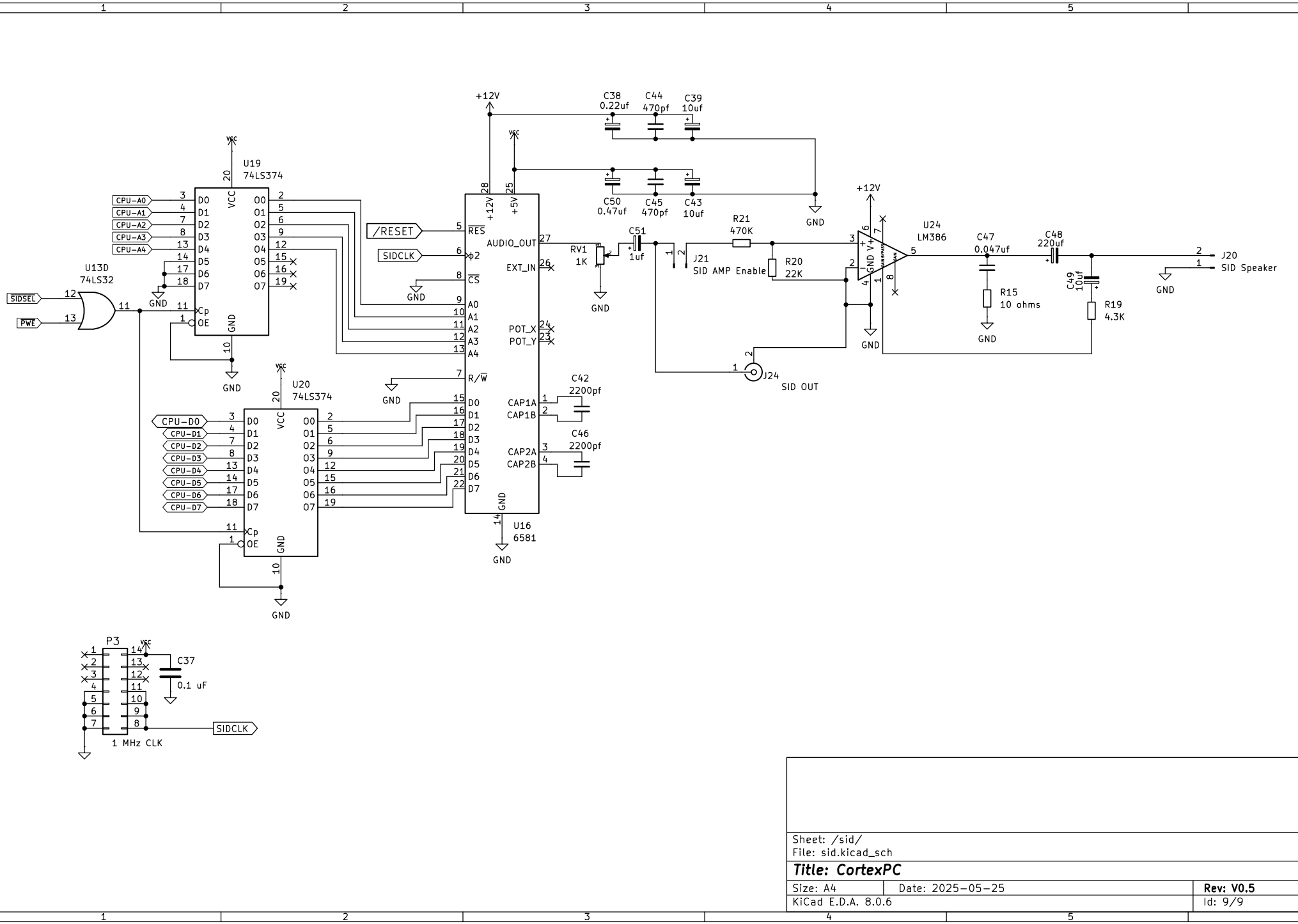


Sheet: /buffers/	
File: buffers.kicad_sch	
Title: CortexPC	
Size: B	Date: 2025-05-25
KiCad E.D.A. 8.0.6	Id: 6/9

Rev: V0.5

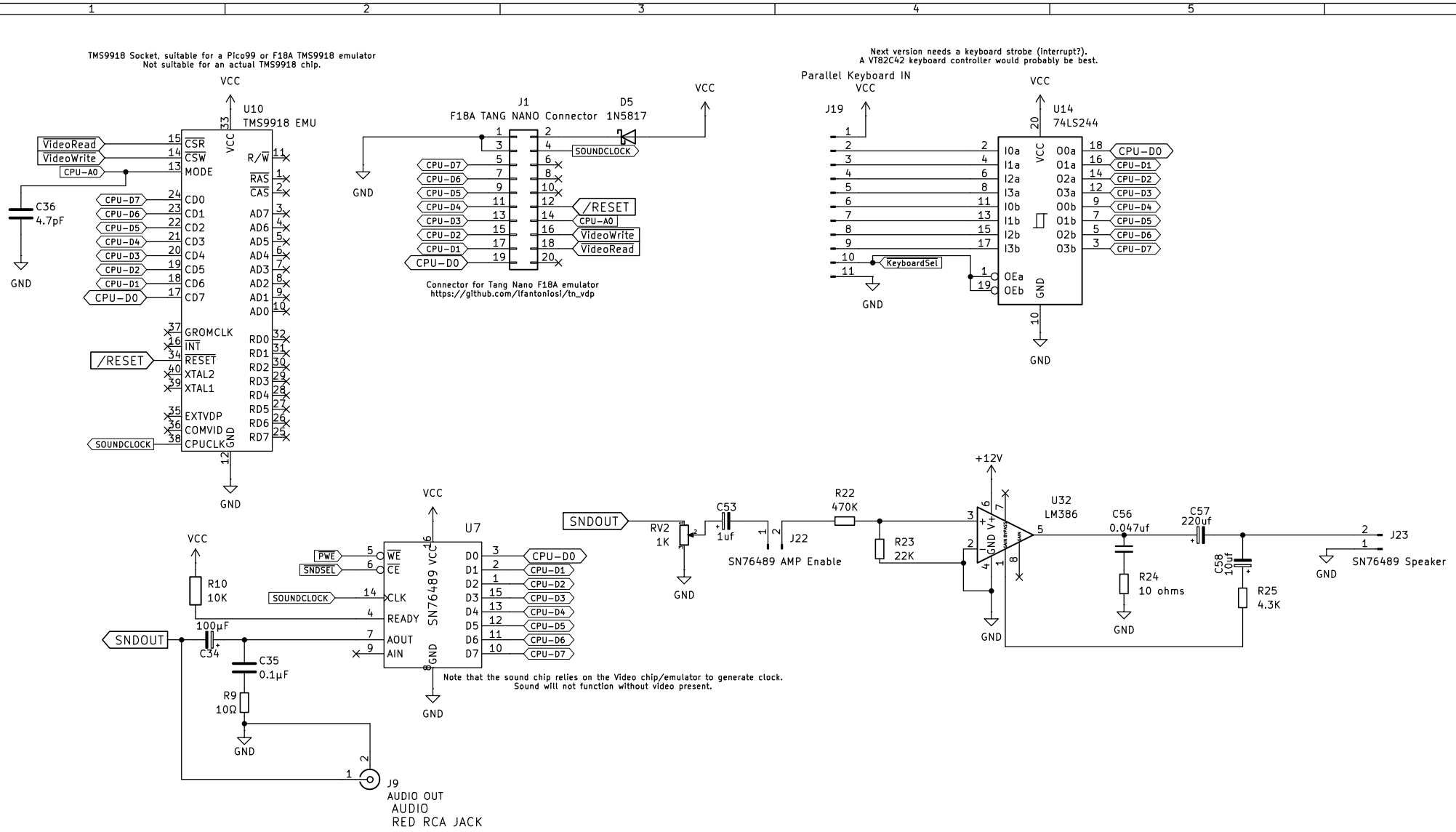


Sheet: /TMS9995CPU/	
File: TMS9995CPU.kicad_sch	
Title: CortexPC	
Size: USLedger | Date: 2025-05-25	**Rev: V0.5**
KiCad E.D.A. 8.0.6	Id: 9/9

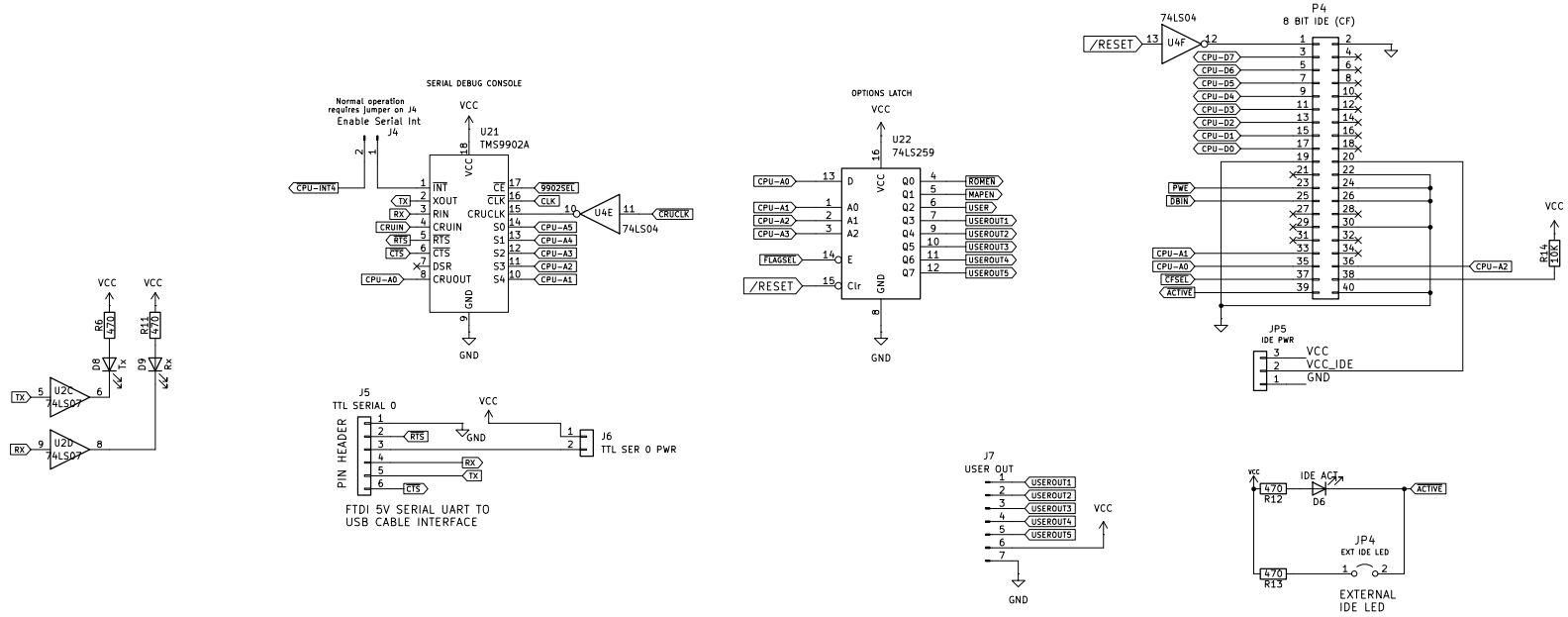


Sheet: /sid/	
File: sid.kicad_sch	
Title: CortexPC	
Size: A4	Date: 2025-05-25
KiCad E.D.A. 8.0.6	Id: 9/9

Rev: V0.5



Sheet: /video/		
File: video.kicad_sch		
Title: CortexPC		
Size: A4	Date: 2025-05-25	**Rev: V0.5**
KiCad E.D.A. 8.0.6		Id: 9/9



Sheet: /IO/	
File: io.kicad_sch	
Title: CortexPC	
Size: B	Date: 2025-05-25
KiCad E.D.A. 8.0.6	Id: 11/9

Rev: V0.5