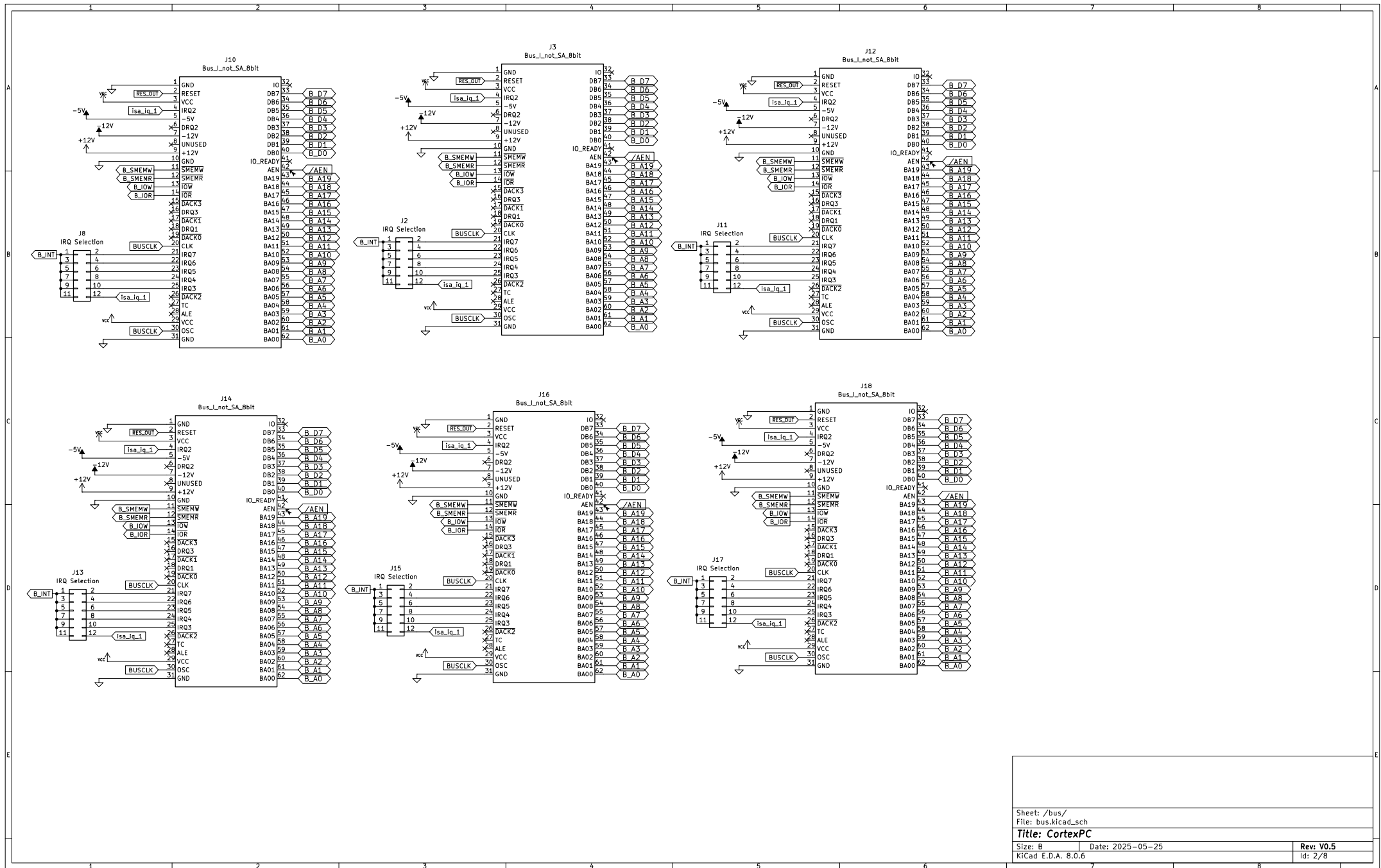
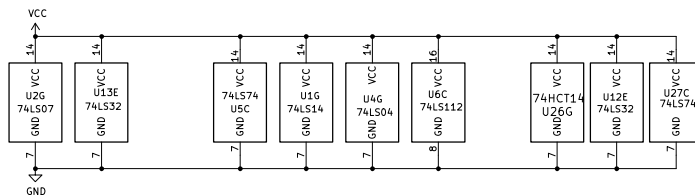
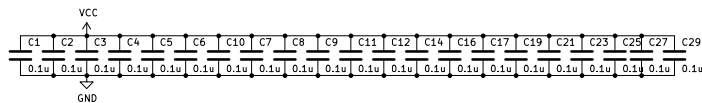
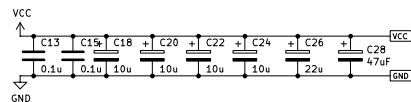
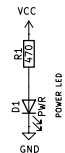
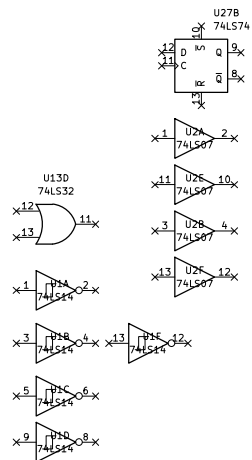


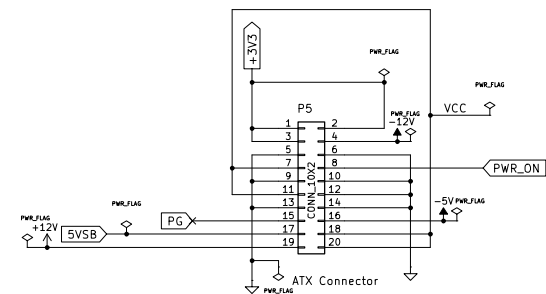
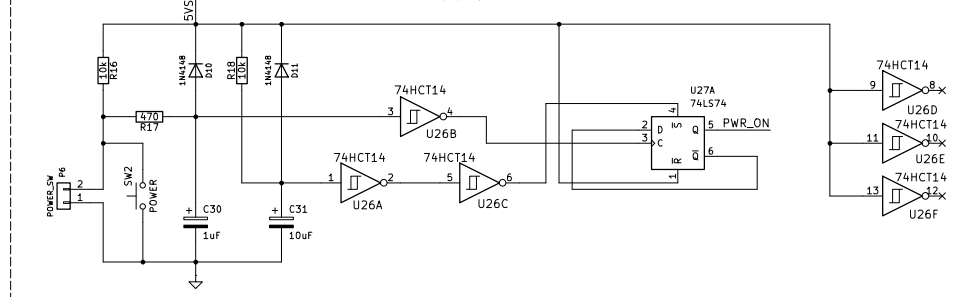
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B	File: bus.kicad_sch TMS9995CPU		File: power.kicad_sch GALS		File: buffers.kicad_sch		File: video.kicad_sch IO		
C	File: TMS9995CPU.kicad_sch		File: GALS.kicad_sch				File: io.kicad_sch		
D									
E									
	1	2	3	4	5	6	7	8	



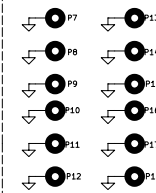
SPARE GATES



ATX Power Supply Control Circuit



MOUNTING HOLES



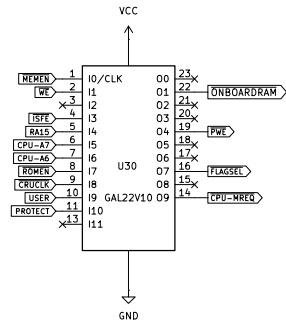
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Title: CortexPC

Size: B Date: 2025-05-25
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TMS9995 MEM GAL22V10



Equation ('+' is 'OR', '*' is 'AND')

$$= \text{MEMEN} + (\text{ROMEN} * \text{RA15} * \text{WE}) + (\text{ISFE} * \text{RA15})$$

$$= \text{WE} + (\text{PROTECT} * \text{USER})$$

$$= \text{CRUCLK} + \text{ISFE} + \text{RA15} + \text{CPU-A7} + \text{CPU-A6}$$

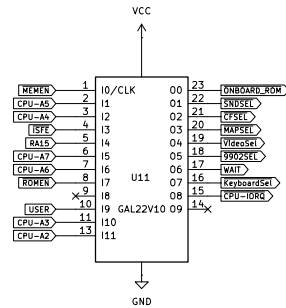
$$= (\text{ISFE} * \text{RA15}) + \text{OFFBOARD_MEM}$$

The memory map is shown in the table below.

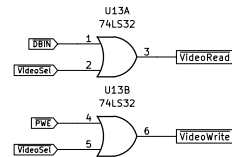
Memory Address	Mapped To
>0000 - >7FFF	ROM when enabled, otherwise RAM
>8000 - >EFFF	RAM
>F000 - >F0FF	TMS 9995 Internal RAM
>F0FC - >F0FF	RAM
>FE00 - >FE03	CF card ATA registers
>FE10 - >FE13	SOUND
>FE20 - >FE23	VVIDEO
>FE30 - >FE33	KEYBOARD
>FE40 - >FE4F	Memory mapper registers 0-15
>FE80 - >FE8F	Offboard I/O (ports 500-5FF)
>FFF0 - >FFF9	RAM
>FFFA - >FFFF	TMS 9995 internal RAM

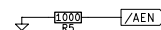
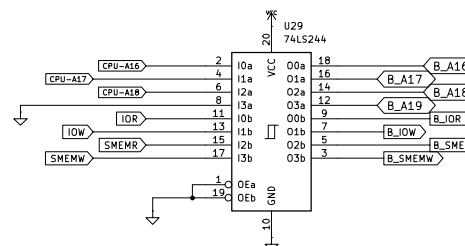
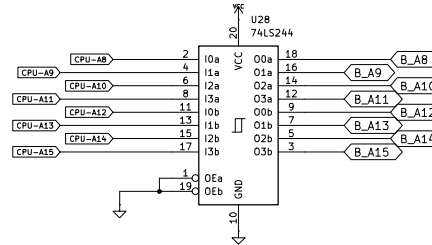
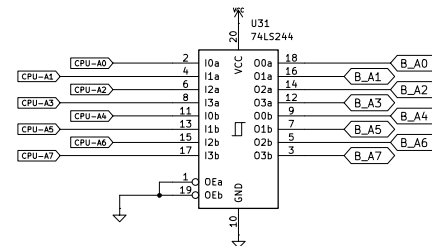
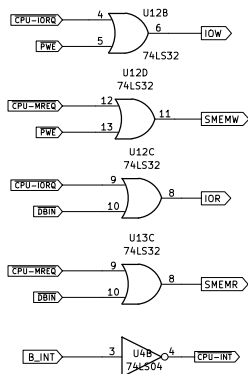
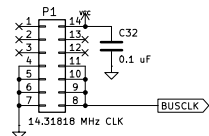
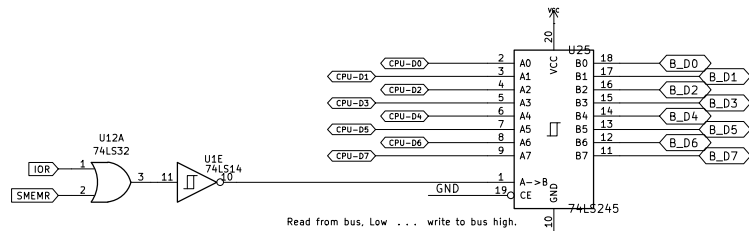
CRU Address	Mapped To
>0000 - >003F	TMS 9902 registers
>0040 - >007F	Control signal latch (further details here)
	(Plus processor internal CRU bits)

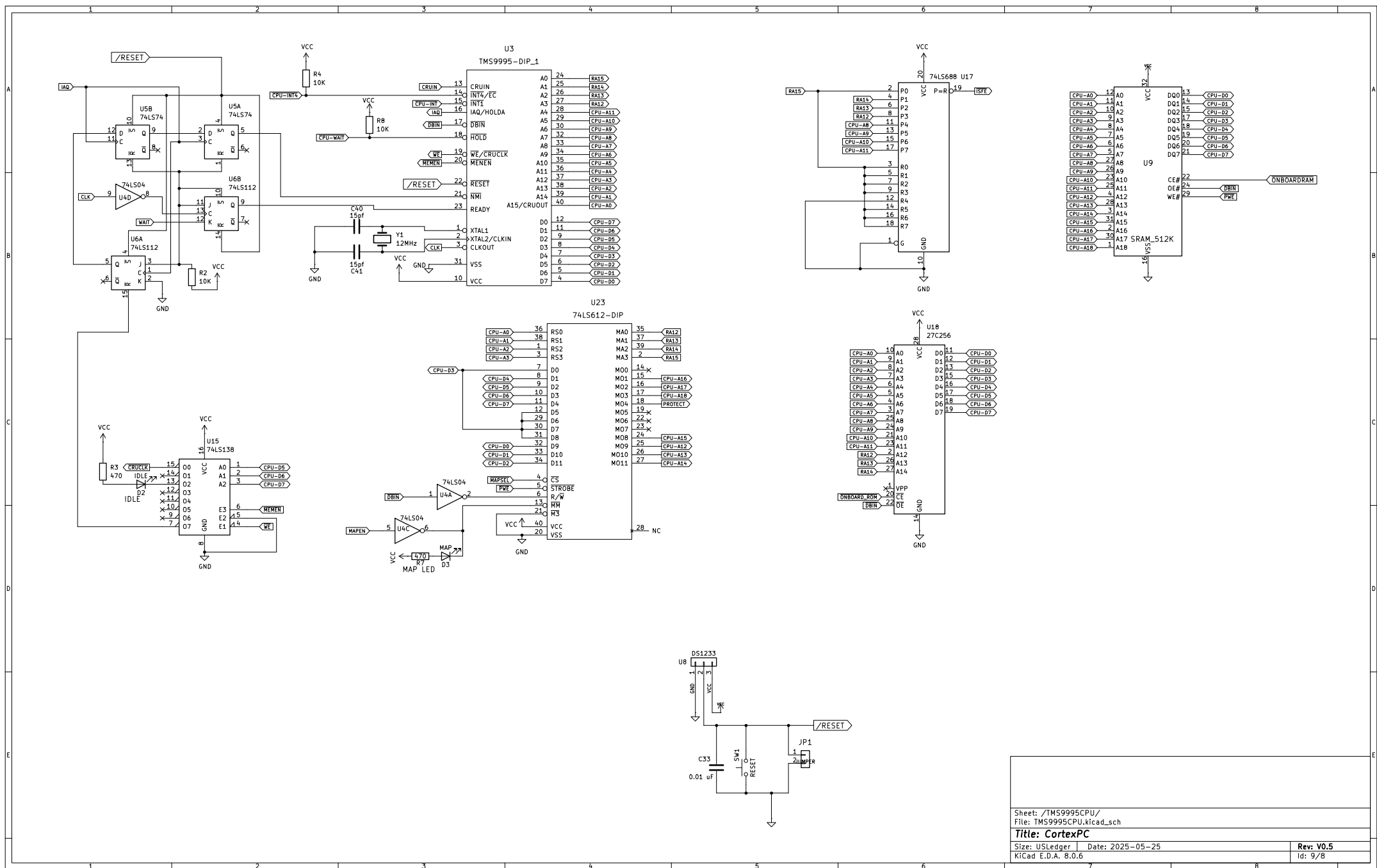
TMS9995 IO GAL22V10



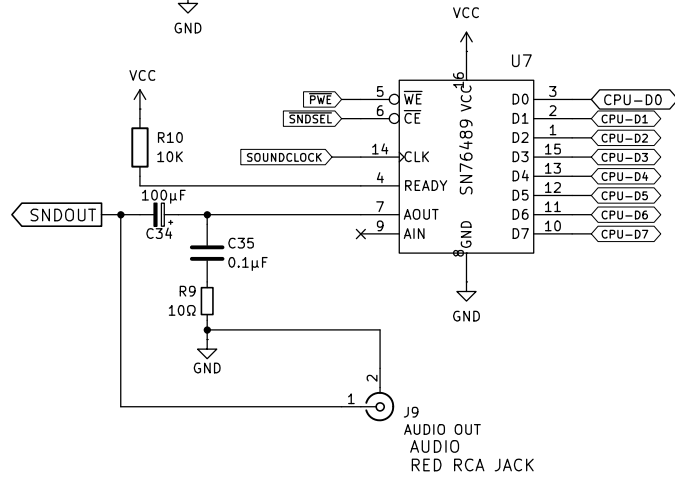
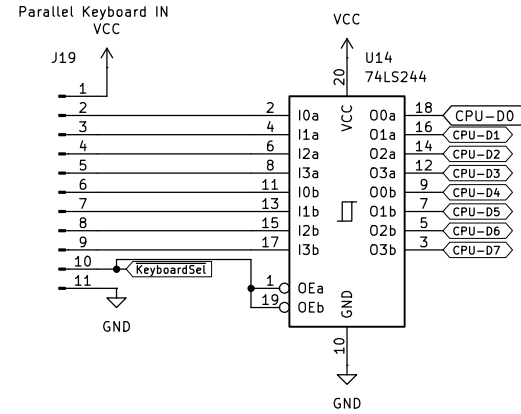
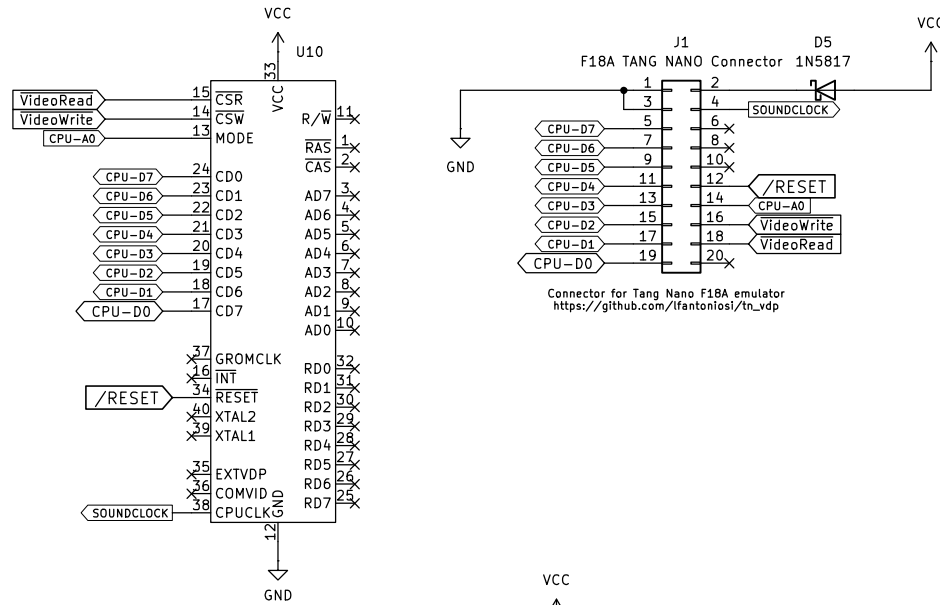
$$\begin{aligned} &= \text{MEMEN} + \text{ROMEN} + \text{RA15} \\ &= \text{MEMEN} + \text{ISFE} + \text{RA15} + \text{CPU-A7} + \text{CPU-A6} + \text{USER} + \text{CPU-A5} + \text{CPU-A4} + \text{CPU-A3} \\ &= \text{MEMEN} + \text{ISFE} + \text{RA15} + \text{CPU-A7} + \text{CPU-A6} + \text{USER} + \text{CPU-A5} + \text{CPU-A4} + \text{CPU-A3} \\ &= \text{MEMEN} + \text{ISFE} + \text{RA15} + \text{CPU-A7} + \text{CPU-A6} + \text{USER} + \text{CPU-A5} + \text{CPU-A4} + \text{CPU-A3} \\ &= \text{MEMEN} + \text{ISFE} + \text{RA15} + \text{CPU-A7} + \text{CPU-A6} + \text{USER} \\ &= \text{ONBOARD_RAM} + \text{ICFSEL} \\ &= \text{MEMEN} + \text{ISFE} + \text{ICFSEL} + \text{MAPSEL} + \text{I9902SEL} + \text{USER} + \text{RA15} \end{aligned}$$







TMS9918 Socket, suitable for a Pico99 or F18A TMS9918 emulator
Not suitable for an actual TMS9918 chip.



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Title: CortexPC

Size: A4 Date: 2025-05-25

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