

## Chip stress test in the CPUxxCMI

Chip	Bus 1 MHz		Bus 2 MHz		Bus 3 MHz		Bus 4 MHz	
ACIA's tested on CPUxxCMI and CPU09SR4								
HD6350	20	0	20	0	20	0	20	0
HD63B50	40	0	40	0	40	0	40	0
MC6850	15	0	15	0	15	0	15	0
MC68B50	13	0	13	0	13	0	13	0
CPU's tested on CPUxxCMI running FLEX								
HD6809	6	0	6	0	6	X	--	--
HD68B09	2	0	2	0	2	0	--	--
MC6809	5	0	5	0	5	X	--	--
MC6809L	2	0	2	X	--	--	--	--
MC68B09	3	0	3	0	3	0	--	--
HD63C09	40	0	40	0	40	0	40	0
CPU's tested on CPUxxCMI in Monitor								
S6802	21	0	21	0	21	0	--	--
MC68B02	10	0	10	0	10	0	--	--

Pcs      Fail      Pcs      Fail      Pcs      Fail      Pcs      Fail  
X Not working!  
-- Not tested.

\* C1 and C2 on the CPUxxCMI are 22pF for 1 & 2 MHz and 15pF for 3 & 4 MHz.

\* Rx 10M smd 1206 resistor between the crystal pins on the solder side.

For 1...4 MHz tests the CPUxxCMI with 16MHz modification and PAL CMI-4\_1 is used.

For 1...3 MHz tests are also done on the standard CPUxxCMI card.

All 09 CPU's are tested running FLEX, the HD63C09 is tested on many CPU09... cards.

All ACIA's are also tested on the CPU09SR4 running UniFLEX.

**Remarkable even all the 1 MHz ACIA's are working on the 16MHz boards.**

### BUT:

The CPUxxCMI has an issue with the oscillator print layout,  
due to the traces on pin-38 and pin-39 between the 68x09 and 68x02 socket.  
On the 68x09 pin-38 is EXTAL and on the 68x02 pin-39 is EXTAL.  
Since the PCB router used the names XTAL and EXTAL,  
the traces cross each other and also run parallel to some data lines.

The MC68x09 chips in particular don't like that and don't work with standard C1 and C2 values.

The 68x02 chips not have a problem with this.

The oscillator gain on the MC68x09 and HD68x09 chips is too low for a 12 MHz crystal.

CS came up with the 10M over the crystal as a solution for the 68x09 chips,  
this will increase the oscillator gain, so the 68B09 will work with a 12MHz crystal.

### Remarks:

The MC68x02 chips require synchronization the MRDY input with the 4f clock.  
Older MC6809 chips with mask code (G7F, T5A, P6F, T6M) require synchronization  
the MRDY input with the 4f clock. CPU09SR4 and CPU09US4 can give a problem