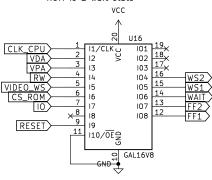
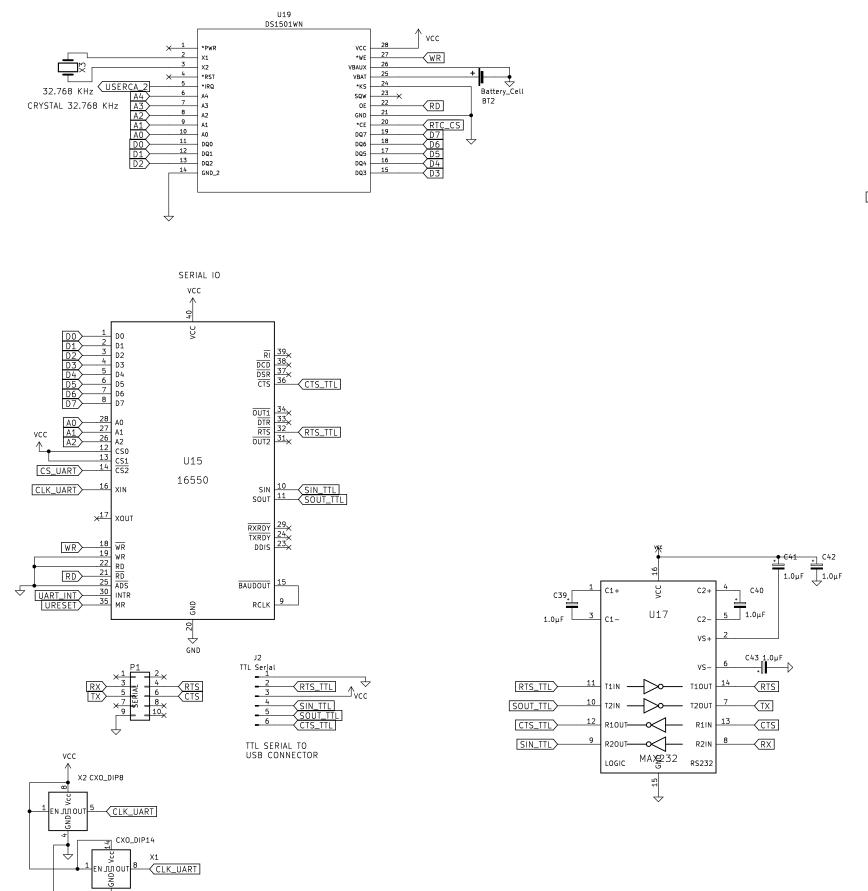
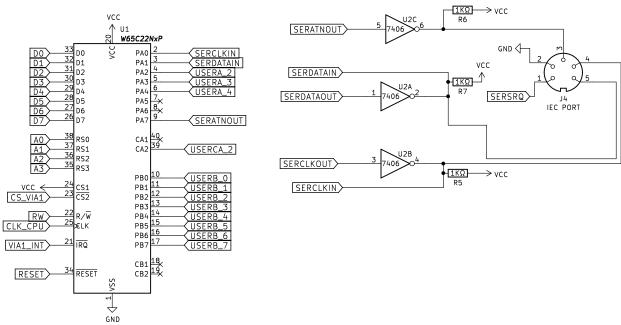
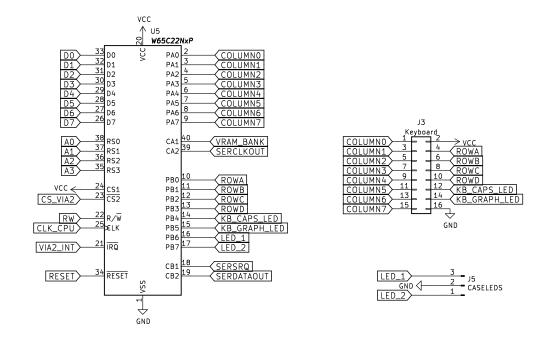


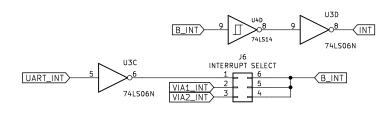
System can be ran with Wait State Generator (U16) out of system Video and IO are 2 wait states ROM is 1 wait state



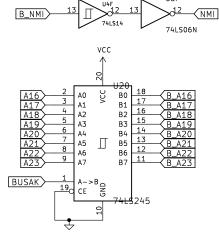


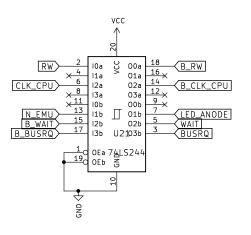


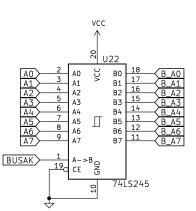




## BUS BUFFERING

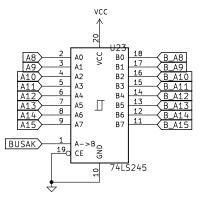


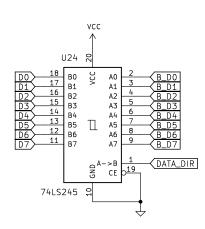


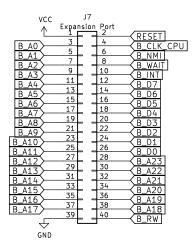


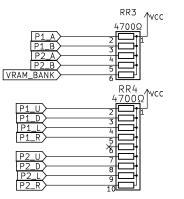
B\_WAIT B\_INT B\_NMI B\_BUSRQ

> INT NMI ABORT



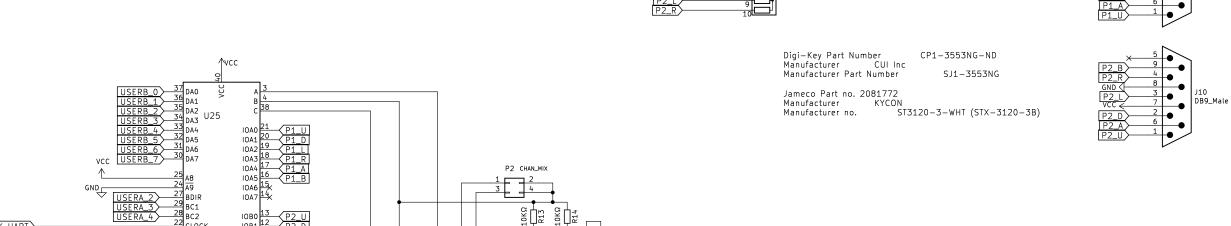






J1 AudioJack3

J9 DB9\_Male



1 2 C44 RV1 270 pF

270 pF

C47<sub>+</sub>

10KΩ R13

R11 10KΩ

2 2 1 10 KΩ

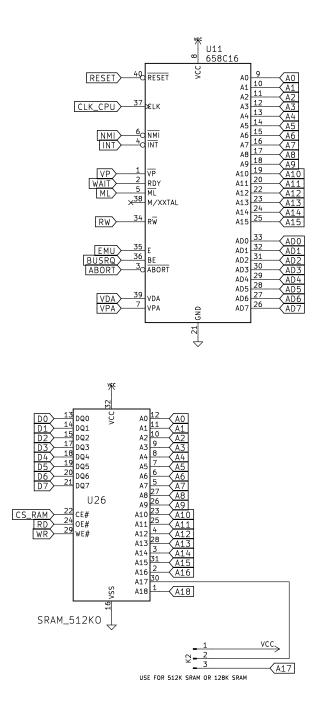
2 3 1 1 10 KΩ

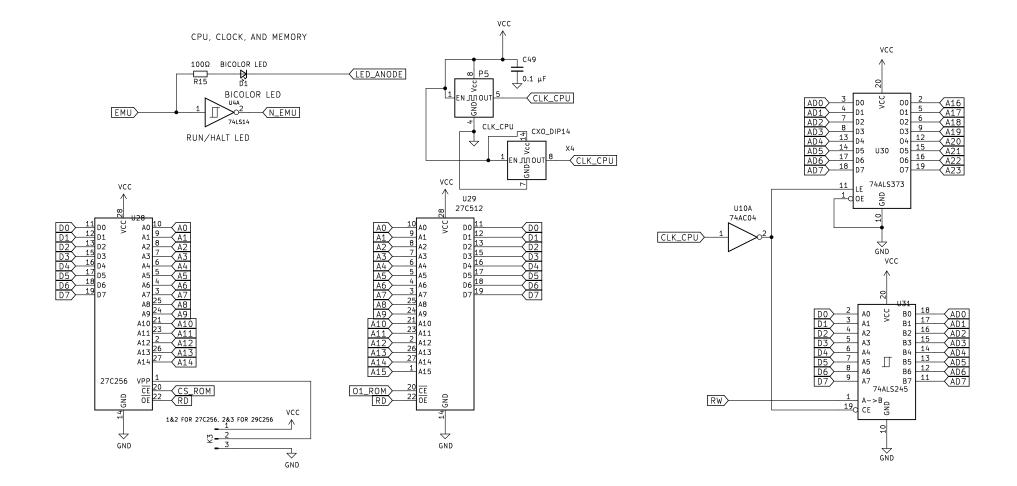
SH THE

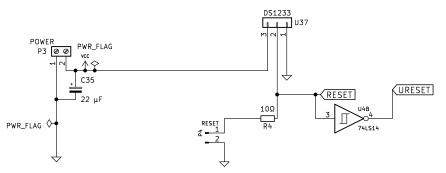
CLK\_UART>

26 SEL 1082 11 12 1082 23 RESET 1083 9 9 4Y - 3 - 8910 1085 8 8 7 7 8 1087 8 8 1087 8 8 1087

X39 TEST1







RESET SWITCH / POWER ON RESET / POWER SWITCH