In hisNAME		
Electronics II	DanialKhashabi(8723001)	Master: Dr.Yavari
Design Project	d.khashabi@gmail.com	

Note: All of simulations are done in HSPICE-2008 and all figures are plotted using "Avanwaves" plotter.

1-Multi-Stage Amplifier Simulation

The problem is to simulate a multi-stage amplifier. Nodes used for coding HSPICE simulation are shown in Fig.1.

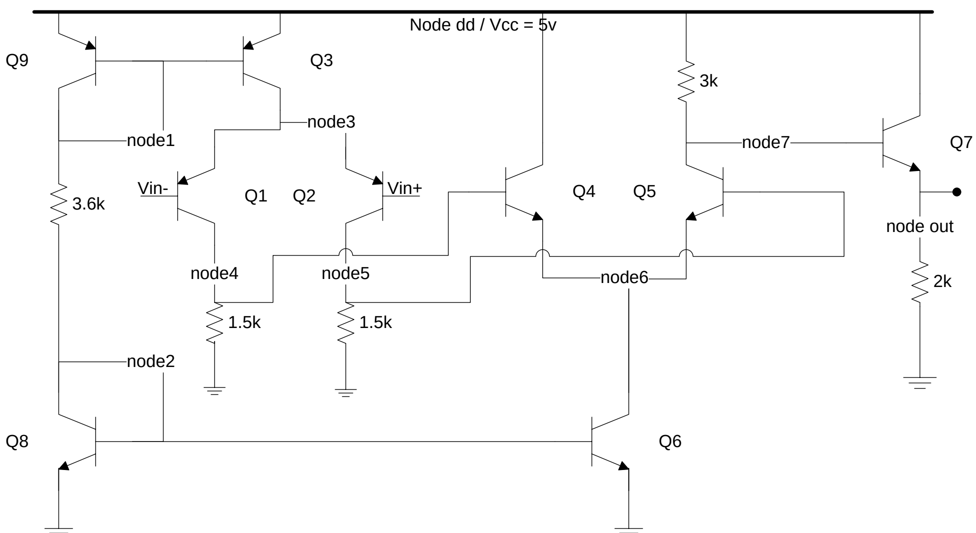

Fig.1.three stage amplifier.

Transistors are modeled as what introduced in project's context:

```
.model nmodnpn (bf = 100, is = 10f, vaf = 20, cje = 5f, cjc = 5f, cjs = 10f, tf = 5p )
.model pmodpnp (bf = 100, is = 10f, vaf = 20, cje = 5f, cjc = 6f, cjs = 10f, tf = 5p )
```

For transistor Q3 which has a double current in comparison to Q9, I_s is set to 20f.

This is the code implemented for simulating the circuit:

HSPICE code

```
Three-stage amplifier analysis

* Transistor Models:
.model nmodnpn (bf = 100, is = 10f, vaf = 20, cje = 5f, cjc = 5f, cjs = 10f, tf = 5p )
.model pmodpnp (bf = 100, is = 10f, vaf = 20, cje = 5f, cjc = 6f, cjs = 10f, tf = 5p )
* BJT with double Is:
.model pmod_2 pnp (bf = 100, is = 20f, vaf = 20, cje = 5f, cjc = 6f, cjs = 10f, tf = 5p )

* Active Elements:
q1      4       in-     3       pmod
q2      5       in+     3       pmod
q3      3       1       dd      pmod_2
q4      dd      4       6       nmod
q5      7       5       6       nmod
q6      6       2       0       nmod
q7      dd      7       out     nmod
q8      2       2       0       nmod
q9      1       1       dd      pmod

* Passive Elements:
rb      1       2       3.6k
```

```
r1      4       0       1.5k
r2      5       0       1.5k
r3      dd      7       3k
r4      out     0       2k

* Power Supplies:
* DC
vcc     dd      0       DC      +5
* This is a bias dc power supply added for biasing transistors:
v_com    com 0  2.5


* Simulation Supplies:
* Transient(maximum output swing):
* vi+           in+     com             sin(0   0.5     40k     0       3k      0)
* vi-           in- com         0


* DC Sweep:
*vi+            in+     0               2.5
*vi-            in-     0       2.5

* AC(frequency response)
vi1             in+     com             AC      1       0
vi2     in- com         0

*Analysis Types:
*.trans         1u              4m      10u
.ac             dec             1000    0.001   150G
*.dc            vi-             -5      5       0.1

.end
```

- **Maximum Output Voltage Swing:**
  Generally there are 2 methods of finding maximum output swing:
  1- Applying a decaying sinusoid voltage source to input pair. So the maximum swing can be found by visualizing output voltage, as bellow:

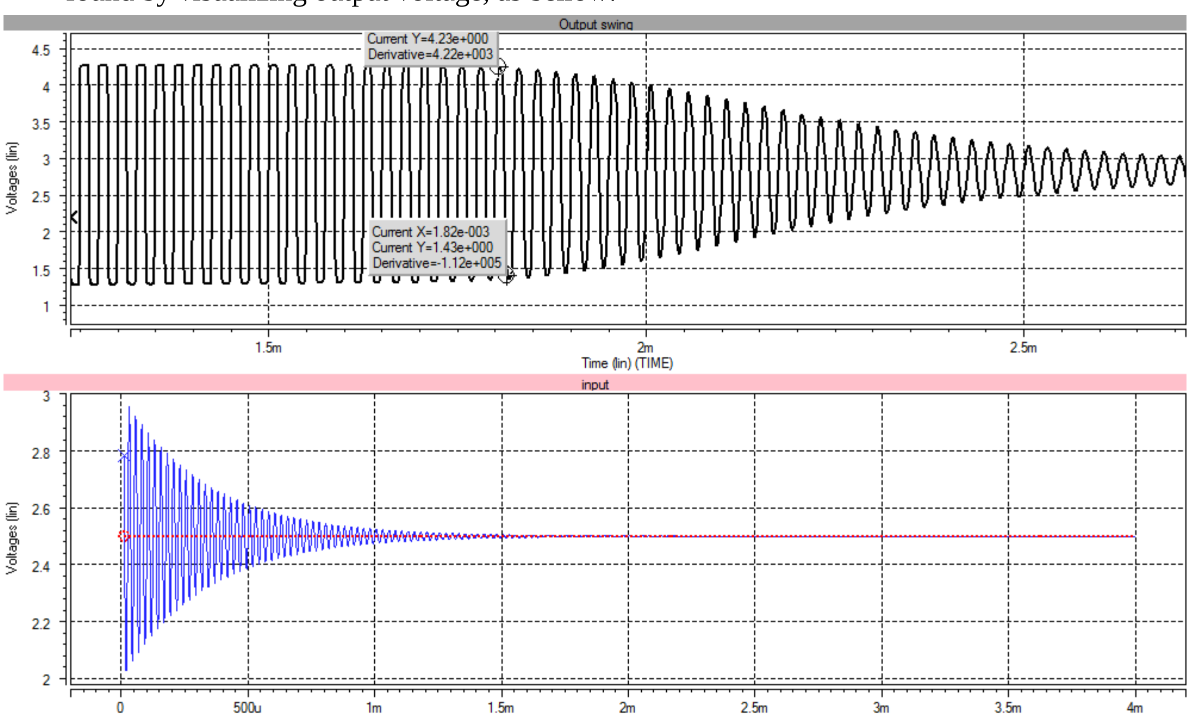

Fig.2. Output voltage swing when input is decaying sinusoids.

2- Finding circuits input-output voltage characteristic (Fig.3) using DC sweep analysis.

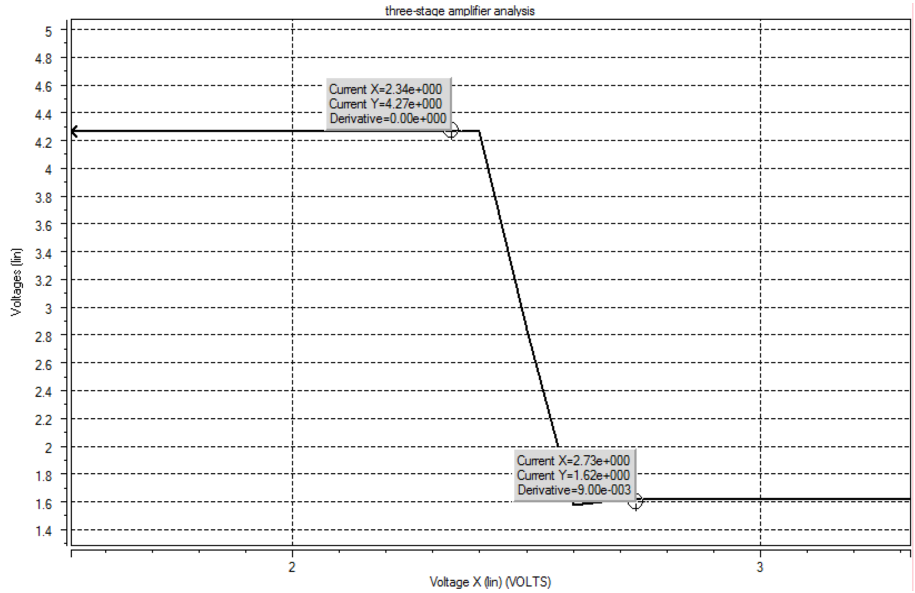

Fig.3. Voltage Input-Output Characteristic.

Regarding to Fig.1 and Fig.2:

$v_o^+ = 4.27$ (v)

$v_o^- = 1.62$ (v)

$\Longrightarrow$ Maximum Output Voltage Swing = (4.27-1.62)/2 = 1.325 (v)

- **Frequency Response:**

  This is done by applying two 0.5v AC power supplies with 180^o phase difference. The output voltage is plotted in Fig.4.

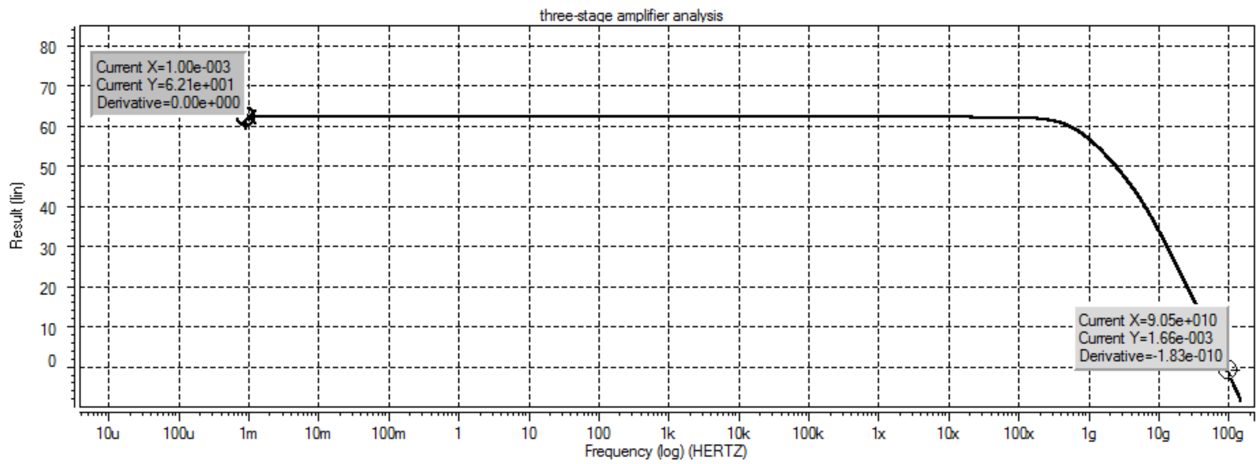

Fig.4. Frequency response of three-stage amplifier, when input is differential.

- **Unity gain frequency:**
  Based on frequency response figure(Fig.4):
  ⟹ Unity-gain Frequency(gain in 0dB) = 90.5 (GHz)

- **DC gain:**
  Based on frequency response:
  ⟹ DC gain(gain in 0 Hz) = 1270 (v/v) or 62.1 (dB)

- **Phase Margin:**
  The phase margin is the difference in phase between the phase curve and -180 degrees, at the point corresponding to the frequency that gives us a gain of 0dB(the unity gain crossover frequency). Regarding to Fig.5 we have:
  ⟹ Phase Margin = -177 – (-180) = 3^{o}

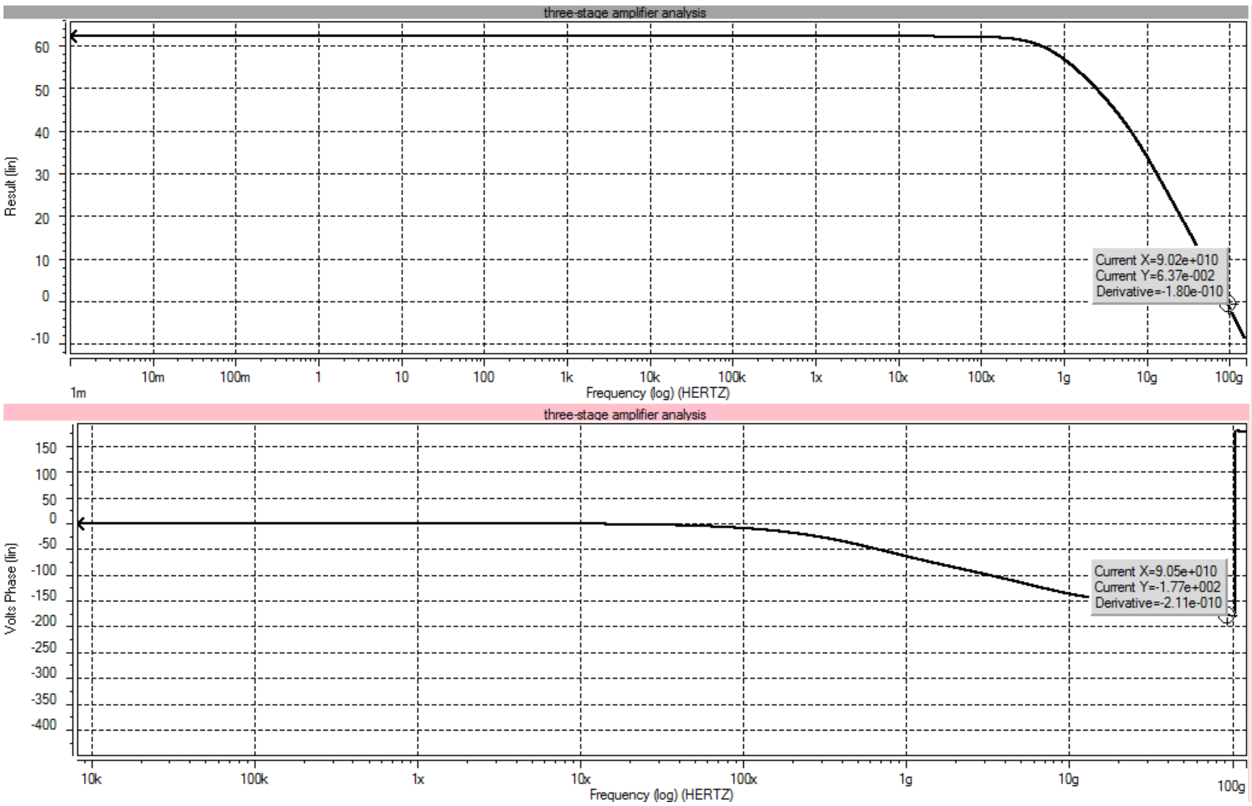

Fig.5. Frequency and phase response of three-stage amplifier, when input is differential.
In phase response, point with unity gain is measured.

2-Class AB Amplifier Simulation:

The problem is to simulate a class-AB power amplifier. Nodes used for coding HSPICE simulation is shown in Fig.6.

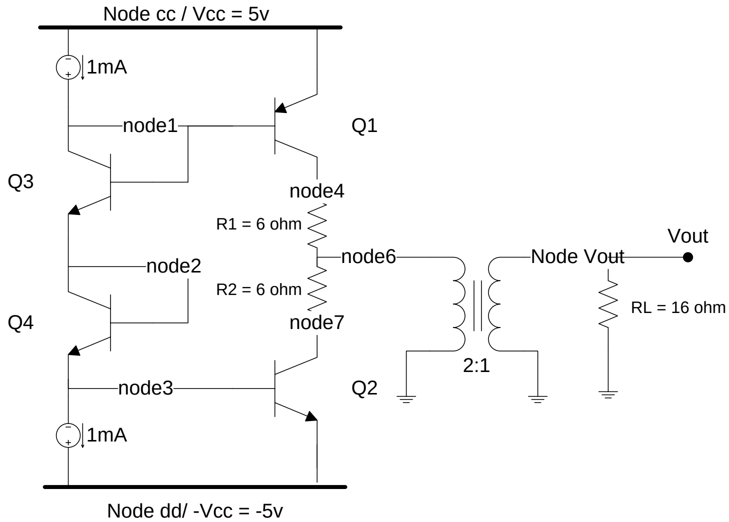

Fig.6. Power Amplifier

Anideal-transformer can be modeled in HSPICE as:

```
Exxx n+ n-TRANSFORMER in+ in- k
```

This is the code implemented for simulating the circuit:

HSPICE code

```
* Class AB Power Amplifier

*** Transistor Model Definition:
.model nmod_1 npn (bf = 50, is = 10f, vaf = 20, cje = 5f, cjc = 5f, cjs = 10f, tf = 5p )
.model nmod_2 npn (bf = 100, is = 2f, vaf = 20, cje = 5f, cjc = 5f, cjs = 10f, tf = 5p )
.model pmodpnp (bf = 50, is = 10f, vaf = 20, cje = 5f, cjc = 6f, cjs = 10f, tf = 5p )

*** Active Elements:
q1          cc      1       6       nmod_1
q2          dd      3       7       pmod
q3          1       1       2       nmod_2
q4          2       2       3       nmod_2

*** Passive Elements:
r1          6       4               6
r2          4       7               6

** Transient:
* rl        out     0               16
** DC Sweep:
rl          4       0               64

** Transient:
* E1        4       0       TRANSFORMER   out         0       0.5

*** Power Supplies:
* Bias:
i1          cc      1       dc            1m
i2          3       dd      dc            1m
v1          cc      0       dc            5
v2          dd      0       dc            -5

*** input:
** Transient:
```

```
vi              0       2       sin             0       12      2k      0       30      0
** DC Sweep:
* vi            0       2       5


*** Analysis:
.trans  1u              100m    1000
* .dc   vi              -7      7               0.2

.end
```

In analysis transformer is eliminated and it’s effect is taken into account. It isdone because it is assumed that the transformer is ideal. So it’s effect can be modeled simply with turn fractions.

We have:

$$\begin{cases} \frac{\hat{\imath}_4}{\hat{\imath}_o} = \frac{1}{2} \\ \frac{\hat{v}_4}{\hat{v}_o} = 2 \end{cases} \quad \rightarrow \frac{R_L^{'}}{R_L} = (2)^2 \rightarrow R_L^{'} = 64(\Omega)$$

Where $R_L^{'}$ is a resistance that is seen from left side if transformer. So we eliminate transformer and R_L put $R_L^{'}$ resistance.

- **Maximum Output Voltage Swing:**
  For getting maximum power conversion efficiency it is necessary to find maximum output swing. There are 2 ways to do it:
  1- Transient Analysis; A Decaying Sinusoid Supply:
  It is done by applying a decaying sinusoid voltage source to input. So the maximum swing can be find by visualizing output voltage, as what is shown in Fig.6.

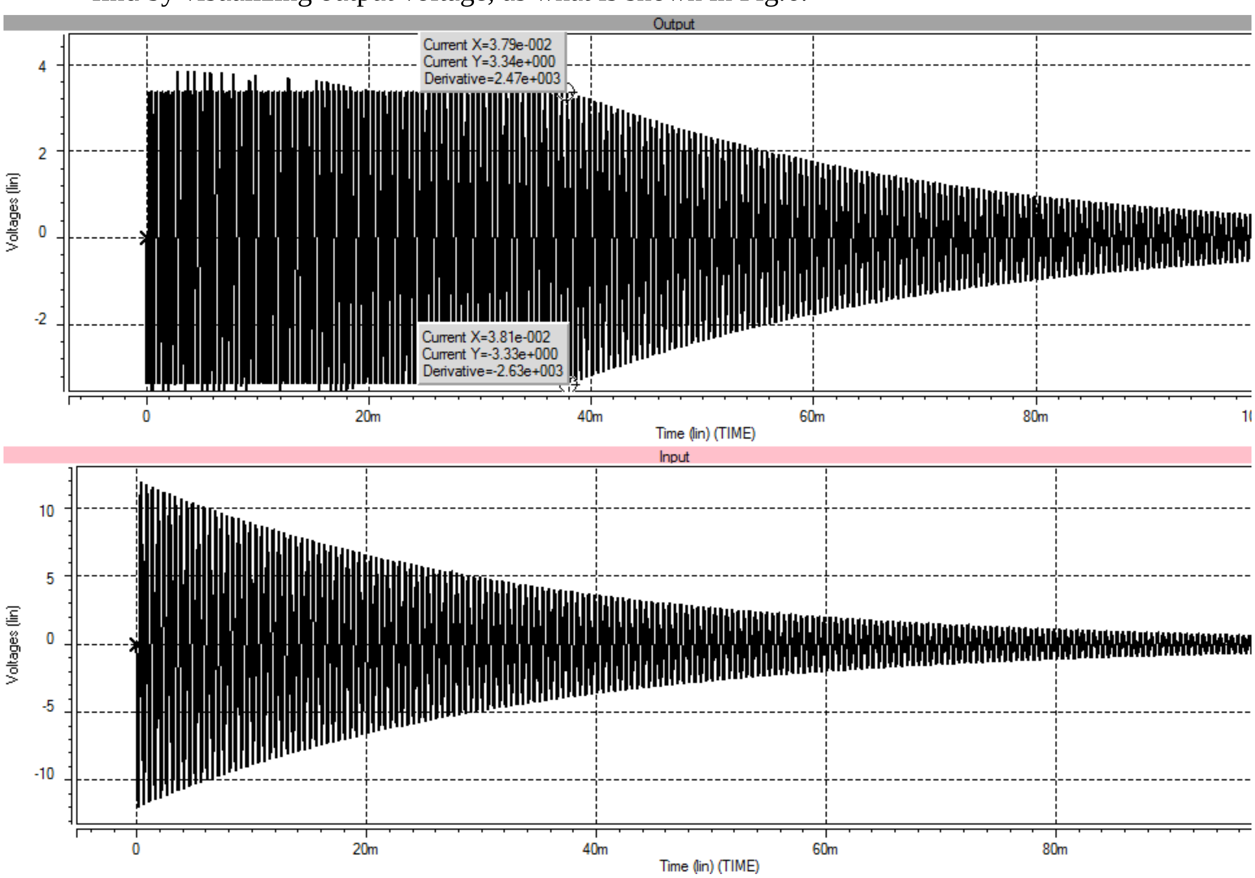

Fig.7. Output voltage swing and Input decaying signal

1- DC Sweep Analysis

In this analysis a dc voltage is used, when it changes from a minimum value to a maximum value. The characteristic figure(vi-vo figure) is shown in Fig.8. Limits on values of Vo are shown in figure.

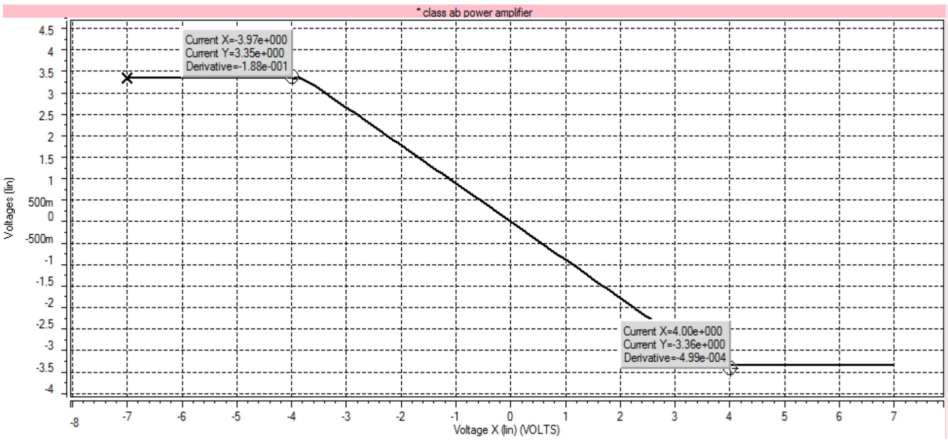

Fig.8. Voltage Input-Output Characteristic.

It is necessary to mention that both methods have same answers.

So, regarding to Fig.6 and Fig.7⟹Maximum Output Voltage Swing:$\hat{v}_4$=3.35 (v)⟹ $\hat{v}_0$=3.35/2=1.67 (v)

- **Maximum Power Conversion Efficiency(When output voltage is pure sinusoids):**

Regarding to above Fig.4:

$$\hat{v}_o = 1.67\,V$$

$$R_L = 16\Omega \qquad \rightarrow \qquad P_L = \frac{\hat{v}^2}{2R_L} = 87.15(mW)$$

In every half-phase a current with maximum $\frac{1}{N}\frac{\hat{v}}{R_L}$ passes throw the output stage, when N = 2 in transformer.

For measuring power given by DC power supplies:

$$\begin{cases} P_{ss}^{+} = Vcc \times \left(\frac{1}{\pi}\frac{1}{2}\frac{\hat{v}}{R_L}\right) = 5 * \left(\frac{1.67}{2\pi*16}\right) \\ P_{ss}^{-} = Vcc \times \left(\frac{1}{\pi}\frac{1}{2}\frac{\hat{v}}{R_L}\right) = 5 * \left(\frac{1.67}{2\pi*16}\right) \end{cases} \qquad \rightarrow \qquad P_{ss} = 2 * 5 * \left(\frac{1.67}{2\pi*16}\right) = 166.17\ (mW)$$

So the maximum power efficiency is:

$$\eta = \frac{P_L}{P_{ss}} = \frac{87.15}{166.17} = 52.46\ \%$$