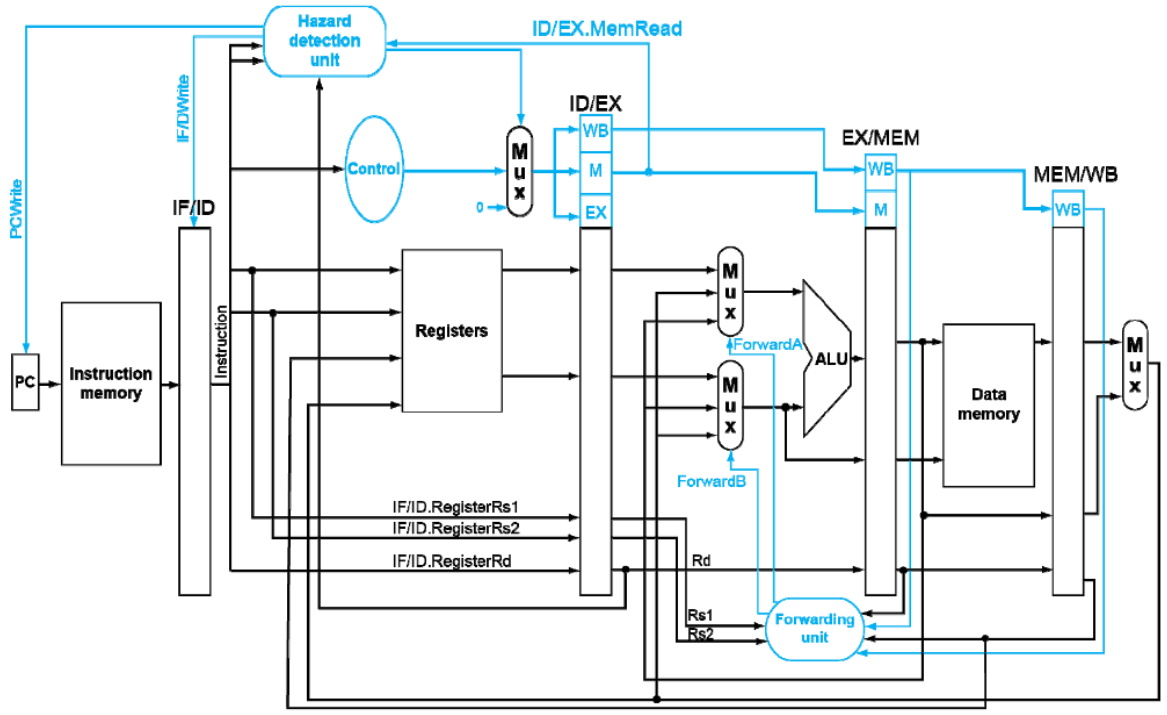
Computer Organization, Spring 2022

LAB 5 : 5-Stage Pipeline Processor

Due : 2022/6/1 23:59

1. Goal

In this lab you should modify the Single Cycle CPU designed from Lab4 and implement a 5-stage Pipeline Processor with IF, ID, EX, MEM and WB stages. For a pipeline processor design, a pipeline register module between each 2 stages is required and the pipeline registers are written when each positive clock edge is triggered. You also need to implement forwarding unit and hazard detection unit.



2. Attached file

- Lab5Answer (Don't modify these file)
- Lab5Code (Your code should put in here)
- lab5TestScript.sh
- readme.txt

3. HW Requirement

(1.) Please use the lab5TestScript.sh we provide you.

(2.) Please implement below

- **Adder.v**
- **ALU_Ctrl.v**
- **alu.v**
- **Decoder.v**
- **Forwarding.v**
- **Hazard_detection.v**
- **Imm_Gen.v**
- **MUX_2to1, 3to1.v**
- **Shift_Left_1.v**
- **Pipeline_CPU.v**
- **IFID_register.v**
- **IDEXE_register.v**
- **EXEMEM_register.v**
- **MEMWB_register.v**

(3.) Testcase

- Basic testcase (without data dependency) (30%)
  - Case 1~6
- Medium testcase (with data dependency) (40%)
  - Case 7~10
- Advanced testcase (30%)
  - Case 11~13
  - Load-use
  - beq and jal instruction

4. How to test

You can use any HDL simulator(Model Sim / Vivado / ISE), but also need to test your code with **lab5TestScript.sh (Only run in UNIX like OS)**. (TA's environment : Ubuntu 20.0.4)

- ❖ **We do not answer the bug of HDL simulator**
- ❖ **Do not modify *.txt file**

Command:

```
$ chmod +x ./lab5TestScript.sh && ./lab5TestScript.sh
```

- The last line is your score

```
==========================
testcase 1 pass
testcase 2 pass
testcase 3 pass
testcase 4 pass
testcase 5 pass
testcase 6 pass
testcase 7 pass
testcase 8 pass
testcase 9 pass
testcase 10 pass
testcase 11 pass
testcase 12 pass
testcase 13 pass
============================================
Basic Score:30
Medium Score:40
Advanced Score:30
Total Score:100
```

5. Grade

5-Stage Pipeline Processor (80%)
Report (20%)

- Detailed description of the implementation
- Implementation results
- Problems encountered and solutions

❖ Late submission: 10% penalty per day
❖ No plagiarism, or you will get 0 points

6. Hand in

- Zip your folder and name it as "**$(groupN)_$(studentid1)_$(studentid2).zip**" (e.g. 1_109000001_109000002.zip) before uploading to e3. Other filenames and formats such as *.rar and *.7z are NOT accepted
  - report.pdf
  - *.v
- Your report should be in **PDF** format.

7. Q&A

- Feel free to ask on HackMD if you need.
    - Lab5 討論區
- We will not debug for you.

8. Reference

- RISC-V card