Computer Organization, Spring 2022

LAB 3 : Single-Cycle CPU (Simple version)

Due : 2022/4/27 23:59

1. Goal

Utilizing the ALU in Lab2 to implement a Simple Single-Cycle CPU. CPU is the most important unit in computer system. Read the document carefully and do the Lab, and you will have the elementary knowledge of CPU.

2. Attached file

- Lab3Answer (Don't modify these file)
- Lab3Code (Your code should put in here)
- lab3TestScript.sh
- readme.txt

3. HW Requirement

(1.) Please use the lab3TestScript.sh we provide you.

(2.) Please implement **Decoder.v , Adder.v , ALU.v , ALU_Ctrl.v, Simple_Single_CPU.v** file we provide you.

(2.) Instruction (80%)

Instruction	Example	Meaning	Opcode	Funct3	Funct7
Addition	add r1, r2, r3	r1 = r2 + r3	0110011	000	0000000
Subtraction	sub r1, r2, r3	r1 = r2 - r3	0110011	000	0100000
Bitwise and	and r1, r2, r3	r1 = r2 & r3	0110011	111	0000000
Bitwise or	or r1, r2, r3	r1 = r2 | r3	0110011	110	0000000
Exclusive OR	xor r1, r2, r3	r1 = r2 ⊕ r3	0110011	100	0000000

Set on less than	slt r1, r2, r3	if(r2 < r3)
		r1 = 1
		else
		r1 = 0
			0110011	010	0000000

Shift left logical	sll r1, r2, r3	r1 = r2 << r3	0110011	001	0000000
Shift right arithmetic	sra r1, r2, r3	r1 = r2 >>> r3	0110011	101	0100000

4. How to test

You can use any HDL simulator(Model Sim / Vivado / ISE), but also need to test your code with **lab3TestScript.sh (Only run in UNIX like OS)**. (TA's environment : Ubuntu 20.0.4)

- ❖ **We do not answer the bug of HDL simulator**
- ❖ **Do not modify *.txt file**

Command:

```
$ chmod +x ./lab3TestScript.sh && ./lab3TestScript.sh
```

- The last line is your score

```
*************** CASE 1 ******************
Testcase 1 PASS
*************** CASE 2 ******************
Testcase 2 PASS
*************** CASE 3 ******************
Testcase 3 PASS
*************** CASE 4 ******************
Testcase 4 PASS
*************** CASE 5 ******************
Testcase 5 PASS
*************** CASE 6 ******************
Testcase 6 PASS
*************** CASE 7 ******************
Testcase 7 PASS
*************** CASE 8 ******************
Testcase 8 PASS
*************** CASE 9 ******************
Testcase 9 PASS
*************** CASE 10 ******************
Testcase 10 PASS
=========================================
Total Score:100
```

5. Grade

Single Cycle CPU (80%)
Report (20%)

- Detailed description of the implementation
- Implementation results
- Problems encountered and solutions

❖ Late submission: 10% penalty per day
❖ No plagiarism, or you will get 0 points

6. Hand in

- Zip your folder and name it as “學號.zip” (e.g. 109000001.zip) before uploading to e3. Other filenames and formats such as *.rar and *.7z are NOT accepted
- Please include ONLY Verilog code (*.v) and your report (*.pdf) in the zipped folder.
- Rename your report to "Report_學號.pdf” (e.g. Report_109000001.pdf)

7. Q&A

- Feel free to ask on HackMD if you need.
  - Lab3 討論區
- We will not debug for you.