Computer Organization, Spring 2022

LAB 2 : 32-bit ALU

Due : 2022/4/6 23:59

1. Goal

The goal of this LAB is to implement a 32-bit ALU (Arithmetic Logic Unit). ALU is the basic computing component of a CPU. Its operations include AND, OR, addition, subtraction, etc. This series of LABs will help you understand the CPU architecture. LAB 3 will be reused; you will use this module in the later LABs.

2. Attached file

- alu_1bit.v
- alu.v
- MUX2to1.v
- MUX4to1.v
- testbench.v
- alu_1bit_tb.v
- *.txt (testcase)

3. HW Requirement

(1.) Please use the testbench.v we provide you.

(2.) Please implement **alu_1bit.v , alu.v , MUX2to1.v , MUX4to1.v** file we provide you.

(2.) Basic instruction set (70%)

ALU action	Function	ALU control input
and	AND	0000
or	OR	0001
add	Addition	0010
sub	Subtract	0110
slt	Set less than	0111
nor	NOR	1100
nand	NAND	1101

(3.) ZCV three flags : zero, carry out and overflow (30%)

- zero : must be set when the output is 0
- cout : must be set when the carry out is 1
- overflow: must be set when overflow happens

4. How to test

You can use any HDL simulator(Model Sim / Vivado / ISE), but also need to test your code with iverilog(Icarus Verilog) and make sure your code can run with iverilog. We will use iverilog to grade Lab2. (TA's environment : Ubuntu 20.0.4)

- ❖ **We do not answer the bug of HDL simulator**
- ❖ **Do not modify *.txt file**

Command:

```
$ iverilog -o lab2 alu.v alu_1bit.v testbench.v MUX*
$ ./lab2
```

- If you see “Congratulation!” you will get 100 points.

```
****************************************************
*              PATTERN RESULT TABLE                *
****************************************************
* PATTERN *              Result              * ZCV *
****************************************************
*      Congratulation! All data are correct!       *
****************************************************
Correct Count: 30
```

5. Grade

32-bit ALU implementation (80%)

- Basic instruction score : 70 points
- ZCV flags score : 30 points

Report (20%)

- Detailed description of the implementation
- Implementation results
- Problems encountered and solutions

❖ Late submission: 10% penalty per day

❖ No plagiarism, or you will get 0 points

6. Hand in

- Zip your folder and name it as “學號.zip” (e.g. 109000001.zip) before uploading to e3. Other filenames and formats such as *.rar and *.7z are NOT accepted
- Please include ONLY Verilog code (*.v) and your report (*.pdf) in the zipped folder.
- Rename your report to "Report_學號.pdf” (e.g. Report_109000001.pdf)

7. Q&A

- Feel free to ask on HackMD if you need.
  - Lab2 討論區
- We will not debug for you.