

Lab6-Cache Simulator

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Notice

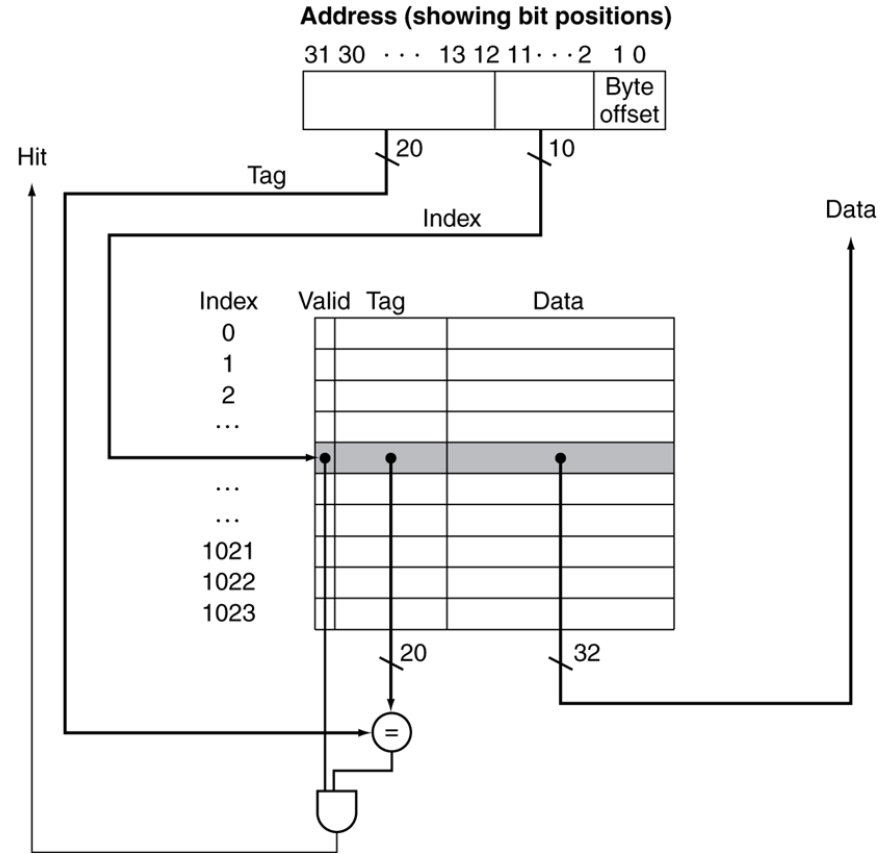
- This lab intends to help you understand in detail how a cache implementation works.
- **Good news: We will provide a template and written in C++ style**
- Lab6 is a group work
- Please follow group ID from the previous lab
- [Lab6討論區](#)

Attached file

- **TODO**
 - ◆ `direct_mapped_cache.cpp`
 - ◆ `set_associative_cache.cpp`
- **RUN**
 - ◆ `./demo.sh`(Lab6 need to run in **UNIX-like** operating system)

Direct Mapped Cache

- 32-bit addresses
- Direct-mapped cache
- Block size: 4B
 - Offset: need 2-bit size
- Cache size: Hold 4KB
 - Index: need 10-bit size
- Tag: 20-bit size ($32 - 10 - 2 = 20$)



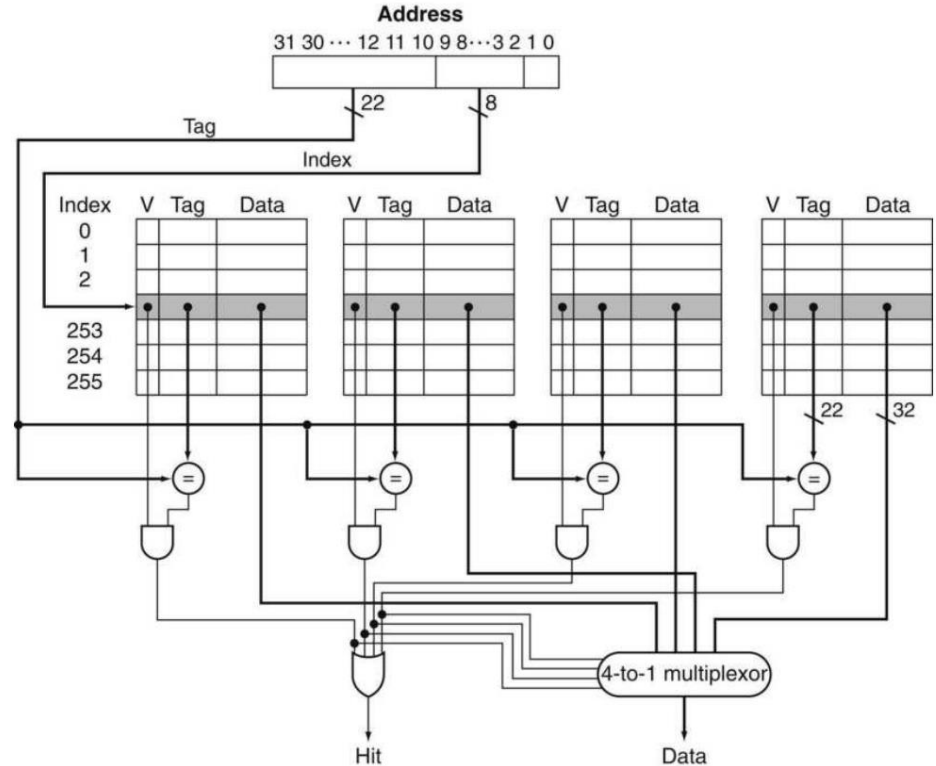
Directed-mapped result (Schematic diagram)

- Complete the following results table

| Miss rate | | Block size (Byte) | | | | |
|----------------------|------|-------------------|----|----|-----|-----|
| | | 16 | 32 | 64 | 128 | 256 |
| Cache size (Byte) | 4k | | | | | |
| | 16k | | | | | |
| | 64k | | | | | |
| | 256k | | | | | |

Set Associative Cache

- 32-bit addresses
- 4-way set associative cache
- Block size: 4B
 - Offset: need 2-bit size
- Cache size: 4KB
 - # of index: $1024/4 = 256$
 - Index: need 8-bit size
- Tag: 22-bit size($32-8-2=22$)



Replacement policy: LRU

- In an associative cache, we have a choice of which block to replace
- The most commonly used scheme is **least recently used (LRU)**, which we used in this lab
- LRU: Replace the one that has been unused for the longest time

| Address of memory block accessed | Hit or miss | Contents of cache blocks after reference | | | |
|----------------------------------|-------------|--|-----------|-------|-------|
| | | Set 0 | Set 0 | Set 1 | Set 1 |
| 0 | miss | Memory[0] | | | |
| 8 | miss | Memory[0] | Memory[8] | | |
| 0 | hit | Memory[0] | Memory[8] | | |
| 6 | miss | Memory[0] | Memory[6] | | |
| 8 | miss | Memory[8] | Memory[6] | | |

N-way set-associative result (Schematic diagram)

- Complete the following results table

| Miss rate | | Associativity (Block size:64B) | | | |
|----------------------|-----|--------------------------------|-------|-------|-------|
| | | 1-way | 2-way | 4-way | 8-way |
| Cache size (Byte) | 1k | | | | |
| | 2k | | | | |
| | 4k | | | | |
| | 8k | | | | |
| | 16k | | | | |
| | 32k | | | | |

Sample test cases

- Direct mapped

| Miss rate | | Block size (Byte) | | | | |
|-------------------|------|-------------------|----------|-----------|-----------|-----|
| | | 16 | 32 | 64 | 128 | 256 |
| Cache size (Byte) | 4k | 0.0795226 | | | | |
| | 16k | | 0.042784 | | | |
| | 64k | | | 0.0234072 | | |
| | 256k | | | | 0.0151914 | |

- Set Associative

| Miss rate | | Associativity (Block size:64B) | | | |
|-------------------|-----|--------------------------------|-----------|-----------|-----------|
| | | 1-way | 2-way | 4-way | 8-way |
| Cache size (Byte) | 1k | | | | |
| | 2k | 0.0827779 | | | |
| | 4k | | 0.0362734 | | |
| | 8k | | | 0.0266625 | |
| | 16k | | | | 0.0229422 |
| | 32k | | | | |