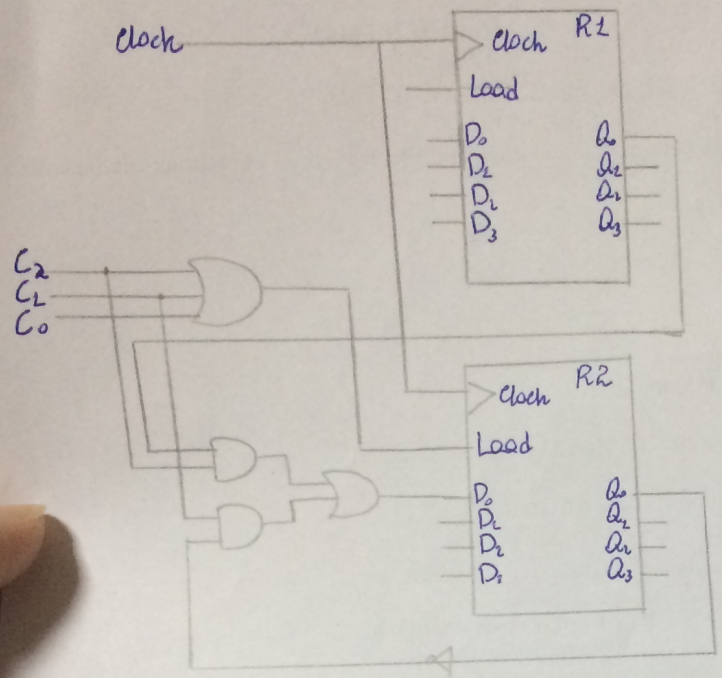
(19) 2 4-bit registers R_1 and R_2

C_0: $R2 \leftarrow 0$

C_1: $R2 \leftarrow \overline{R2}$

C_2: $R_2 \leftarrow R_1$



(22) A register cell for register B: S_1: $B \leftarrow B+A$

S_0: $B \leftarrow B+1$

B_i	A_i	C_i	B_{i+1}	C_{i+1}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

S_0	B_i	CB_{i+1}	B_{i+1}	C_{i+1}
1	0	0	0	0
1	0	1	0	0
1	1	0	1	0
1	1	1	1	1

B_i	B_{i+1}	C_{i+1}
0	1	0
1	0	1