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Homework 4

Chapter 4

③ Given: 00110101 11001010

a) Clear odd positions to zero
AND with 01010101 01010101

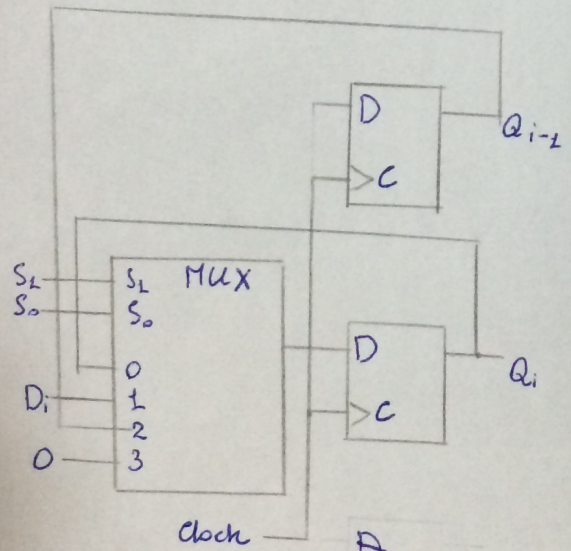
So:
$$\begin{array}{r} 00110101\ 11001010 \\ \wedge\ 01010101\ 01010101 \\ \hline 00010101\ 01000000 \end{array}$$

b) set rightmost 4 bits to 1
OR with 0000000000001111

c) complement the most significant 8 bits
XOR with 1111111100000000

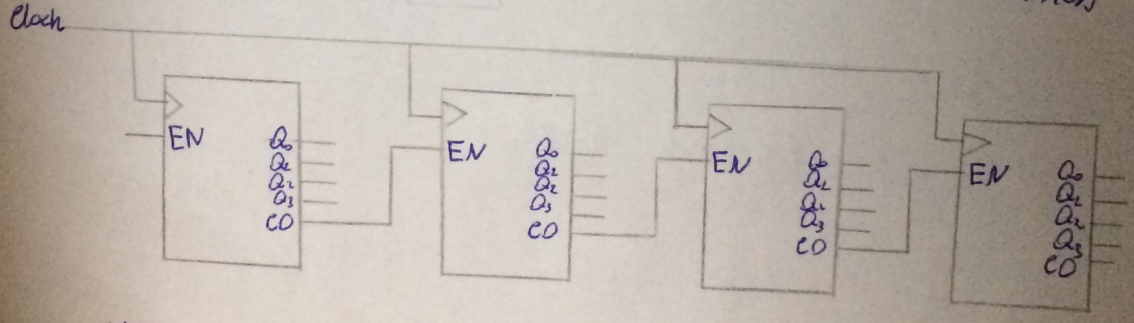
④ 8 bit operand: 11001010
Shift left: 10010100 Shift right: 01100101

⑤



S_1	S_0	Register Operation
0	0	~~Load parallel data~~ No change
0	1	Load parallel data
1	0	Shift down
1	1	Clear register to 0

⑩ 16-bit serial-parallel counter using four 4-bit parallel counters



Maximum # of AND gates – 4