

A

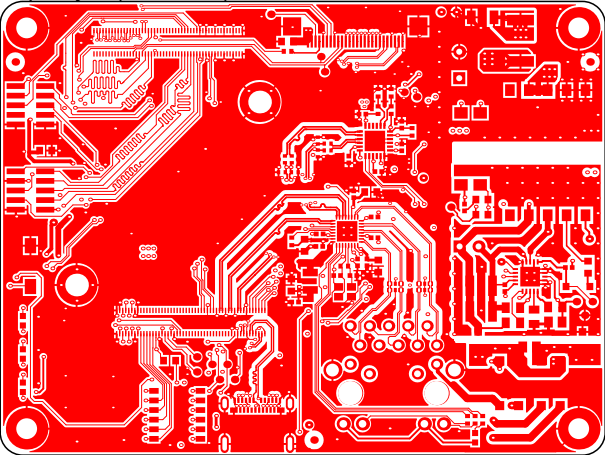
B

C

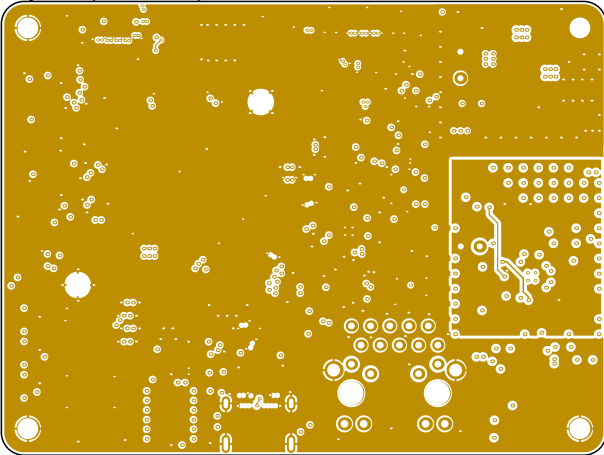
D

E

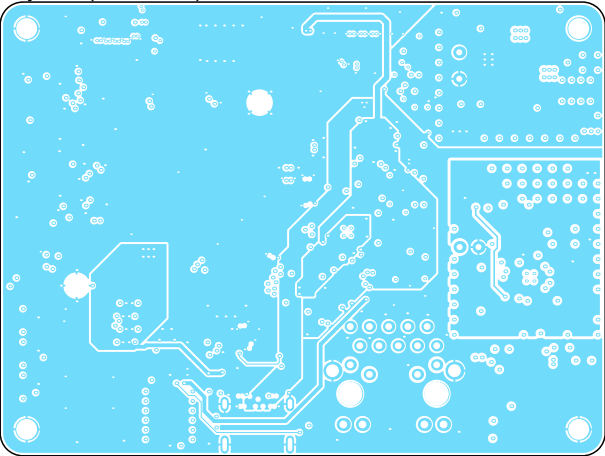
Top Layer (Scale 1:1)



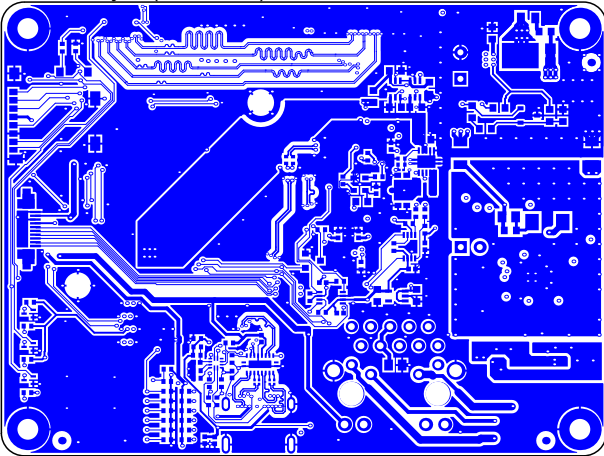
Layer 2 (Scale 1:1)



Layer 3 (Scale 1:1)



Bottom Layer (Scale 1:1)



FABRICATION NOTES:

Fabricate per IPC-6011 & IPC-6012 CLASS 2
Inspect per IPC-A-600 CLASS 2
Test per IPC-TM-650

- * PCB has 4 copper layers
- * Copper thicknesses are finished and include base foil plus Cu plating on plated layers.
- * PCB thickness: 63mil +/- 3mil
- * Min. trace width/clearance: 4/4mil
- * Min. hole drill/ring: 8mil/16mil
- * All vias-in-pad shall be plugged and plated over (VIPPO)
- * Soldermask gang relief is allowed for pads in same footprint, if footprint is NSMD.
- * Silkscreen, non-conductive epoxy ink, color: white
- * Soldermask colour: Green
- * Remove silkscreen as needed to prevent ink on any exposed copper
- * Surface finish: ENIG
- * Hole dimensions are finished size, +/-3mil
- * Linear board dimension tolerance: +/-10mil
- * Bow, twist, warp not to exceed 0.75% of greatest diagonal span
- * PCB shall be UL Recognized printed wiring board (ZPMV2), minimum flammability rating 94V-0
- * PCB shall be marked with fabricator company or trade name, UL mark, and date code using legend ink on secondary side
- * All PCBs shall be electrically tested for opens and shorts per gerber. Test marking shall be marked on second side.

Fabricator shall panelize the PCB using mouse bites and tab routing. V-scoring not allowed.

Controlled impedance differential pairs shall be within +/-10% of target impedance. See sheets below for more detail.

Title: **BW2098POE**

Number: D2098000

Revision: R4M1
E3

Date: 22/05/2024

Sheet: 1 of 5

Drawn by: Brian Weinstein

LUXonjs

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Layer Stack Legend

Layer	Thickness	Type	Gerber	Df	Dk
Top Overlay		Legend	GTO		
Top Solder	0.59mil(0.015mm)	Solder Mask	GTS		3,8
Top Layer	1.69mil(0.043mm)	Signal	GTL		
	8.27mil(0.210mm)	Dielectric		0,013	4,2
Layer 2	1.42mil(0.036mm)	Signal	G1		
	39.37mil(1.000mm)	Dielectric		0,013	4,2
Layer 3	1.42mil(0.036mm)	Signal	G2		
	8.27mil(0.210mm)	Dielectric		0,013	4,2
Bottom Layer	1.69mil(0.043mm)	Signal	GBL		
Bottom Solder	0.59mil(0.015mm)	Solder Mask	GBS		3,8
Bottom Overlay		Legend	GBO		
Total thickness: 63.31mil(1.608mm)					

Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
⊙	145	8.00mil(0.203mm)	Plated	
⊞	416	10.00mil(0.254mm)	Plated	
▽	4	23.62mil(0.600mm)	Plated	
□	4	31.50mil(0.800mm)	Plated	
○	14	35.43mil(0.900mm)	Plated	
◇	4	40.16mil(1.020mm)	Plated	
⊕	2	66.93mil(1.700mm)	Plated	
⊛	4	108.27mil(2.750mm)	Plated	
⊛	2	118.11mil(3.000mm)	Plated	
⊛	2	125.98mil(3.200mm)	Plated	+/-0.00mil(0.000mm)
597 Total				

Title: **BW2098POE**

Number: D2098000 Revision: R4M1
E3

Date: 22/05/2024 Sheet: 2 of 5

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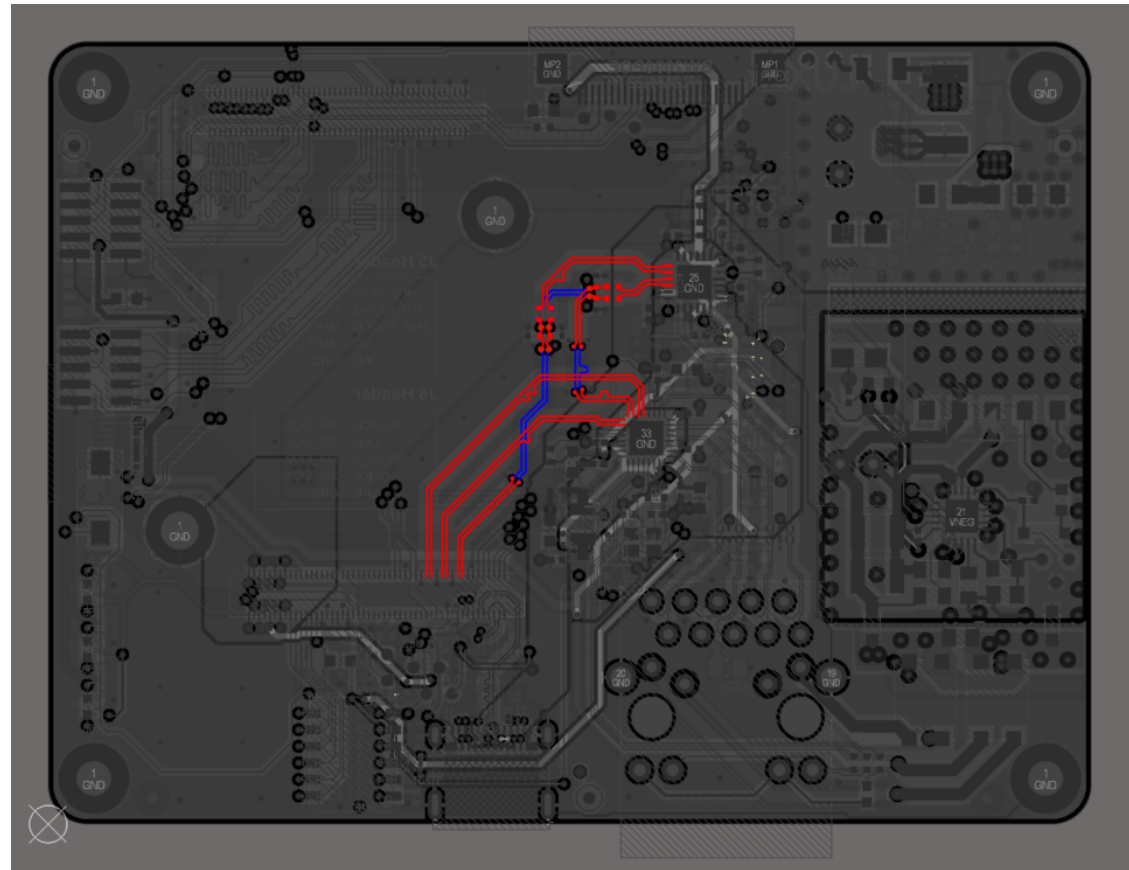
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85 OHM (+/-10%) DIFF PAIRS

PCIe differential pairs



Transmission Line Structure Table

Target Impedance	Calculated Impedance	Trace layer	Lower Trace Width	Upper Trace Width	Gap	Reference layers
100	99.96	Top Layer	5.1mil(0.130mm)	5.1mil(0.130mm)	4.0mil(0.102mm)	Layer 2
90	91.41	Top Layer	7.0mil(0.178mm)	7.0mil(0.178mm)	4.0mil(0.102mm)	Layer 2
85	85.01	Top Layer	8.8mil(0.223mm)	8.8mil(0.223mm)	4.0mil(0.102mm)	Layer 2
100	99.99	Layer 2	2.6mil(0.066mm)	2.0mil(0.052mm)	4.0mil(0.102mm)	Top Layer,Layer 3
90	90.00	Layer 2	3.4mil(0.087mm)	3.4mil(0.087mm)	4.0mil(0.102mm)	Top Layer,Layer 3
85	85.00	Layer 2	4.3mil(0.110mm)	4.3mil(0.110mm)	4.0mil(0.102mm)	Top Layer,Layer 3
100	99.99	Layer 3	2.6mil(0.066mm)	2.0mil(0.052mm)	4.0mil(0.102mm)	Layer 2,Bottom Layer
90	90.00	Layer 3	3.4mil(0.087mm)	3.4mil(0.087mm)	4.0mil(0.102mm)	Layer 2,Bottom Layer
85	85.00	Layer 3	4.3mil(0.110mm)	4.3mil(0.110mm)	4.0mil(0.102mm)	Layer 2,Bottom Layer
100	99.96	Bottom Layer	5.1mil(0.130mm)	5.1mil(0.130mm)	4.0mil(0.102mm)	Layer 3
90	91.41	Bottom Layer	7.0mil(0.178mm)	7.0mil(0.178mm)	4.0mil(0.102mm)	Layer 3
85	85.01	Bottom Layer	8.8mil(0.223mm)	8.8mil(0.223mm)	4.0mil(0.102mm)	Layer 3

Xonjs

INTIAL

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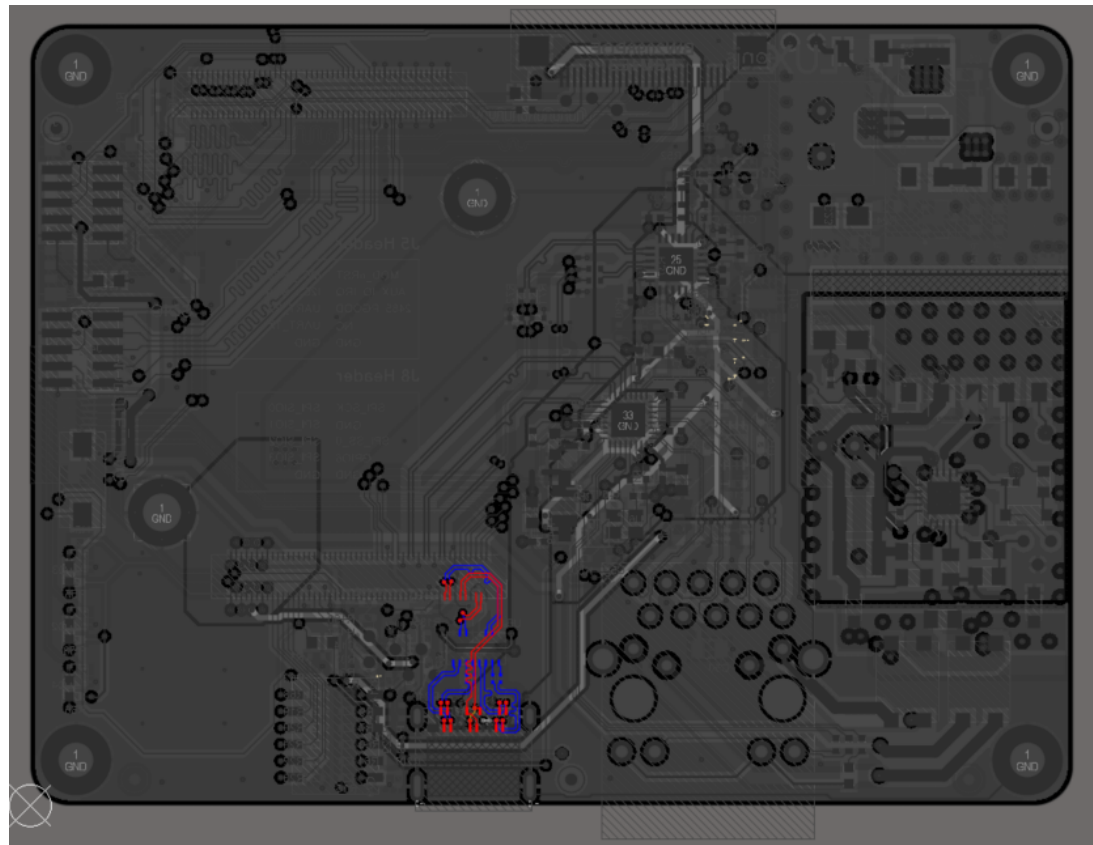
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90 OHM (+/-10%) DIFF PAIRS

USB differential pairs



Transmission Line Structure Table

Target Impedance	Calculated Impedance	Trace layer	Lower Trace Width	Upper Trace Width	Gap	Reference layers
90	91.41	Top Layer	7.0mil(0.178mm)	7.0mil(0.178mm)	4.0mil(0.102mm)	Layer 2
90	91.41	Bottom Layer	7.0mil(0.178mm)	7.0mil(0.178mm)	4.0mil(0.102mm)	Layer 3

Title: BW2098POE	
Number: D2098000	Revision: R4M1 E3
Date: 22/05/2024	Sheet: 4 of 5
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