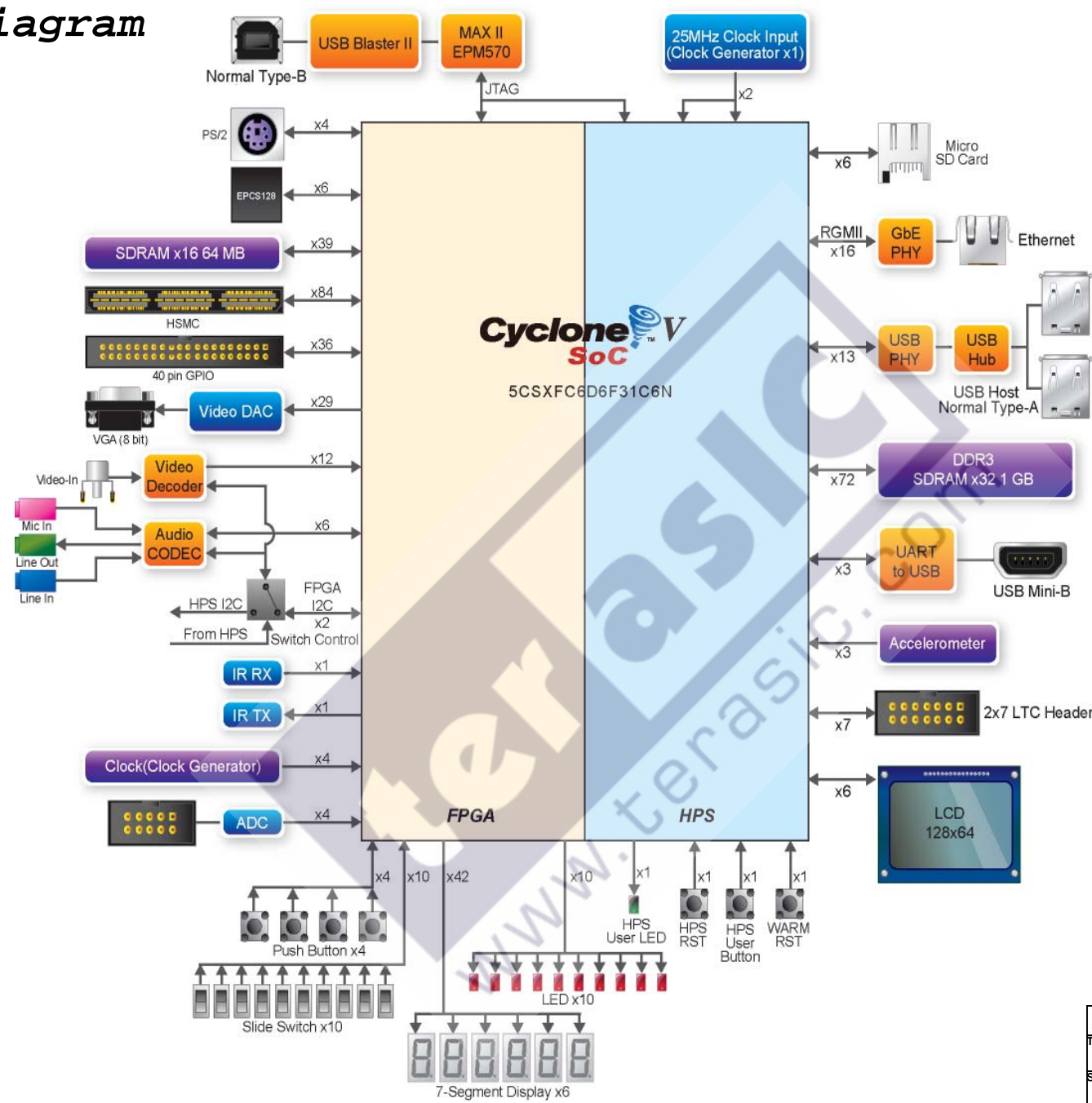
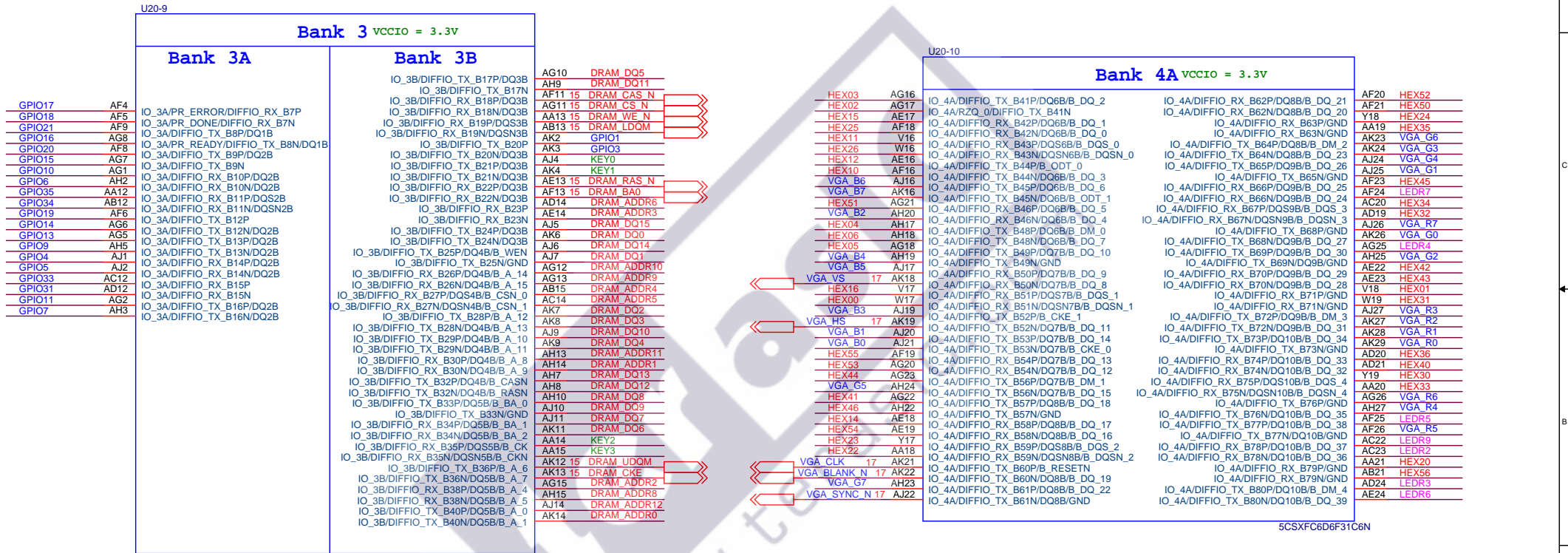


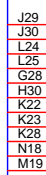
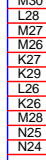
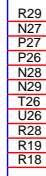
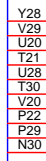
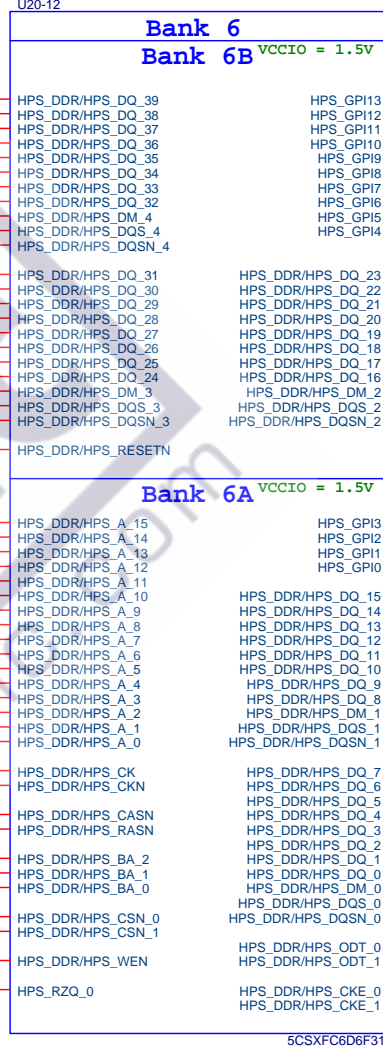
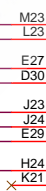
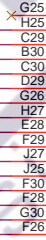
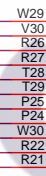
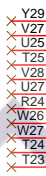
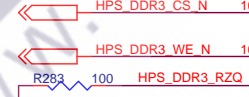
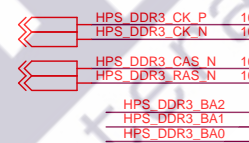
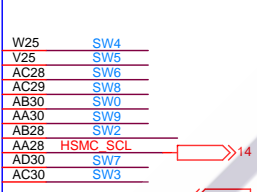
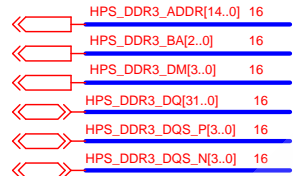
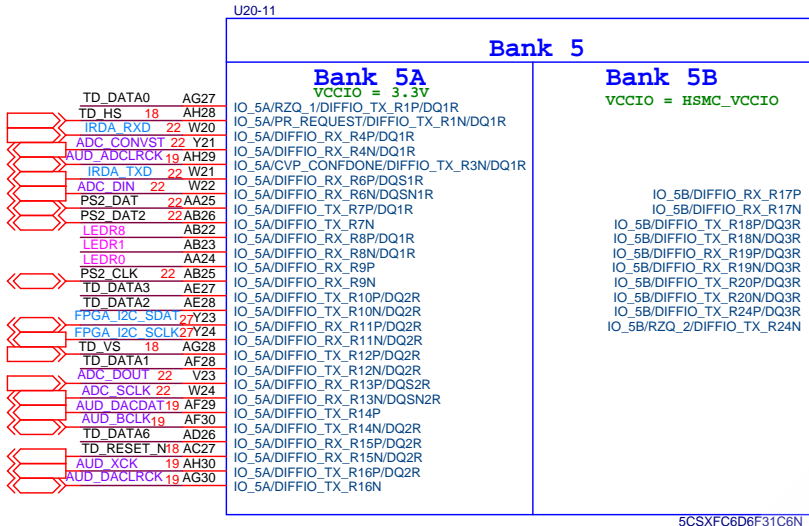
ALTERA Cyclone V SoC Development & Education Board (DE10-Standard)

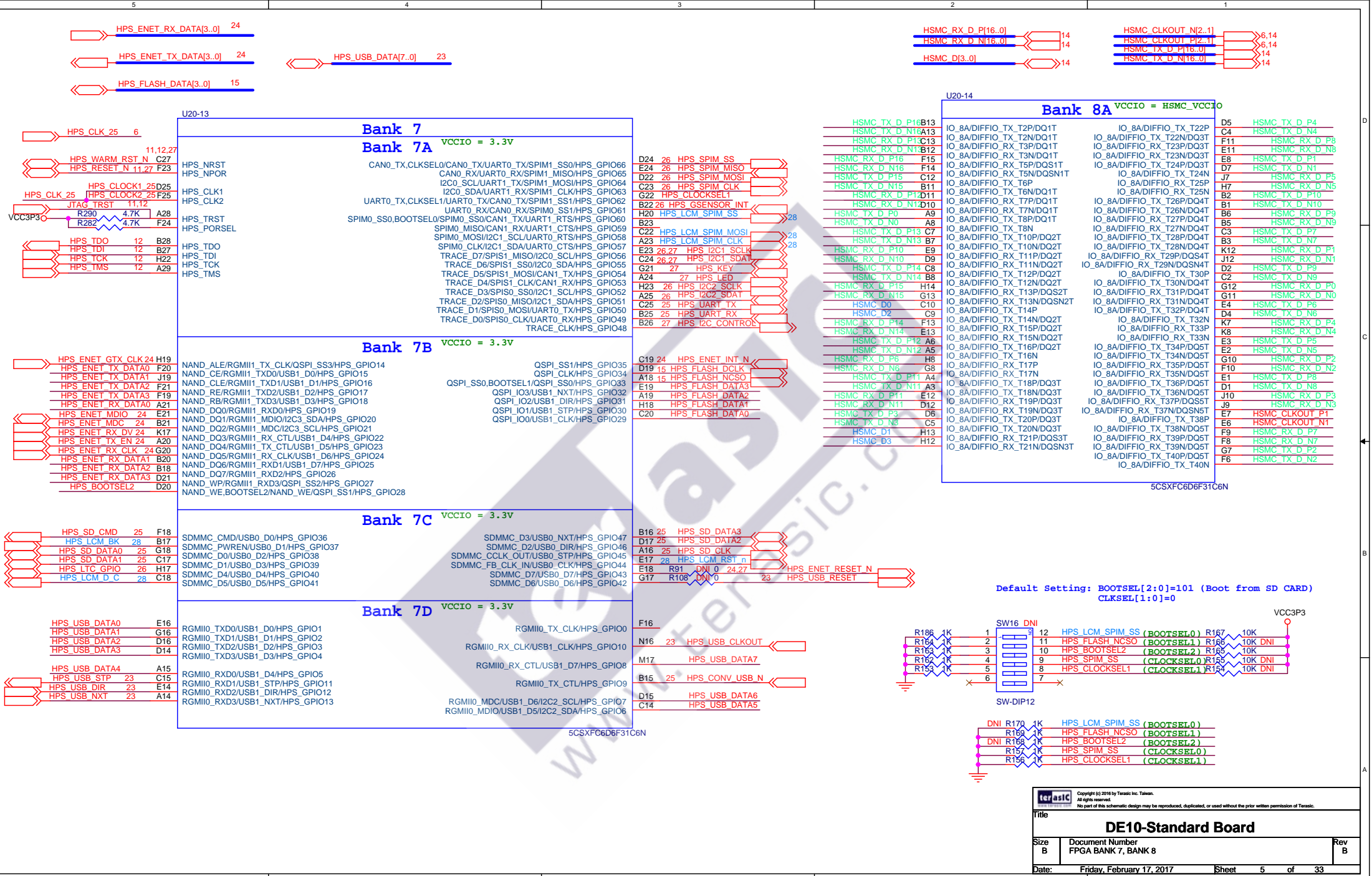
PAGE	CONTENT	PAGE	CONTENT
1	Cover Page	18	ADV7180 Video Decoder
2	Block Diagram	19	Audio CODEC
3	FPGA BANK 3, BANK 4	20	7-Segment Display, LED
4	FPGA BANK 5, BANK 6	21	FPGA BUTTON, Switch
5	FPGA BANK 7, BANK 8	22	ADC, PS2, IR Tx, IR Rx
6	FPGA Clocks, GND	23	2-port USB Host
7	Transceiver	24	1 Gigabit Ethernet
8	FPGA Configuration	25	UART to USB, SD CARD
9	FPGA Decoupling	26	Accelerometer, LTC Connector
10	FPGA Power	27	I2C Multiplexer, HPS BUTTON, HPS LED
11	USB Blaster II	28	LCD
12	JTAG Chain	29	Power - 1.1V
13	GPIO	30	Power - 5V, 3.3V
14	HSMC	31	Power - 9V, 2.5V, 1.5V
15	SDRAM, HPS QSPI Flash	32	Power - 1.2V, 1.8V, DDR3 VREF, DDR3 VTT
16	HPS DDR3 SDRAM	33	Power - VCCIO_HSMC & HSMC_VCCPD
17	ADV7123 VGA		

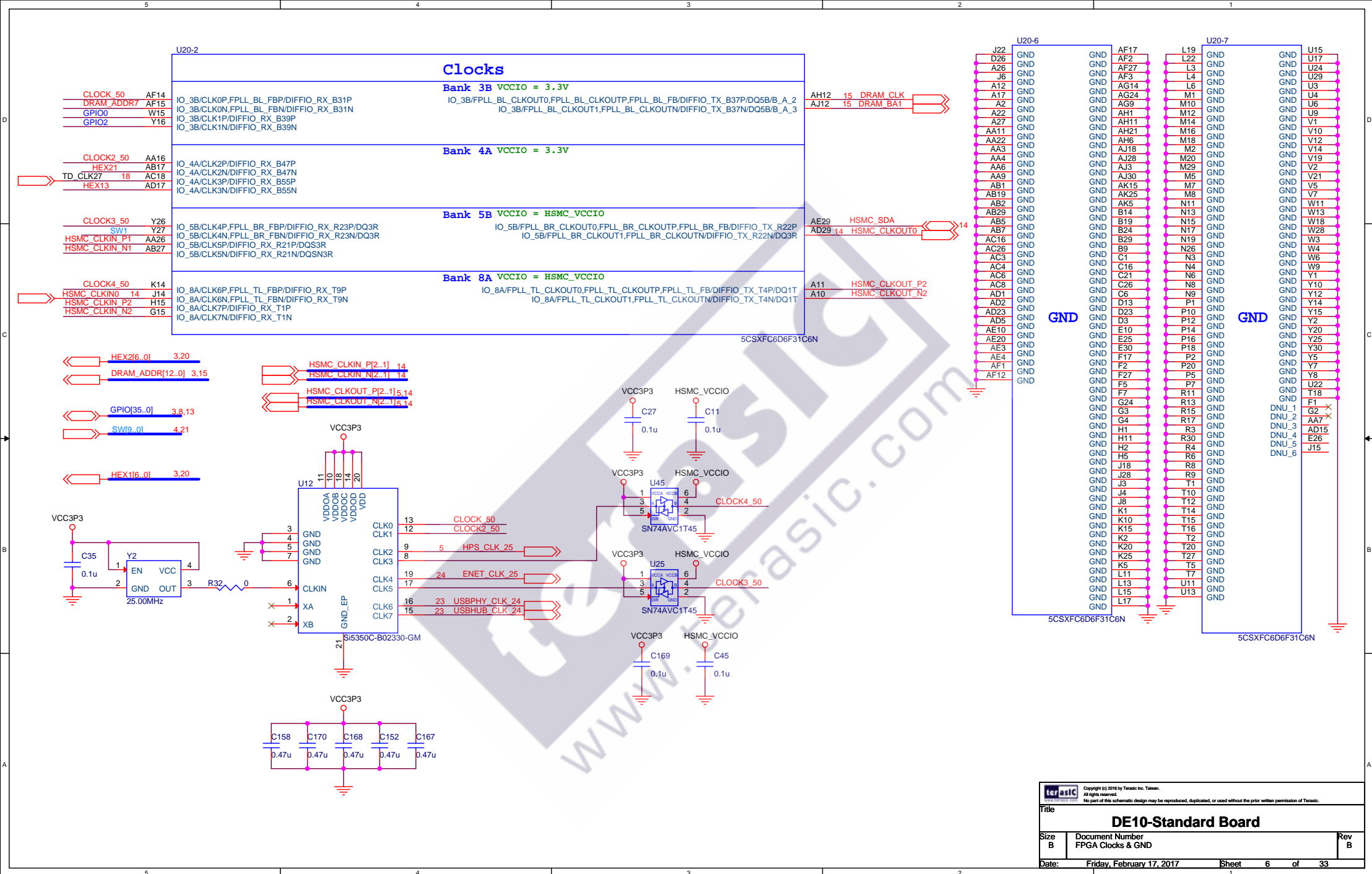
Block Diagram

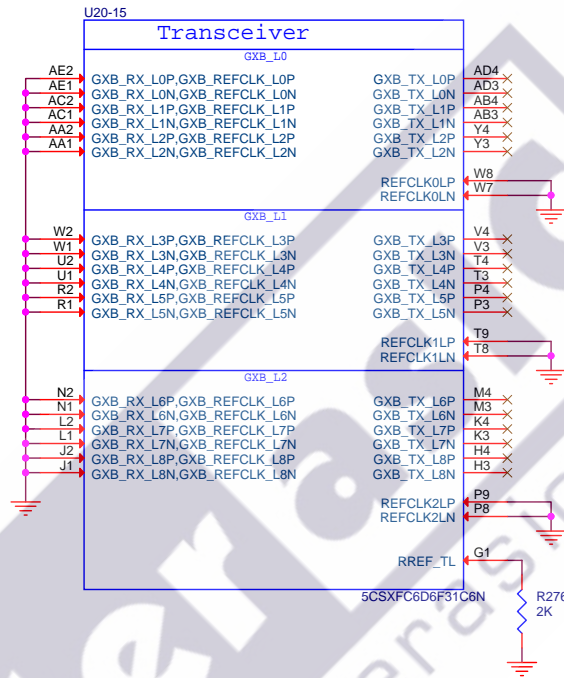









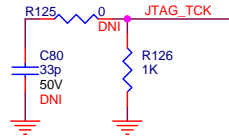




 Copyright (c) 2016 by Terasic Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
DE10-Standard Board		
Size B	Document Number Transceiver	Rev B
Date:	Friday, February 17, 2017	Sheet 7 of 33

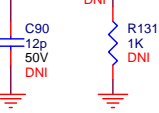
USB Blaster

FPGA_TDI	12
JTAG_TMS	12
JTAG_TCK	12
FPGA_TDO	12



Design Note:
Optional termination resistor
for DCLK

CAD Note:
Place near FPGA DCLK pin



JTAG_TCK	AC5
JTAG_TMS	V9
FPGA_TDO	AB9
FPGA_TDI	U8
EPCQ_DCLK	U7
EPCQ_AS_DATA0	AE6
EPCQ_AS_DATA1	AE5
EPCQ_AS_DATA2	AE8
EPCQ_AS_DATA3	AC7
EPCQ_NCS0	AB8
GPIO24	AE9
GPIO26	AE12
GPIO28	AD9
GPIO30	AD11
GPIO22	AF10
GPIO29	AD10
GPIO25	AE11
GPIO32	AC9
GPIO8	AH4
GPIO23	AE7
GPIO12	AG3
GPIO27	AD7

Configuration

Bank 3A VCCIO = 3.3V

TCK
TMS
TDO
TDI
DCLK

Bank 5A VCCIO = 3.3V

IO_5A/INIT_DONE/DIFFIO_RX_R2P
IO_5A/CRC_ERROR/DIFFIO_RX_R2N
IO_5A/DEV_OE/DIFFIO_TX_R5P
IO_5A/NCEO/DIFFIO_TX_R3P/DQ1R
IO_5A/DEV_CLRN/DIFFIO_TX_R5N/DQ1R

Bank 9A

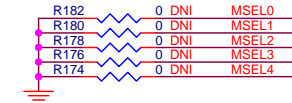
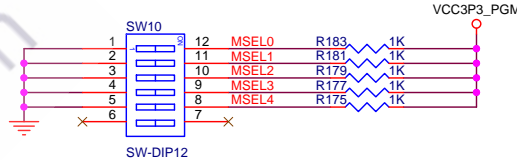
CONF_DONE
NSTATUS
NCONFIG
NCE

AS_DATA0/ASDO/DATA0
AS_DATA1/DATA1
AS_DATA2/DATA2
AS_DATA3/DATA3
NCS0/DATA4
IO_3A/DATA5/DIFFIO_TX_B2N
IO_3A/DATA6/DIFFIO_RX_B1N/DQ1B
IO_3A/DATA7/DIFFIO_TX_B2P/DQ1B
IO_3A/DATA8/DIFFIO_RX_B1P/DQ1B
IO_3A/DATA9/DIFFIO_TX_B4N/DQ1B
IO_3A/DATA10/DIFFIO_RX_B3N/DQSN1B
IO_3A/DATA11/DIFFIO_TX_B4P
IO_3A/DATA12/DIFFIO_RX_B3P/DQSN1B
IO_3A/DATA13/DIFFIO_TX_B6N/DQ1B
IO_3A/DATA14/DIFFIO_RX_B5N/DQ1B
IO_3A/DATA15/DIFFIO_TX_B6P/DQ1B
IO_3A/CLKUSR/DIFFIO_RX_B5P/DQ1B

MSEL0
MSEL1
MSEL2
MSEL3
MSEL4

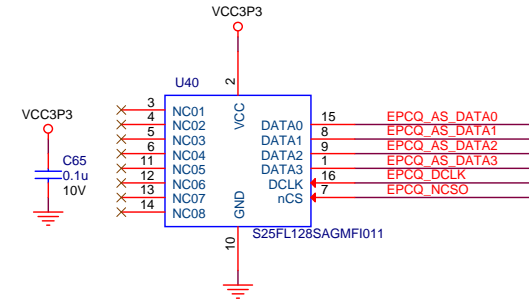
5CSXFC6D6F31C6N

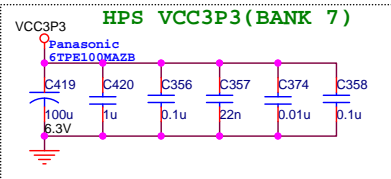
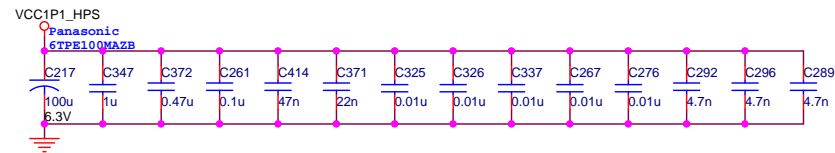
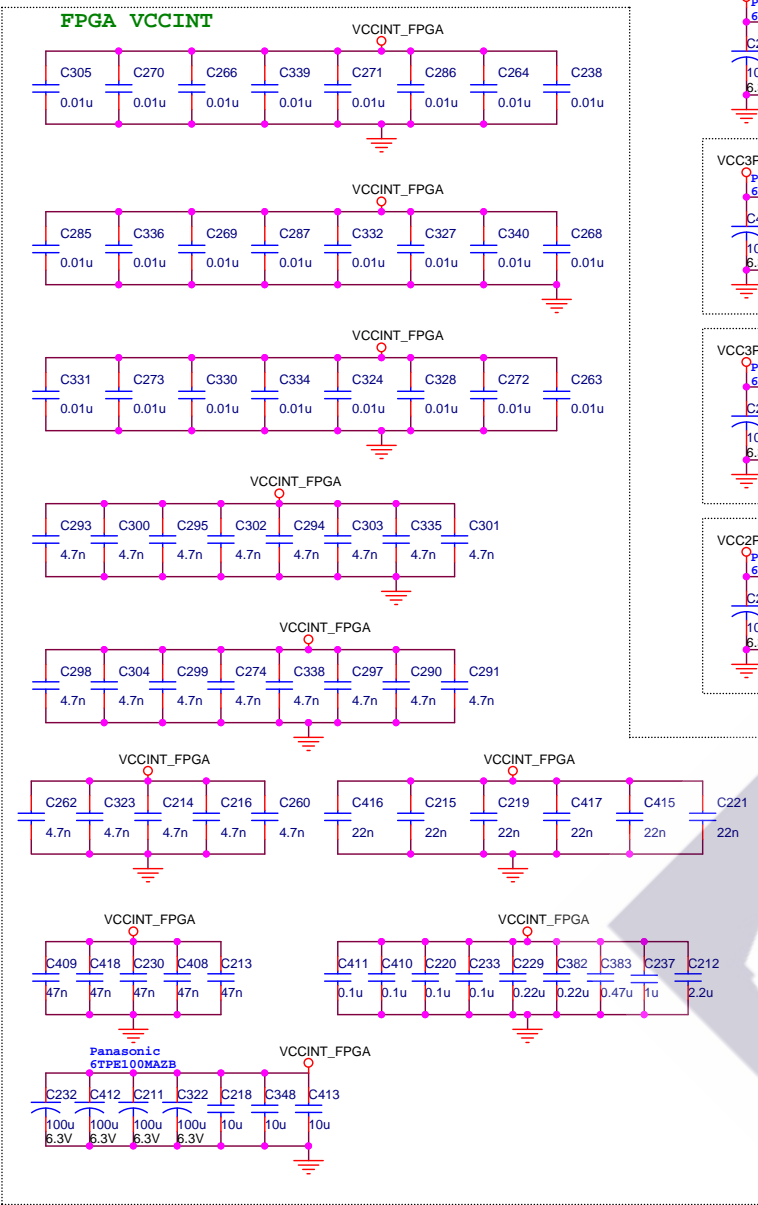
Fix MSEL[4:0]=10010 in AS Fast Mode



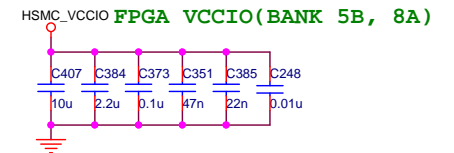
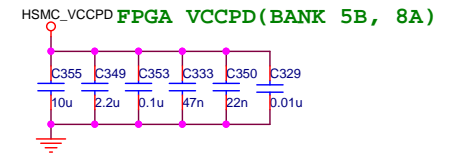
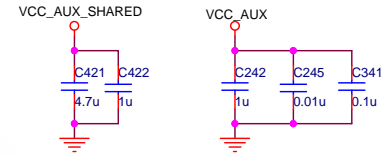
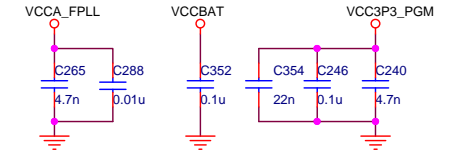
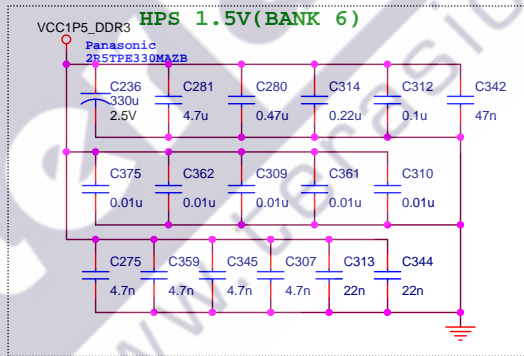
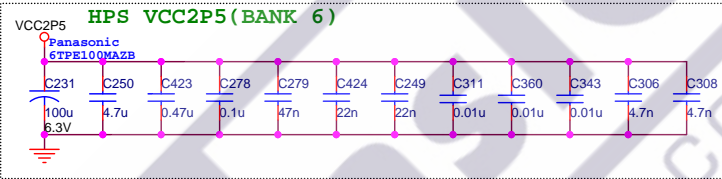
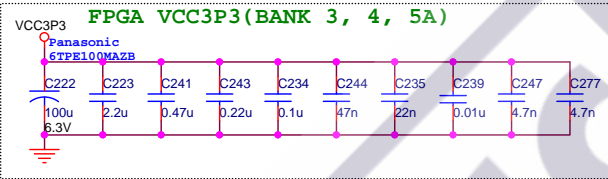
TD_DATA[7..0] 4,18

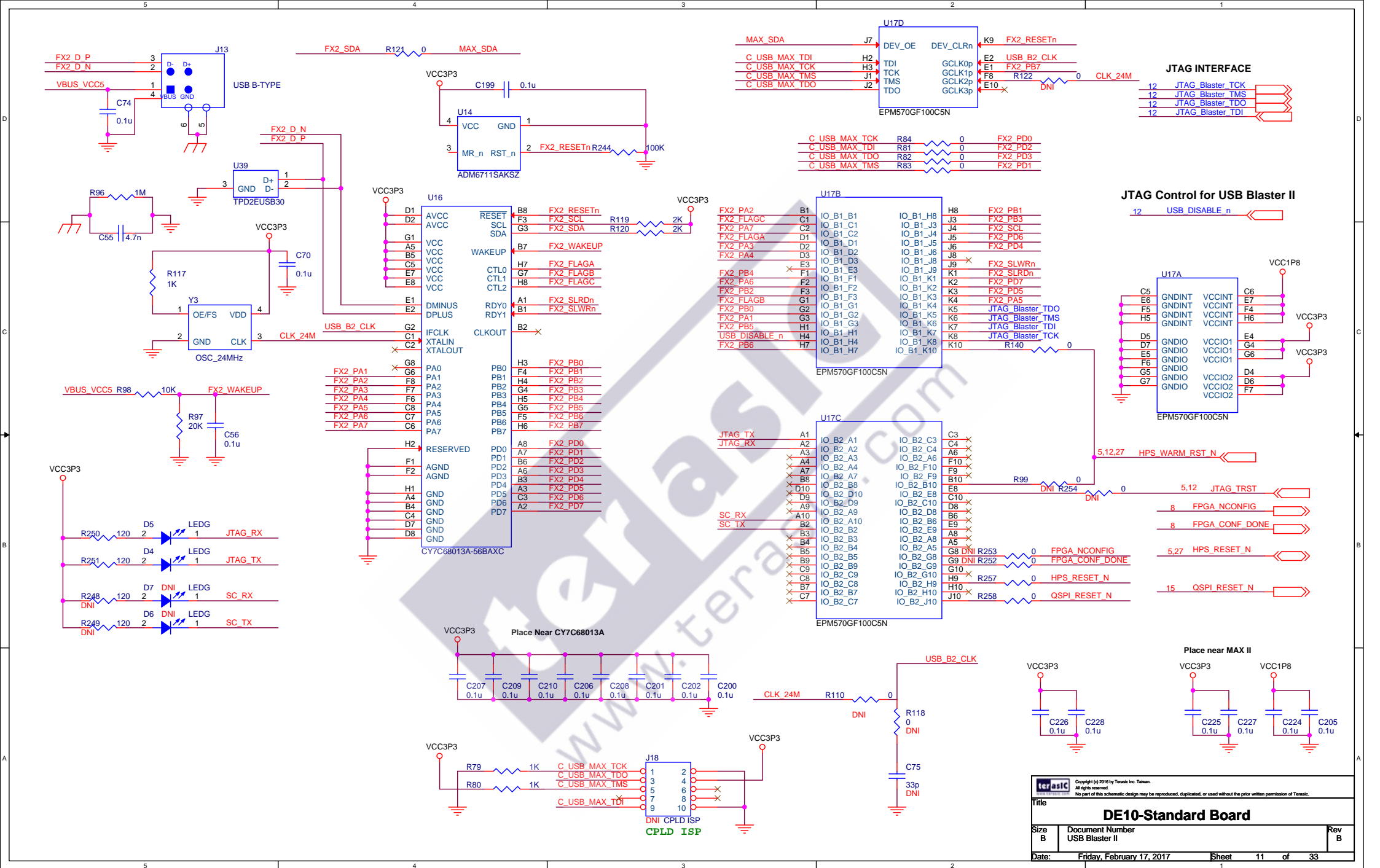
GPIO[35..0] 3,6,13

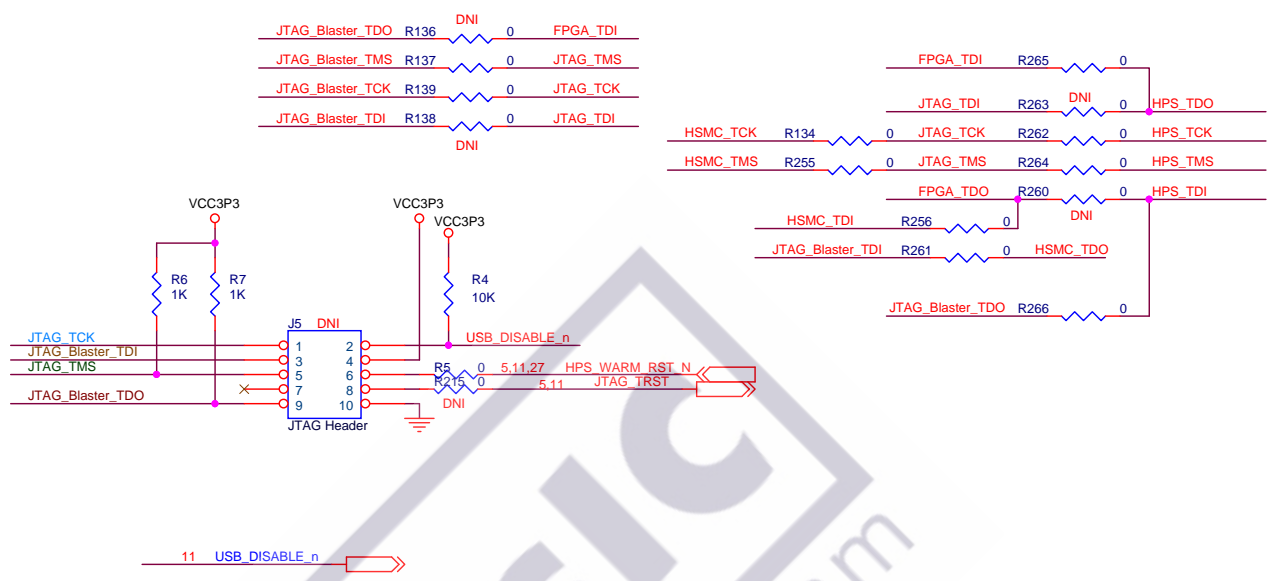
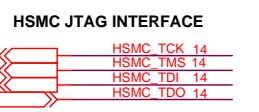
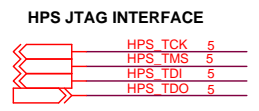
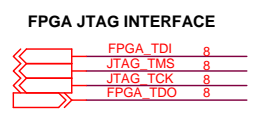




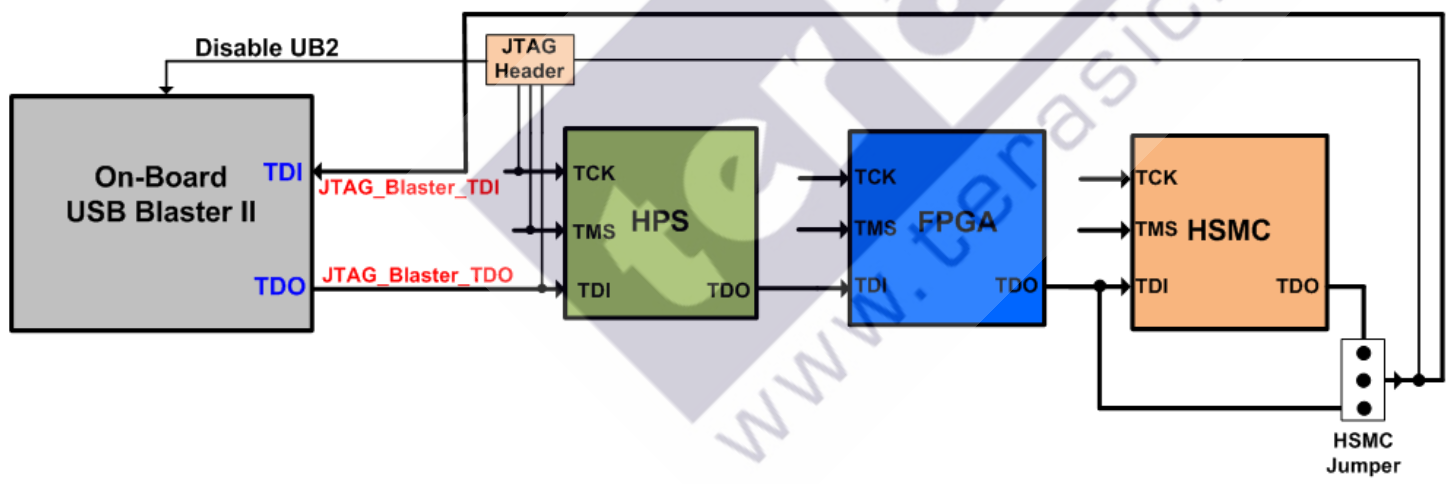
Place C394 close to J20/G23 pin

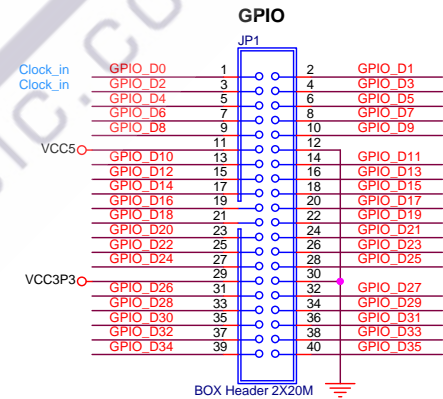
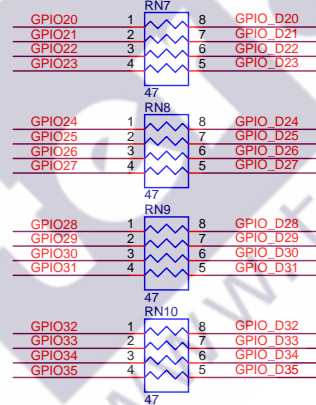
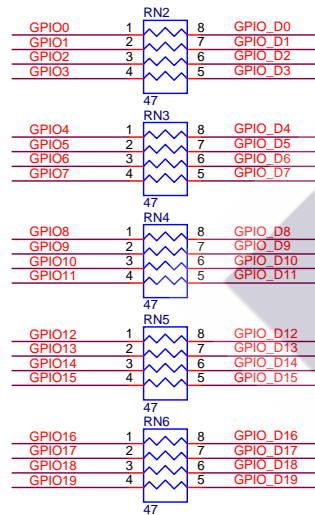
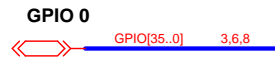
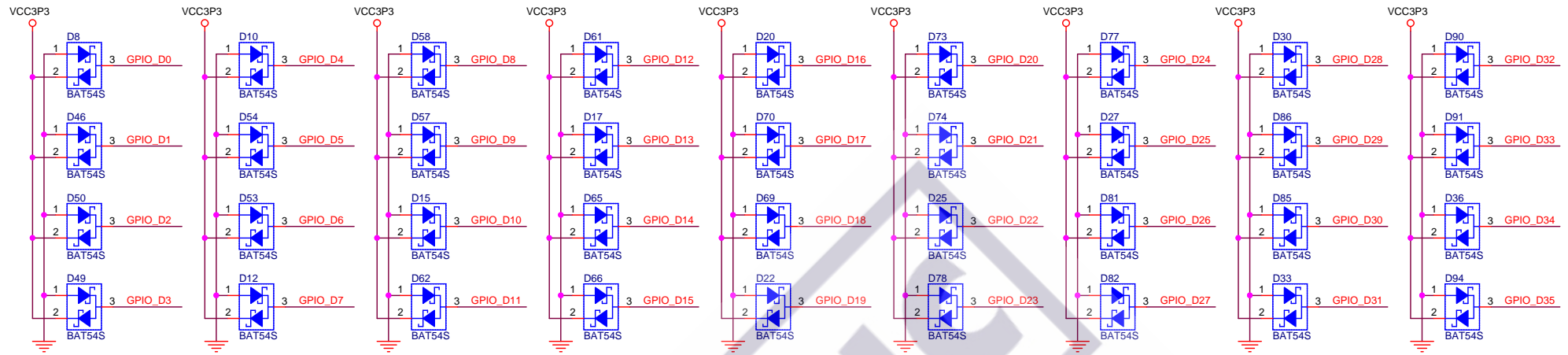


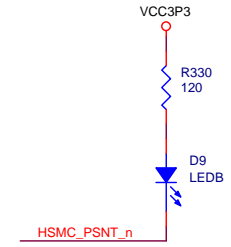
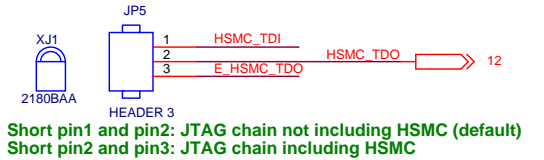
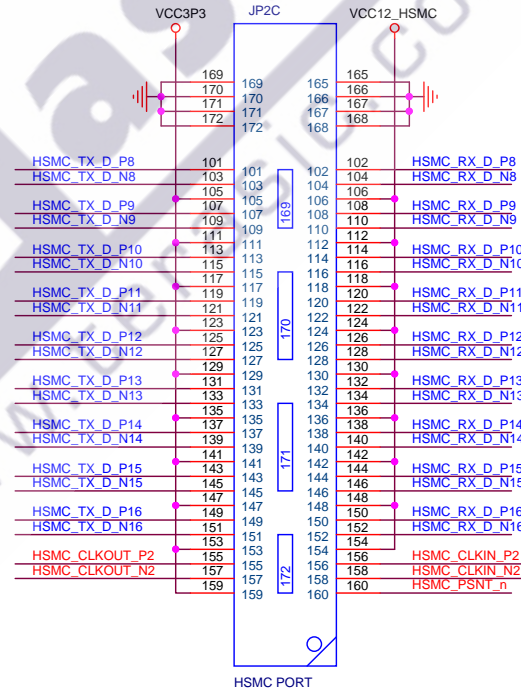
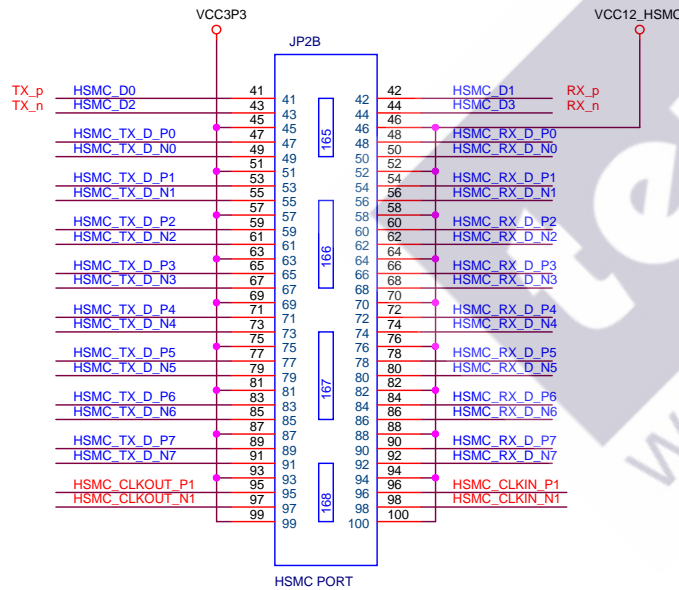
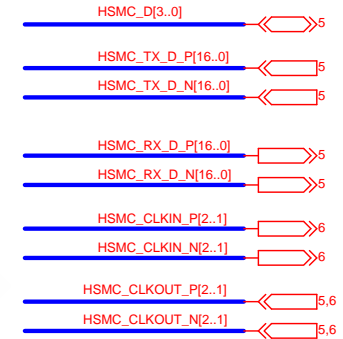
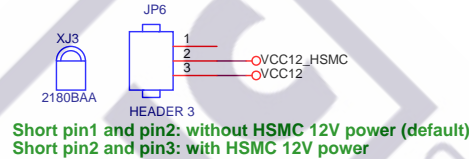
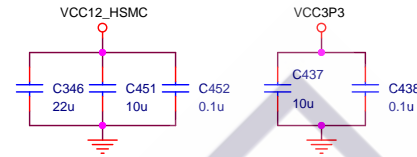
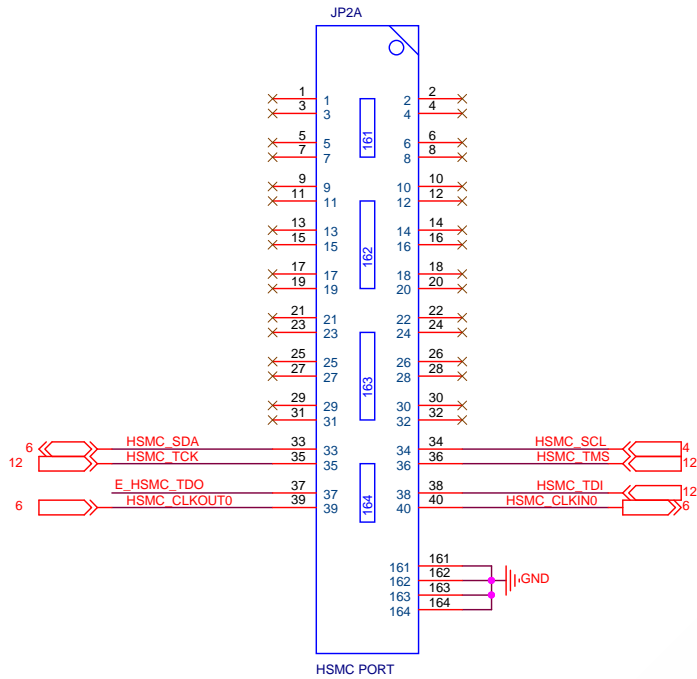




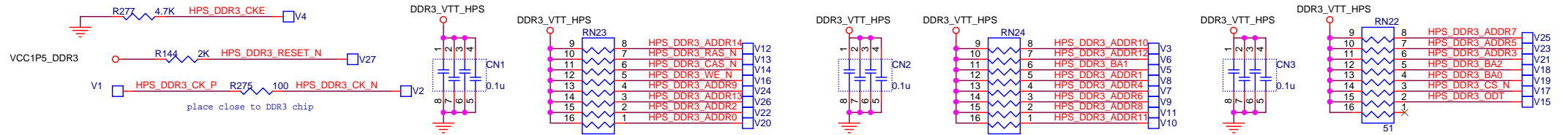
JTAG Chain



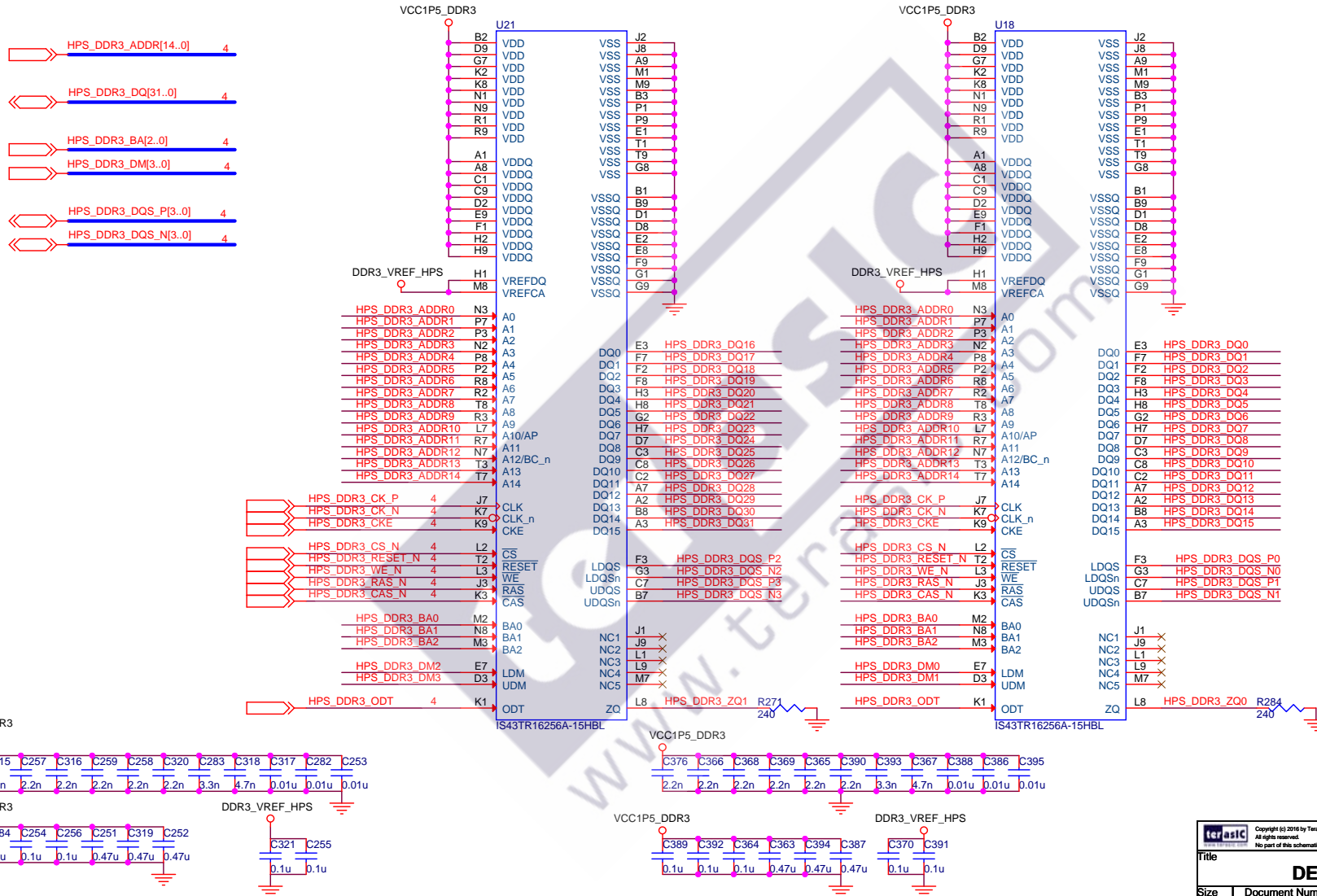


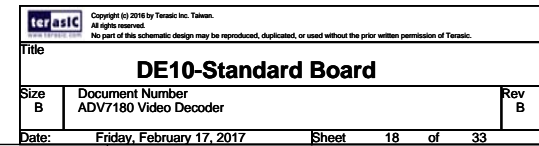


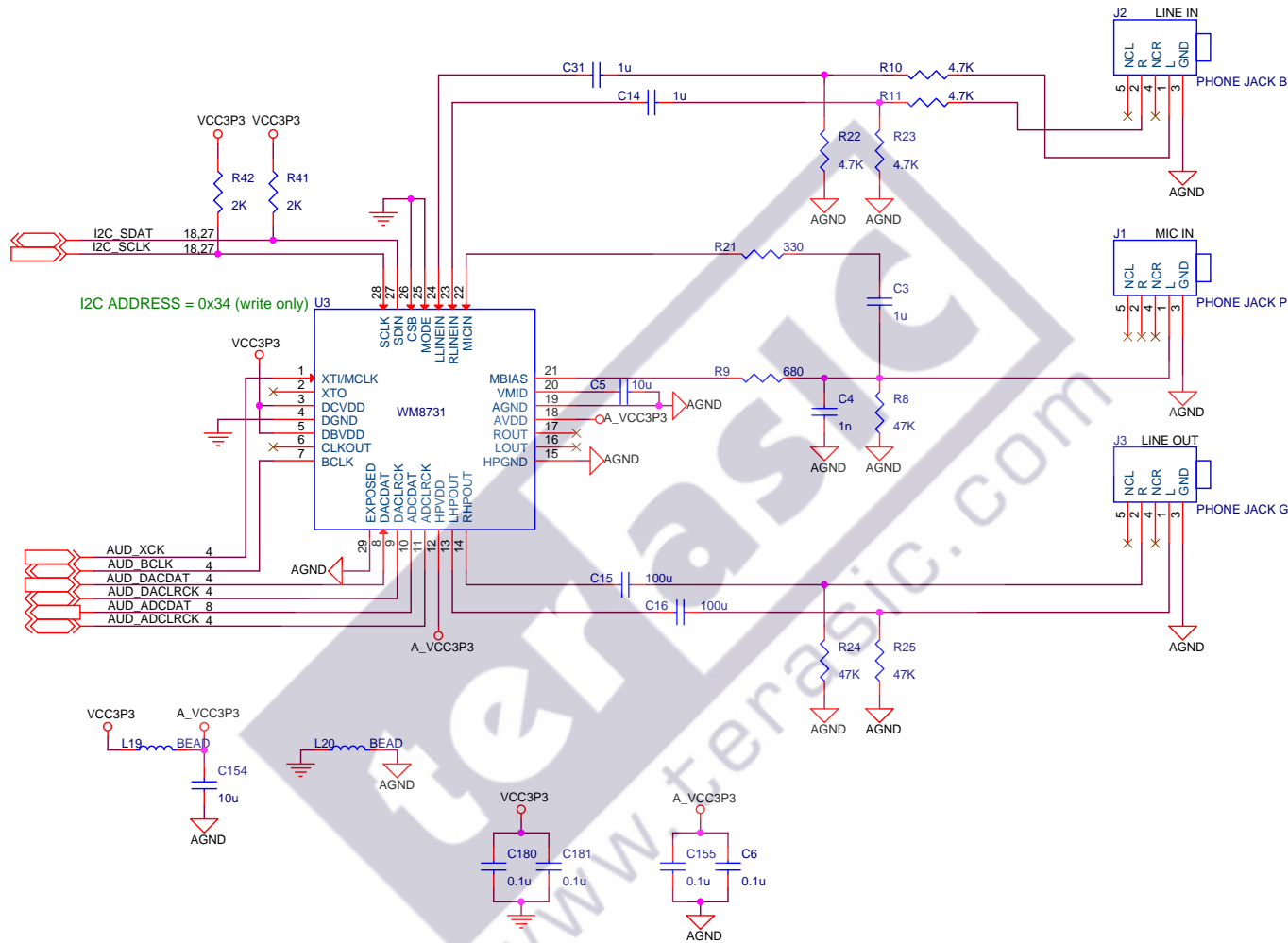
<div> <div>terasic</div> <div>Copyright (c) 2016 by Terasic Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.</div> </div>		
Title		
DE10-Standard Board		
Size	Document Number	Rev
B	HSMC	B
Date:	Friday, February 17, 2017	Sheet 14 of 33

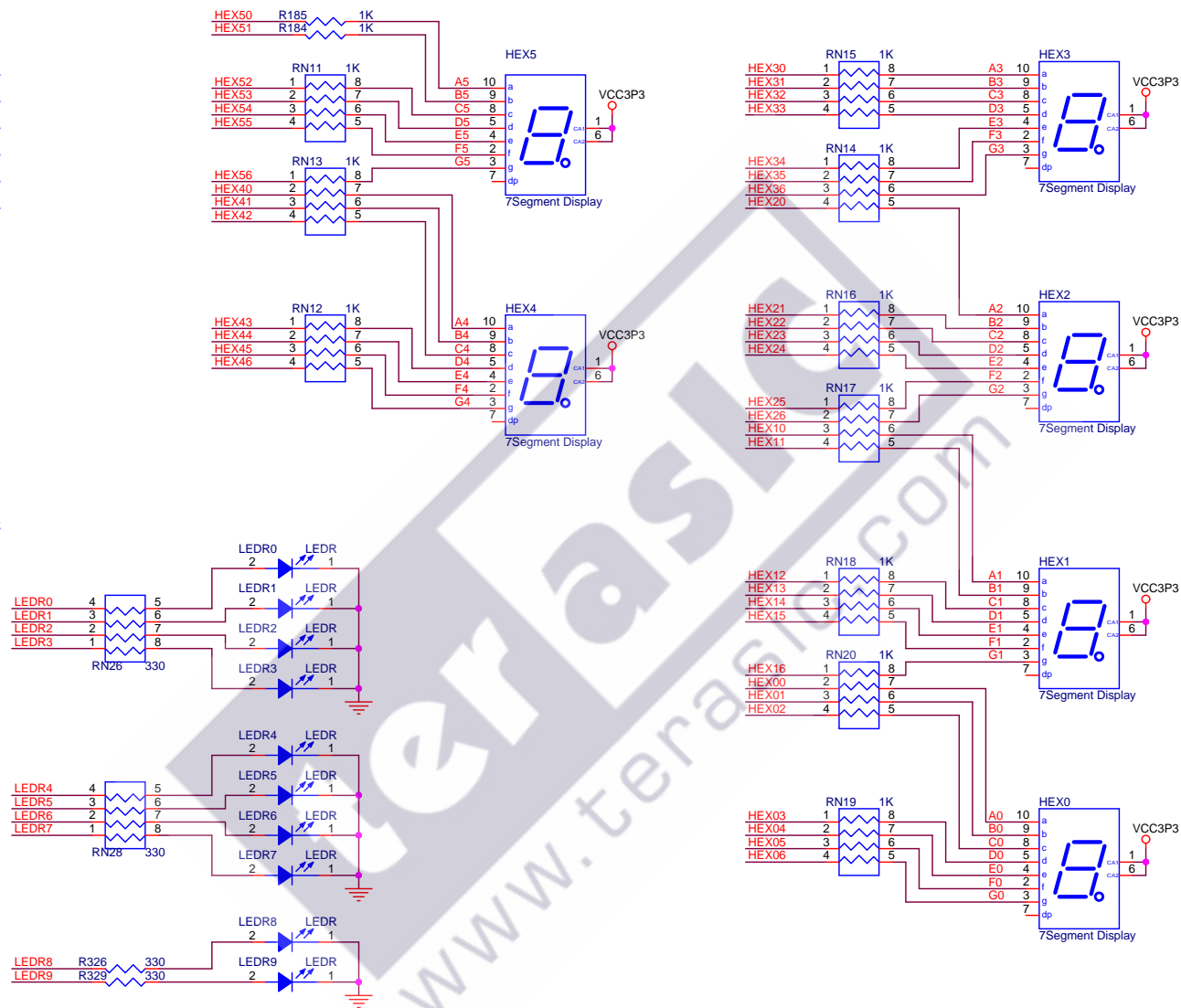
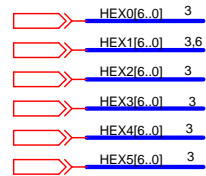


Note:you can only swap the DQ signals within x8 group (e.g. 0-7,8-15,16-23,24-31) on the DDR3 chips Note:you can swap the signals on the OCT resistor array(include NC pin)

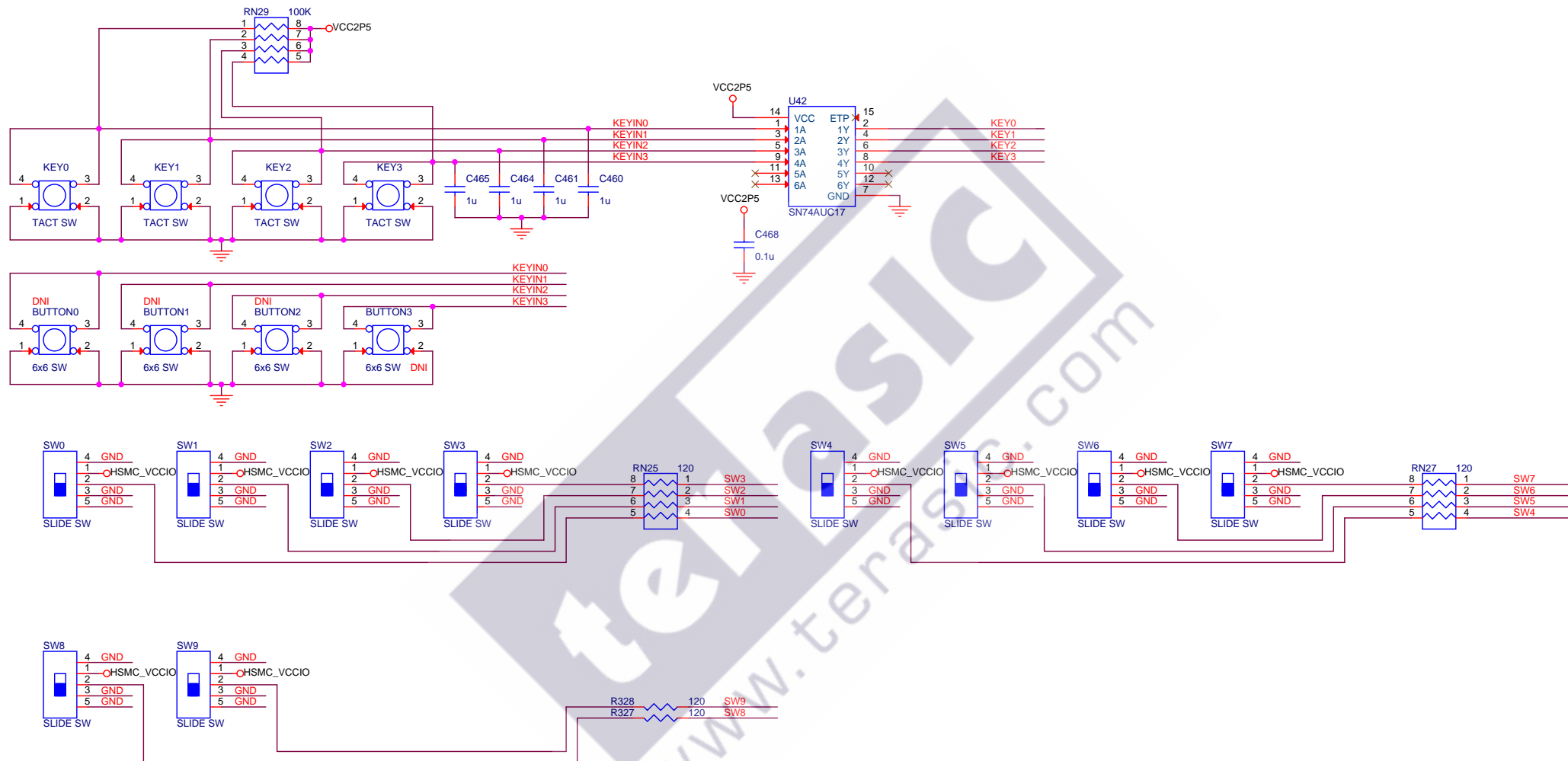


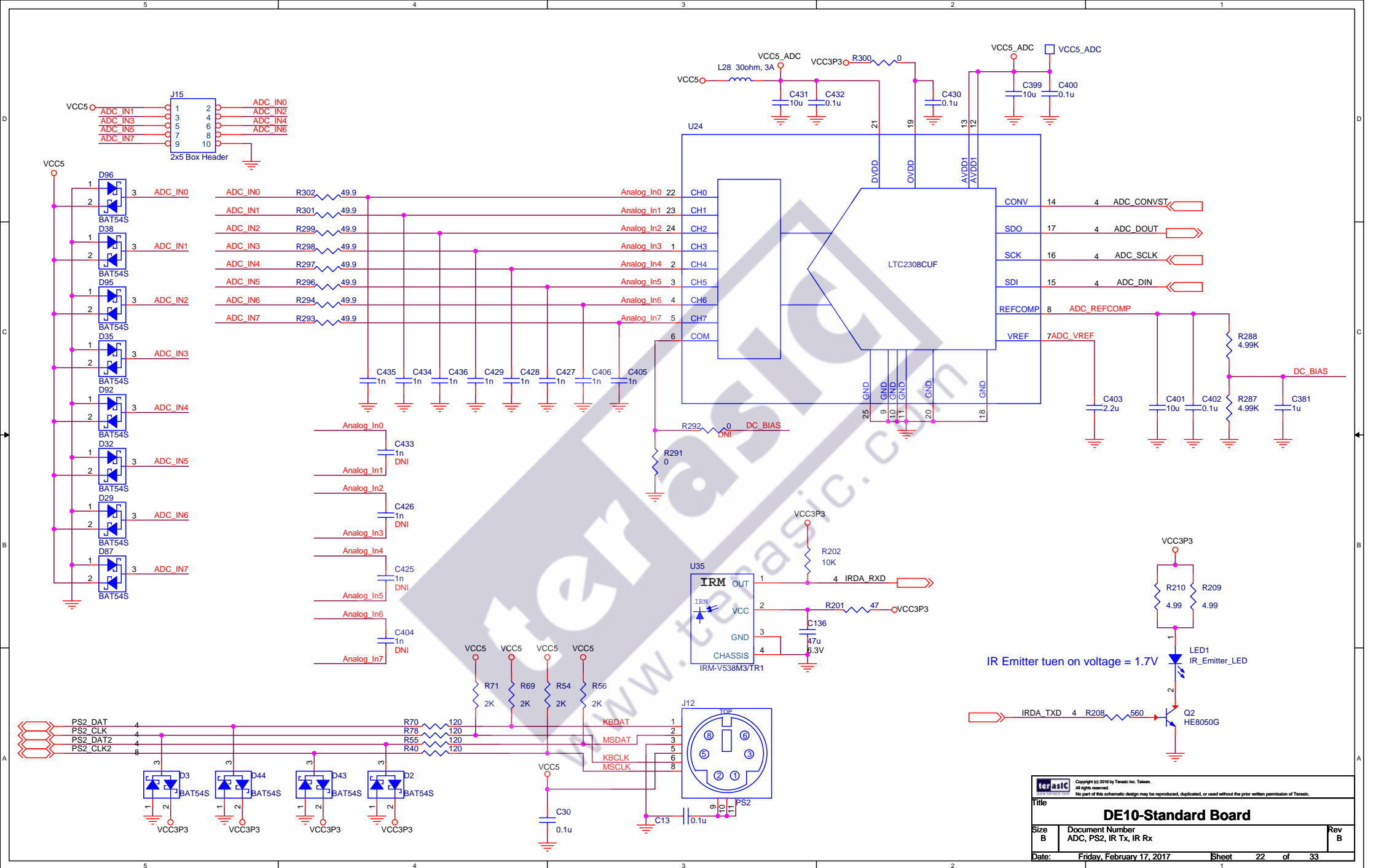




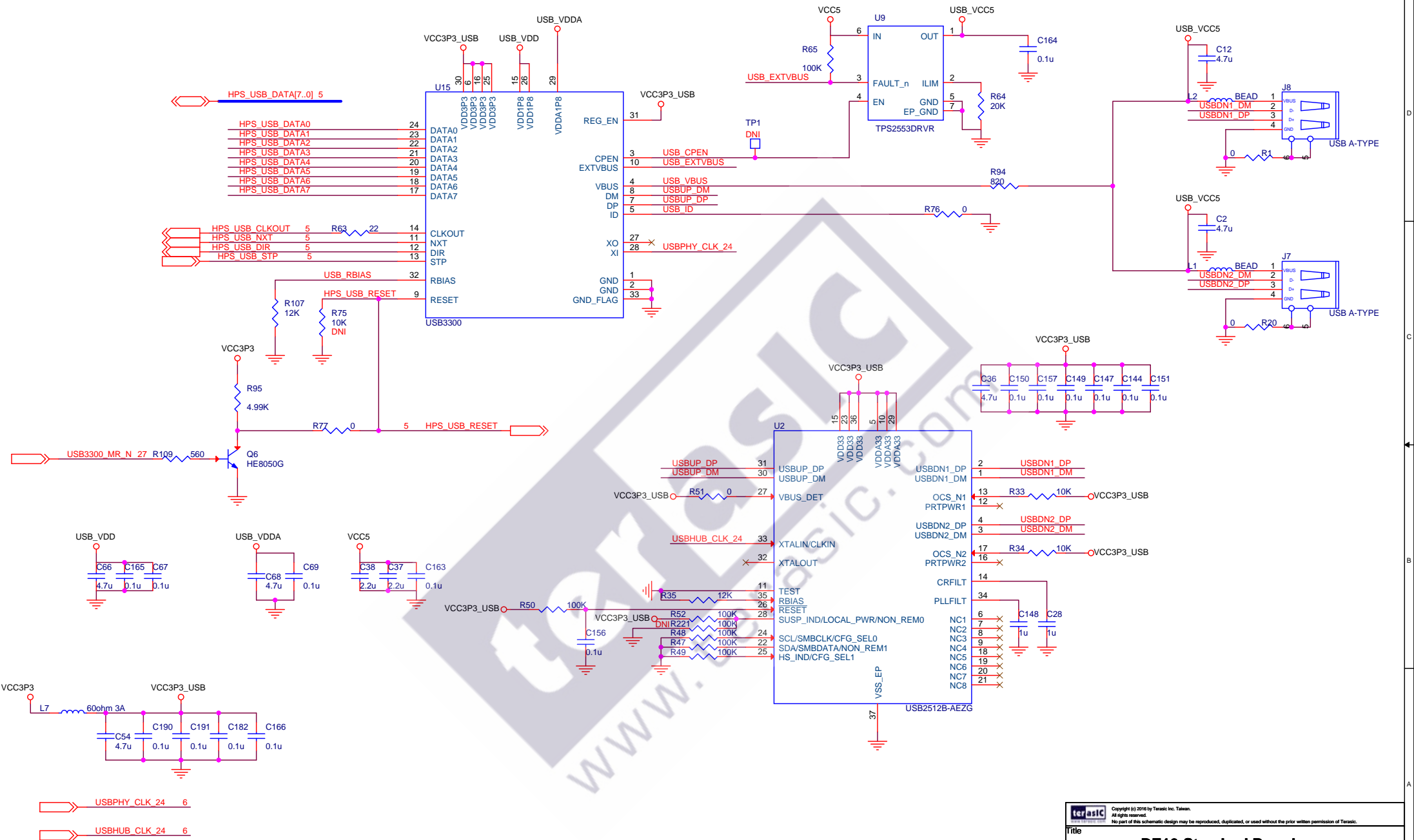


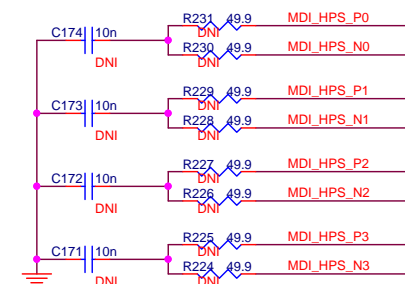
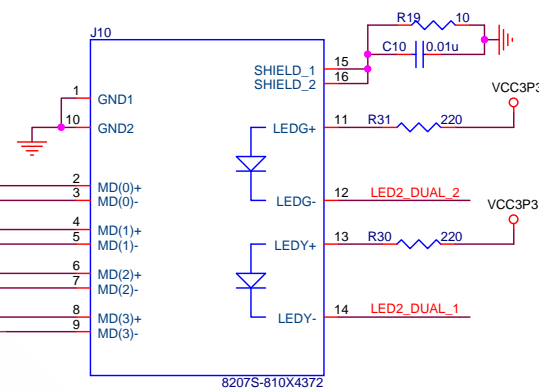
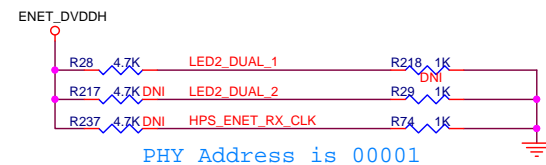
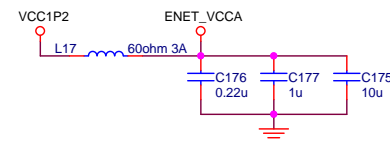
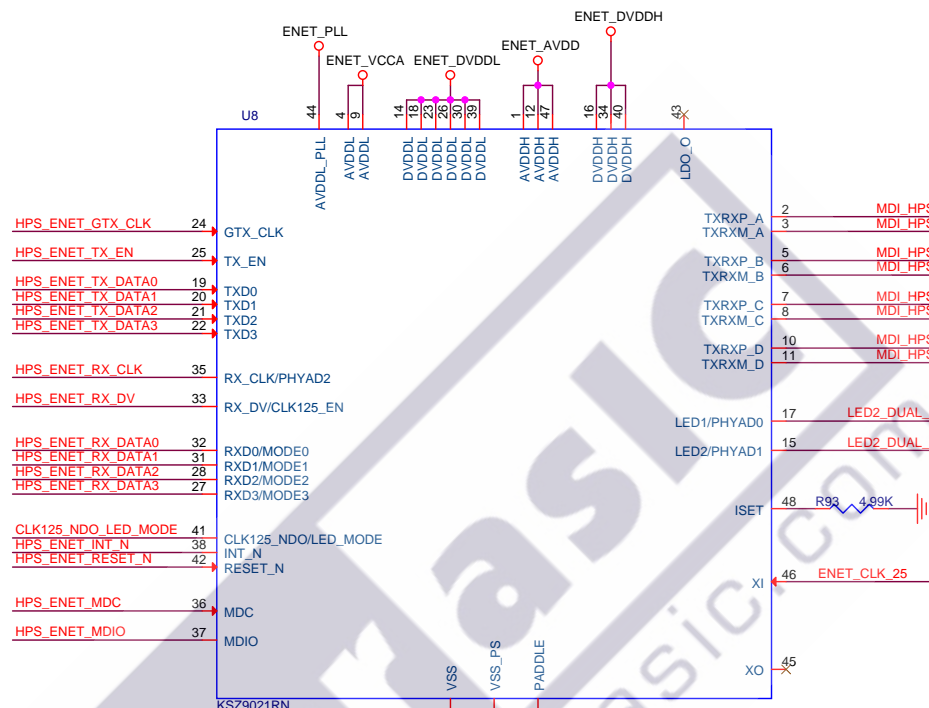
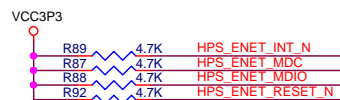
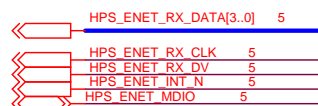
KEY[3..0] 3
SW[9..0] 4,6

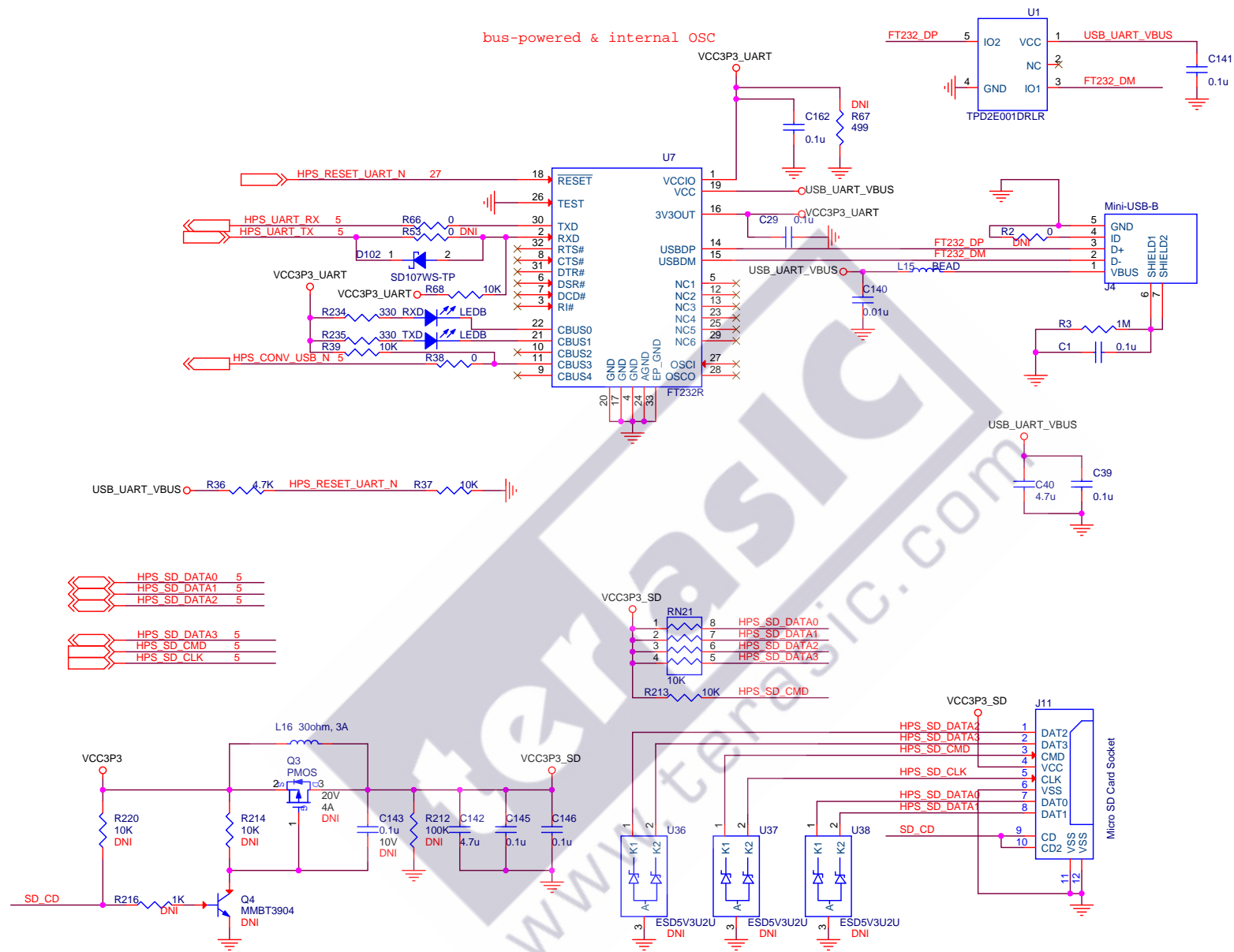


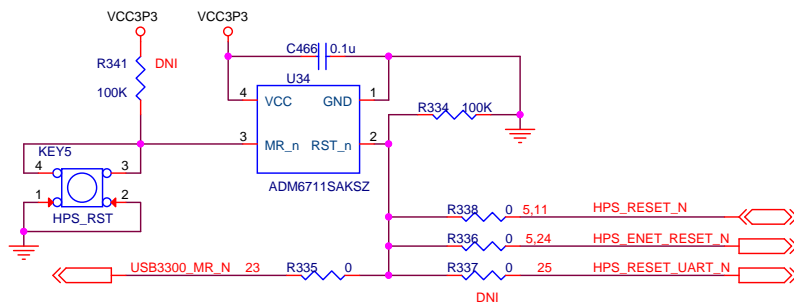


<div> <div>terasic</div> <div>Copyright (c) 2016 by Terasic Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.</div> </div>		
Title		
DE10-Standard Board		
Size	Document Number	Rev
B	ADC, PS2, IR Tx, IR Rx	B
Date:	Friday, February 17, 2017	Sheet 22 of 33



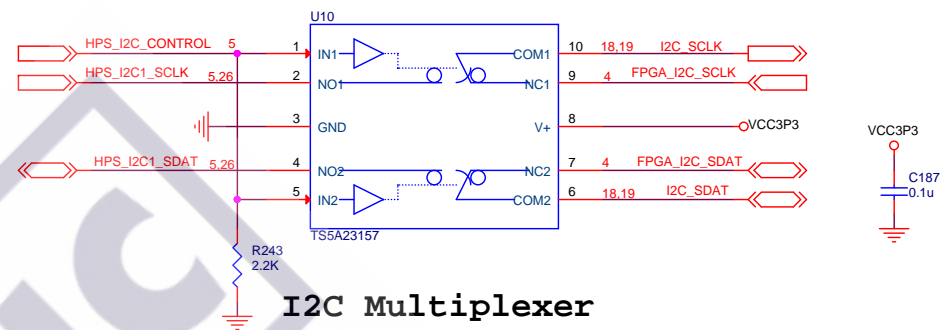




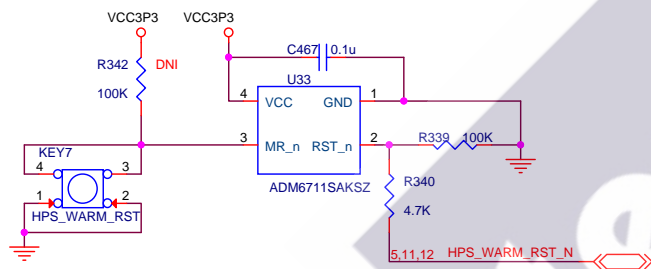


HPS Cold Reset

LOW --> NC to/from COM = ON and NO to/from COM = OFF
HIGH --> NC to/from COM = OFF and NO to/from COM = ON



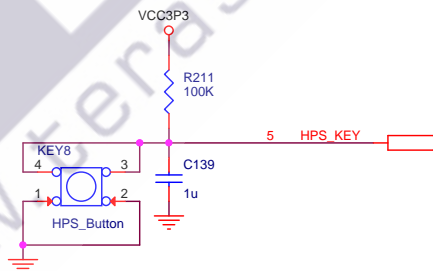
I2C Multiplexer



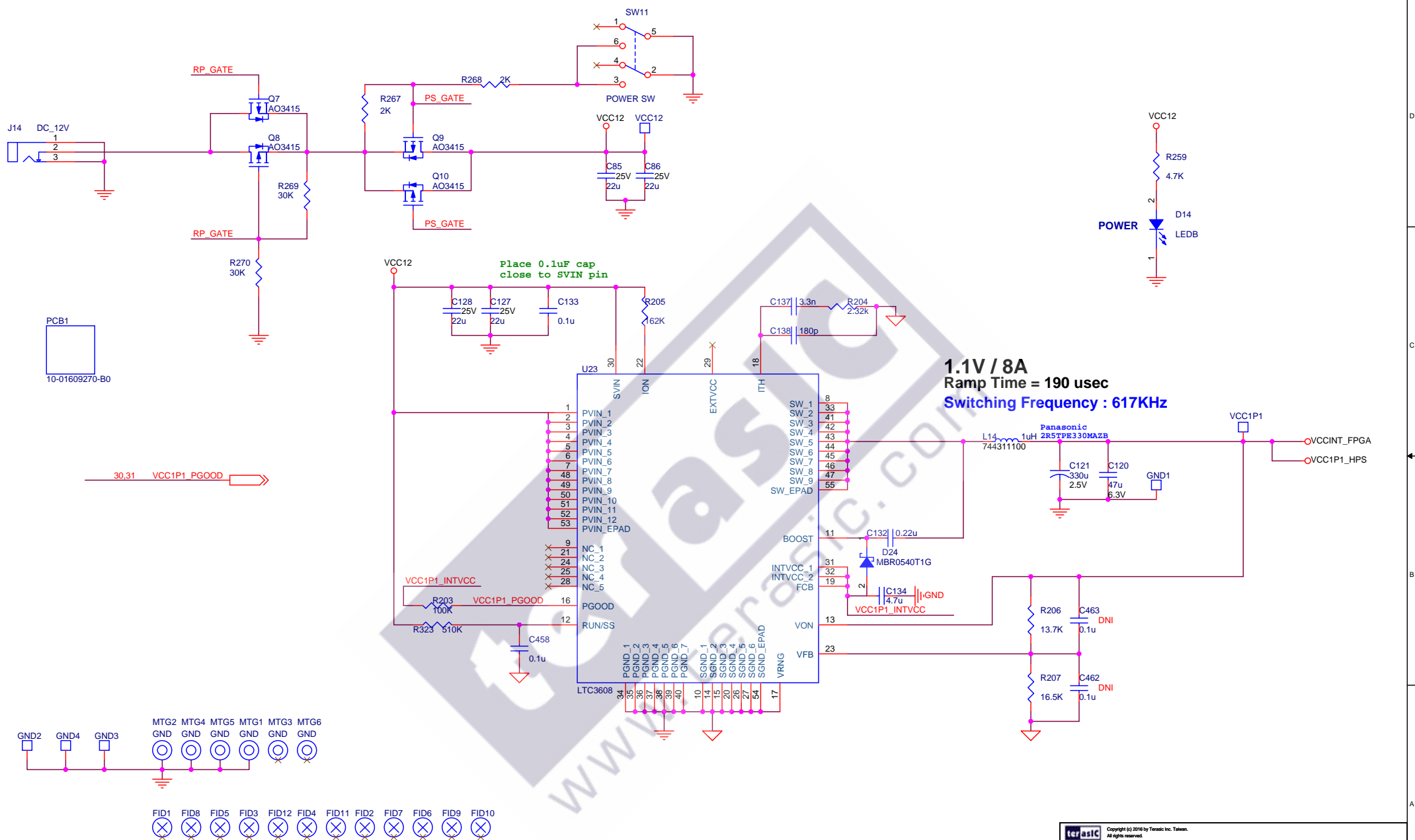
HPS Warm Reset

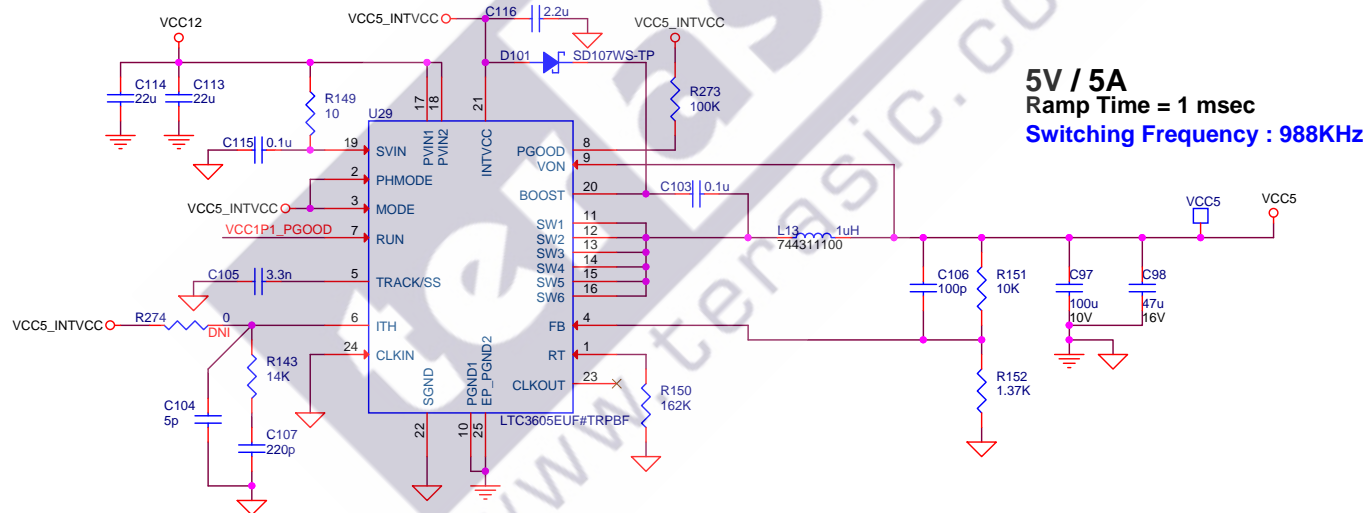
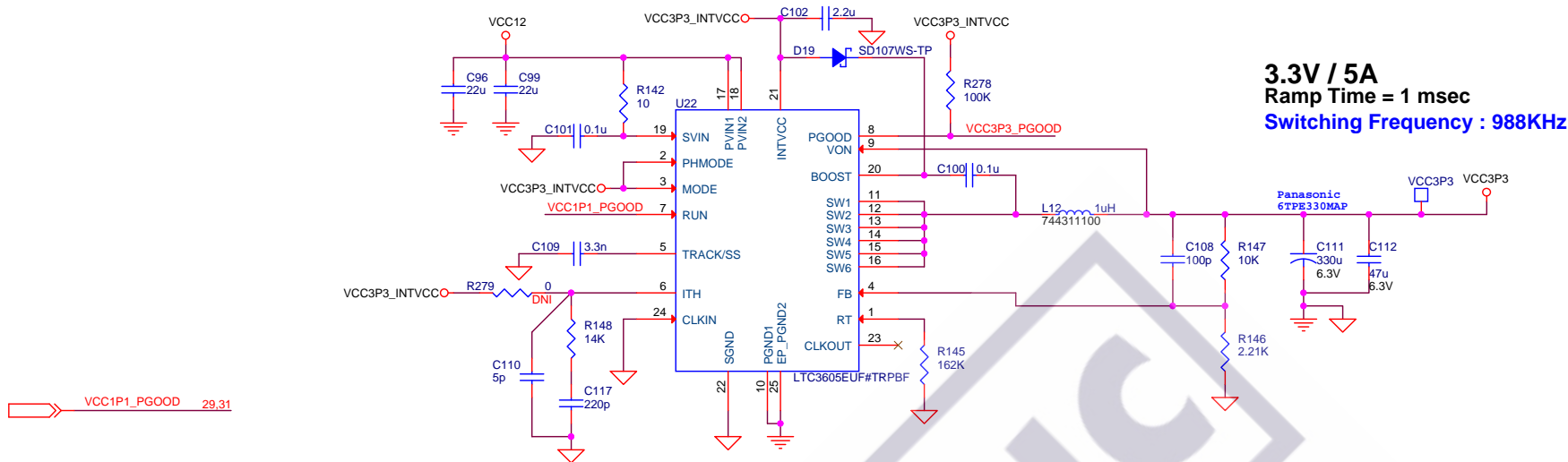


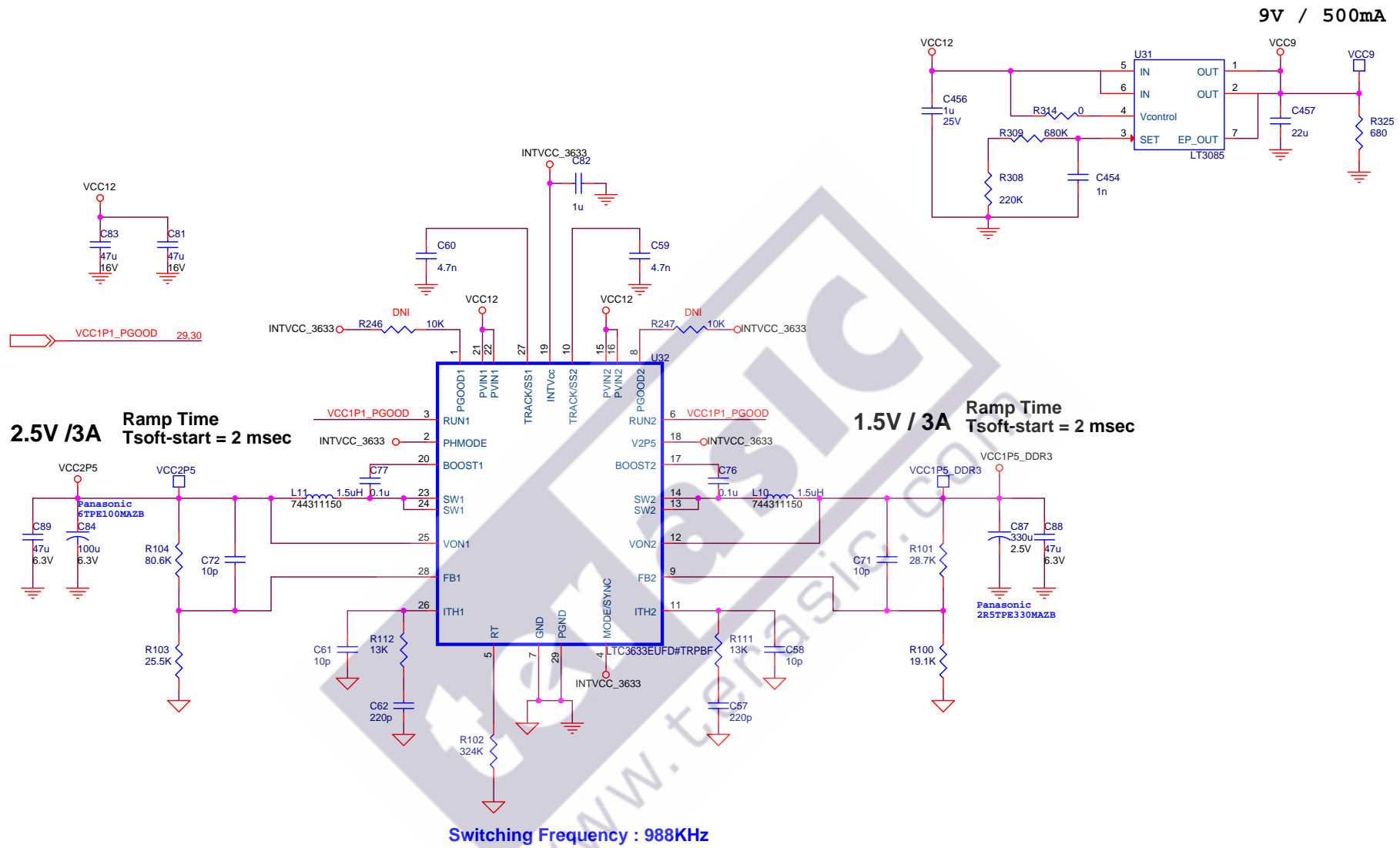
HPS User LED



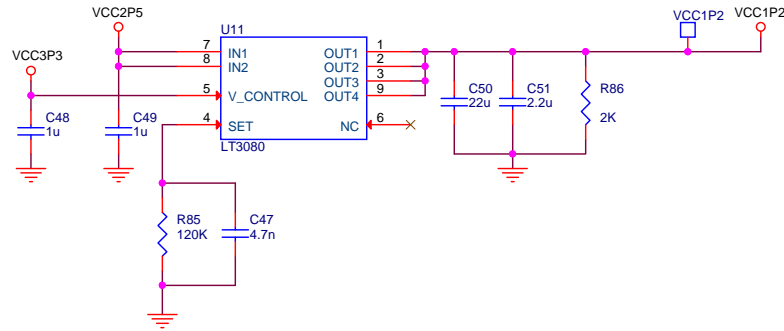
HPS User Button



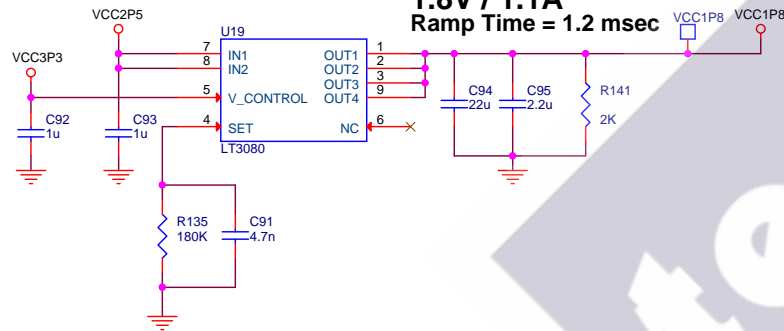




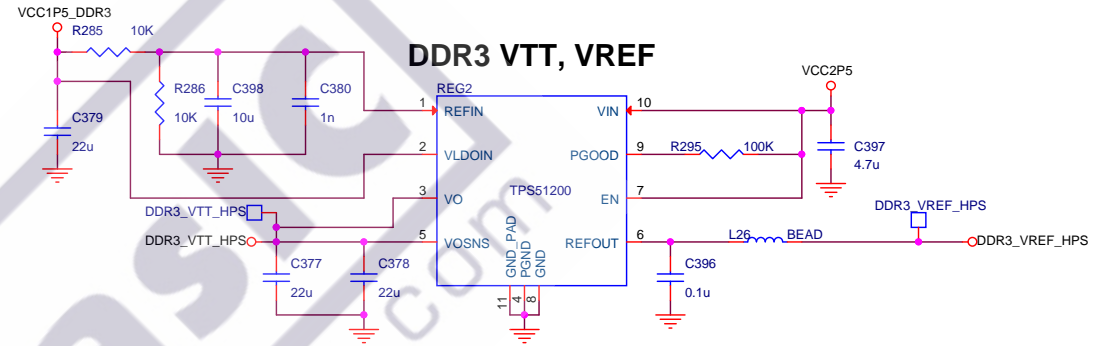
1.2V / 1.1A
Ramp Time = 0.8msec



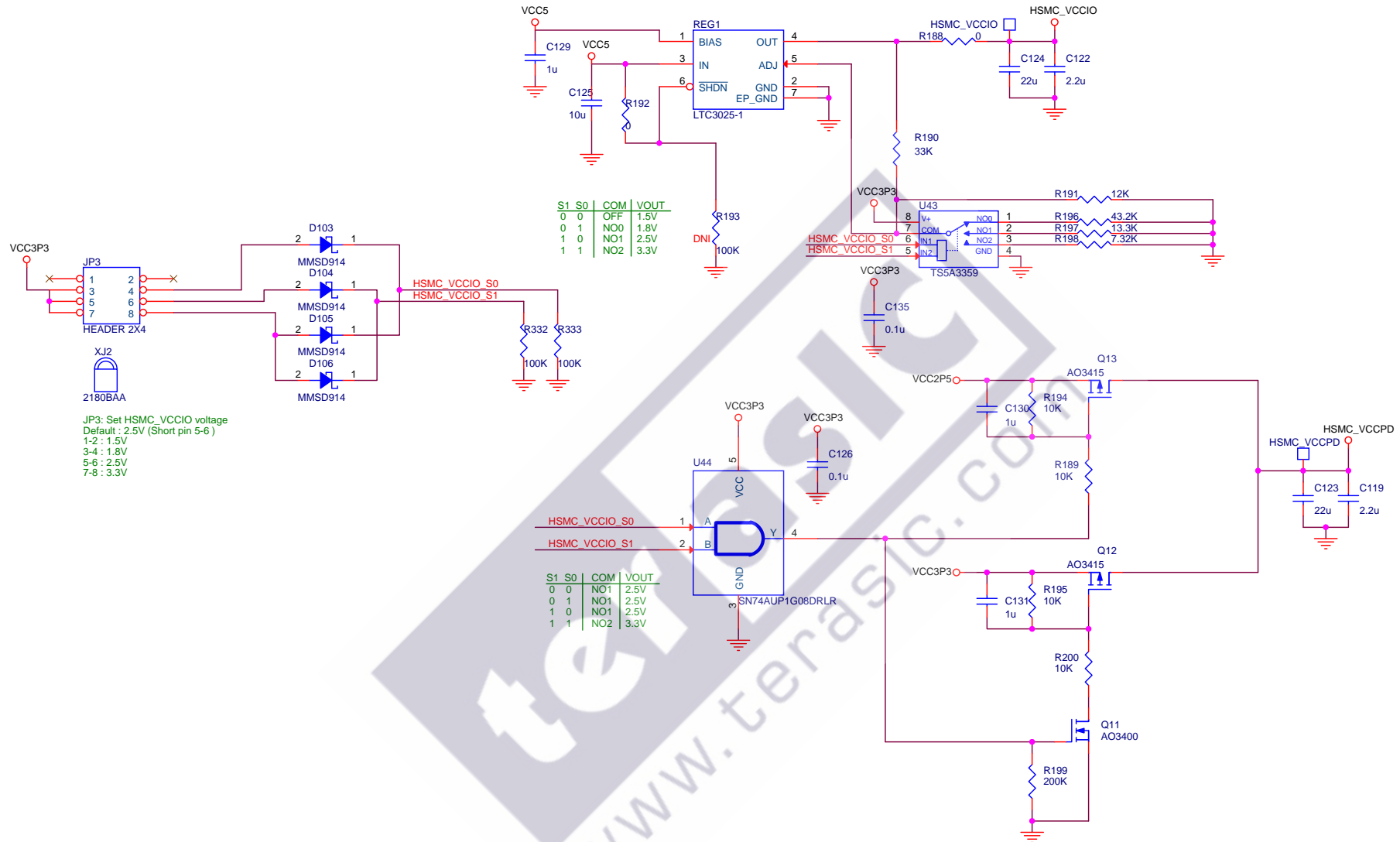
1.8V / 1.1A
Ramp Time = 1.2 msec




DDR3 VTT, VREF



HSMC_VCCIO / 0.5A Adjustable: 3.3/2.5/1.8/1.5 V
Default: 2.5V



 Copyright (c) 2016 by Terasic Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
DE10-Standard Board		
Size	Document Number	Rev
B	Power - VCCIO_HSMC & HSMC_VCCPD	B
Date:	Friday, February 17, 2017	Sheet 33 of 33