ECE 545 Project 1
Suitable for Individual Students
Specification

Hardware Implementation of the xxHash Fast Digest Algorithm

Develop a hardware implementation of the XXH32 fast digest algorithm described in the following specification:

Y. Collet and S. Josefsson, "xxHash fast digest algorithm," available at

https://www.ietf.org/archive/id/draft-josefsson-xxhash-00.html

Reference Implementation in C:

https://github.com/easyaspi314/xxhash-clean/blob/master/xxhash32-ref.c

Optimization Target:

Optimize your design for the maximum throughput over the number of LUTs ratio.

Table of Input/Outputs:

Name	Direction	Width	Meaning
clk	in	1	System clock
reset	in	1	System reset. Clears all internal registers and returns the controller to the initial state.
din	in	32	Data input (a correctly formatted message word)
din_ready	out	1	Hash module ready to accept data input
din_valid	in	1	Data input present at the din input
din_in_last	in	1	Last word of data
din_valid_bytes	in	4	A 4-bit encoding indicating which bytes of din belong to the data input
dout	out	32	Data output (hash value)
dout_ready	in	1	A follow-up circuit ready to accept data
dout_valid	out	1	Data output present at the dout output