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XxHash32 Project - Verification

The top-level entity, the interface, was verified for functional correctness by testing 5 different scenarios. The 5 different scenarios consist of 5 different binary strings, which are the following:

Scenario 1:
x”0000_0001_0000_0010_0000_0100_0000_1000”
Description: 4 Words (16 bytes). Exactly 1 stripe.
Expected Hash: x"C3213C80"

Scenario 2:
x”0000_0001_0000_0010”
Description: 2 words (8 bytes), early exit, 2 remaining words.
Expected Hash: x"46650803"

Scenario 3:
"0000_0001_0000_0010_0000_0100_0000_1000_0001_0000_01"
Description: 5 words, 1 byte (21 bytes), 1 stripe, 1 remaining word, 1 remaining byte.
Expected Hash: x"E5D228DD"

Scenario 4:
"0000_0001_0000_0010_0000_0100_0302_01"
Description: 3 words, 3 bytes (15 bytes), early exit, 3 remaining words, 3 remaining bytes.
Expected Hash: x"71B282B6"

Scenario 5:
"0000_0001_0000_0010_0000_0100_0000_1000_0001_0000_0010_0000_0100_00001000_0000_0102_0304_0607_0809_0A0B_0E0F_ F0F1_F2F3_ FADE_CADE_ FACA_DEFF_ F4F5_F6F7_F8F9_FA "
Description: 15 words, 3 bytes (63 bytes), 3 stripes, 3 remaining words, 3 remaining bytes.
Expected Hash: x"250F0F2A"

Notes: Each binary string is provided in 32-bit packets presented at din with corresponding din_valid_bytes and other control signals. Please refer to assumptions or the provided testbench under any doubts.

Reasoning: The 5 different scenarios were deliberately chosen based on the description provided, as they cover all the possible paths of the xxHash32 algorithm. Scenarios 1-3 were also used for the Datapath, as these are the 3 main scenarios/paths of the algorithm, Scenarios 4 and 5 were later added to include a more exhaustive test of the interface. The values of the chosen binary strings were chosen at random. Since a reference implementation for the algorithm is available in C, it was easy to calculate the Hash for any input and then compare it to the one obtained during simulation.

Strategy: As mentioned above, the Datapath was the first to be tested, using scenarios 1-3. Initially, outputs were incorrect. In order to debug, the reference C implementation was modified to print intermediate values of all relevant operations. The values printed were then used to compare with the ones obtained during simulation; the values were compared by manually inspecting the simulation window. The Datapath was then corrected by checking the first incorrect intermediate value and then checking the function/components responsible for these values. Since during the Datapath testbench control signals must be manually asserted, this also revealed errors in control logic and the need for more/less control signals in the Datapath, all these issues were corrected at this stage by both modifying the way control signals are asserted in the tb and modifying the Datapath as needed, until all 3 scenarios produced the expected output. At this point, the Datapath is believed to be fully functional, and no further changes were made.

With the Datapath assumed to be fully functional, the verification of the controller was skipped and instead the Interface was directly tested, as any issues found at this stage are assumed to be directly related to the controller. Initially only scenarios 1-3 were used, and the output was initially incorrect. Once again intermediate values obtained with the modified reference implementation were used to compared against simulation, once the first incorrect intermediate value is spotted, the control signals in the ASM chart and VHDL code are checked, and any incorrect/missing signals are corrected. Once all the issues with the controller were corrected, the interface produced all the correct values for scenarios 1-3. Scenarios 4-5 were then added to double check for correct behavior, with both scenarios passing without the need for further modification. At this stage, the whole unit is believed to be fully functional.

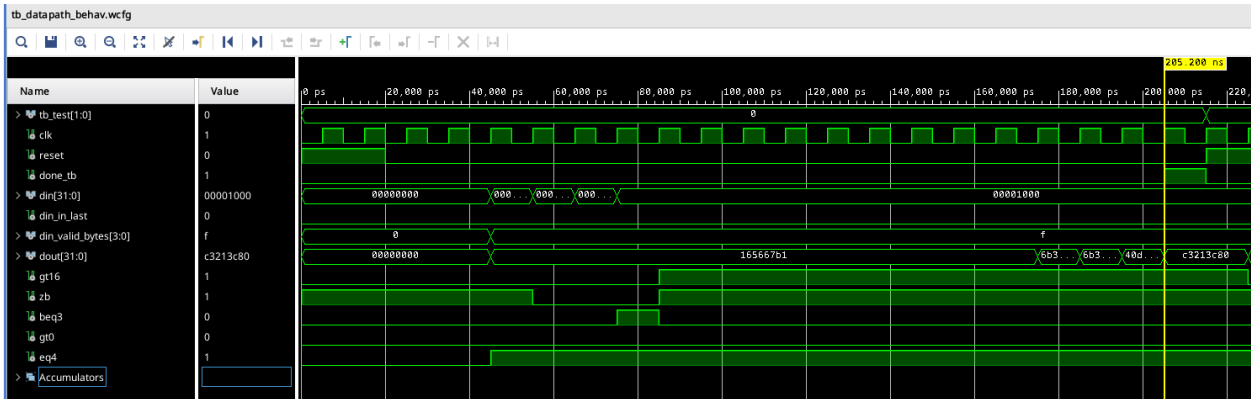
Results/Screenshots of the simulation window can be found in the following pages.

Datapath TB Results (Behavioral)

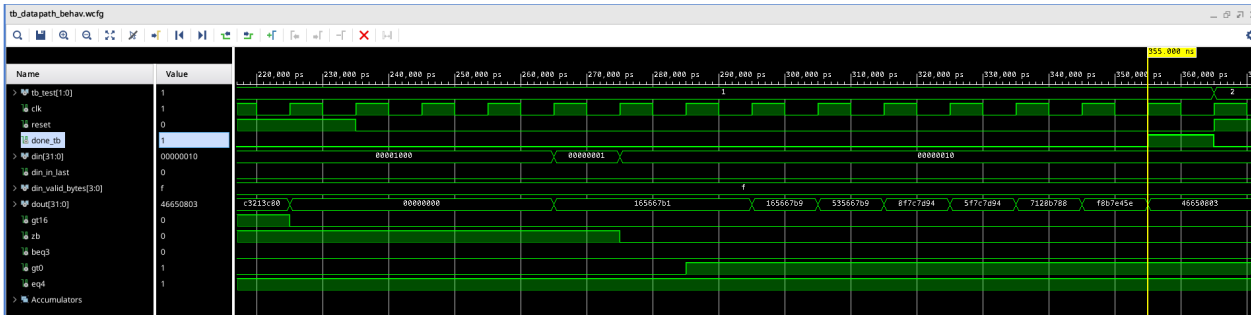
Summary:

```
# run 5000ns
Warning: Correct Output, Scenario 1 Passed
Time: 210 ns  Iteration: 0  Process: /tb_datapath/stim  File: /home/daps/Documents/xxHash32_Project/xxHash32/xxHash32.srcs/sim_1/new/tb_datapath.vhd
Time: 210 ns, Actual output: C3213C80, Expected output: C3213C80
Warning: Correct Output, Scenario 2 Passed
Time: 360 ns  Iteration: 0  Process: /tb_datapath/stim  File: /home/daps/Documents/xxHash32_Project/xxHash32/xxHash32.srcs/sim_1/new/tb_datapath.vhd
Time: 360 ns, Actual output: 46650803, Expected output: 46650803
Warning: Correct Output, Scenario 3 Passed
Time: 640 ns  Iteration: 0  Process: /tb_datapath/stim  File: /home/daps/Documents/xxHash32_Project/xxHash32/xxHash32.srcs/sim_1/new/tb_datapath.vhd
Time: 640 ns, Actual output: E5D228DD, Expected output: E5D228DD
INFO: [USF-XSim-96] XSim completed. Design snapshot 'tb_datapath_behav' loaded.
```

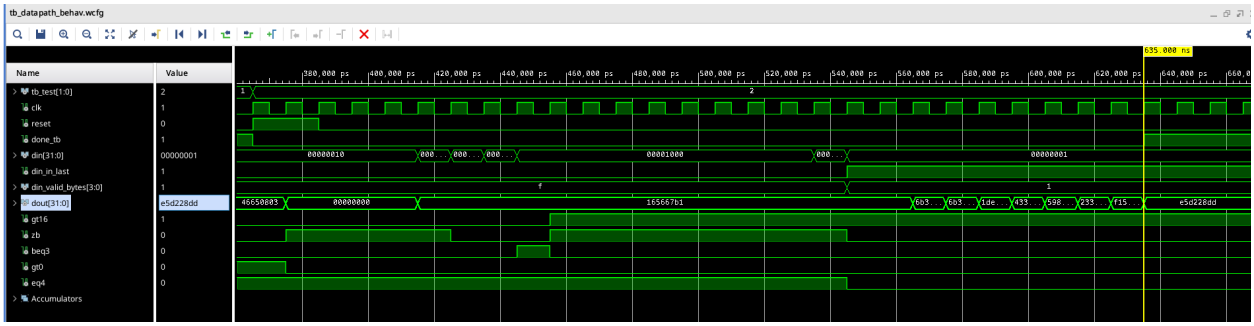
Scenario 1:



Scenario 2:



Scenario 3:

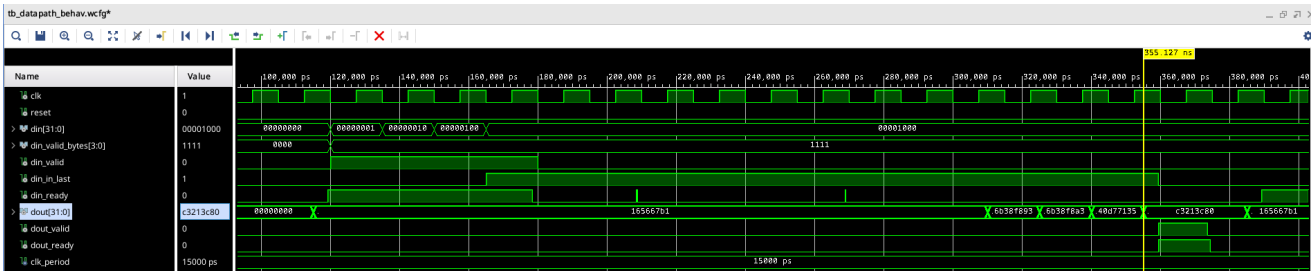


Interface TB Results (Post-Implementation Timing)

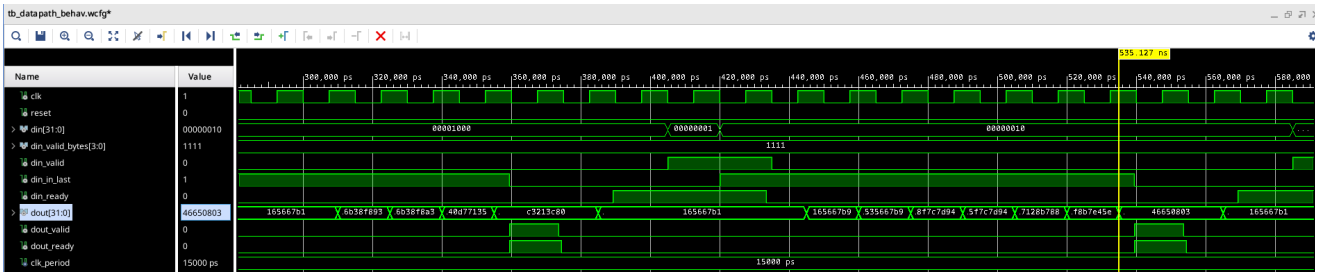
Summary:

```
# run 5000ns
Warning: Correct Output, Scenario 1 Passed
Time: 366860 ps  Iteration: 0  Process: /tb_interface/stim  File: /home/daps/Documents/xxHash32_Project/xxHash32/xxHash32.srcs/sim_1/new/tb_interface.vhd
Time: 366 ns, Actual output: C3213C80, Expected output: C3213C80
Warning: Correct Output, Scenario 2 Passed
Time: 546860 ps  Iteration: 0  Process: /tb_interface/stim  File: /home/daps/Documents/xxHash32_Project/xxHash32/xxHash32.srcs/sim_1/new/tb_interface.vhd
Time: 546 ns, Actual output: 46650803, Expected output: 46650803
Warning: Correct Output, Scenario 3 Passed
Time: 936860 ps  Iteration: 0  Process: /tb_interface/stim  File: /home/daps/Documents/xxHash32_Project/xxHash32/xxHash32.srcs/sim_1/new/tb_interface.vhd
Time: 936 ns, Actual output: E5D228DD, Expected output: E5D228DD
Warning: Correct Output, Scenario 4 Passed
Time: 1311860 ps  Iteration: 0  Process: /tb_interface/stim  File: /home/daps/Documents/xxHash32_Project/xxHash32/xxHash32.srcs/sim_1/new/tb_interface.vhd
Time: 1311 ns, Actual output: 71B282B6, Expected output: 71B282B6
Warning: Correct Output, Scenario 5 Passed
Time: 2241860 ps  Iteration: 0  Process: /tb_interface/stim  File: /home/daps/Documents/xxHash32_Project/xxHash32/xxHash32.srcs/sim_1/new/tb_interface.vhd
Time: 2241 ns, Actual output: 250F0F2A, Expected output: 250F0F2A
launch_simulation: Time (s): cpu = 00:00:15 ; elapsed = 00:00:09 . Memory (MB): peak = 9341.094 ; gain = 3.004 ; free physical = 36552 ; free virtual = 50898
```

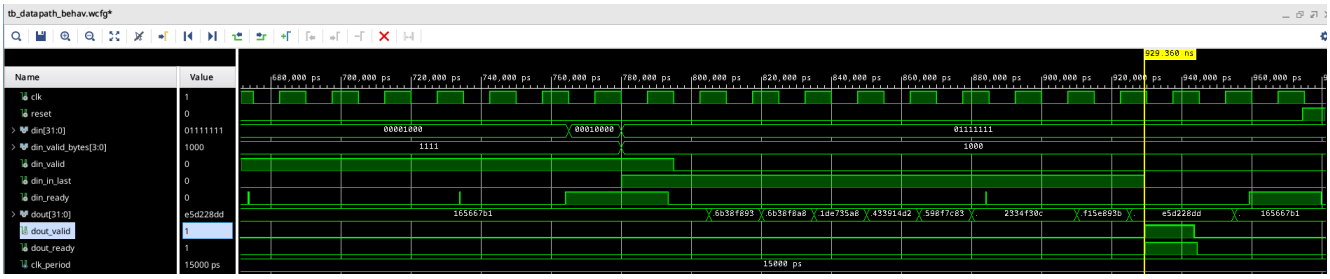
Scenario 1:



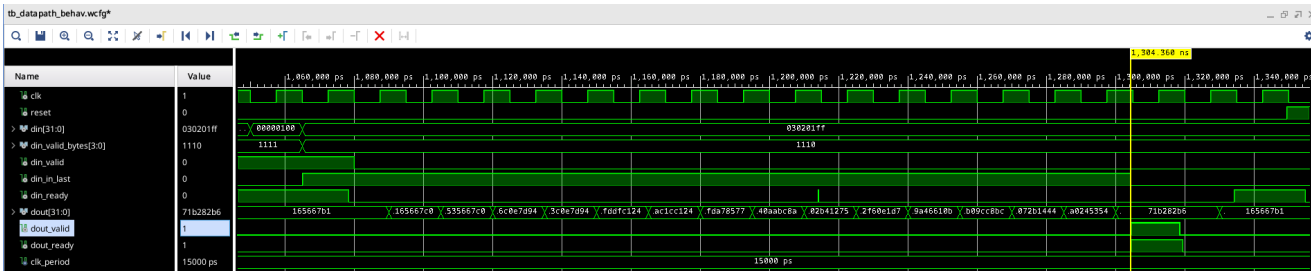
Scenario 2:



Scenario 3:



Scenario 4:



Scenario 5: