Diego Perez Sanchez

xxHash32 Project – Results

Device Used: xc7a12tcpg238-3

Timing Results

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.266 ns	Worst Hold Slack (WHS):	0.210 ns	Worst Pulse Width Slack (WPWS):	8.950 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	497	Total Number of Endpoints:	497	Total Number of Endpoints:	237

All user specified timing constraints are met.

Minimum clock = Target_Clk – WNS = 20 – 5.266 = 14.734ns

Maximum Frequency = 1/Minimum clock = 67.87 MHz

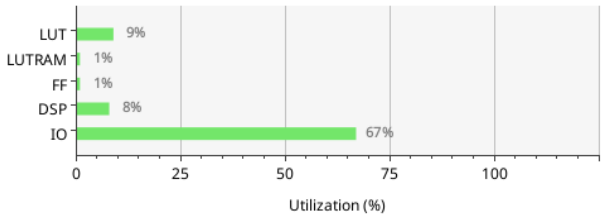
Utilization Results

Hierarchy

Name	Slice LUTs (8000)	Slice Registers (16000)	Slice (3650)	LUT as Logic (8000)	LUT as Memory (5000)	DSPs (40)	Bonded IOB (112)	BUFGCTRL (32)
interface	695	204	215	663	32	3	75	1
u_controller (controller)	493	5	145	493	0	0	0	0
u_datapath (datapath)	203	199	147	171	32	3	0	0
u_acc (reg)	32	33	32	32	0	0	0	0
u_acc1 (reg_0)	0	32	8	0	0	0	0	0
u_acc2 (reg_1)	0	32	8	0	0	0	0	0
u_acc3 (reg_2)	4	32	11	4	0	0	0	0
u_acc4 (reg_3)	60	32	25	60	0	0	0	0
u_buf_idx (counter)	4	2	4	4	0	0	0	0
u_buffer (data_buffer)	32	0	8	0	32	0	0	0
u_byte_cnt (reg_4)	41	32	16	41	0	0	0	0
u_mult (mult32)	25	0	13	25	0	3	0	0
u_ptr (counter_5)	0	2	1	0	0	0	0	0
u_rem_words (reg__parameterized0)	3	2	3	3	0	0	0	0

Summary

Resource	Utilization	Available	Utilization %
LUT	695	8000	8.69
LUTRAM	32	5000	0.64
FF	204	16000	1.28
DSP	3	40	7.50
IO	75	112	66.96



Analysis / Conclusions:

The main utilization is on IO due to the several amount of ports present and their bitwidths, 75 IO pins are used, which is consistent with the ports, as in total 75 bits are required among all ports. The DSP usage is low (3) because it is only used by the multiply unit, which is only instantiated once and reused across multiple stages. The controller uses the most amount o f LUTs as logic, which is consistent due to the several amount of states and conditions that must be check for transitioning between them. Furthermore, it is also in charge of generating a significant amount of control signals. The LUT as memory is only used for the buffer; buffer size is relatively small, which also keeps LUTRAM utilization very small. FFs are mostly used for Datapath, where they are being used for counters and accumulators, meanwhile the controller only uses 5 FF, which are likely being used to register the current state, as there are 23 states in total, and at least 5 bits are required to represent 23 possible states. Overall, the utilization of this design is relatively low. Because of this, the xc7a12tcpg238-3 was chosen as the device for the design, as it is one of the FPGAs with the least amount of resources in the in the artix 7 family, and its smaller size makes routing easier, leading to smaller delays.