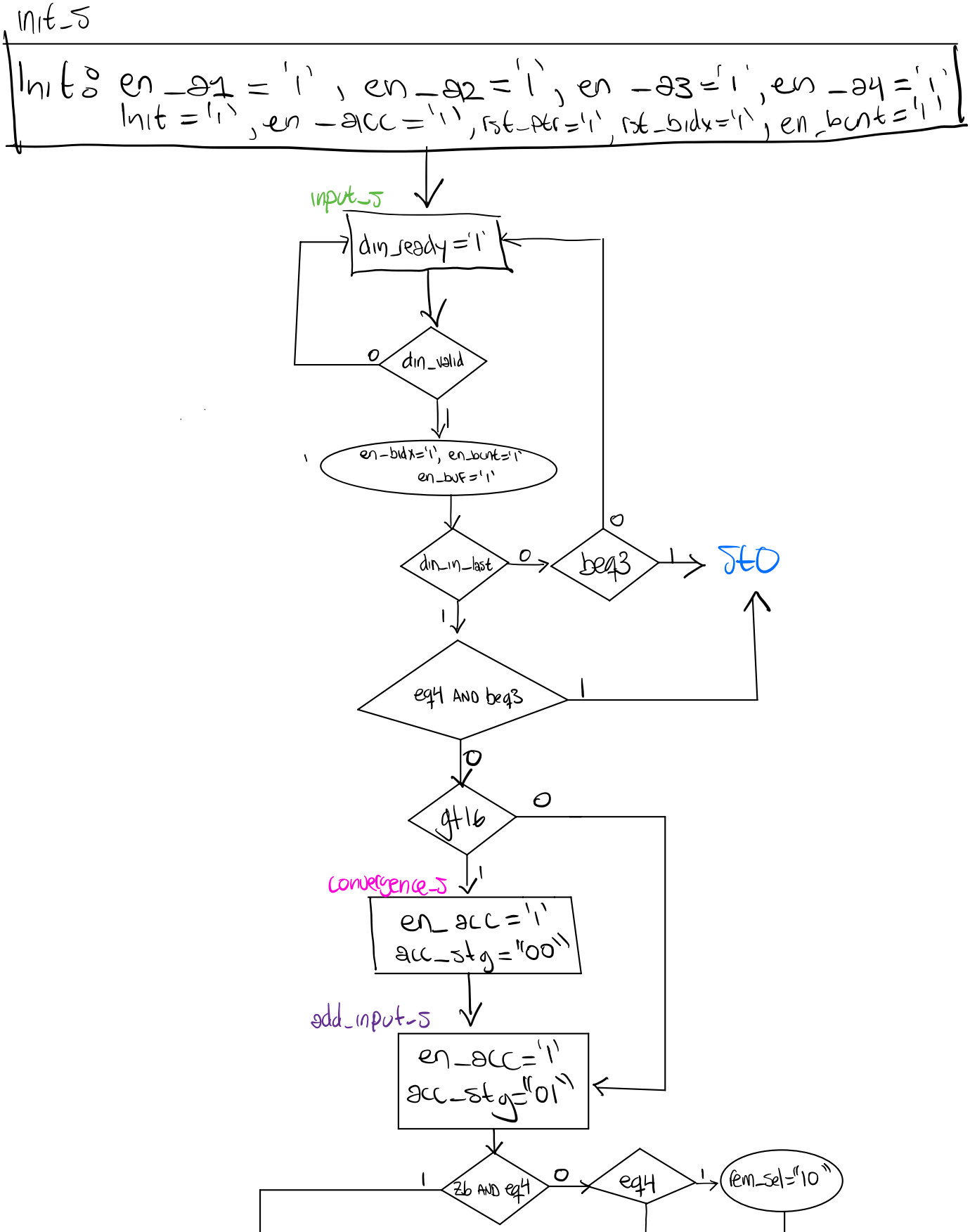
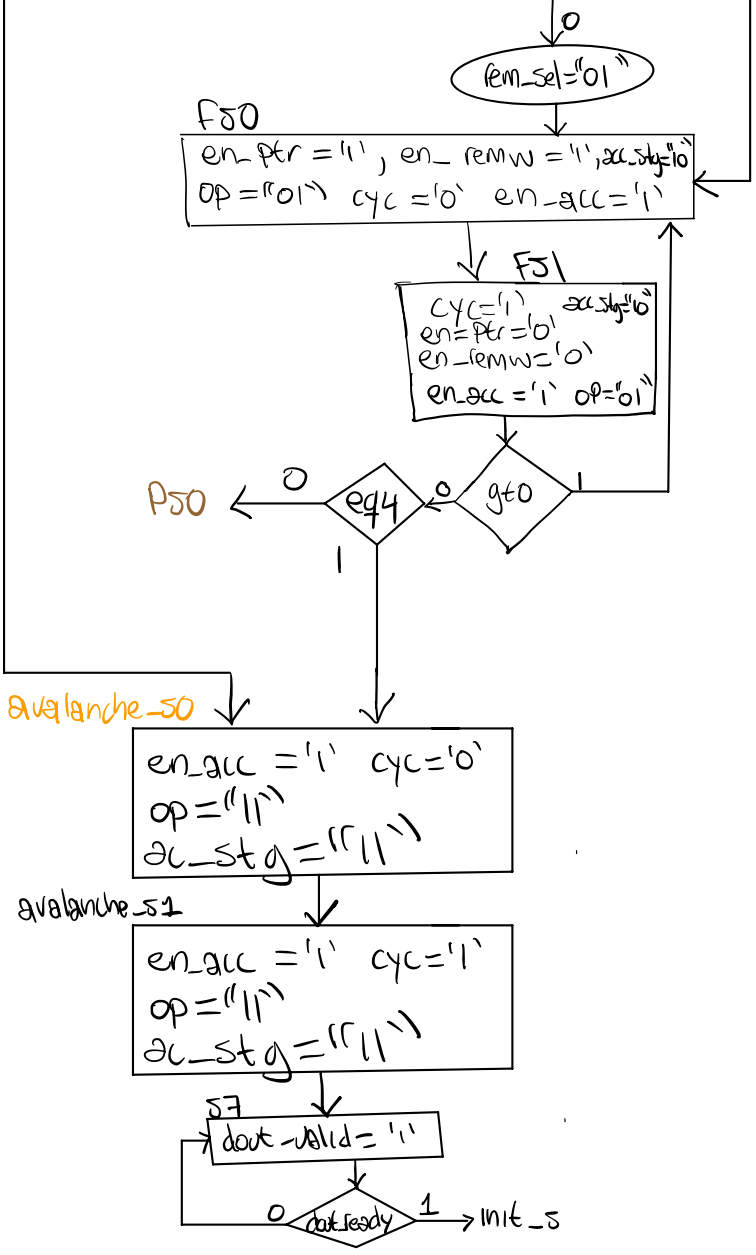
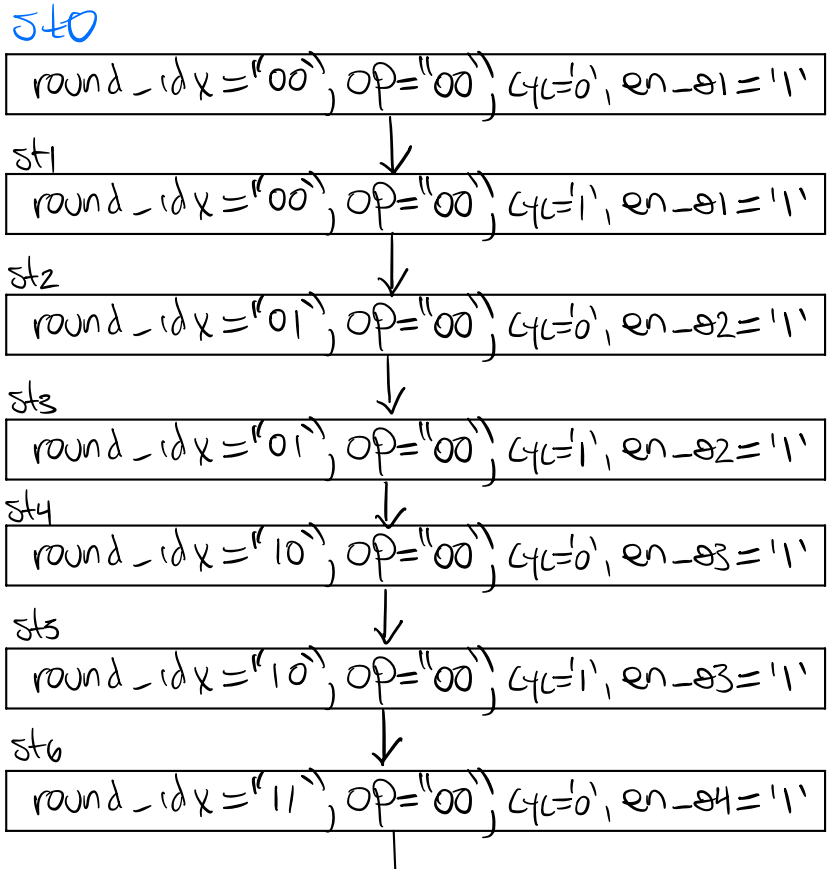
Diego Pérez Sanchez. xxHASH32 Controller ASM

All signals assumed to be (others => '0') unless otherwise stated

reset = 1 in any state will result in transition to init_s.




0
rem_sel="01"
F50
en_ptr='1', en_remw='1', acc_stg="10"
op="01" cyc='0' en_acc='1'
F51
cyc='1' acc_stg="10"
en_ptr='0'
en_remw='0'
en_acc='1' op="01"
P50
0
eq4
0
gt0
1
1
avalanche_50
en_acc='1' cyc='0'
op="11"
ac_stg="11"
avalanche_51
en_acc='1' cyc='1'
op="11"
ac_stg="11"
57
dout_valid='1'
0
dout_ready
1
init_5


st0
round_idx="00", op="00", cyc='0', en_s1='1'
st1
round_idx="00", op="00", cyc='1', en_s1='1'
st2
round_idx="01", op="00", cyc='0', en_s2='1'
st3
round_idx="01", op="00", cyc='1', en_s2='1'
st4
round_idx="10", op="00", cyc='0', en_s3='1'
st5
round_idx="10", op="00", cyc='1', en_s3='1'
st6
round_idx="11", op="00", cyc='0', en_s4='1'

st7
round_idx="11", op="00", cyc='1', en_sh='1'
din_in_last
0
input_s
1
gf16
1
convergence_s
0
add_input_s

P50
op="110" cyc='0' acc_sty="10"
din_valid_bytes3
0
1
byte_sel="00"
en_acc='1'
P51
op="110" cyc='1' byte_sel="00" en_acc='1' acc_sty="10"
P52
op="110" cyc='0' acc_sty="10"
din_valid_bytes2
0
1
byte_sel="01"
en_acc='1'
P53
op="110" cyc='1' byte_sel="01" en_acc='1' acc_sty="10"
P54
op="110" cyc='0' acc_sty="10"
din_valid_bytes1
0
1
byte_sel="10"
en_acc='1'
P55
op="110" cyc='1' byte_sel="10" en_acc='1' acc_sty="10"
avalanche_s0