Lab 1:: Combinational Circuits Lab

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Problems

1. **Design a circuit that has three inputs and two outputs. Output 1 indicates when the 3-bit unsigned input is odd and output 2 indicates when the 3-bit unsigned input value is even. Provide the initial equations that describe your circuit and minimize your output equations using k-maps. Draw your circuits from the minimized equations using AND, OR, and NOT gates. Now, given that you have two outputs, two initial equations, two k-maps, and two solutions, you should have two circuits:**

    1a.These circuits should be minimal, but, what does this mean?

    1b. If possible, draw a (third) simpler circuit that will give both outputs.

Truth Table:

Input			Output	
a	b	c	EVEN	ODD
0	0	0	1	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	1	0
1	1	1	0	1

EVEN Logical Equation:

a’b’c’+a’bc’+ab’c’+abc’=EVEN

EVEN KMAP:

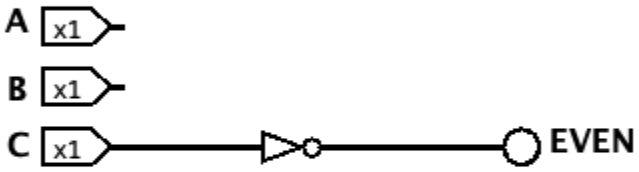
	BC

A	00	01	10	11
0	1	0	1	0
1	1	0	1	0

Using the KMAP above we can simplify the equation too:

EVEN = c’

EVEN Circuit:



Description:
The only time that a binary number is odd is when there is a 1 in the right-most bit or in this case if we go by the labels above if c is true. Therefore our original equation can be simplified to EVEN= c’. Using this simplified equation, all we need is an inverter coming from c to the output even in order to display the correct output.

ODD Logical Equation:

a’b’c+a’bc+ab’c+abc=ODD

ODD KMAP:

A	BC 00	01	10	11
0	0	1	1	0
1	0	1	1	0

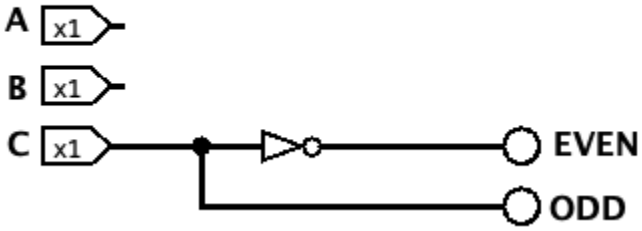
After using the ODD KMAP we can minimize the equation too:

ODD = c

ODD Circuit:

Description:
As stated before we are really only looking at value c in order to determine whether or not a binary numbers integer value is even or odd. Therefore we know that if we simplify our original equation for odd we will get, ODD=c. Using this simplified version we can see that there is simply going to be a wire from the c input to the Odd output.

ODD AND EVEN CIRCUIT:



Description:
If we apply what we found for the previous two circuits we can combine these two circuits into the same circuit by simply having the c input wire be split to the two outputs and having there still be one inverter.

2. Design a circuit that has four inputs and three outputs. Output one indicates whether the two's complement signed 4-bit input is larger than 5, output two indicates if the signed 4-bit input is smaller than -5, and output three indicates that the signed 4-bit input is equal to zero. Provide the initial equations that describe your circuit and minimize your output equations using k-maps. Draw your circuits from the minimized equations using AND, OR, and NOT gates.

1. **Redraw your equations using NAND gates only.**
2. **You should have three NAND gate circuits. Think about whether or not you can reuse common segments of your NAND-only circuits. If so, draw a new common circuit that is as minimal as you can achieve and describe your process for creating your circuit. If not discuss why it's not possible.**

Truth Table:

Input				Output		
a	b	c	d	X (>5)	Y(<-5)	Z(0)
0	0	0	0	0	0	1
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	0	1	0	0	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	0
1	0	1	0	0	1	0
1	0	1	1	0	0	0
1	1	0	0	0	0	0
1	1	0	1	0	0	0
1	1	1	0	0	0	0
1	1	1	1	0	0	0

X(>5) KMAP:

AB \ CD	00	01	11	10
00	0	0	0	0
01	0	0	1	1
11	0	0	0	0
10	0	0	0	0

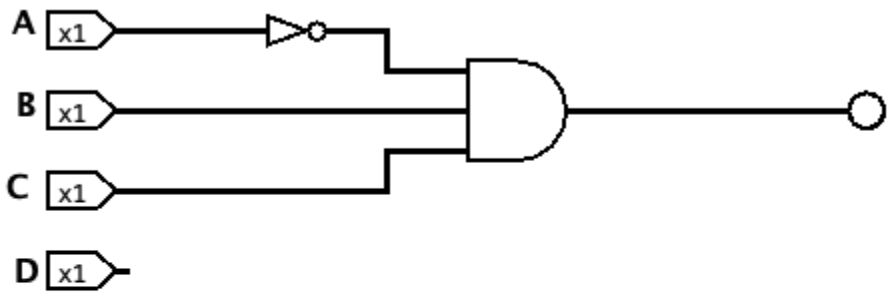
X Unsimplified equation:

X= a'bcd' +a'bcd

X Simplified equation:

X= a'bc

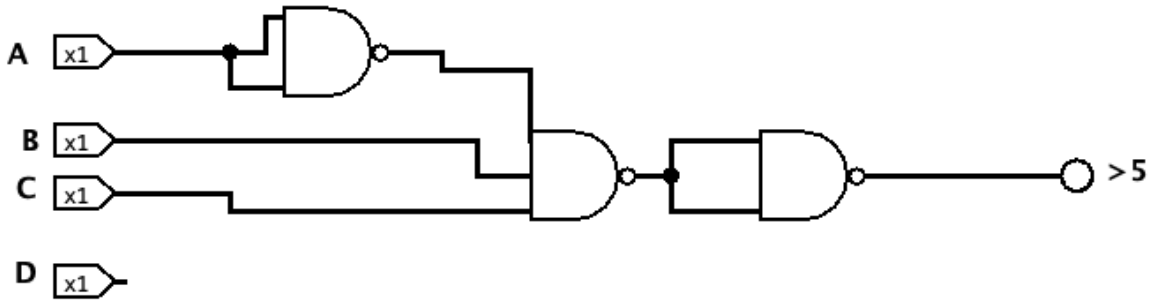
X Circuit (W/O NAND):



Description:

Using the simplified equation we can see that the value of input D does not effect the desired output and therefore is not connected to this specific circuit. Therefore in the end we should have one inverter for the input A and the inputs of B and C enter an AND gate to get the specified output.

X Circuit NAND:



Description:
If we use our knowledge of NAND gates and apply it to the circuit above we can see that there are two NAND gates connected to eachother to create an AND gate and one NAND gate to create an inverter for the A input.

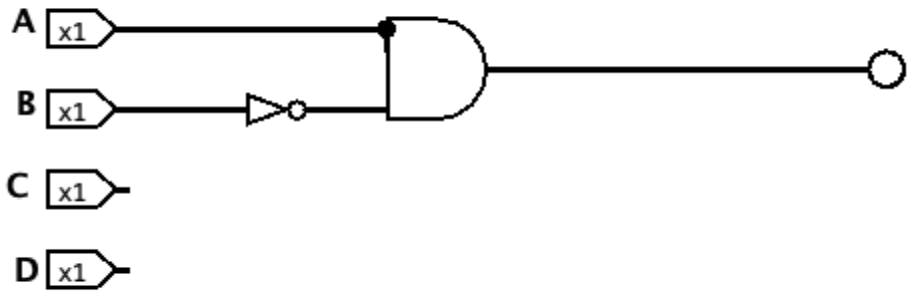
Y(<-5) Truth Table:

AB \ CD	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0	0	0
10	1	1	0	1

Y Equation:
Y= ab'c'd'+ab'c'd+ab'cd'

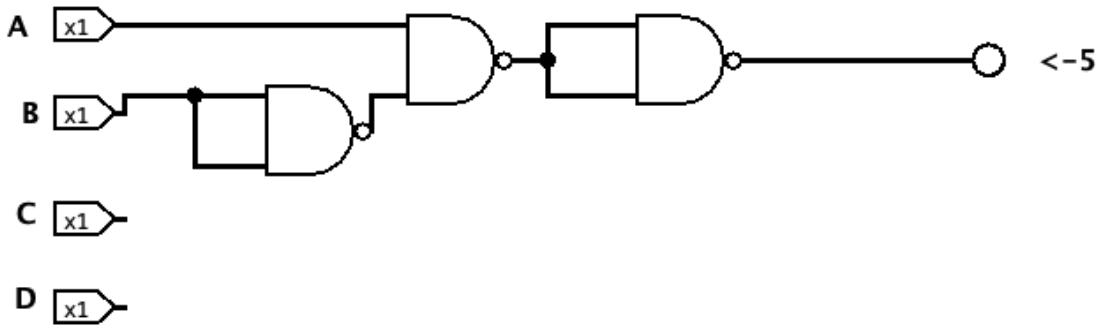
Y Simplified Equation:
Y=ab'
Using the KMAP above we can see that there are some inputs that are not exactly needed to get the specified output. Therefore we can use it to find the minimal equation for output Y.

Y Circuit (W/O NAND):



Description:
Using the simplified equation for the specified output we can see that there is no need to connect input C or D into the circuit in this case. I inverted the value of B and added an AND gate to get the specified output.

Y Circuit (NAND):



Description:
If we use our knowledge of NAND gates and apply it to the circuit above we can see that there are two NAND gates connected to eachother to create an AND gate and one NAND gate to create an inverter for the B input.

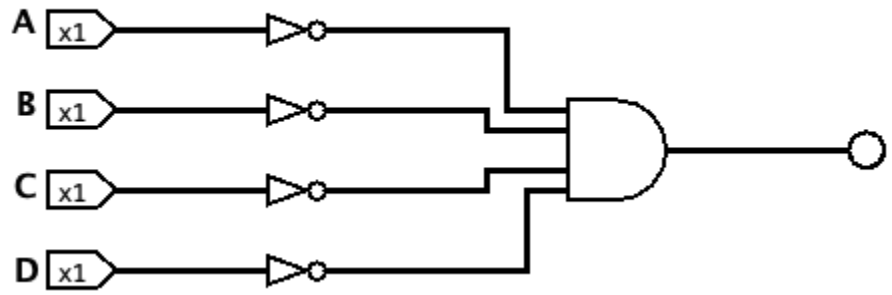
Z(0) Truth Table:

AB \ CD	00	01	11	10
00	1	0	0	0
01	0	0	0	0
11	0	0	0	0

AB \ CD	00	01	11	10
10	0	0	0	0

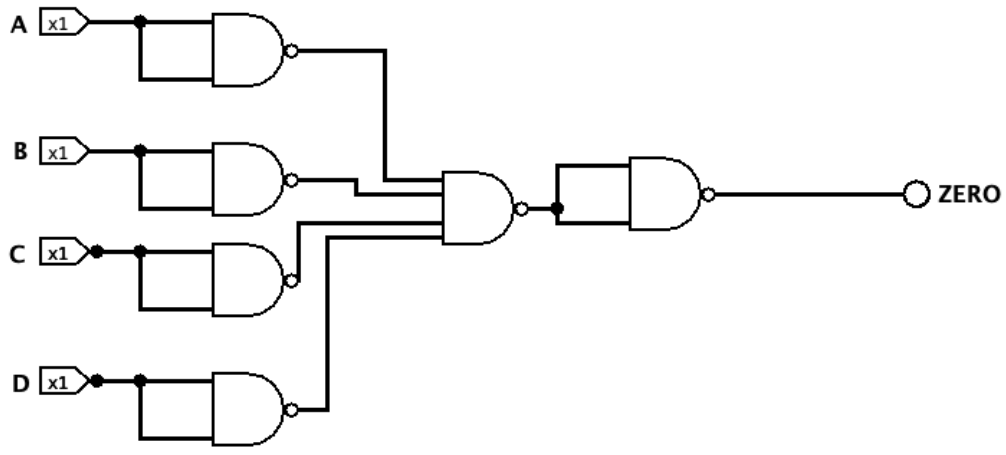
Z equation:
a'b'c'd'=Z

Z Circuit (W/O NAND):



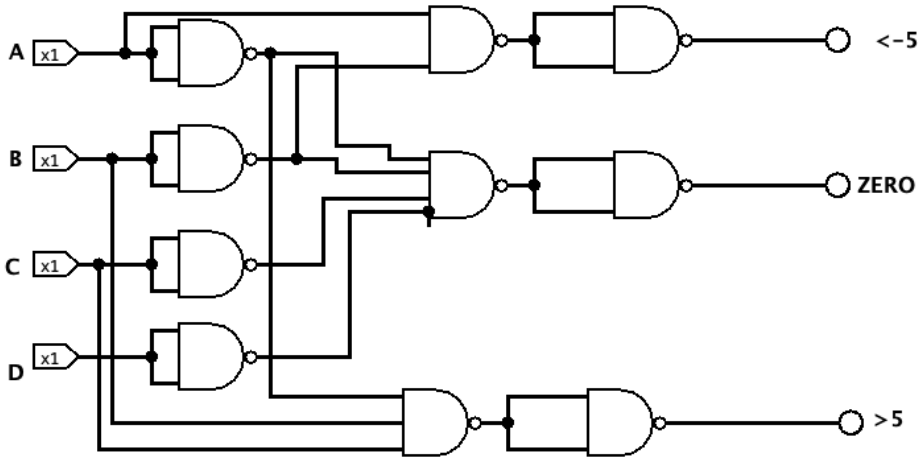
Description:
This desired input is to find out if the input results in a zero therefore we have 4 inverters and an AND gate present. Using the KMAP and the truthtable we can see that there is only one instance where this output will be true and that is if all inputs are inverted.

Z Circuit (NAND):



Description:
Using out knowledge of NAND gates and the circuit made previously we will have 5 NAND gates to give us the desired input.

Combined Circuit with NAND:



Description:
If we use the Truth Table and the KMAP with each logical equation we can combine all of the circuits into one using the NAND gates that we have. In the end we will have 10 NAND gates for the specified outputs.

3. Consider an apartment that has two bedrooms and a shared hallway to a common area. There is a single hall light and a switch in each room to turn on the hall light. No matter what position each switch is in, flipping either switch turns the hall light on if off, or off if on. Your goal is to design a logic circuit to represent this problem. Define the inputs and outputs and then provide the initial equations that describe your circuit and minimize your output equations using k-maps. Draw your circuits from the minimized equations using AND, OR, and NOT gates.

1. **Now that you've designed this circuit can you reduce the number of gates? You may use any kind of gates that we have discussed in class.**

Truth Table:

Input		Output
A	B	Light
0	0	0
0	1	1
1	0	1

1	1	0

LIGHT KMAP:

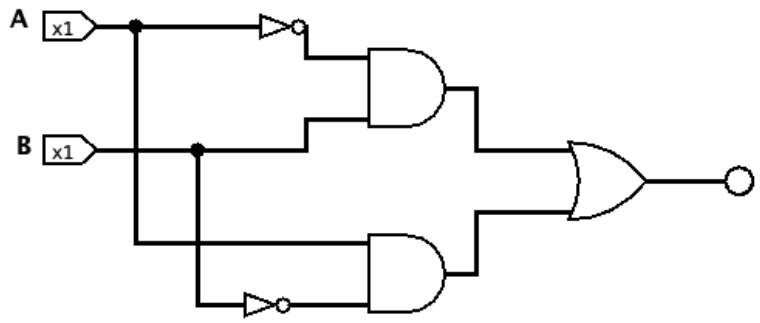
A	B 0	1
0	0	1
1	1	0

LIGHT Equation with Simplification:

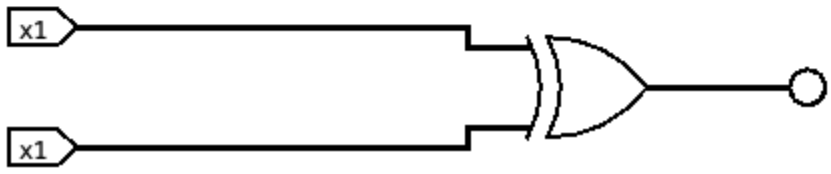
a'b +ab'=LIGHT

a ⊕ b = LIGHT

Unsimplified Circuit:



Simplified Circuit:



Description:
If we use the unsimplified equation and the truthtable above we can see that the circuit needed to get the desired output is composed of two inverters, two AND gates and an OR gate. I specifically used this circuit to get to my next conclusion that the desired output can be done by implementing one XOR Gate.

2. **Your landlord is thinking of adding a third bedroom. Can your design be easily modified to accommodate this? Why or why not?**

If the landlord is adding a third bedroom the design cannot be easily modified to accommodate this due to the fact that when inputting the third bedroom there will be no way for that bedroom to turn the light back on if either of the other bedrooms has the light switched on. If we simply added another input on the XOR gate or the gate above the output would not be correct and therefore there is not a way to simply add another bedroom that would have the same simplicity as the two bedrooms would.

4. A given circuit has four inputs. Two of the inputs are considered the fractional portion of a binary number while the other two inputs are considered the integral portion of the binary number. The outputs of this circuit should represent a 2-bit binary number associated with the 4-bit input but with rounding up and down. In other words, if the input is greater or equal to 0.5, the output should represent the input rounded up. Otherwise, its output should represent the input rounded down to the nearest integer. Note: For this exercise, you may assume that the input will never be larger than can be represented by the output, in other words, it will not *overflow.* You may treat any overflow input conditions as don't care. Provide a truth table, a reduced Boolean equation, and a circuit diagram for your solution using AND, OR, and NOT gates.

Truth Table:

Input				Output	
a	b	c	d	X	Y
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	0	1
0	1	0	1	0	1
0	1	1	0	1	0

0	1	1	1	1	0
1	0	0	0	1	0
1	0	0	1	1	0
1	0	1	0	1	1
1	0	1	1	1	1
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

X KMAP:

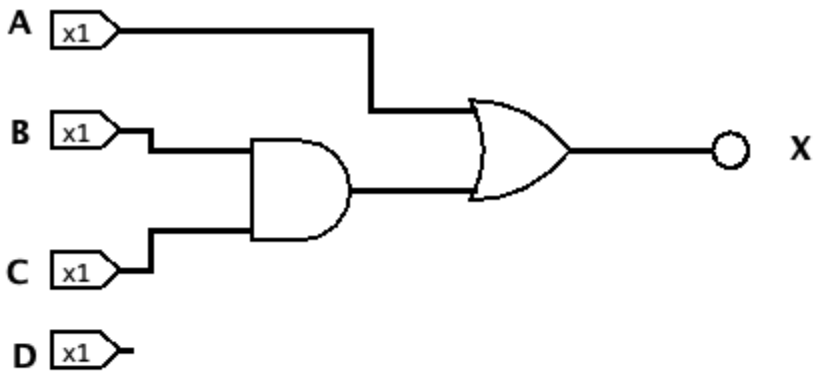
AB \ CD	00	01	11	10
00				
01			1	1
11	1	1	1	1
10	1	1	1	1

X Equation:

X = A+BC

Using the KMAP we have reduced the equation and the outputs down to the equation above.

X Circuit:



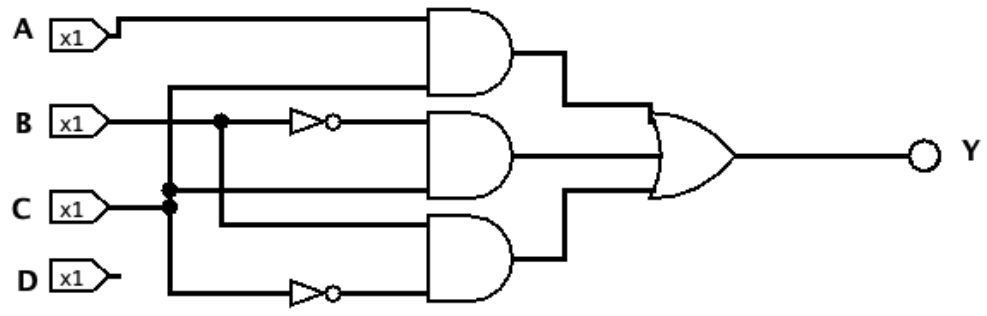
Description:
The simplified equation for this input and the KMAP above shows that one of the inputs here do not effect the desired output of the circuit and therefore there will not be a need to implement that input (input D) to this circuit. We can see that there is a total of 2 gates.

Y KMAP:

AB	CD 00	01	11	10
00			1	1
01	1	1		
11	1	1	1	1
10			1	1

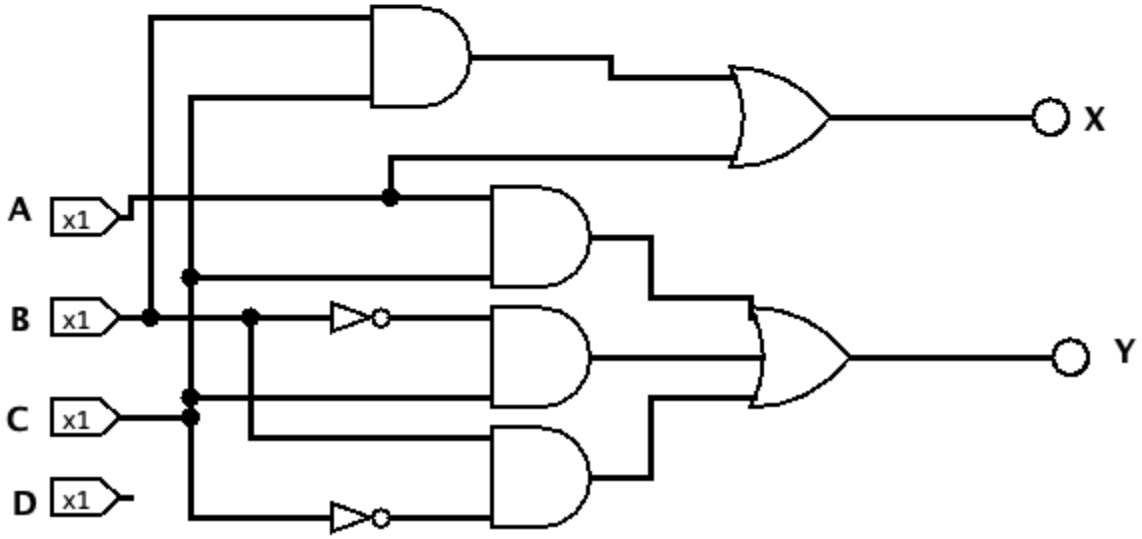
Y Equation:
Y = BC' + AC+B'C
Using the KMAP above we can simplify the logical equation to the one written above.

Y Circuit:



Description:
Using the KMAP and the simplified equation we can see that again there is no need for the fourth input in order to get the desired output of our circuit. The above circuit can be simplified to habeing 3 gates instead of 6 gates if we implement an XOR gate on the inputs B and C and then have the input A be OR'ed with those two inputs.

X AND Z CIRCUIT:



Description:
The above input is a combination of the findings that we had at the end of simplifying both of our outpu equations. In this case we used the inputs in multiple ways in order to get the output that is desired for each of the specific equations. There are multiple ways to simplify this circuit with the implementation of an XOR gate and some other reworkings.