Tabla 1

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

C\AB	00	01	10	11
0	1	1	1	0
1	0	0	1	1

Y = A'C'+AC+B’C’

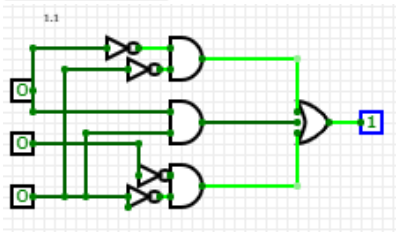


Tabla 2

A	B	C	Y
0	0	0	1
0	0	1	X
0	1	0	0
0	1	1	0
1	0	0	X
1	0	1	1
1	1	0	0
1	1	1	0

C\AB	00	01	10	11
0	1	0	X	0
1	X	0	1	0

Y = B’

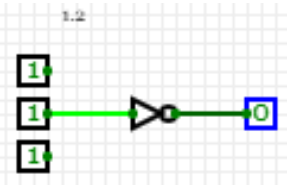


Tabla 3

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

CD\AB	00	01	10	11
00	1	0	1	0
01	0	1	0	0
10	1	0	1	0
11	0	1	0	1

Y = A'B'C'D'+A'B'CD+A'BC'D+A'BCD' + AB'C'D +AB'CD'+ABC'D'+ABCD

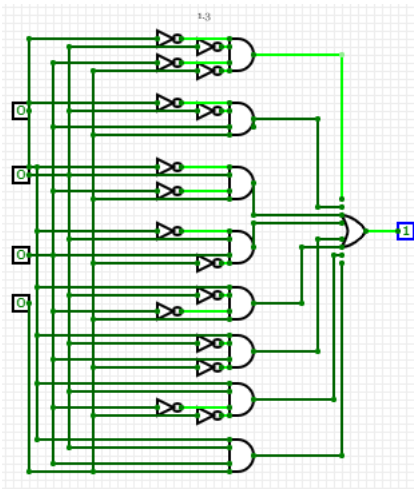
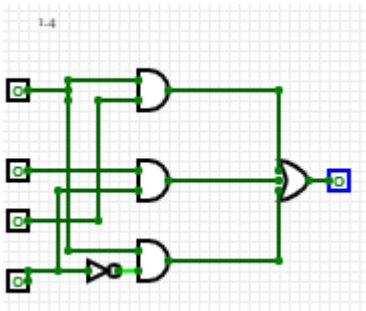


Tabla 4

A	B	C	D	Y
0	0	0	0	X
0	0	0	1	X
0	0	1	0	X
0	0	1	1	0
0	1	0	0	0
0	1	0	1	X
0	1	1	0	0
0	1	1	1	X
1	0	0	0	1
1	0	0	1	0
1	0	1	0	X
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	X
1	1	1	1	1

CD\AB	00	01	10	11
00	X	0	1	1
01	X	X	0	1
10	X	0	X	X
11	0	X	1	1

Y = AD'+AC+BD

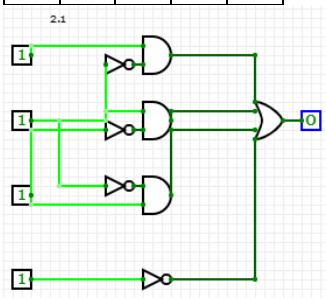


Parte 2

1. $Y = A \cdot B \cdot C \cdot D' + A \cdot (B \cdot C \cdot D)' + (A + B + C + D)'$
   $Y=AB'+BC'+B'C+D'$

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

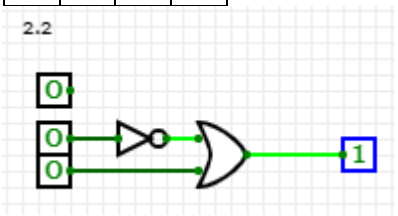
CD\AB	00	01	10	11
00	1	1	1	1
01	0	1	1	1
10	1	1	1	1
11	1	0	1	0



2. $Y = A' \cdot B \cdot C + (B \cdot C')' + B \cdot C$
   $Y=B'+C$

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

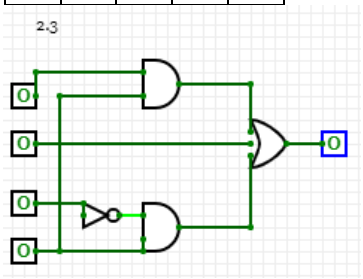
C\AB	00	01	10	11
0	1	0	1	0
1	1	1	1	1



3. $Y = (A + B + C)' \cdot D + A \cdot D + B$
   Y=AD+B+C'D

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

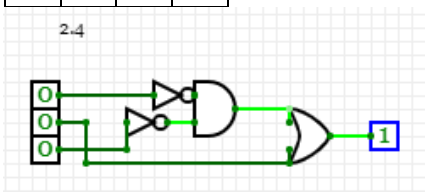
CD\AB	00	01	10	11
00	0	1	0	1
01	1	1	1	1
10	0	1	0	1
11	0	1	1	1



4. $Y = B \cdot C + A' \cdot B' \cdot C' + B \cdot C'$
   $Y=B+A'C'$

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

C\AB	00	01	10	11
0	1	1	0	1
1	0	1	0	1



CODIGO GATES

GATES: Bloc de notas

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```
module GATES1(input wire A, B, C, output wire Y);

// ECUACIÓN A IMPLEMENTAR: A'C'+AC+B'C' 1.1

  assign Y=(~A & ~C) | (A & C) | (~B & ~C);

endmodule

module GATES2(input wire A, B, C,D, output wire Y);

// ECUACIÓN A IMPLEMENTAR: A’B’C’D’+A’B’CD+A’BC’D+A’BCD’ + AB’C’D +AB’CD’+ABC’D’+A

  assign Y=(~A & ~B &~C & ~D) | (~A & ~B & C & D) | (~A & B & ~C & D) | (~A & B &

endmodule

module GATES3(input wire A, B, C, D, output wire Y);

// ECUACIÓN A IMPLEMENTAR: AD'+AC+BD 1.4

  assign Y=(~A & ~C) | (A & C) | (~B & ~C);

endmodule

module GATES4(input wire A, B, C, D, output wire Y);

// ECUACIÓN A IMPLEMENTAR: AB'+BC'+B'C+D' 2.1

  assign Y=(A & ~B) | (B & ~C) | (~B & C) | (~D);

endmodule
```

Lm 9, Col 15 | 100% | Windows (CRLF) | UTF-8

GATES_tb: Bloc de notas

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```
module testbench();

  reg P1, P2, P3, P4;
  wire Y1, Y2, Y3, Y4;

  GATES1 G1(P1, P2, P3, Y1);
  GATES2 G2(P1, P2, P3, P4, Y2);
  GATES3 G3(P1, P2, P3, P4, Y3);
  GATES4 G4(P1, P2, P3, P4, Y4);

  initial begin
    $display("A B C | Y");
    $display("-------");
    $monitor("%b %b %b | %b", P1, P2, P3, Y1);
    P1 = 0; P2 = 0; P3 = 0;
    #1 P3 = 1;
    #1 P2 = 1; P3 = 0;
    #1 P3 = 1;
    #1 P1 = 1; P2 = 0; P3 = 0;
    #1 P3 = 1;
    #1 P2 = 1; P3 = 0;
    #1 P3 = 1;
//    #1 $finish;
  end

  initial begin
    #8
    $display("\n\n");
    $display("A B C D | Y");
    $display("------------");
    $monitor("%b %b %b %b | %b", P1, P2, P3, P4, Y2);
    P1 = 0; P2 = 0; P3 = 0; P4 = 0;
    #1 P4 = 1;
    #1 P3 = 1; P4 = 0;
    #1 P4 = 1;
```

Lm 101, Col 13 | 100% | Windows (CRLF) | UTF-8

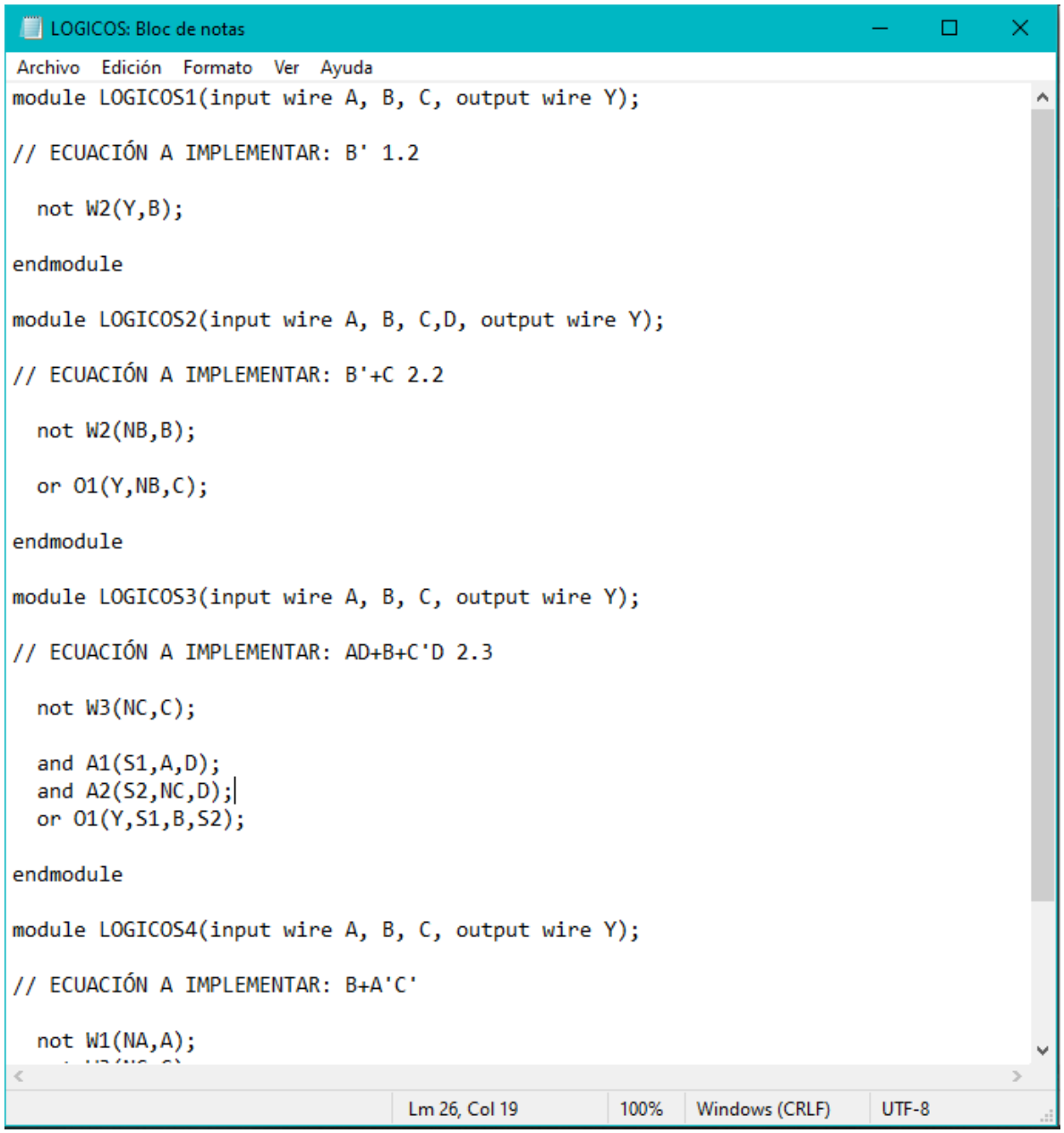
GATES_tb: Bloc de notas

Archivo Edición Formato Ver Ayuda

```
initial begin
    #25
    $display("\n\n");
    $display("A B C D | Y");
    $display("------------");
    $monitor("%b %b %b %b | %b", P1, P2, P3, P4, Y3);
    P1 = 0; P2 = 0; P3 = 0; P4 = 0;
    #1 P4 = 1;
    #1 P3 = 1; P4 = 0;
    #1 P4 = 1;
    #1 P2 = 1; P3 = 0; P4 = 0;
    #1 P4 = 1;
    #1 P3 = 1; P4 = 0;
    #1 P4 = 1;
    #1 P1 = 1; P2 = 0; P3 = 0; P4 = 0;
    #1 P4 = 1;
    #1 P3 = 1; P4 = 0;
    #1 P4 = 1;
    #1 P2 = 1; P3 = 0; P4 = 0;
    #1 P4 = 1;
    #1 P3 = 1; P4 = 0;
    #1 P4 = 1;
//    #1 $finish;
  end
initial begin
    #42
    $display("\n\n");
    $display("A B C D | Y");
    $display("------------");
    $monitor("%b %b %b %b | %b", P1, P2, P3, P4, Y4);
    P1 = 0; P2 = 0; P3 = 0; P4 = 0;
    #1 P4 = 1;
    #1 P3 = 1; P4 = 0;
    #1 P4 = 1;
    #1 P2 = 1; P3 = 0; P4 = 0;
```

Lm 101, Col 13 | 100% | Windows (CRLF) | UTF-8

COGICO COMPUERTAS LOGICAS


LOGICOS: Bloc de notas
Archivo Edición Formato Ver Ayuda
module LOGICOS1(input wire A, B, C, output wire Y);
// ECUACIÓN A IMPLEMENTAR: B' 1.2
not W2(Y,B);
endmodule
module LOGICOS2(input wire A, B, C,D, output wire Y);
// ECUACIÓN A IMPLEMENTAR: B'+C 2.2
not W2(NB,B);
or O1(Y,NB,C);
endmodule
module LOGICOS3(input wire A, B, C, output wire Y);
// ECUACIÓN A IMPLEMENTAR: AD+B+C'D 2.3
not W3(NC,C);
and A1(S1,A,D);
and A2(S2,NC,D);
or O1(Y,S1,B,S2);
endmodule
module LOGICOS4(input wire A, B, C, output wire Y);
// ECUACIÓN A IMPLEMENTAR: B+A'C'
not W1(NA,A);
Lm 26, Col 19
100%
Windows (CRLF)
UTF-8

LOGICOS: Bloc de notas

Archivo Edición Formato Ver Ayuda

```
endmodule

module LOGICOS2(input wire A, B, C,D, output wire Y);

// ECUACIÓN A IMPLEMENTAR: B'+C 2.2

  not W2(NB,B);

  or O1(Y,NB,C);

endmodule

module LOGICOS3(input wire A, B, C, output wire Y);

// ECUACIÓN A IMPLEMENTAR: AD+B+C'D 2.3

  not W3(NC,C);

  and A1(S1,A,D);
  and A2(S2,NC,D);
  or O1(Y,S1,B,S2);

endmodule

module LOGICOS4(input wire A, B, C, output wire Y);

// ECUACIÓN A IMPLEMENTAR: B+A'C'

  not W1(NA,A);
  not W3(NC,C);

  and A1(S1,NA,NC);
  or O1(Y,S1,B);

endmodule
```

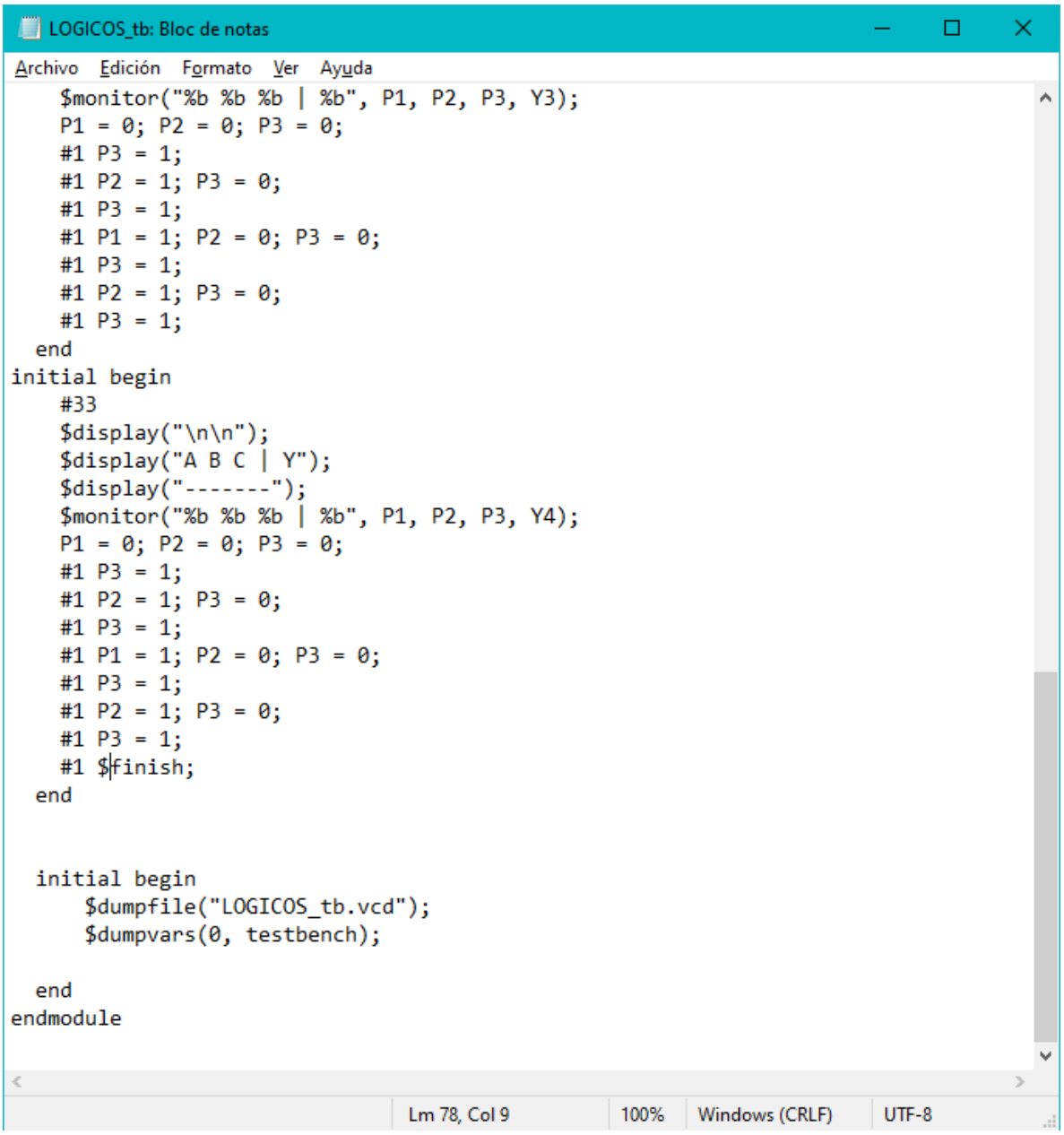
Ln 26, Col 19 | 100% | Windows (CRLF) | UTF-8

LOGICOS_tb: Bloc de notas

Archivo Edición Formato Ver Ayuda

```
module testbench();

  reg P1, P2, P3, P4;
  wire Y1, Y2, Y3, Y4;

  LOGICOS1 L1(P1, P2, P3, Y1);
  LOGICOS2 L2(P1, P2, P3, P4, Y2);
  LOGICOS3 L3(P1, P2, P3, Y3);
  LOGICOS4 L4(P1, P2, P3, Y4);

  initial begin
    $display("A B C | Y");
    $display("-------");
    $monitor("%b %b %b | %b", P1, P2, P3, Y1);
    P1 = 0; P2 = 0; P3 = 0;
    #1 P3 = 1;
    #1 P2 = 1; P3 = 0;
    #1 P3 = 1;
    #1 P1 = 1; P2 = 0; P3 = 0;
    #1 P3 = 1;
    #1 P2 = 1; P3 = 0;
    #1 P3 = 1;
  end

  initial begin
    #8
    $display("\n\n");
    $display("A B C D | Y");
    $display("------------");
    $monitor("%b %b %b %b | %b", P1, P2, P3, P4, Y2);
    P1 = 0; P2 = 0; P3 = 0; P4 = 0;
    #1 P4 = 1;
    #1 P3 = 1; P4 = 0;
    #1 P4 = 1;
    #1 P2 = 1; P3 = 0; P4 = 0;
```

Lm 78, Col 9 | 100% | Windows (CRLF) | UTF-8


LOGICOS_tb: Bloc de notas
Archivo Edición Formato Ver Ayuda
$monitor("%b %b %b | %b", P1, P2, P3, Y3);
P1 = 0; P2 = 0; P3 = 0;
#1 P3 = 1;
#1 P2 = 1; P3 = 0;
#1 P3 = 1;
#1 P1 = 1; P2 = 0; P3 = 0;
#1 P3 = 1;
#1 P2 = 1; P3 = 0;
#1 P3 = 1;
end
initial begin
#33
$display("\n\n");
$display("A B C | Y");
$display("-------");
$monitor("%b %b %b | %b", P1, P2, P3, Y4);
P1 = 0; P2 = 0; P3 = 0;
#1 P3 = 1;
#1 P2 = 1; P3 = 0;
#1 P3 = 1;
#1 P1 = 1; P2 = 0; P3 = 0;
#1 P3 = 1;
#1 P2 = 1; P3 = 0;
#1 P3 = 1;
#1 $finish;
end
initial begin
$dumpfile("LOGICOS_tb.vcd");
$dumpvars(0, testbench);
end
endmodule
Lm 78, Col 9
100%
Windows (CRLF)
UTF-8

REPOSITORIO ONLINE

https://github.com/dar17320/Lab-4