Secondary Memory Interface (SMI)

Extracted from Broadcom data sheet.

G.J. van Loo, 26-11-2017

The Secondary Memory Interface (SMI) is intended for use with devices that might otherwise slow down or interfere with system operations if they were connected directly to the system bus. It is intended to:

- Connect to 8-bit, 9-bit, 16-bit and 18-bit register based devices.
- Support both RD/WR and Enable/Direction style devices (Mode80 and Mode68).
- Support MIPI DBI and Nokia MeSSI standard devices.
- Support the use of small and large page multiplexed NAND devices.
- Minimise the performance impact that connecting slow devices would cause by running the SMI bus off a slower asynchronous clock.
- Allow precise control of all SMI bus timings.

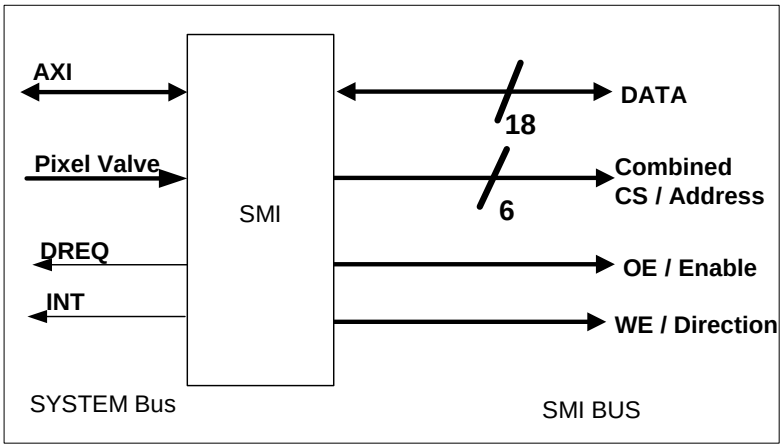

Figure 1 SMI

1 Connecting devices to the Secondary Memory Interface

The Secondary Memory Interface has the following external pins:

SD[17:0]

These pins are the external data bus for the Secondary Memory Interface. The peripheral supports 8-bit, 9-bit, 16-bit and 18-bit devices.

SA[5:0]

These pins combine the traditional functionality of Chip Select pins and Address pins.

When the bus is idle these pins will be driven high. By carefully choosing the value to be placed on these pins when the bus is in use it is possible to use these pins as either Chip Selects, or Address pins.

For example, the bus can support 3 devices, each with up to 3 address pins like this:

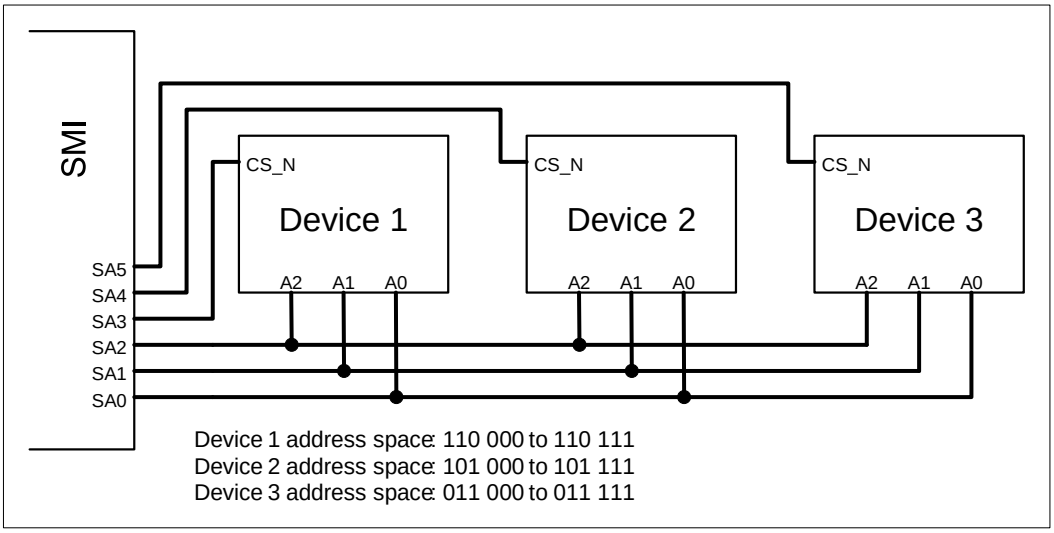

Figure 2 Three Devices With Three Address Pins

Or if fewer devices are fitted it is possible to support devices with more address pins.

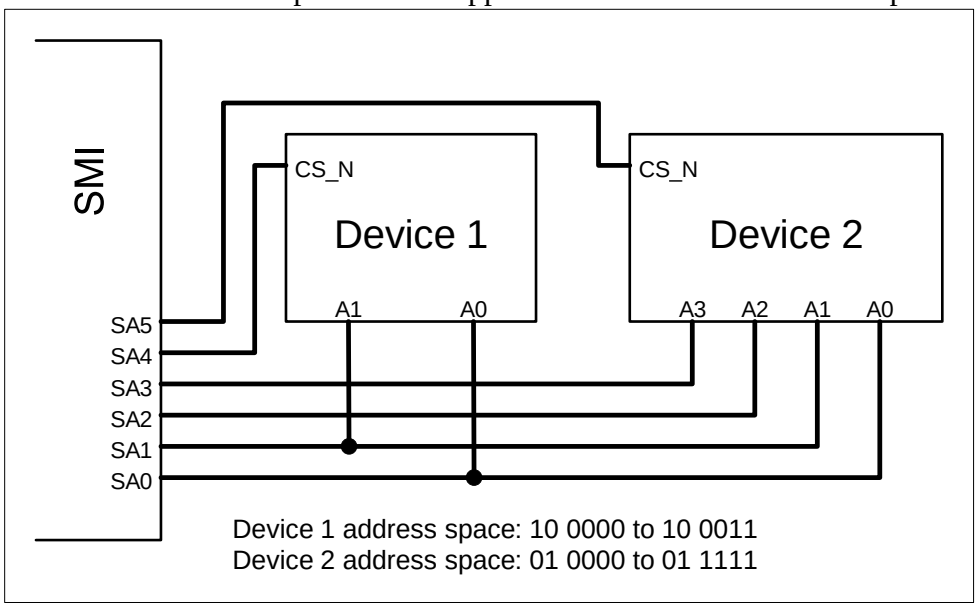

Figure 3 Two Devices With Up To Four Address Pins

Devices which only have an active high chip select can be connected to the Secondary Memory Interface, but only one such device can be connected. All SA[5:0] pins are driven high when the Secondary Memory Interface is idle, so such a device would be selected at those times. It is therefore not possible to connect a Mode68 device with an active high chip select.

SOE_N/SE and SWE_N/SRW_N

These signals act as the read and write strobes for Intel style devices (Mode80 devices), and also as direction and enable signals for Motorola style devices (Mode68 devices).

Mode 68 and Mode80 devices can be mixed on the bus as the bus mode is programmable in the device configuration registers (SMIDSx). As there are 3 configuration registers a different one can be used for each device.

2 External Bus Timings

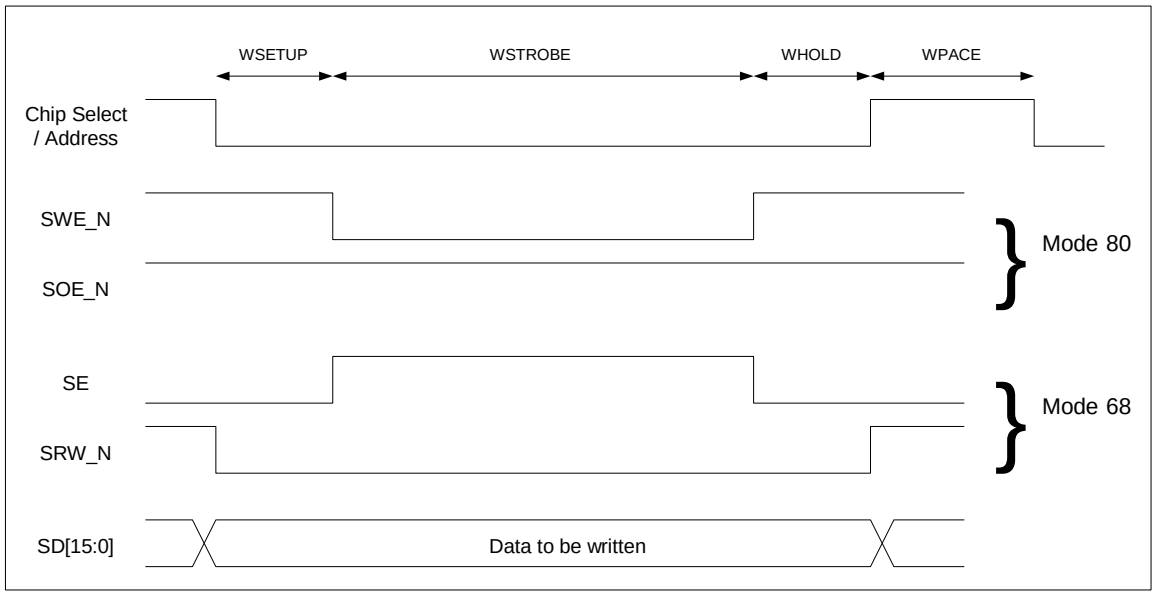

Figure 4 Write Cycle Timings

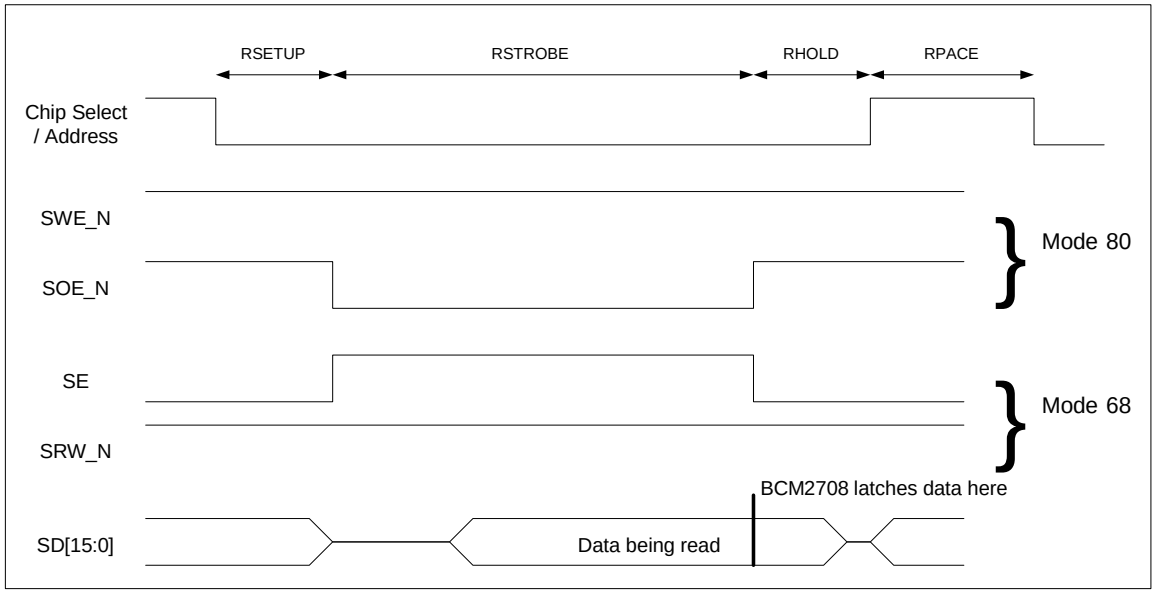

Figure 5 Read Cycle Timings

3 Switching between Mode80 and Mode68 devices

The bus will always remain in the mode last used. If it becomes necessary to change the mode of the bus then the mode will be changed BEFORE the address is put onto the bus so that no devices will be enabled. After changing the mode of the bus the interface will wait a time equal to the setup time of the transfer about to occur. On reset Mode80 device settings are used.

4 Theory of Operation

The SMI can be programmed to carry out a sequence of transfers in one direction (either reading or writing) to one address. The number of transfers in the sequence is programmable.

Data is passed between the system AXI bus and an external peripheral device via two asynchronous FIFOs. This ensures that the system AXI bus is never blocked and does not have to wait for a slow external peripheral and the SMI bus can be run at a slower speed.

The FIFOs may be accessed either by the CPU polling the SMI, or by an external DMA engine using DREQ signals to moderate the data flow.

When idle the bus will have:

- All CS/address pins driven high.
- All data pins driven with the last value written.
- OE/WE will be driven high if last transfer was Mode80, otherwise both low.

Direct writes can be performed whilst a sequence of transfers is taking place. This allows control type operations to be performed whilst a large data transfer is underway.

4.1 Programmed Write

A programmed write will perform SMI_L writes to an address on the SMI bus.

Before enabling the SMI (see SMI_CS register), the length of the required transfer should be written to the SMI_L register. The address to be used should be written to the SMI_A register and the write device settings written to the relevant SMI_DSW register if necessary. The SMI should then be enabled and any relevant control bits set up (such as WRITE to indicate a device write). The transfer is started by writing a 1 to the START bit of SMI_CS.

Data is then written into the write FIFO (SMI_D) either directly by the CPU as space becomes available (reflected by the status flags) or by DMA using DREQ to moderate the flow. As long as there is available data to write the SMI will perform successive writes to the external device using the timings specified by the selected SMI_DSW register. By keeping the write FIFO full it should be possible to write data to the external device at its maximum transfer rate. Writing to the write FIFO when there is insufficient space will result in some or all of the data written being ignored.

4.2 Programmed Read

A programmed read will perform SMI_L reads from an address on the SMI bus.

As with writing, the SMI is configured and instructed to perform the transfer automatically. The SMI will repeatedly read from the device until the transfer completes or the read FIFO fills up.

If the read FIFO becomes full the SMI will stop reading from the device until there is space in the read FIFO to store the read data.

For programmed reads and writes the SMI_A, SMI_L and SMI_DSR and/or SMI_DSW registers must not be written to whilst the SMI is enabled. The SETERR bit in the SMI_CS register will be set if this has occurred and can be cleared by writing a 1 to this bit.
Similarly the WRITE, PAD, DMAP and PXLDAT bits of the SMICS register must be written before or on the same write as the SMI is enabled.

4.3 Direct Write

A direct write will perform a single write to the specified address on the SMI bus. It can be performed whilst a programmed transfer is taking place.

The address for the direct write must be written to the SMI_DA register and the data to the SMI_DD register. With the peripheral enabled the direct transfer is started by writing a 1 to the START bit in the SMID_CS register and a write configured by writing a 1 to the WRITE bit. The peripheral will schedule the write even with a programmed transfer in progress and will return a 1 to the DONE bit in SMID_CS when complete.

4.4 Direct Read

A direct read will perform a single read from the specified address on the SMI bus. It can be performed whilst a programmed transfer is taking place.

The address for the direct read must first be written to the SMI_DA register. With the peripheral enabled the direct transfer is started by writing a 1 to the START bit in the SMI_DCS register, and a read configured with the WRITE bit set to 0. The peripheral will schedule the read even with a programmed transfer in progress and will return a 1 to the DONE bit in SMI_DCS when complete.

Reading the SMI_DD register while this done flag is set returns the read data. The DONE flag is cleared by writing a 1 to this bit in the SMI_DCS register.

The SMI_DA and SMI_DD registers must not be written to whilst a direct transfer is active. The SETERR bit will be set if this has occurred and can be cleared by writing a 1 to this bit.

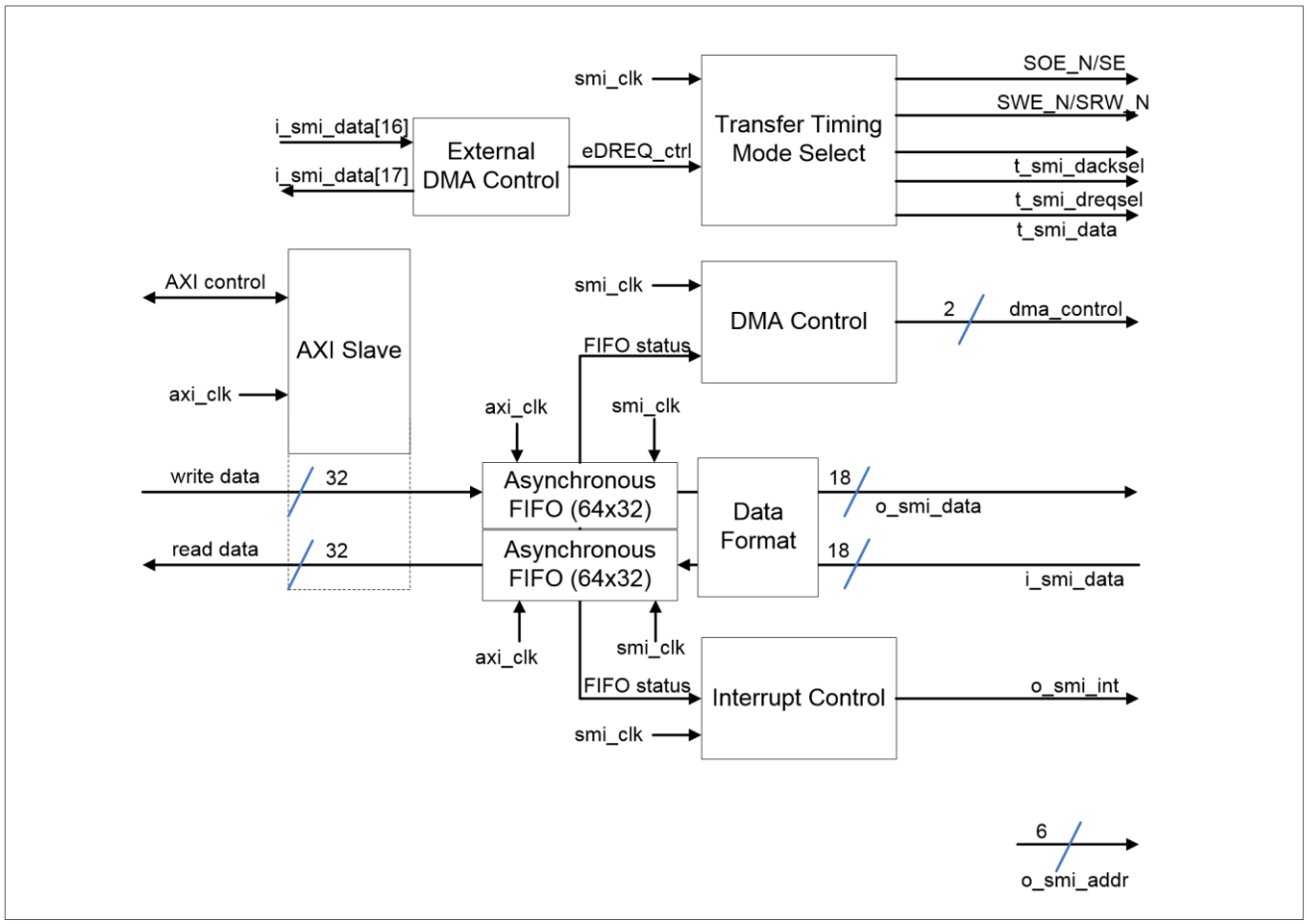

Figure 6 SMI Architecture

5 Architecture

Figure 6 shows the general architecture of the SMI block. There are three state machines, one to control the output timing to the external device, one to control the interface to the AXI bus and one to control external DREQ handling. There are two 256-byte asynchronous FIFOs to handle read and write transfers to the device.

When writing to an external device data is written to the write FIFO from the AXI slave, clocked by the AXI clock, and read out by the device, clocked by the SMI clock.

When reading from an external device the device writes to the read FIFO, clocked by the SMI clock, and the AXI slave reads out data, clocked by the AXI clock.

There are also additional blocks to control interrupts and the DMA. External DMA requests may be passed through the SMI using the top two bits of the data bus.

6 Output Data Modes

The SMI can interface with 8-bit, 9-bit, 16-bit and 18-bit register devices. Numerous data formats are supported, as detailed in this section. Data may be written to the FIFO in 16-bit RGB565 format or 32-bit XRGB format. Depending on the format of the data being transferred the WFORMAT bit in the relevant SMI_DSW register must be written to. For SWAP modes the WSWAP bit in the same SMI_DSW register must also be written to. For all the pixel modes shown the PXLDAT bit in the

SMI_CS register must be set to ensure each FIFO entry corresponds to the required number of external transfers. For example, for PXLDAT set to 1 and WFORMAT set to 0 for a 16-bit interface, one 32-bit FIFO entry corresponds to two external transfers over the SMI data bus, the lower 16 bits forming the data for the first transfer and the upper 16 bits for the second transfer. The SMI_L register would have to be written with a value twice as large as the number of 32-bit words written to the write FIFO.

6.1 18-bit Interface

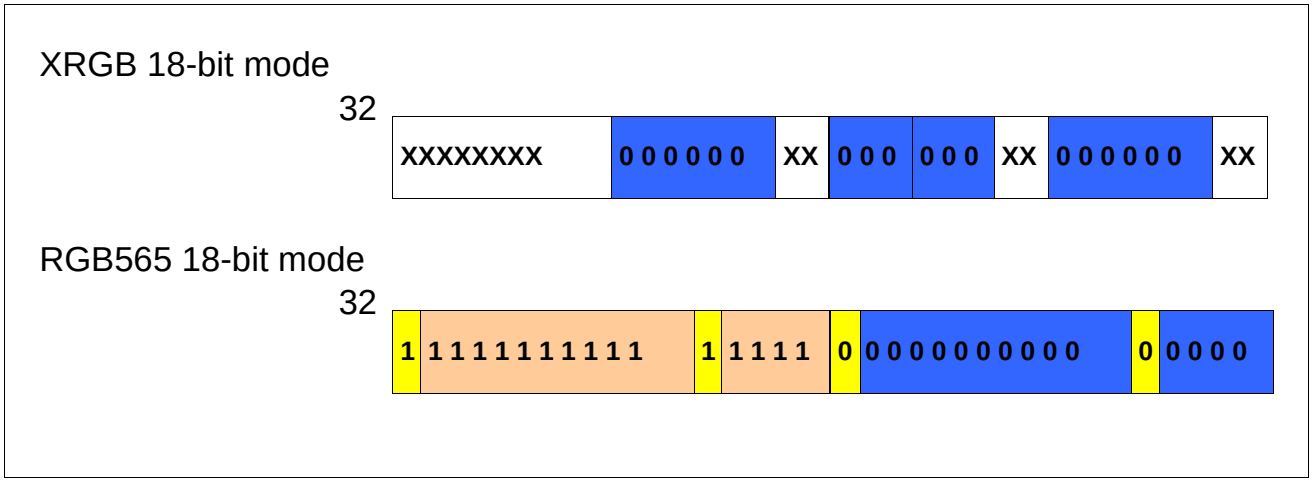

Figure 7 18-bit Interface Modes

Bits are selected as shown in the diagram. For RGB565 input data the bits highlighted in yellow specify repeated bits to form an 18-bit value. The output format is:

SD[17:0] = { FIFO[15:11], FIFO[15], FIFO[10:0], FIFO[4] }

Two 16-bit values are stored per location in the FIFO to save space. Each of the bit orders may be reversed in SWAP for little ordered support.

6.2 16-bit Interface

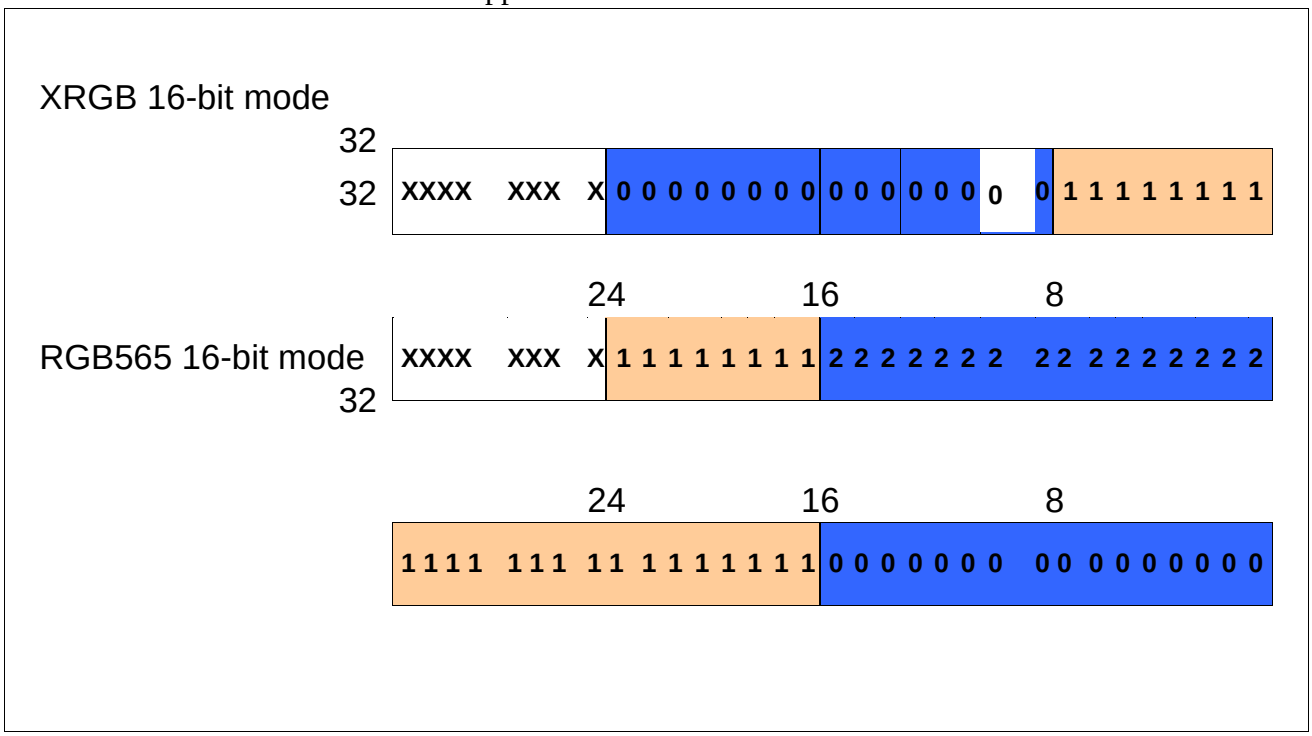

Figure 8 16-bit Interface Modes

These 16-bit modes support MIPI DBI and Nokia MeSSI standard displays.

6.3 9-bit Interface

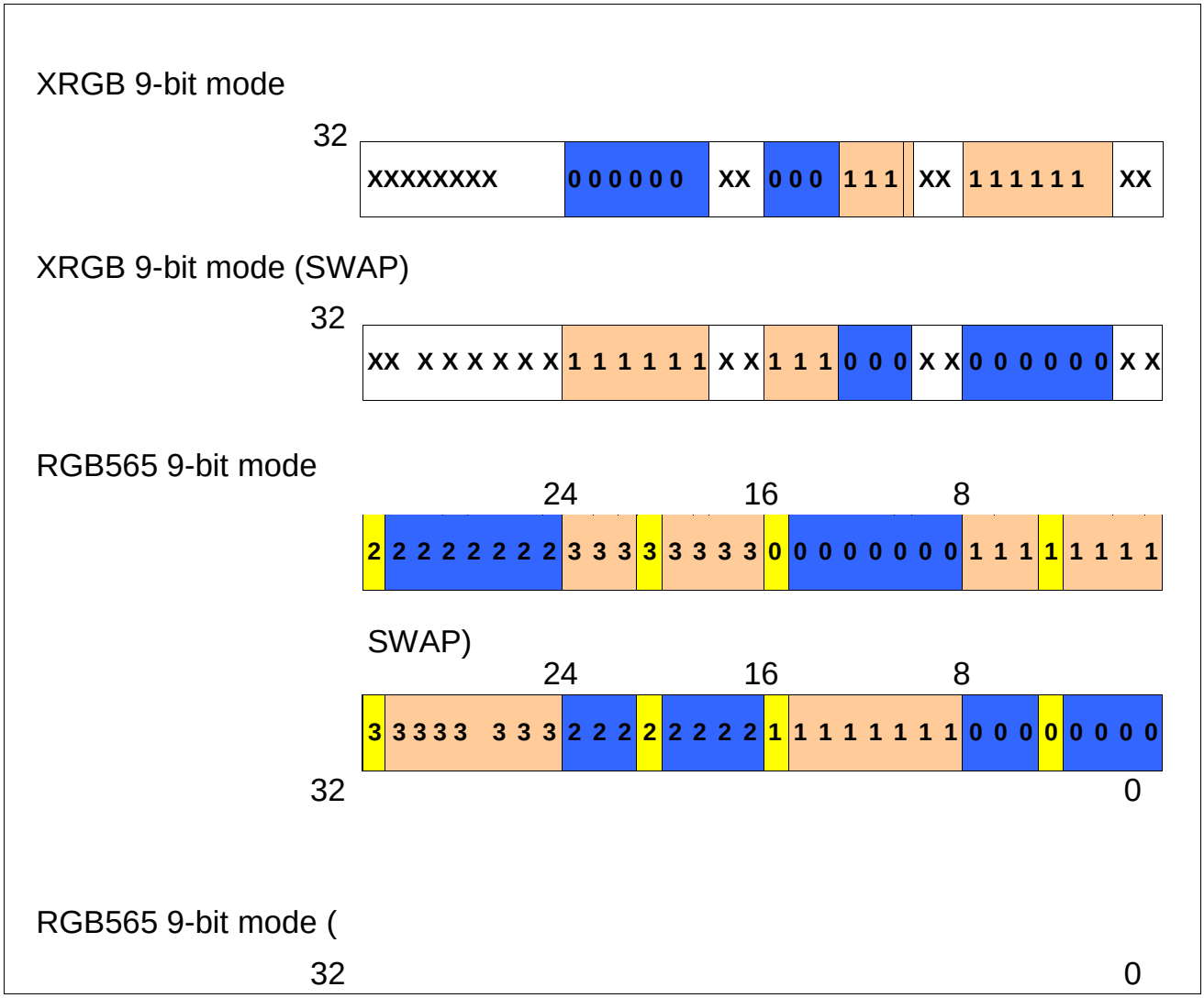

Figure 9 9-bit Interface Modes

For RGB565 input data the bits highlighted in yellow specify repeated bits to form a 9-bit value. The output format is for the first transfer is:

SD[8:0] = { FIFO[7:0], FIFO[4] } The output

format for the second transfer is:

SD[8:0] = { FIFO[15:11], FIFO[15], FIFO[10:8] }

In each case, the data is big-ordered. These modes support MIPI DBI and Nokia MeSSI standard devices.

6.4 8-bit Interface

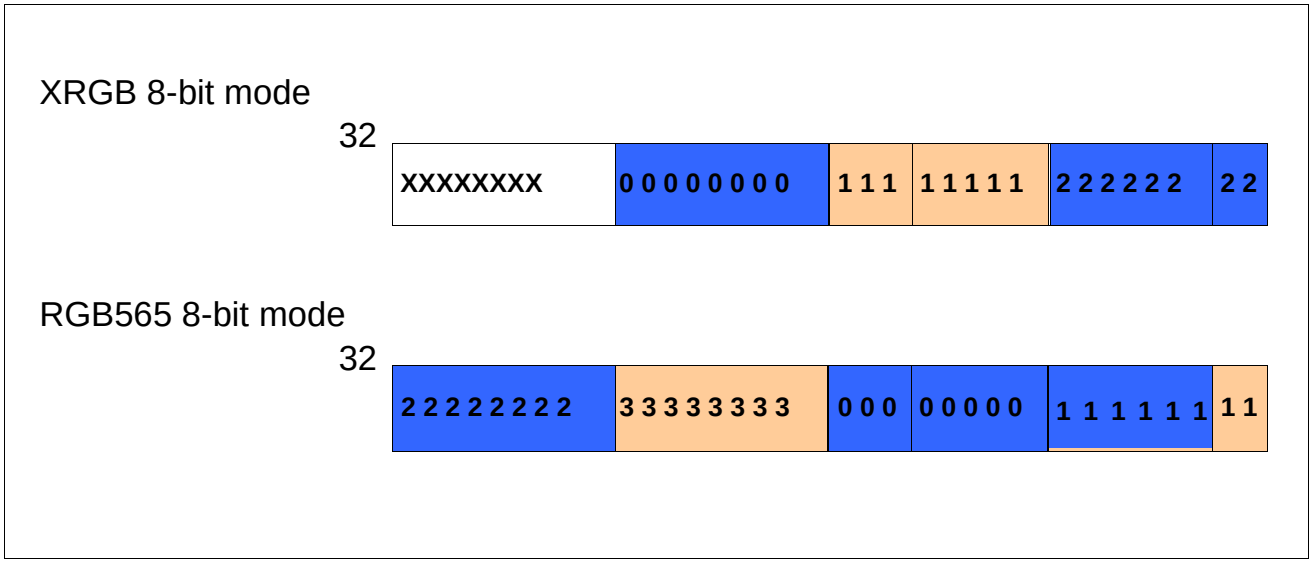

Figure 10 8-bit Interface Modes

These 8-bit modes support MIPI DBI and Nokia MeSSI standard devices.

There are also direct pass modes which take the lowest 8/9/16/18-bits of the input word and output this to the external data bus. To enable these modes the PXLDAT bit of the SMI_CS register must be cleared. In this case the FORMAT and SWAP bits are ignored.

7 Input Data Format

In order to save space in the read FIFO read data is packed into 32-bit words in designated formats depending on the interface width. These are equivalent to the output data formats to ensure consistency. For example, if the WFORMAT bit is set for an 8-bit interface, 3 read transfers will fill one 32-bit word with the top 8 bits left free as padding.

For 9 and 18-bit interfaces swapped input formatting is possible by setting the WSWAP bit for SWAP mode. These WFORMAT and WSWAP bits are only present in the SMI_DSW registers but they apply to both read and write transfer settings.

7.1 Register MAP

SMI Register Map			
Address	**Register Name**	**Description**	**Size**
SMI Register Offsets from SMI_BASE			
0x00	SMI_CS	Secondary Memory Interface Control / Status	32
0x04	SMI_L	Secondary Memory Interface Length	32
0x08	SMI_A	Secondary Memory Interface Address	10
0x0C	SMI_D	Secondary Memory Interface Data	32
0x10	SMI_DSR0	SMI Device Read Settings 0	32

0x14	SMI_DSW0	SMI Device Write Settings 0	32
0x18	SMI_DSR1	SMI Device Read Settings 1	32
0x1C	SMI_DSW1	SMI Device Write Settings 1	32
0x20	SMI_DSR2	SMI Device Read Settings 2	32
0x24	SMI_DSW2	SMI Device Write Settings 2	32
0x28	SMI_DSR3	SMI Device Read Settings 3	32
0x2C	SMI_DSW3	SMI Device Write Settings 3	32
0x30	SMI_DC	SMI DMA Control	32
0x34	SMI_DCS	SMI Direct Control / Status	4
0x38	SMI_DA	SMI Direct Address	10
0x3C	SMI_DD	SMI Direct Data	18
0x40	SMI_FD	SMI FIFO Debug	32

Table 1 SMI Register Assignment

7.2 SMI_CS - SMI Control and Status Register Definition

SMI_CS

SYNOPSIS The SMI Control and Status register is used to enable the SMI, configure transfers and monitor peripheral status.

Bit(s)	Field Name	Description	Type	Reset
31	RXF	RX FIFO is Full 0 = RX FIFO is not full. 1 = RX FIFO is full, no further external transfers can take place.	R	0
30	TXE	TX FIFO is Empty 0 = TX FIFO is not empty. 1 = TX FIFO is empty, no further external transfers can take place.	R	1
29	RXD	RX FIFO contains Data 0 = RX FIFO contains no data or the transfer direction is set to WRITE. 1 = RX FIFO contains at least 1 word of data that can be read and the transfer direction is set to READ.	R	0
28	TXD	TX FIFO can accept Data 0 = TX FIFO cannot accept new data or the transfer direction is set to READ. 1 = TX FIFO can accept new at least 1 word of data and the transfer direction is set to WRITE.	R	1
27	RXR	RX FIFO needs Reading 0 = RX FIFO is less than ¾ full or the transfer direction is set to WRITE. 1 = RX FIFO is at least ¾ full or the transfer has finished and the FIFO still needs reading. The transfer direction must be set to READ.	R	0
26	TXW	TX FIFO needs Writing 0 = TX FIFO is at least ¼ full or the transfer direction is set to READ. 1 = TX FIFO is less than ¼ full and the transfer direction is set to WRITE.	R	1

25	AFERR	An AXI FIFO Error has occurred. 0 = No FIFO error. 1 = A FIFO error has occurred – either a read of the RFIFO when empty or a write of the WFIFO when full. This is a latching error bit and it must be cleared by writing 1 to this bit.	R/W	0

24	PRDY	Force the SMI to appear not ready on the AXI bus if the appropriate FIFO Is not ready. 0 = SMI appears ready all the time and all AXI transfers to it will complete. 1 = SMI will stall the AXI bus when reading or writing data to SMI_D unless there is room in the FIFO for writes or there is data available for a read. Setting this bit may cause the AXI bus to become locked or may seriously impact system performance.	R/W	0
23-16	---	Reserved	-	-
15	EDREQ	External DREQ received – indicates the status of the external devices DREQ when in DMAP mode. 0 = No external DREQ received. 1 = External DREQ received.	R	0
14	PXLDAT	Pixel Data – enables pixel formatting modes. 0 = Pixel modes not enabled (direct modes). 1 = Pixel modes enabled. The data in the FIFO's will be appropriately packed to suit the pixel format selected.	R/W	0
13	SETERR	A Setup Error has occurred. 0 = No error writing to setup registers. 1 = Setup registers were written to when enabled. This is a latching error bit and it must be cleared by writing 1 to this bit.	R/W	0
12	PVMODE	Pixel Valve Mode 0 = Pixel Valve mode disabled. 1 = Pixel Valve mode enabled. Transmit data is taken from the pixel valve interface rather than the AXI input.	R/W	0
11	INTR	Interrupt on RX 0 = Don't generate interrupts on RXR condition. 1 = Generate interrupt while RXR = 1.	R/W	0
10	INTT	Interrupt on TX 0 = Don't generate interrupts on TXW condition. 1 = Generate interrupt while TXW = 1.	R/W	0
9	INTD	Interrupt on DONE 0 = Don't generate interrupts on DONE condition. 1 = Generate interrupt while DONE = 1.	R/W	0
8	TEEN	Tear Effect Mode Enable 0 = TE mode disabled. 1 = TE mode enabled. Programmed transfers will wait for a TE trigger before starting.	R/W	0
7-6	PAD	Padding Words – This indicates the number of FIFO words to be discarded at the start of a transfer. For write transfers this indicates the number of words that will be taken from the TX FIFO but will not be transmitted. For read transfers this indicates the number of words that will be received from the peripheral (after packing) but will not be written into the RX FIFO.	R/W	0
5	WRITE	Sets the Transfer Direction on the SMI bus. 0 = Transfers will read from external devices. 1 = Transfers will write to external devices.	R/W	0
4	CLEAR	Clear the FIFOs 0 = No effect. 1 = Writing a _1' to this bit causes the FIFOs to be reset to the empty state. This bit is auto clearing and will always be read as a zero.	W	0
3	START	Start Transfer 0 = No effect. 1 = Writing a _1' to this bit will start a transfer if one is not already taking place. This bit is auto clearing and will always be read as a zero.	W	0
2	ACTIVE	Indicates the current Transfer Status 0 = Transfer is not taking place. 1 = Transfer is taking place.	R	0

1	DONE	Indicates the current transfer is complete. This is set when the last transmit word has been written out of the SMI or the last receive word has arrived.	R/W	0
		The bit is reset by writing a 1 to this bit or setting the START bit. 0 = No meaning. 1 = The transfer has finished.		
0	ENABLE	Enable the SMI This bit is OR'd with the ENABLE bit in the SMI_DCS register. If either bit is set then the SMI is enabled. 0 = Disable the SMI. This puts the SMI in a power-saving state with minimal clocking, however the SMI control registers can still be read and written. 1 = Enable the SMI.	R/W	0

Table 2 SMI Control & Status register (SMI_CS)

7.3 SMI_L - SMI Transfer Length Register Definition

SMI_L

Synopsis The SMI Length register is used to specify the number of transfers on the SMI bus. It is specified in words, where a word can be either 8, 9, 16 or 18-bits depending upon the width setting for the external device. If this register is read during a transfer it will contain the number of words transferred so far.

Bit(s)	Field Name	Description	Type	Reset
31-0	LENGTH	Write: This sets the number of words to transfer over the external bus. The words can be either of 8,9,16 or 18 bits wide depending upon the output width that has been set in the SMI_DSx registers. Read: Contains the value written to the register unless a transfer is active, in which case it contains the number of words transferred so far.	R/W	0

Table 3 SMI Transfer Length register (SMI_L)

7.4 SMI_A - SMI Address Register Definition

SMI_A

Synopsis The SMI Address register is used to specify the address presented on the SMI bus when transfers take place.

Bit(s)	Field Name	Description	Type	Reset
31-10	---	Unused	-	-
9-8	DEVICE	Indicates which set of device settings should be used for the transfer. 00 = Device settings 1 01 = Device settings 2 10 = Device settings 3 11 = Device settings 3	R/W	0x0
7-6	---	Unused	-	-
5-0	ADDR	Address to be used for transfers and presented on the SMI Bus.	R/W	0x00

Table 4 SMI Address register (SMI_A)

7.5 SMI_D - SMI Data Register Definition

SMI_D

Synopsis The Secondary Memory Interface Data register is used to read / write data to the SMI bus. Data written here is placed in the Transmit FIFO. Data read here is taken from the Receive FIFO.

Bit(s)	Field Name	Description	Type	Reset
31-0	DATA	Reading returns data that has been read from external devices. Data written here is written out to external devices.	R/W	0

Table 5 SMI Data register (SMI_D)

7.6 SMI_DC - SMI DMA Control Register Definition

SMI_DC

Synopsis The SMI DMA Control register is used to specify the behaviour for the DMA DREQ and Panic signals on the AXI bus. The SMI can generate a TX and a RX DREQ to control an external AXI DMA. It can also generate a PANIC signal to indicate that it is running out of FIFO space.

Bit(s)	Field Name	Description	Type	Reset
31-29	---	Unused	-	-
28	DMAEN	DMA Enable – enables the generation of DREQ and Panic signals to control the AXI bus DMA transfers. 0 = No DREQ or Panic will be issued. 1 = DREQ and Panic will be generated when the FIFO levels reach the programmed levels.	-	-
27-25	---	Unused	-	-
24	DMAP	Enable external DREQ Mode. In this mode the top 2 bits of the SMI data are used as DREQ and DREQ_ACK signals and can be used to pace the flow of data on the external SMI bus. This is separate to the normal AXI DMA behaviour. This must be used in conjunction with the RDREQ or WRREQ bits in the device settings registers. 0 = Top two data pins used as SMI data. 1 = Top two data pins used for external DMA requests.	-	-
23-18	PANICR	RX Panic Threshold level. A RX Panic will be generated when the RX FIFO exceeds this threshold level. This will instruct the AXI RX DMA to increase the priority of its bus requests.	R/W	0x30
17-12	PANICW	TX Panic threshold level. A TX Panic will be generated when the TX FIFO drops below this threshold level. This will instruct the AXI TX DMA to increase the priority of its bus requests.	R/W	0x10
11-6	REQR	RX DREQ Threshold Level. A RX DREQ will be generated when the RX FIFO exceeds this threshold level. This will instruct an external AXI RX DMA to read the RX FIFO. If the DMA is set to perform burst reads, the threshold must ensure that there is sufficient data in the FIFO to satisfy the burst.	R/W	0x20
5-0	REQW	TX DREQ Threshold Level. A TX DREQ will be generated when the TX FIFO drops below this threshold level. This will instruct an external AXI TX DMA to write more data to the TX FIFO.	R/W	0x20

Table 6 SMI DMA Control (SMI_DC)

7.7 SMI_DSRx - SMI Device Read Setting Register Definitions

SMI_DSR0, SMI_DSR1, SMI_DSR2, SMI_DSR3

Synopsis The SMI Device Read Setting registers are used to configure the timings and bus configurations used for reads of an external device. There are 3 such registers, allowing 3 different configuration settings to be specified.

When a Read is performed, the read address used specifies which of these setting registers is applied.

Bit(s)	Field Name	Description	Type	Reset
31-30	RWIDTH	WIDTH – Read Transfer Width 00 = 8bit 01 = 16bit 10 = 18bit 11 = 9bit	R/W	0
29-24	RSETUP	Duration between chip select being asserted and read strobe going active. Specified in SMI bus clock cycles, min 1 cycle, max 64 cycles.	R/W	0x01
23	MODE68	0 = the external bus will operate in a System-80 compliant way. 1 = the external bus will operate in a System-68 compliant way.	R/W	0
22	FSETUP	0 = always apply the setup time. 1 = a setup time is only applied to the first transfer after de-assertion of chip select.	R/W	0
21-16	RHOLD	Duration between read strobe going inactive and chip select de-asserting. Specified in SMI bus clock cycles, min 1 cycle, max 64 cycles.	R/W	0x01
15	RPACEALL	Selects if RPACE applies to all buss accesses 0 = RPACE only applies to accesses through the same device settings. 1 = RPACE applies to the next access regardless of the device settings used.	R/W	0
14-8	RPACE	Duration between chip select de-asserting and any other transfer being allowed on the bus. Specified in SMI bus clock cycles, min 1 cycles, max 128 cycles.	R/W	0
7	RDREQ	External Read DREQ The top 2 SMI data bits can be used as DREQ (SD[16]) and DREQ_ACK (SD[17]). These can be used used to pace the reads. This must be used in conjunction with the DMAP bit in SMI_CS. 0 = Don‘t use external DMA request. Reads always happen. 1 = Use external DMA request to pace device reads. A read will only happen for each DREQ, DREQ_ACK cycle.	R/W	0
6-0	RSTROBE	Duration that the read strobe should be active. Specified in SMI bus clock cycles, min 1 cycle, max 128 cycles.	R/W	0x0c

Table 7 SMI Device Read Settings (SMI_DSRx)

7.8 SMI_DSWx - SMI Device Write Setting Register Definitions

SMI_DSW0, SMI_DSW1, SMI_DSW2, SMI_DSW3

Synopsis The SMI Device Write Setting registers are used to configure the timings and bus configurations used for writes to an external device. There are 3 such registers, allowing 3 different configuration settings to be specified.

When a Write is performed, the write address used specifies which of these setting registers is applied.

Bit(s)	Field Name	Description	Type	Reset
31-30	WWIDTH	WIDTH – Write Transfer Width 00 = 8bit 01 = 16bit 10 = 18bit 11 = 9bit	R/W	0
29-24	WSETUP	Duration between chip select being asserted and write strobe going active. Specified in SMI bus clock cycles, min 1 cycle, max 64 cycles.	R/W	0x01
23	WFORMAT	FORMAT – Input Pixel Format 0 = 16-bit RGB565 1 = 32-bit RGBX8888	R/W	0
22	WSWAP	SWAP – Swap Modes Enabled 0 = Pixel data bits not swapped 1 = Pixel data bits swapped	R/W	0

21-16	WHOLD	Duration between write strobe going inactive and chip select de-asserting. Specified in SMI bus clock cycles, min 1 cycle, max 64 cycles.	R/W	0x01
15	WPACEALL	Selects if WPACE applies to all bus accesses 0 = WPACE only applies to accesses through the same device settings. 1 = WPACE applies to the next access regardless of the device settings used.	R/W	0
14-8	WPACE	Duration between chip select de-asserting and any other transfer being allowed on the bus. Specified in SMI bus clock cycles, min 1 cycles, max 128 cycles.	R/W	0
7	WDREQ	External Write DREQ The top 2 SMI data bits can be used as DREQ (SD[16]) and DREQ_ACK (SD[17]). These can be used used to pace the writes. This must be used in conjunction with the DMAP bit in SMI_CS. 0 = Don‘t use external DMA request. Writes always happen. 1 = Use external DMA request to pace device Writes. A write will only happen for each DREQ, DREQ_ACK cycle.	R/W	0
6-0	WSTROBE	Duration that the write strobe should be active. Specified in SMI bus clock cycles, min 1 cycle, max 128 cycles.	R/W	0x0c

Table 8 SMI Device Write Settings (SMI_DSWx)

7.9 SMI_DCS - SMI Direct Control and Status Register Definition

SMI_DCS

Synopsis The SMI Direct Control / Status register is used to control direct mode transfers. A direct write will be fitted in even if a normal data transfer is taking place.

Bit(s)	Field Name	Description	Type	Reset
31-4	---	Unused	-	-
3	WRITE	WRITE – Transfer Direction 0 = Transfers will read from external devices. 1 = Transfers will write to external devices.	R/W	0
2	DONE	DONE – Direct Transfer Complete 0 = No meaning. 1 = A transfer has finished. Writing a ‗1‘ to this bit will clear this flag	R/W	0
1	START	START – Start Transfer 0 = No effect. 1 = Writing a ‗1‘ to this bit will start a transfer if one is not already taking place.	W	0
0	ENABLE	Enable the SMI This bit is OR‘d with the ENABLE bit in the SMI_CS register. If either bit is set then the SMI is enabled. 0 = Disable the SMI. This puts the SMI in a power-saving state with minimal clocking, however the SMI control registers can still be read and written. 1 = Enable the SMI.	R/W	0

Table 9 SMI Direct Control / Status (SMI_DCS)

7.10 SMI_DA - SMI Direct Mode Address Register Definition

SMI_DA

Synopsis The SMI Direct Mode Address register is used to specify the address presented on the external pins when a Direct Mode transfer takes place. This register should be written with the address and device settings before the direct mode transfer is started.

Bit(s)	Field Name	Description	Type	Reset

31-10	---	Unused	-	-
9-8	DEVICE	Indicates which set of device settings should be used for the transfer. 00 = Device settings 1 01 = Device settings 2 10 = Device settings 3 11 = Device settings 3	R/W	0x0
7-6	---	Unused	-	-
5-0	ADDR	Address to be used for direct mode transfers	R/W	0x00

Table 10 SMI Direct Mode Address (SMI_DA)

7.11 SMI_DD - SMI Direct Mode Data Register Definition

SMI_DD

Synopsis The SMI Direct Mode Data register is used to read / write the data for a Direct Mode transfer. If a Direct Mode write is performed, the write data must be written here before the Direct mode write is started. If a Direct mode read is performed, the data read from the external device will be available here once the read has completed (as indicated by the DONE bit in the SMI_DCS reg)

Bit(s)	Field Name	Description	Type	Reset
31-18	---	Unused	-	-
17-0	DATA	Reading gives data that has been read from external devices. Writing is used to provide the data that should be written to external devices.	R/W	0

Table 11 SMI Direct Mode Data (SMI_DD)

7.12 SMI_FD - SMI FIFO Debug Register Definition

SMI_FD

Synopsis The Secondary Memory Interface FIFO Debug register is used to indicate FIFO fill levels for debug purposes.

Bit(s)	Field Name	Description	Type	Reset
31-14	---	Unused	-	-
13-8	FLVL	FIFO High Count Level This indicates the maximum FCNT level reached during the last set of transfers. The level is reset at the start of each new transfer. The	R/W	0
7-6	---	Unused	-	-
5-0	FCNT	FIFO Count This indicates the FIFO fill level of the currently active FIFO. If doing a write transfer then it will indicate the TX FIFO, else the RX FIFO.	R/W	0

Table 12 SMI FIFO Debug (SMI_FD)