PHYC30170 Physics with Astronomy and Space Science Lab 1; Electronics

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I. INTRODUCTION

This report features 8 exercises of the 31 included in the 3rd Year Electronics Laboratory manual [2]. The exercises make use of a combination of simulations carried out on a computer and actual physically creating the circuits to measure them. Many areas of electronics were covered including RC circuits, diodes, transistors, op-amps, and DACs.

II. EXERCISE 5: RC CIRCUITS

A. Theory

Exercise 5 involves the construction and measurement of a RC circuit. An RC circuit is one which consists of a resistor and capacitor. The capacitor stores charge and the resistor controls the rate at which it discharges [1]. This time dependent discharge is an exponential decay given by the following equation:

$$V_{\text{out}} = V_{\text{in}} \exp\left(\frac{-t}{RC}\right) \tag{1}$$

where V_{in} is the input voltage and V_{out} is the voltage output measured by the voltmeter in figure 1. R and C are simply the resistance and capacitance respectively. The factor $1/RC$ is defined as the decay constant which solely determines the rate of decay [2].

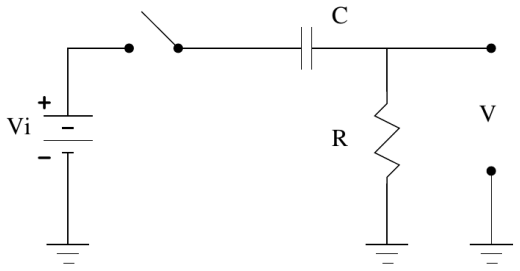

FIG. 1: A sample RC circuit as described in the lab manual [2].

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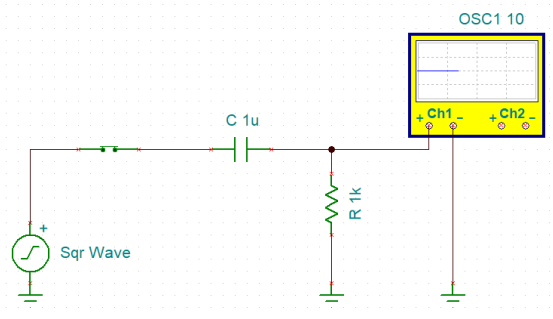

FIG. 2: The circuit construction created in TINA for simulation.

B. Methodology

The RC circuit depicted in figure 1 was constructed in DesignSoft's TINA [3], a circuit simulator. This construction is shown in figure 2. A virtual oscilloscope was used in place of a voltmeter to measure the signal as a function of time. The component values of the capacitor and resistor were chosen as directed by the exercise and a square wave of frequency 20 Hz with peak to peak amplitude of 5 V was used as the input. The circuit was simulated and the signal was recorded. The circuit was then constructed physically on a breadboard and the same measurement was made using an oscilloscope. The signals of the simulation, the measurement, and the analytical solution were then compared and the decay constants determined.

C. Results & Analysis

The measured data from the breadboard were plotted in figure 3 along with the analytical solution calculated using equation 1. The decay constant of the analytical solution was calculated from the values of the resistor and the capacitor however, the decay constants for the measured data and simulation data were determined using least squares fitting of the signal. The decay constants for each method were recorded in table I along with their uncertainty which was determined by the square root of the diagonal elements of the covariance matrix.

We notice that the amplitude of the simulation data is approximately twice that in the measured data. This is due to an inconsistency in the definition of amplitude, be it peak to peak amplitude or average to peak. We can still see clearly that the shape of the data matches what is expected and therefore dividing by two will yield

Method	Decay Constant (s^{-1})	Uncertainty
Analytical	1000	N/A
Simulation	1012.884	$\mathcal{O}10^{-6}$
Measured	895.937	$\mathcal{O}10^{-6}$

TABLE I: Decay constants for exercise 5. The uncertainties were determined by the square root of the diagonal elements of the covariance matrix for least squares fitting

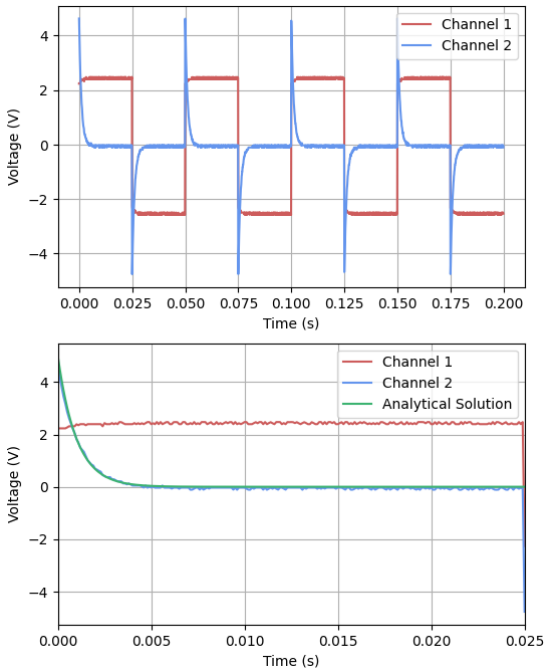

FIG. 3: Input and output signals from the RC circuit in exercise 5. Channel 1 is the square wave driving the circuit whereas channel 2 is the output. The exponential decay response is clearly shown in the lower graph ($\frac{1}{2}$ period) in comparison to the analytical solution.

the result under peak to peak amplitude. This is done explicitly in this exercise as shown in figures 4 and 5 however, for all further exercises where this applies - unless otherwise specified - this can be assumed to have been done.

For consistency, in this report we shall use the term amplitude to refer to peak to peak amplitude as this is the definition used by the oscilloscope which was used to generate and measure signals for the majority of these exercises.

III. EXERCISE 7: RC CIRCUITS AND FREQUENCY FILTERS

A. Theory

Exercise 7 demonstrates how the same RC circuit as in exercise 5 can be used to make a high pass filter [2]. A high pass filter is a signal filter which allows higher frequencies to pass through unaffected but attenuates signals beyond a cut-off frequency. The combination of a resistor with a capacitor makes it possible to have voltage dividers dependent on frequency [4]. This frequency dependence arises from the impedance of the capacitor.

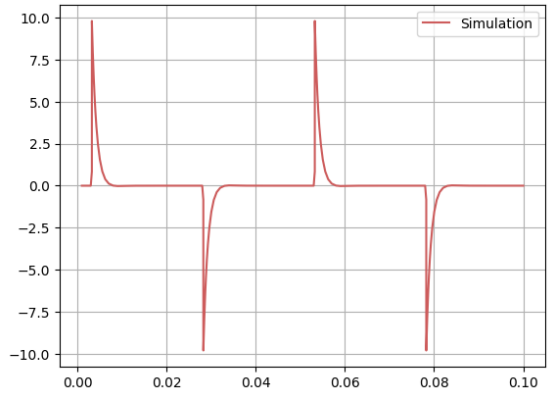

FIG. 4: Simulation data generated by TINA, is exponential decay the same shape as the analytical and the measured.

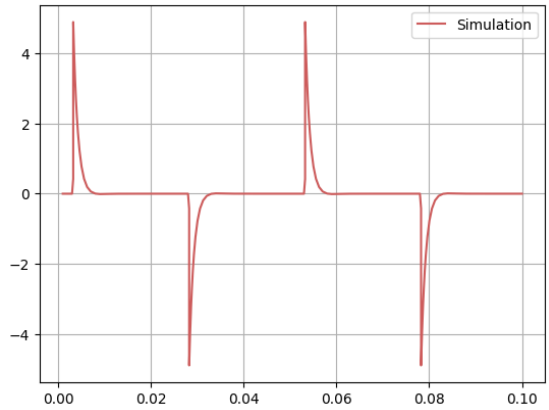

FIG. 5: The simulated data using peak to peak amplitude.

$$Z_C = -\frac{j}{\omega C} \tag{2}$$

where j is the imaginary number $j = \sqrt{-1}$, C is the capacitance, and ω is the angular frequency. For the circuit in figure 1, by Ohm's law we have a current:

$$I = \frac{V_{\text{in}}}{Z_{\text{total}}} = \frac{V_{\text{in}}}{R - Z_C} \tag{3}$$

and hence we can calculate the voltage across the resistor, V_{out}, by substitution and rationalisation of the denominator:

$$V_{\text{out}} = IR = V_{\text{in}} \frac{[R + (\frac{j}{\omega C})]R}{R^2 + (\frac{1}{\omega^2 C^2})} \tag{4}$$

with a magnitude of:

$$V_{\text{out}} = V_{\text{in}} \frac{R}{\left[R^2 + \left(\frac{1}{\omega^2 C^2}\right)\right]^{\frac{1}{2}}} = V_{\text{in}} \frac{\omega RC}{\left[1 + (\omega RC)^2\right]^{\frac{1}{2}}} \tag{5}$$

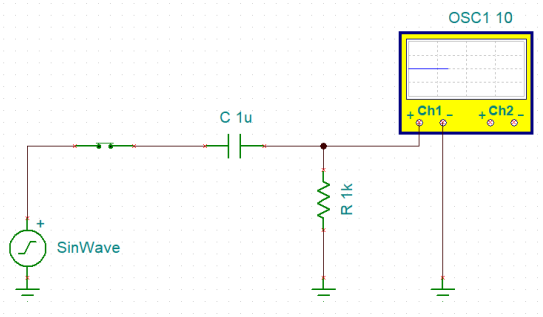

FIG. 6: The circuit diagram created in TINA to measure the amplitude and phase response of an RC circuit.

this is derived in full by Horowitz and Hill [4] where they also determine the phase analyticity to be:

$$\phi = \arctan\left(\frac{-1}{\omega RC}\right) \tag{6}$$

which derives from the total impedance.

B. Methodology

The aim of this exercise was to simulate and measure the amplitude and phase response of the RC circuit from exercise 5 when driven by a sin wave. The circuit was designed and created in TINA as shown in figure 6. Note that this circuit is predominantly the same as in figure 2 in exercise 5, with the only difference being in the wave generated by the voltage generator. The circuit was simulated and the amplitude and phase response were recorded. The circuit was then constructed physically and the amplitude and phase response were measured using an oscilloscope for frequencies of 1 Hz, 10 Hz, 100 Hz, 1 kHz, 10 kHz, 100 kHz, and 1 MHz.

C. Results & Analysis

The amplitude and phase data simulated by TINA was plotted in figure 7 along with the data measured from the physical circuit. It is clear that the data matches within the bounds of uncertainty. The uncertainty for these measurements were made either from the measuring limitations of the oscilloscope (i.e. the amount of decimals displayed) or where the measurement was not constant - such as in cases of low frequency ($< 10\,\text{Hz}$) - the average and standard deviation of 10 measurements was taken.

These simulation curves displayed, and hence the data, match that described by equations 5 and 6. We see that the circuit behaves at a high pass filter with negative gain for frequencies lower than 1 kHz. The output is out of phase for these lower frequencies and results in destructive interference.

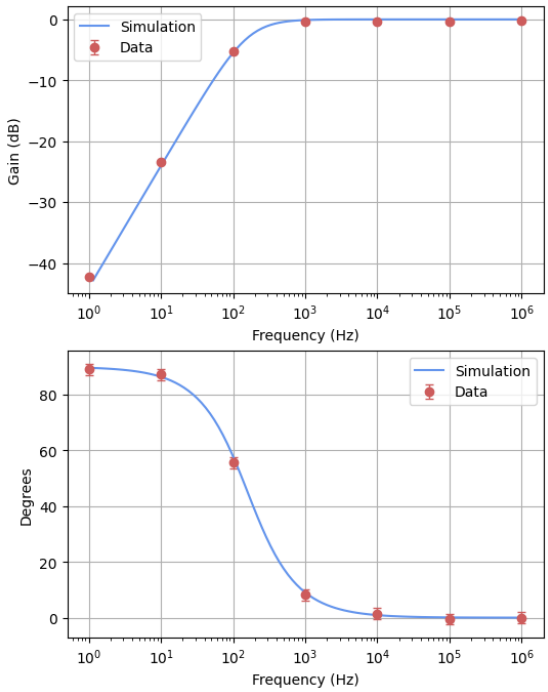

FIG. 7: Bode plot of exercise 7. The circuit is a high pass filter with $R = 1\text{k}\Omega$, $C = 1\mu\text{F}$. Note that errorbars are included on both graphs however in some cases are to small to see.

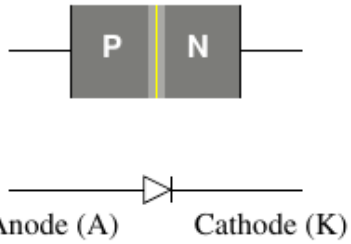

FIG. 8: Above: the PN junction of the diode. Below: the schematic symbol of the diode [2].

IV. EXERCISE 12: DIODES

A. Theory

The aim of exercise 12 is determine the I-V curve for a diode in forward and reverse bias. A diode is a PN junction which is either in forward bias or reverse bias depending on the direction of current flow across it, see figure 8 [2]. When forward biased the voltage source is connected such that the anode is positive compared to the cathode, current will flow. When reverse biased, the voltage source is opposite in polarity with respect to forward bias. The cathode has a positive voltage compared to the anode. Due to the nature of PN junctions no current will flow up to a breakdown voltage [2].

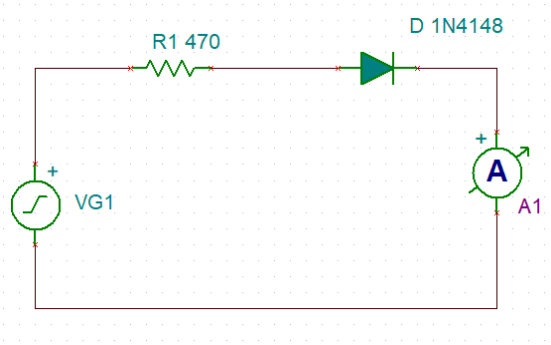

FIG. 9: Circuit diagram create in TINA for exercise 12. Note that this doesn't include the capacitor added in the second half of the exercise.

B. Methodology

The aim of this exercise was to measure the I-V curve for the 1N1418 diode. A circuit was designed in TINA to do this using a resistor to limit the current flow and a voltage source to vary to vary the input voltage, see figure 9. A multimeter was used to measure the current. A 470 Ω resistor was chosen to limit the current flow. The voltage was varied between −10 V and 10 V and recorded and plotted in figure 10.

The circuit was then driven with a AC sin wave with frequency 500 Hz and peak-to-peak amplitude of 3 V. The voltage drop across the resistor was measured by subtracting oscilloscope measurements of the voltage before and after the resistor. This oscilloscope data was recorded and plotted in figure 11. A 10 μF capacitor was added in parallel across the resistor and the measurement was repeated. This was recorded and plotted in figure 12.

C. Results & Analysis

From figure 10 we can see the linear proportionality of current to voltage as depicted by Ohm's law when in forward bias. In reverse bias we see no current as the breakdown voltage of the diode was much higher than the maximum output of the voltage generator and hence any leak-through current was too small to be measured by the multimeter. According to a manufacturer data-sheet [5], the 1N4148 diode needs a reverse bias voltage of $\approx$ 75 V before it leaks a current on the order of micro-amps.

When driven with the sin wave, we see no voltage across the resistor when the AC signal is in reverse bias, and a peak when the signal is in forward bias. This is again expected and due to the diode stopping current flow in reverse bias. When the capacitor is added, we see a similar effect but with some distinct differences. The capacitor in parallel causes less current to flow across the resistor making for a smaller peak voltage drop across it,

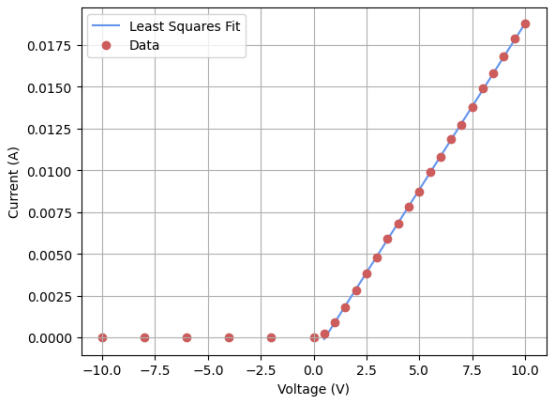

FIG. 10: I-V curve for the circuit in forward and reverse bias. As the breakdown voltage of the diode was much higher than the maximum output of the voltage generator and hence any leak-through current was too small to be measured by the multimeter.

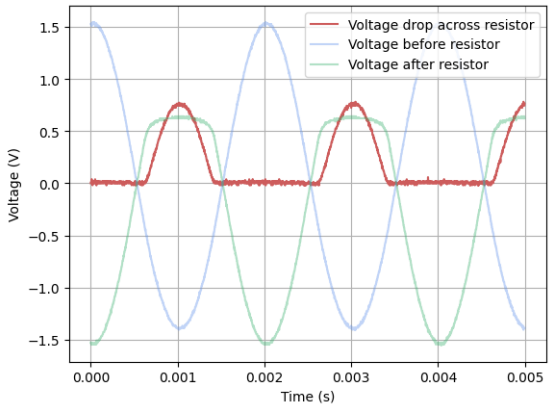

FIG. 11: Voltage drop over the resistor when the circuit from exercise 12 was driven by a sin wave.

this can be visually seen. We also see a delay in the peak voltage drop across the resistor, and a sustained voltage drop even during reverse bias. This is due to the nature of the capacitor taking time to charge and discharge. We see the peak voltage drop lag behind as the capacitor charges and we see a decaying voltage drop in reverse bias as the capacitor discharges.

V. EXERCISE 19: TRANSISTORS AS A CURRENT AMPLIFIER

A. Theory

A transistor is a 3 terminal semiconductor device comprised of the joining of two PN junctions. They can be arranged in two layouts, npn or pnp, see figure 13 [4]. In this exercise, a transistor is used as an amplifier. A small current I_B must flow into the base to allow current I_C to flow through the detector. The current gain - the ratio between these two currents - is determined by the

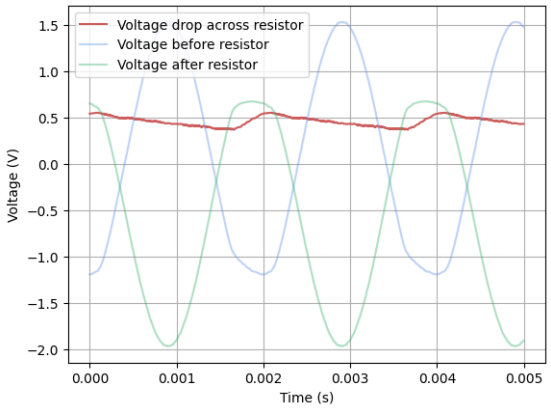

FIG. 12: Voltage drop over the resistor with a capacitor in parallel, when the circuit from exercise 12 was driven by a sin wave.

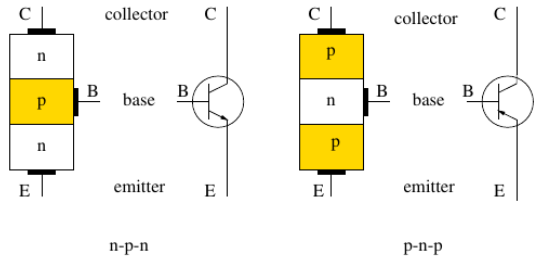

FIG. 13: A diagram of the two layouts of transistors [2].

following equation [4].

$$\beta = \frac{I_C}{I_B} \tag{7}$$

B. Methodology

This exercise aims to simulate a current amplifying circuit and calculate the current gain for a 2N4400 transistor. The circuit was designed and simulated in TINA, see figure 14. The resistor values were chosen as given by the lab manual [2], with their purpose being to reduce the current flow into the base of the transistor. The TINA software's DC analysis was used to measure the current from the ammeters. These currents were recorded and then equation 7 was used to calculate the current gain based on the current running through the collector and the base.

C. Results & Analysis

Equation 7 was used to calculate the current gain of the circuit using the data from figure 14. With a base current of 42.75 μA and a collector current of 3.69 mA, the current gain, β, was calculated to be $\beta = 86.32$.

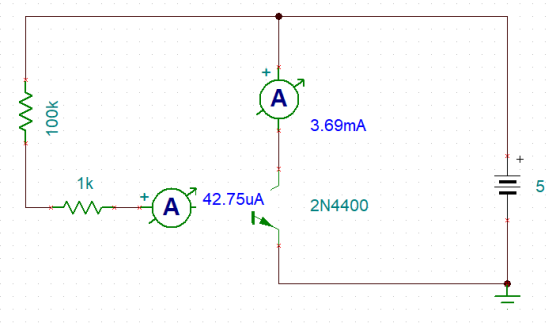

FIG. 14: The circuit setup in TINA to demonstrate current amplification with transistors.

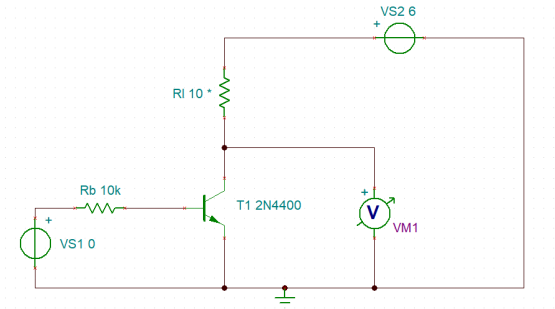

FIG. 15: The circuit diagram for exercise 20, created in TINA. The load resistor, *Rl*, was setup so that it could be varied.

VI. EXERCISE 20: TRANSISTORS AS A SWITCH

A. Theory

Another applications of transistors is as a switch. Make for good switches as they are small, cheap, reliable, and can switch rapidly [2]. Similarly to how the current amplifier required a current (and hence voltage) through the base to allow current to flow through the collector, if we think of the path from the collector to the emitter as the primary path, then the voltage at the base controls if the current can flow through this path. The "switch" is on if there is sufficient voltage at the base (approx. 0.7 V), and off where there isn't.

The aim this exercise is the vary the load resistance and look at the effect it has on the switching action. The load resistor is placed in series with the collector of the transistor. The output voltage from a sample circuit (figure 15) is expected to look as shown in figure 16. This graph is split up into three distinct sections. In section A the transistor switch is off, there is no current flowing from the collector and hence the output is 6 V. In section B, the transistor switch is partially on, as the current increases, the voltage across the load resistor increases and the output drops. In section C, the transistor is fully on and said to be saturated [2].

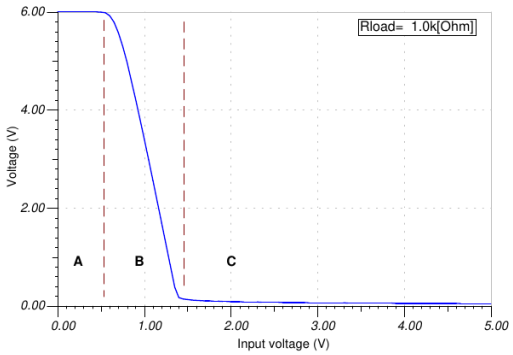

FIG. 16: A diagram of the voltage response with a load resistor of resistance 1 kΩ [2].

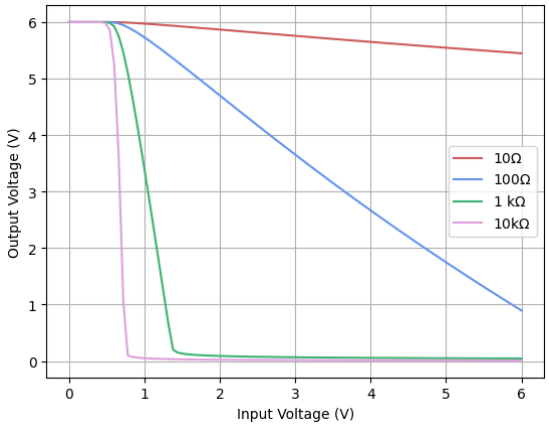

FIG. 17: The results from exercise 20. We see that the lower load resistances never reach saturation.

B. Methodology

The circuit was constructed in TINA as directed by the exercise [2], see figure 15. The load resistor was set up as a control target in TINA to vary its resistance during analysis. The voltage response for load resistances of 10 Ω, 100 Ω, 1 kΩ, and 10 kΩ were simulated and recorded in figure 17.

C. Results & Analysis

Each voltage response simulation for each load resistor was recorded and plotted in figure 17. We see that the results match that of what is expected in figure 16. We see that the slope of the B section of the voltage response depends on the load resistance with a higher resistance yielding a sharper slope. The lower load resistances of 10 Ω and 100 Ω never reach saturation for an input voltage less than the voltage before the load resistor.

VII. EXERCISE 21: LDR CONTROLLED SWITCH

A. Theory

In this exercise, an LDR is used in a voltage divider to control the voltage at the base of the transistor. The aim was to create an LED alarm which would light up if in darkness but be off in brightness. The LDR changes resistance based on the level of light with its highest resistance in darkness. This will change the voltage at the base of the transistor as determined by the voltage divider equation [6]:

$$V_{\text{out}} = V_{\text{in}} \frac{R_2}{R_1 + R_2} \tag{8}$$

where V_{out} is the potential before the pair of resistors R_1 and R_2, V_{in} is the potential between the resistors.

B. Methodology

The circuit was first designed in TINA as shown in figure 18. Here the resistors labelled R and LDR make the voltage divider. Note that the LDR here is represented as a resistor for simplicity of simulation. With reference to the voltage divider, equation 8, R_1 is the resistor labelled R, and R_2 is the lDR. The component values for this circuit were determined analytically. First the circuit was split into two loops: one containing the battery, LED, load resistor, and the collector and emitter of the transistor. The other containing the battery, R_1 and the LDR.

The first loop was considered such that the current flowing through was sufficient to light the LED. The load resistance was chosen to set this current, based on the voltage after the LED, calculated using the reverse-bias voltage of the LED. The manual recommends a current of 5 mA and hence using Ohm's law, the resistor was determined to ideally be 640 Ω. As the resistors available to use were a limited selection, a 680 Ω resistor was used instead. The second loop was considered to have greater than 0.7 V at the base of the transistor when the LDR had high resistance and less than 0.7 V when the LDR had low resistance. The LDR was measured in complete darkness and in the light of the room to find its resistance at these levels of brightness. The voltage divider equation was then used to determine that $R_1 = 10\,\Omega$ would provide sufficient voltage at the base. A small resistor R_b at the base terminal of the transistor was used to limit the current through the transistor. A value of 1 Ω was chosen. The circuit was then simulated to check if the values chosen were correct before it was constructed. The circuit was constructed and it was determined visually if the circuit worked as expected.

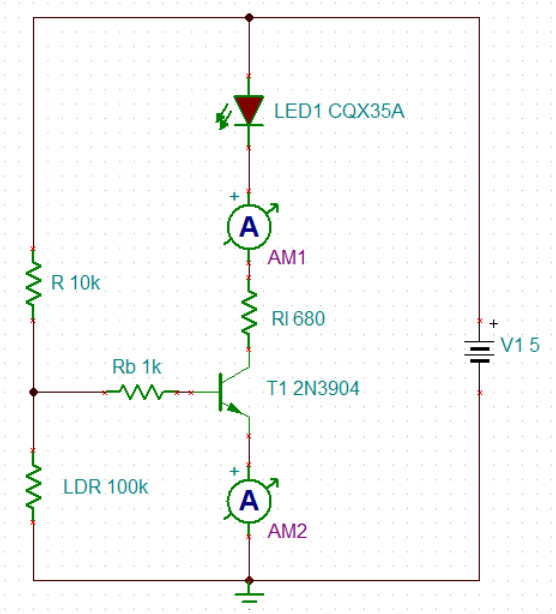

FIG. 18: Circuit diagram for exercise 21 as designed in TINA. Here the LDR is represented as a 100k resistor to emulate it being in darkness.

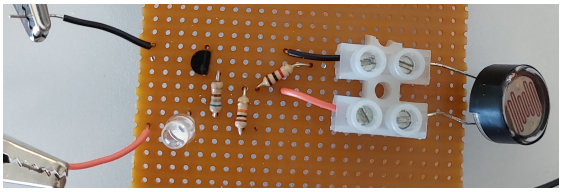

FIG. 19: A picture of the circuit from exercise 21. The circuit is powered but the LED is off as the LDR is receiving light.

C. Results & Analysis

The LDR was measured to have a $\approx 1\,\mathrm{k\Omega}$ resistance in the light of the room and $\approx 100\,\mathrm{k\Omega}$ in darkness. The circuit was constructed and behaved as expected. In figure 19, we see the circuit in the light of the room, the LED is off. In figure 20, we see the circuit with the LDR covered, the LED is on and hence the circuit works as expected.

The average yearly cost of this circuit was calculated. The power requirement of the circuit was calculated to be 2.25 mW when the LED was off, and 25.75 mW when the LED was on. Assuming an average of 12 hours of brightness and 12 hours of darkness in each day and a unit cost (cost per kWh) to be 0.18 euro, the yearly cost of the circuit was determined to be 2.21 cent. See appendix 1 for the full calculation.

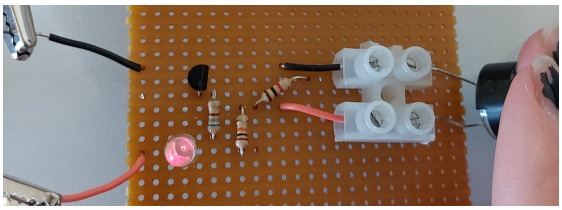

FIG. 20: A picture of the circuit from exercise 21. The circuit is powered and the LED is on as the LDR is covered and not receiving light.

VIII. EXERCISE 25: NON-INVERTING AMPLIFIER

A. Theory

An Op-Amp (Operational Amplifier) is a integrated circuit device which can make it easier to construct amplifiers or other systems in circuits [2]. An Op-Amp has two input terminals and acts as a differential amplifier, amplifying the difference between the inputs by a constant gain.

Negative feedback is when a portion of amplified output signal is fed back into the inverting input [4]. An Op-Amp with negative feedback can be described by two rules [2]: 1. The output tries to to make the voltage difference between the inputs zero. 2. The inputs draw no current. Negative feedback can be used to allow the gain of the amplifier to be controlled by the feedback network [2]. The gain of the circuit is the ratio between the output and input signals. It can be calculated in decibels by the following relation [7]:

$$L_V = 20\log_{10}\left(\frac{V}{V_0}\right)\ \mathrm{dB} \tag{9}$$

where V is the output voltage and V_0 is the input voltage. The ratio of the voltages can also be determined by the feedback network resistors, as derived in section 5.5 of the manual [2]:

$$\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = 1 + \frac{R_f}{R_i} \tag{10}$$

where R_f and R_i are the resistors in the feedback loop labelled in figure 21.

B. Methodology

A simple amplifying Op-Amp circuit was constructed following the diagram from the manual [2], see figure 21. Components were chosen such to obtain a gain of 20 dB. Using equation 9 a voltage ratio of $\frac{V}{V_0} = 10 = 1 + \frac{R_f}{R_i}$ was determined and subsequently suitable resistors could be chosen to satisfy equation 10. As the ratio of $\frac{R_f}{R_i} = 9$ is impractical, a ratio of $\frac{R_f}{R_i} = 10$ was used to match

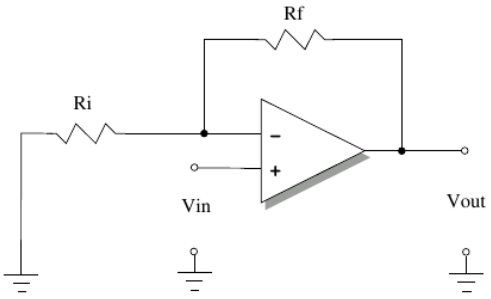

FIG. 21: The circuit diagram provided by the manual for exercise 25 [2].

Frequency (Hz)	Output (V)
10	5.43
100	5.43
1000	5.43
10000	5.41
12000	3.10
15000	2.37
20000	1.56
25000	1.01
30000	0.680

TABLE II: The data measured using the oscilloscope for exercise 25.

the components available. Resistors $R_f = 47\,\mathrm{k\Omega}$ and $R_i = 4.7\,\mathrm{k\Omega}$ were used. The circuit was driven by a 1 kHz sine wave which was recorded using an oscilloscope along with the output. A $1\,\mu$F capacitor was then inserted across R_f and the measurement was repeated.

C. Results & Analysis

The results measured from the oscilloscope were recorded in table II and III and the gain was plotted against frequency in figures 22 and 23 for the circuit without and with the capacitor respectively. This calculation was done using equation 9.

For the circuit without the capacitor we see a constant gain up to a specific frequency where the gain attenuates, this frequency was 10^4 Hz. Note although the exercise asked for a gain of 20 dB, the gain here is higher. This is due to the altering of the ratio as mentioned in the theory section to accommodate for the components available to use.

For the circuit with the capacitor we see the same shape but with a reduced bandwidth. This is because of the inverse frequency dependence of the impedance of a capacitor as described by equation 2. As the frequency increases, the voltage at the inverting input approaches that of the non-inverting input and the gain hence goes to zero.

Frequency (Hz)	Output (V)
10	1.361
12	1.36
14	1.32
16	1.27
18	1.21
20	1.11
25	0.9
30	0.8
40	0.7
50	0.63
70	0.57
100	0.527
200	0.52
500	0.51
1000	0.5
5000	0.5
10000	0.5
25000	0.5
43000	0.5

TABLE III: The data measured using the oscilloscope for exercise 25 with the inclusion of the $1\,\mu$F capacitor.

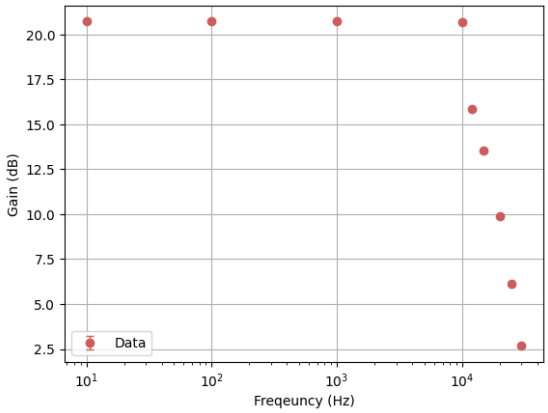

FIG. 22: Data from the measurements of exercise 25. We see a constant gain until the attenuation frequency.

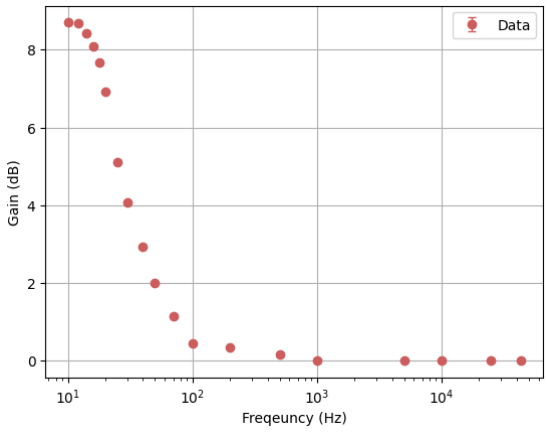

FIG. 23: Data from the measurements of exercise 25 with the insertion of the capacitor. We see a smaller bandwidth.

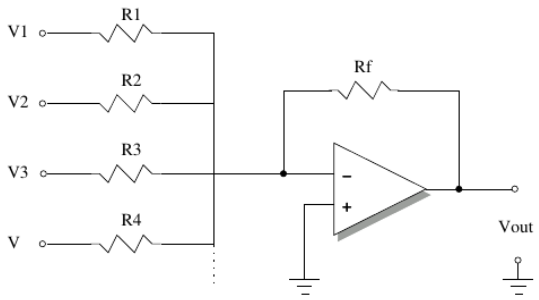

FIG. 24: A sample summing amplifier use to make DAC circuits [2].

IX. EXERCISE 27: DIGITAL-TO-ANALOGUE CONVERTER

A. Theory

A Digital-to-Analogue Converter, or DAC, is a circuit which takes a digital signal such as a binary number and converts it to an analogue voltage. In a 4-bit DAC, a four digit binary number is used to represent a signal (i.e. 1011). The DAC circuit will then output a voltage corresponding to the input signal. A common DAC circuit uses a summing amplifier to sum the currents from input branches corresponding to the signal, see figure 24. The output voltage is a combination of each of the input voltages weighted by their corresponding resistor. The output voltage is given by the following equation [2]:

$$V_{\text{out}} = -R_f \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \cdots + \frac{V_N}{R_N} \right) \qquad (11)$$

B. Methodology

A DAC circuit was constructed in TINA following the sample summing amplifier in figure 24. A 4-bit signal was used as the input with a digital voltage high of 5 V and a low of 0 V. Switches were used to manually select the input signal. From the binary number 0000 to 1111 there are 16 numbers inclusive. Each of these was mapped to a voltage with $0000 \rightarrow 0\,\text{V}$ and $1111 \rightarrow -3\,\text{V}$ and the rest were spaced evenly between. Equation 11 was then used to determine the input resistance needed to achieve these results. Using the input signals which isolated one resistor (i.e. 0001, 0010, 0100, and 1000), a ratio between each input resistor and R_f could be determined. R_f was then arbitrarily picked and the input resistors were calculated based on these ratios.

C. Results & Analysis

The circuit diagram as constructed in TINA is shown in figure 25 with an input of 0000, and in figure 26 with an input of 1111. It can clearly be seen that resistances chosen map the DAC accordingly. Note that an ideal Op-Amp was used in this instance.

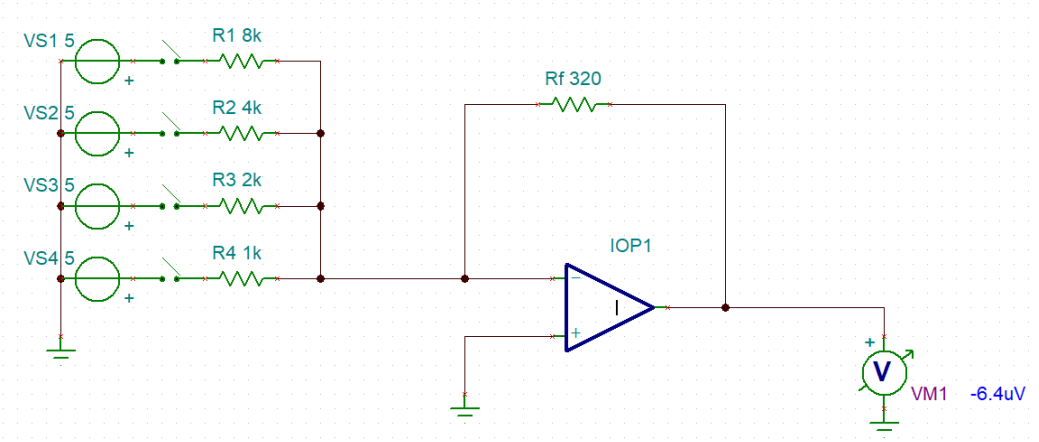
VS1 5
VS2 5
VS3 5
VS4 5
R1 8k
R2 4k
R3 2k
R4 1k
Rf 320
IOP1
V
VM1
-6.4uV

FIG. 25

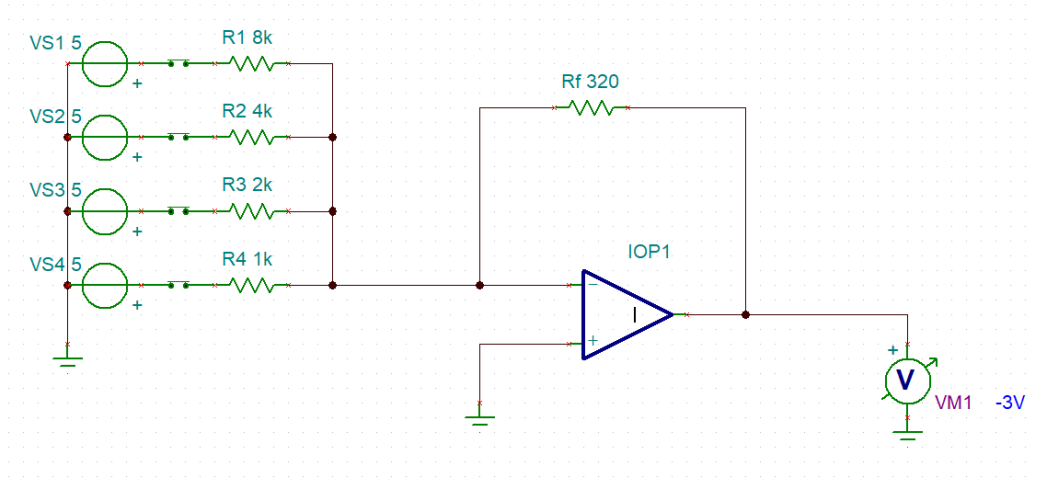
VS1 5
VS2 5
VS3 5
VS4 5
R1 8k
R2 4k
R3 2k
R4 1k
Rf 320
IOP1
V
VM1
-3V

FIG. 26

[1] J. Pumplin, RC Circuits, https://web.pa.msu.edu/courses/2000fall/phy232/lectures/rccircuits/rc.html, accessed on 14/03/23.
[2] J. Quinn, *3rd Year Electronics Laboratory*, Department of Experimental Physics National University of Ireland, Dublin.
[3] TINA Circuit Simulator, https://www.tina.com/, accessed on 15/03/23.
[4] P. Horowitz and W. Hill, *The art of electronics*, 2nd ed. (Cambridge University Press, Cambridge, 1989).
[5] *1N/FDLL 914/A/B / 916/A/B / 4148 / 4448 Small Signal Diode*, Fairchild Semiconductor Corporation, accessed on 23/03/23.
[6] Yida, Voltage Dividers – Circuits, Equation and Applications, https://www.seeedstudio.com/blog/2019/10/09/voltage-dividers-everything-you-need-to-know/, accessed on 19/03/23.
[7] Tontechnik-Rechner, Voltage Gain and Power Gain, http://www.sengpielaudio.com/calculatorVoltagePower.htm, accessed on 20/03/23.

Appendix A: Circuit cost calculation for exercise 21