Validating Hardware and SimPoints with gem5: A RISC-V Board Case Study

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Architecture simulators are a common and powerful tool in computer architecture design. It is essential that results reported by simulators are trustworthy. The accuracy of simulators should be evaluated by comparing their reported statistics and results to their counterparts in real hardware. We will present our methodology and tools for validating hardware with gem5, specifically focusing on a RISC-V board modeled after SiFive's HiFive Unmatched, called the RISCVMatched in gem5.

1 Methodology and Tools

Our work involves connecting components of gem5 Standard Library, such as the cache, memory, and processor, into one cohesive board. This board reduces the length of a gem5 runscript by at least 6 lines since we do not need to declare a cache hierarchy, memory, etc. in the runscript. It also involves improving the accuracy of the board with respect to real-life by finetuning the board's parameters. To validate the accuracy of our hardware model, we have used Vertical Research Group's Microbenchmarks and SPEC2006 benchmark suite as our evaluation tools.

2 Contributions

Our work contributes the RISCVMatched to gem5, and also provides a methodology to finetune a gem5 configuration to closely match real-life systems. This methodology involves using microbenchmarks to identify the specific components of the gem5 board that require tuning, and using SimPoints to get simulation results faster, overall resulting in a more accurate performance with respect to a benchmark suite.

3 Validation of the RISCV-Matched

We are conducting a test to compare the Instructions Per Cycle (IPC) ratio of the system under test, which can be either gem5 or the HiFive Unmatched, with the IPC of the HiFive Unmatched itself (calculated by perf). Specifically, we compare the ratio of the IPC of gem5 to the IPC of the HiFive Unmatched, and the ratio of the IPC of the HiFive Unmatched to its own IPC. When comparing our gem5 RISC-V board against the microbenchmark results, our results indicate a high level of accuracy and fidelity in our hardware model. This accuracy is more pronounced in control, execution, dependency, and storage types of microbenchmarks. A similar analysis is conducted for SPEC2006 as well. We have also validated gem5 with SimPoints, demonstrating that they can be a substitute for entire simulations, saving significant simulation time and resources.

4 Conclusion

Our finetuned board shows an improvement of around 18.4% in the Mean Squared Logarithmic Error for IPC Ratio of gem5 with respect to the perf over the default configuration. Similar data is seen for SPEC2006 as well, with improvements of 13.1% for SPEC2006 Ref and 10.3% for SPEC2006 Train. Our research contributes to gem5 by showcasing its promising capabilities in validating hardware designs, specifically in the context of RISC-V boards. Our findings also highlight the potential of gem5 as a powerful tool for hardware validation and simulation and pave the way for further research and development in computer architecture.