ESP32-C3 Series

Datasheet Version 1.9

Ultra-Low-Power SoC with RISC-V Single-Core CPU
2.4 GHz Wi-Fi (802.11 b/g/n) and Bluetooth® 5 (LE)
Optional 4 MB flash in the chip's package
QFN32 (5×5 mm) package

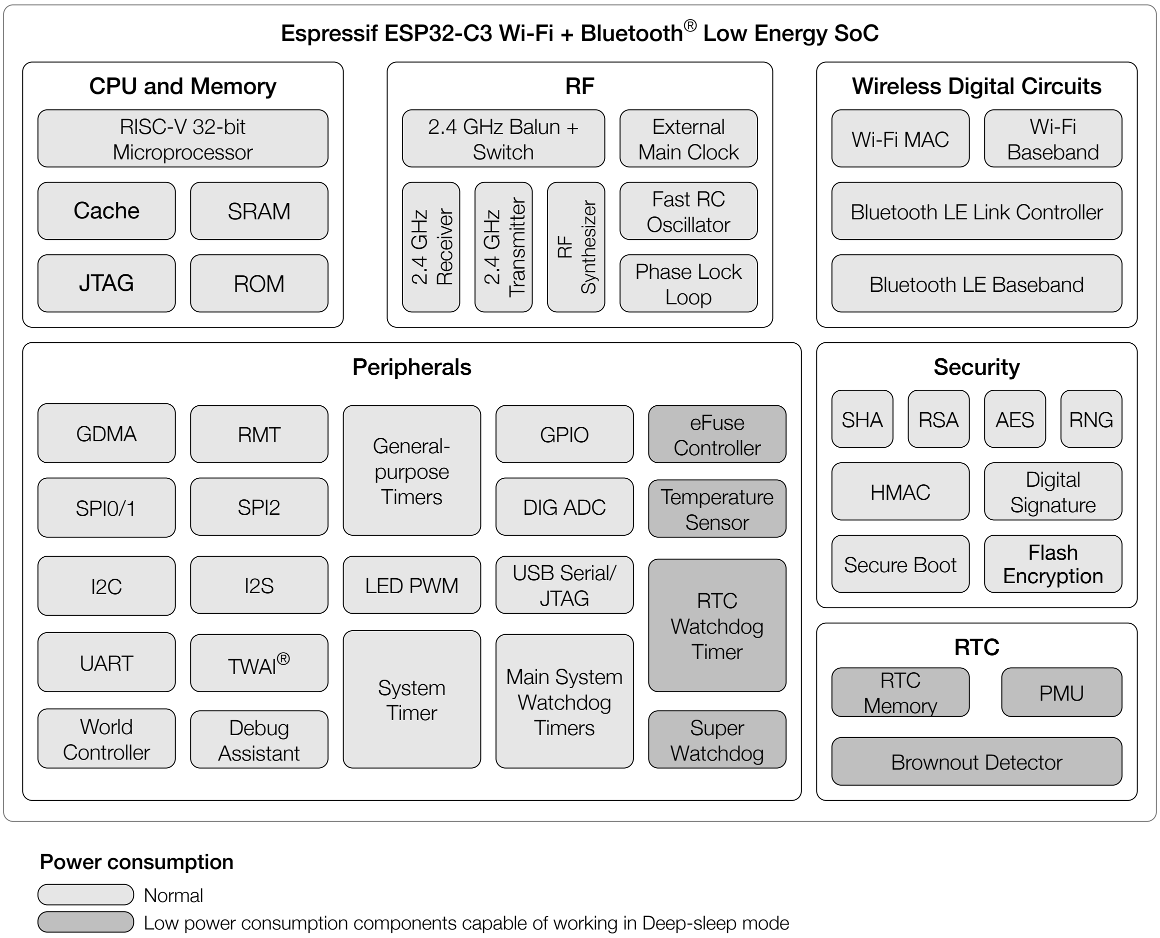
Including:

- ESP32-C3
- ESP32-C3FN4 – End of life
- ESP32-C3FH4
- ESP32-C3FH4AZ – Not Recommended for New Design (NRND)
- ESP32-C3FH4X – Recommended

Product Overview

ESP32-C3 is an low-power and highly-integrated MCU-based so
Bluetooth® Low Energy (Bluetooth LE).

The functional block diagram of the SoC is shown below.



ESP32-C3 Functional Block Diagram

For more information on power consumption, see Section 4.1.3.6 Power Management Unit

Features

Wi-Fi

- IEEE 802.11b/g/n-compliant
- Supports 20 MHz, 40 MHz bandwidth in 2.4 GHz band
- 1T1R mode with data rate up to 150 Mbps
- Wi-Fi Multimedia (WMM)
- TX/RX A-MPDU, TX/RX A-MSDU
- Immediate Block ACK
- Fragmentation and defragmentation
- Transmit opportunity (TXOP)
- Automatic Beacon monitoring (hardware TSF)
- Four virtual Wi-Fi interfaces
- Simultaneous support for Infrastructure BSS in Station mo
  promiscuous mode
  Note that when ESP32-C3 scans in Station mode, the SoftAP c
  channel
- Antenna diversity
- 802.11mc FTM

Bluetooth®

- Bluetooth LE: Bluetooth 5, Bluetooth mesh
- High power mode (20 dBm)
- Speed: 125 Kbps, 500 Kbps, 1 Mbps, 2 Mbps
- Advertising extensions
- Multiple advertisement sets
- Channel selection algorithm #2
- Internal co-existence mechanism between Wi-Fi and Blueto

CPU and Memory

- 32-bit RISC-V single-core processor, up to 160 MHz
- CoreMark® score:
  - 1 core at 160 MHz: 407.22 CoreMark; 2.55 CoreMark/MHz
- 384 KB ROM
- 400 KB SRAM (16 KB for cache)

- 8 KB SRAM in RTC
- In-package flash (see ESP32-C3 Series Ordering Information)
- SPI, Dual SPI, Quad SPI, and QPI interfaces that allow conn
- Access to flash accelerated by cache
- Supports flash in-Circuit Programming (ICP)

Advanced Peripheral Interfaces

- 22 or 16 programmable GPIOs
- Digital interfaces:
  - Three SPI
  - Two UART
  - I2C
  - I2S
  - Remote control peripheral, with 2 transmit channels and
  - LED PWM controller, with up to 6 channels
  - Full-speed USB Serial/JTAG controller
  - General DMA controller (GDMA), with 3 transmit channels
  - TWAI® controller compatible with ISO 11898-1 (CAN Specifc
- Analog interfaces:
  - Two 12-bit SAR ADCs, up to 6 channels
  - Temperature sensor
- Timers:
  - Two 54-bit general-purpose timers
  - Three digital watchdog timers
  - Analog watchdog timer
  - 52-bit system timer

Power Management

- Fine-resolution power control through a selection of cloc and individual power control of internal components
- Four power modes designed for typical scenarios: Active, M
- Power consumption in Deep-sleep mode is 5 µA
- RTC memory remains powered on in Deep-sleep mode

Security

- Secure boot - permission control on accessing internal and
- Flash encryption - memory encryption and decryption
- 4096-bit OTP, up to 1792 bits for users
- Cryptographic hardware acceleration:
  - AES-128/256 (FIPS PUB 197)
  - SHA Accelerator (FIPS PUB 180-4)
  - RSA Accelerator
  - Random Number Generator (RNG)
  - HMAC
  - Digital signature

RF Module

- Antenna switches, RF balun, power amplifer, low-noise rec
- Up to +21 dBm of power for an 802.11b transmission
- Up to +20 dBm of power for an 802.11n transmission
- Up to -105 dBm of sensitivity for Bluetooth LE receiver (12

Applications

With low power consumption, ESP32-C3 is an ideal choice for I

- Smart Home
- Industrial Automation
- Health Care
- Consumer Electronics
- Smart Agriculture
- POS Machines
- Service Robot
- Audio Devices
- Generic Low-power IoT Sensor H
- Generic Low-power IoT Data Log

Note:

Check the link or the QR code to make sure that you use the latest ve
https://www.espressif.com/documentation/esp32-c3_datasheet

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1 ESP32-C3 Series Comparison

1.1 Nomenclature

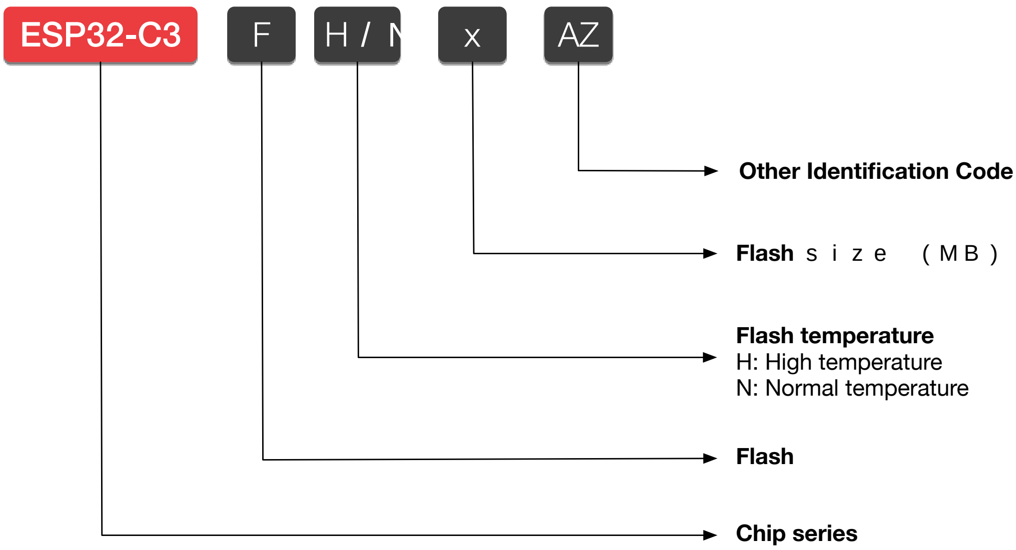

Figure 1-1. ESP32-C3 Series Nomenclature

1.2 Comparison

Table 1-1. ESP32-C3 Series Comparison

Ordering Code[1]	In-Package Flash[6]	Ambient Temp.[2] (°C)	Package (mm)	GPIO[4]	Chip Revision[5]
ESP32-C3[3]	—	–40 ~ 105	QFN32 (5*5)	22	v0.4
ESP32-C3FN4 (End of Life)	4 MB	–40 ~ 85	QFN32 (5*5)	22	v0.4
ESP32-C3FH4	4 MB	–40 ~ 105	QFN32 (5*5)	22	v0.4
ESP32-C3FH4AZ (NRND)	4 MB	–40 ~ 105	QFN32 (5*5)	16	v0.4
ESP32-C3FH4X (Recommended)	4 MB	–40 ~ 105	QFN32 (5*5)	16	v1.1

[1] For details on chip marking and packing, see Section 7 Packaging.

[2] Ambient temperature specifies the recommended temperature range of the environment immediately outside an Espressif chip.

[3] ESP32-C3 requires an SPI flash off the chip's package. For pin mapping, see Section 2.6 Pin Mapping Between Chip and Flash.

[4] SPI0/SPI1 pins for flash connection are not bonded for varia…

[5] All chip revisions have the same SRAM size, but chip revisi… available space for users than chip revision v0.4. Chip re… details in Compatibility Advisory for ESP32-C3 Chip Revision v1.1. For how to identify chip r… to ESP32-C3 Series SoC Errata.

[6] For information about in-package flash, see Section 4.1.2.1 Internal Memory. … chip operates at a maximum clock frequency of 80 MHz and does … a requirement for a higher flash clock frequency of 120 MHz or … contact us.

2 Pins

2.1 Pin Layout

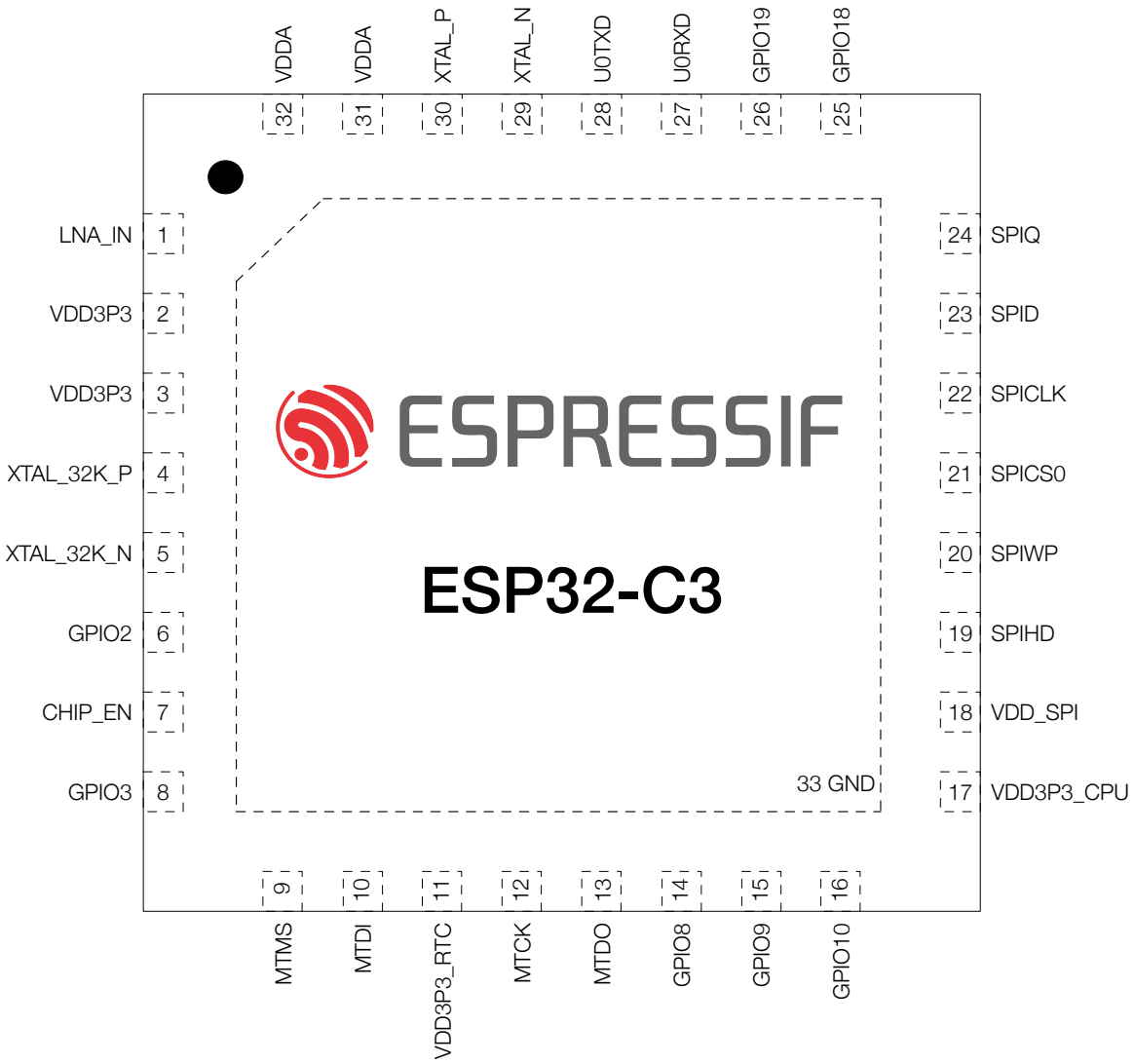

Figure 2-1. ESP32-C3FH4, and ESP32-C3FN4 Pin Layout (

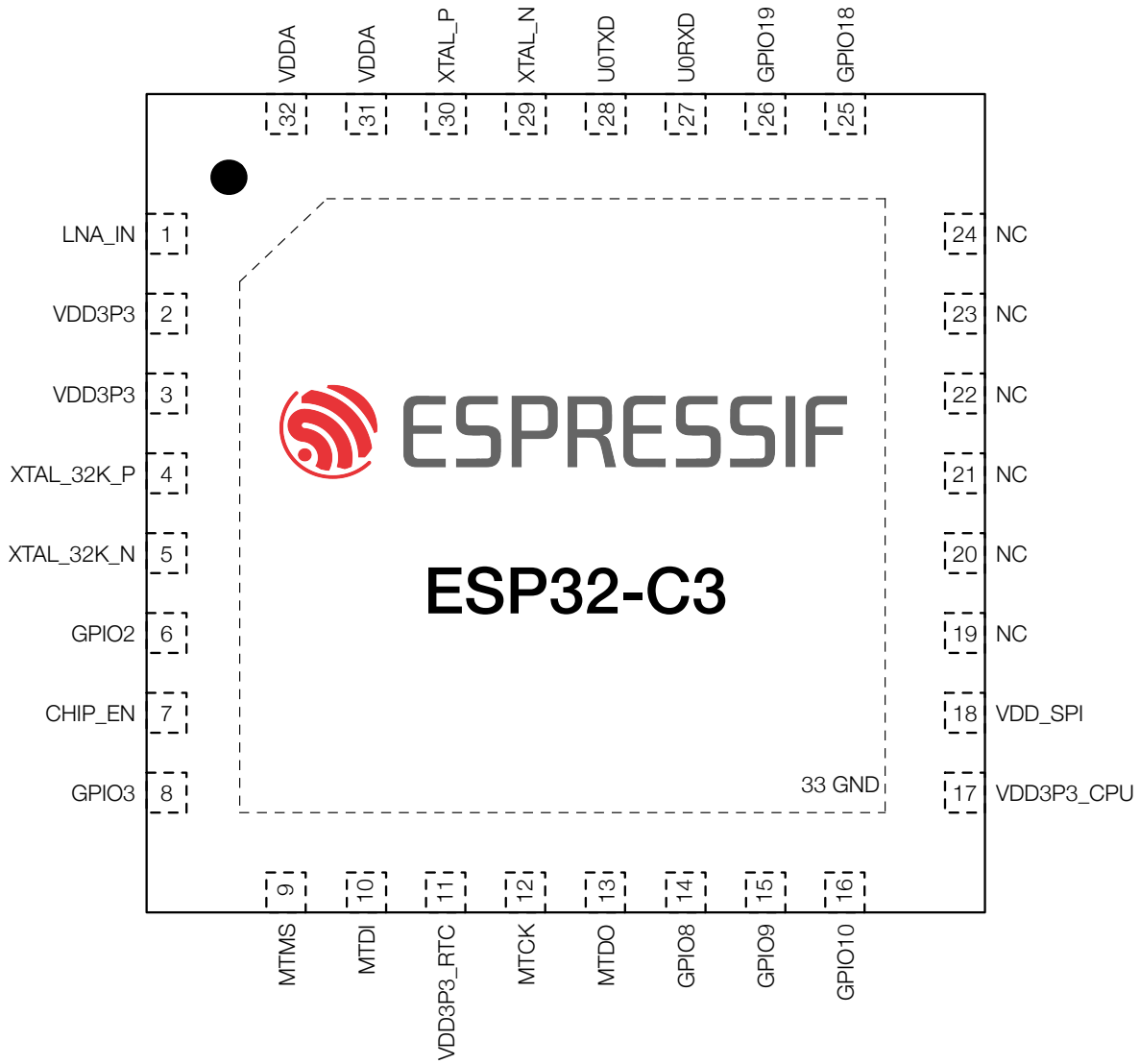

Figure 2-2. ESP32-C3FH4X and ESP32-C3FH4AZ Pin Lay

2.2 Pin Overview

The ESP32-C3 chip integrates multiple peripherals that r
the chip package size reasonably small, the number of ava
route all the incoming and outgoing signals is through pi
programmable registers (see ESP32-C3 Technical Reference Manual > Chapter IO MUX and GPIO Matrix).

All in all, the ESP32-C3 chip has the following types of p

- IO pins with the following predefined sets of functions to
  - Each IO pin has predefined IO MUX functions – see Table 2-4 IO MUX Functions
  - Some IO pins have predefined analog functions – see Table 2-6 Analog Functions

  Predefined functions means that each IO pin has a set of direct cor
  on-chip peripherals. During run-time, the user can co
  set to connect to a certain pin at a certain time via men

- Analog pins that have exclusively analog functions – see Table 2-7 Analog Pins
- Power pins that supply power to the chip components – see 2.5 Power Pi

Table 2-1 Pin Overview gives an overview of all the pins. For more inf
each pin type below, or Appendix A – ESP32-C3 Consolidated Pin Overv

Table 2-1. Pin Overview

Pin No.	Pin Name	Pin Type	Pin Providing Power [2-4]	Pin Settings [5]		Pin Function Se [1]	
				At Reset	After Reset	IO MUX	Analog
1	LNA_IN	Analog					
2	VDD3P3	Power					
3	VDD3P3	Power					
4	XTAL_32K_P	IO	VDD3P3_RTC			IO MUX	Analog
5	XTAL_32K_N	IO	VDD3P3_RTC			IO MUX	Analog
6	GPIO2	IO	VDD3P3_RTC	IE	IE	IO MUX	Analog
7	CHIP_EN	Analog					
8	GPIO3	IO	VDD3P3_RTC	IE	IE	IO MUX	Analog
9	MTMS	IO	VDD3P3_RTC		IE	IO MUX	Analog
10	MTDI	IO	VDD3P3_RTC		IE	IO MUX	Analog
11	VDD3P3_RTC	Power					
12	MTCK	IO	VDD3P3_CPU		IE [6]	IO MUX	
13	MTDO	IO	VDD3P3_CPU		IE	IO MUX	
14	GPIO8	IO	VDD3P3_CPU	IE	IE	IO MUX	
15	GPIO9	IO	VDD3P3_CPU	IE, WPU	IE, WPU	IO MUX	
16	GPIO10	IO	VDD3P3_CPU		IE	IO MUX	
17	VDD3P3_CPU	Power					
18	VDD_SPI [8]	Power [9]	VDD3P3_CPU			IO MUX	
19	SPIHD	IO	VDD_SPI / VDD3P3_CPU	WPU	IE, WPU	IO MUX	
20	SPIWP	IO	VDD_SPI / VDD3P3_CPU	WPU	IE, WPU	IO MUX	

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Table 2-1 – cont'd from previous page

Pin No	Pin Name [9]	Pin Type	Pin Providing Power [2] [4]	Pin Setting At Reset [5]	Pin Setting After Reset [5]	Pin Function Set IOMUX [1]	Pin Function Set Analog [1]
21	SPICS0	IO	VDD_SPI / VDD3P3_CPU [3]	WPU	IE, WPU	IOMUX	
22	SPICLK	IO	VDD_SPI / VDD3P3_CPU [3]	WPU	IE, WPU	IOMUX	
23	SPID	IO	VDD_SPI / VDD3P3_CPU [3]	WPU	IE, WPU	IOMUX	
24	SPIQ	IO	VDD_SPI / VDD3P3_CPU [3]	WPU	IE, WPU	IOMUX	
25	GPIO18	IO	VDD3P3_CPU			IOMUX	Analog
26	GPIO19	IO	VDD3P3_CPU		USB_PU	IOMUX	Analog
27	U0RXD	IO	VDD3P3_CPU		IE, WPU	IOMUX	
28	U0TXD	IO	VDD3P3_CPU		WPU [7]	IOMUX	
29	XTAL_N	Analog					
30	XTAL_P	Analog					
31	VDDA	Power					
32	VDDA	Power					
33	GND	Power					

1. Bold marks the pin function set in which a pin has its default function. See also Table 5-1 in Chapter 5 IO MUX and GPIO Matrix.

2. In column Pin Providing Power, digital power pins powered by VDD_SPI:
   - Power actually comes from the internal power rail supplied by VDD_SPI. See also Section 2.5.2 Typical Power Supply Scheme.

3. In column Pin Providing Power, digital power pins powered by VDD3P3_CPU / VDD_SPI:
   - Pin Providing Power (either VDD3P3_CPU or VDD_SPI) can be configured in register RTC_CNTL_DIG_PWC_REG. See ESP32-C3 Technical Reference Manual > Chapter IO MUX and GPIO Matrix.

4. The default drive strength for each pin is as follows:
   - GPIO2, GPIO3, MTMS, and MTDI: 10 mA
   - GPIO18, GPIO19: 40 mA
   - All other pins: 20 mA

5. Column Pin Setting shows predefined settings at reset and after reset with the following options:
   - IE – input enabled
   - WPU – internal weak pull-up resistor enabled
   - WPD – internal weak pull-down resistor enabled
   - USB_PU – USB pull-up resistor enabled
     - By default, the USB function is enabled for USB pins (i.e., GPIO18 and GPIO19), and the USB pull-up resistor. The USB pull-up resistor is controlled by the USB Serial/JTAG Controller. The pull-up resistor value is controlled by USB_SERIAL_JTAG_EXCHG_PINS_OVERRIDE. See ESP32-C3 Technical Reference Manual > Chapter USB Serial/JTAG Controller.
     - When the USB function is disabled, USB pins are used as regular IO pins, and the pull-up/pull-down resistors are disabled by default (configurable by WPU/WPD). For ESP32-C3 see ESP32-C3 Technical Reference Manual > Chapter IO MUX and GPIO Matrix.

6. Depends on the value of EFUSE_DIS_PAD_JTAG
   - 0 - default value. Input enabled, and internal weak pull-up resistor enabled.
   - 1 - input enabled (IE)

7. Output enabled

8. By default VDD_SPI is the power supply pin for in-package and off-package flash/PSRAM. If VDD_SPI is connected to an off-package flash, and this flash is powered by another power supply, please refer to ESP32-C3 Technical Reference Manual > Chapter IO MUX and GPIO Matrix.

9. For ESP32-C3FH4AZ and ESP32-C3FH4X, pins with 4 integrated flash (marked as "flash") are internally connected.

Some pins have glitches during power-up. See details in T

Table 2-2. Power-Up Glitches on Pins

Pin	Glitch[1]	Typical Time Period (ns)
MTCK	Low-level glitch	5
MTDO	Low-level glitch	5
GPIO10	Low-level glitch	5
U0RXD	Low-level glitch	5
GPIO18	High-level glitch	50000

[1] Low-level glitch: the pin is at a low level out
period;
High-level glitch: the pin is at a high level
time period;
Pull-down glitch: the pin is at an internal w
during the time period;
Pull-up glitch: the pin is at an internal wea
the time period.
Please refer to Table 5-4 for detailed parameters about lov
and pull-down/up.

2.3 IO Pins

2.3.1 IO MUX Functions

The IOMUX allows multiple input/output signals to be con
ESP32-C3 can be connected to one of the three signals (2-4
IOMUX Functions.

Among the three sets of signals:

- Some are routed via the GPIO Matrix (GPIO0, GPIO1, etc.), which incorporates int circuitry for mapping signals programmatically. It g However, the fexibility of programmatic mapping come signals. For details about connecting to peripherals ESP32-C3 Technical Reference Manual > Chapter IO MUX and GPIO Matrix.
- Some are directly routed from certain peripherals (U0TXD, MTCK, etc.), including UART0 and SPI2 - see Table 2-3 IOMUX Functions.

Table 2-3. Peripheral Signals Routed via

Pin Fun	Signal	Description
U0TXD	Transmit data	UART0 interface
U0RXD	Receive data	
MTCK	Test clock	JTAG interface for debugging
MTDO	Test Data Out	
MTDI	Test Data In	
MTMS	Test Mode Select	
SPIQ	Data out	3.3 V SPI0/1 interface for connection to i via the SPI bus. It supports 1-, 2-, 4-lin 2.6 Pin Mapping Between Chip and Flash
SPID	Data in	
SPIHD	Hold	
SPIWP	Write protect	
SPICLK	Clock	
SPICS...	Chip select	
FSPIQ	Data out	SPI2 interface for fast SPI connection. I modes
FSPID	Data in	
FSPIHD	Hold	
FSPIWP	Write protect	
FSPICLK	Clock	
FSPICS0	Chip select	

Table 2-4 IOMUX Functions shows the IOMUX functions of IO pins.

Table 2-4. IOMUX Pin Functions

Pi No	IOMUX GPIO Name[2]	IOMUX Function[1, 2, 3] F0	Type[3]	F1	Typ	F2	Type
4	GPIO0	GPIO0	I/O/T	GPIO0	I/O/T		

Cont'd on next page

Table 2-4 – cont'd from previous page

Pin No	IOMUX GPIO Name[2]	IOMUX Function[1] F0	Type[3]	F1	Type	F2	Type
5	GPIO1	GPIO1	I/O/T	GPIO1	I/O/T		
6	GPIO2	GPIO2	I/O/T	GPIO2	I/O/T	FSPIQ	I1/O/T
8	GPIO3	GPIO3	I/O/T	GPIO3	I/O/T		
9	GPIO4	MTMS	I1	GPIO4	I/O/T	FSPIHD	I1/O/T
10	GPIO5	MTDI	I1	GPIO5	I/O/T	FSPIWP	I1/O/T
12	GPIO6	MTCK	I1	GPIO6	I/O/T	FSPICLK	I1/O/T
13	GPIO7	MTDO	O/T	GPIO7	I/O/T	FSPID	I1/O/T
14	GPIO8	GPIO8	I/O/T	GPIO8	I/O/T		
15	GPIO9	GPIO9	I/O/T	GPIO9	I/O/T		
16	GPIO10	GPIO10	I/O/T	GPIO10	I/O/T	FSPICS0	I1/O/T
18	GPIO11	GPIO11	I/O/T	GPIO11	I/O/T		
19	GPIO12	SPIHD	I1/O/T	GPIO12	I/O/T		
20	GPIO13	SPIWP	I1/O/T	GPIO13	I/O/T		
21	GPIO14	SPICS0	O/T	GPIO14	I/O/T		
22	GPIO15	SPICLK	O/T	GPIO15	I/O/T		
23	GPIO16	SPID	I1/O/T	GPIO16	I/O/T		
24	GPIO17	SPIQ	I1/O/T	GPIO17	I/O/T		
25	GPIO18	GPIO18	I/O/T	GPIO18	I/O/T		
26	GPIO19	GPIO19	I/O/T	GPIO19	I/O/T		
27	GPIO20	U0RXD	I1	GPIO20	I/O/T		
28	GPIO21	U0TXD	O	GPIO21	I/O/T		

[1] Bold marks the default pin functions in the default boot mode. See Chip Boot Mode Control.

[2] Regarding highlighted GPIOs, see 2.3.3 Restrictions for GPIOs.

[3] Each IOMUX function (Fn, n = 0 in GPIOn) has associated type(s). The detailed description of types is as follows:

- I – input. O – output. T – high impedance.
- I1 – input; if the pin is assigned an input function, a logic 1 is always applied to the function.
- I0 – input; if the pin is assigned an input function, a logic 0 is always applied to the function.

2.3 Analog Functions

Some IO pins also have functions for analog peripherals (such as ADC). These analog signals are routed to the Analog Functions, see 2-Analog Functions.

Table 2-5. Analog Signals Routed to Analog Functions

Pin Function	Signal	Description
ADC..._CH..	ADC1/2 channel	ADC1/2 analog interface
USB_D- USB_D+	Data - Data +	USB Serial/JTAG function
XTAL_32K_N XTAL_32K_P	Negative clock Positive clock	32 kHz external clock input/output connected to ESP32-C3's crystal

Table 2-6 shows the analog functions of IO pins.

Table 2-6. Analog Functions

Pin No	Analog Name [1] [2]	Analog Function [2] F0	F1
4	GPIO0	XTAL_32K_P	ADC1_CH0
5	GPIO1	XTAL_32K_N	ADC1_CH1
6	GPIO2		ADC1_CH2
8	GPIO3		ADC1_CH3
9	GPIO4		ADC1_CH4
10	GPIO5		ADC2_CH0
25	GPIO18	USB_D-	
26	GPIO19	USB_D+	

[1] Bold marks the default pin functions in the default boot mode. See also Chapter 3 Chip Boot Mode Control.

[2] Regarding highlighted, see Section 2.3.1 Restrictions for GPIOs.

2.3 Restrictions for GPIOs

All IO pins of ESP32-C3 have GPIO pin functions. However, for different purposes based on the requirements. Some I consider the multiplexed nature and the limitations whe

In tables of this chapter, highlighting. The non-highlighted GPIO recommended for use first. If more pins are needed, the hig avoid conflicts with important pin functions.

The highlighted IO pins have the following important pin

- GPIO – allocated for communication with in-package flas details, see Section 2.6 Pin Mapping Between Chip and Flash.
- GPIO – have one of the following important functions:
  - Strapping pins – need to be at certain logic levels at start 3 Boot Configurations
  - USB_D+/D- – by default, connected to the USB Serial/JTAG pins need to be reconfigured.
  - JTAG interface – often used for debugging. See Table 2-3 IO MUX Functions. To free these up, the pin functions USB_D+/D- of the USB Serial/JTAG Controller can be used instead.
  - UART interface – often used for debugging. See Table 2-3 IO MUX Functions.
  - ADC2 – no restrictions, unless Wi-Fi is connected. ADC2_CH0 analog fu (see Table 2-4 Analog Functions) cannot be used with Wi-Fi simultan

See also Appendix A – ESP32-C3 Consolidated Pin Overview.

2.4 Analog Pins

Table 2-7. Analog Pins

Pin No	Pin Name	Pin Type	Pin Function
1	LNA_IN	I/O	Low Noise Amplifer (RF LNA) input / ou
7	CHIP_EN	I	High: on, enables the chip (powered up Low: off, disables the chip (powered d Note: Do not leave the CHIP_EN pin foa
29	XTAL_N	—	External clock input/output connecte
30	XTAL_P	—	oscillator. P/N means differential c

2.5 Power Supply

2.5.1 Power Pins

The chip is powered via the power pins described in Table 2-8. Power Pins.

Table 2-8. Power Pins

Pin No	Pin Name	Direction	Power Supply[1][2] Power Domain / Other	IO Pins[3]
2	VDD3P3	Input	Analog power domain	
3	VDD3P3	Input	Analog power domain	
11	VDD3P3_RTC	Input	RTC and part of Digital power domain	RTC power domain
17	VDD3P3_CPU	Input	Digital power domain	Digital IO
18	VDD_SPI[4]	Input	In-package fash (backup power line)	
		Output	In-package and off-package fash	SPI clock IO
31	VDDA	Input	Analog power domain	
32	VDDA	Input	Analog power domain	
33	GND	—	External ground connection	

[1] See in conjunction with 2.5.2 Power Scheme.

[2] For recommended and maximum voltage values, see 5.1 Absolute Maximum Ratings and 5.2 Recommended Operating Conditions.

[3] Digital IO pins are those powered by VDD3P3_CPU, and those powered by VDD3P3_RTC and so on, as shown in 2.5.2 Power Scheme. See also 2.4.1 Power Pins > Column Providing Power.

[4] To configure VDD_SPI as ESP32-C3 output, please refer to ESP32-C3 Technical Reference Manual > Chapter Low-power Management.

2.5.2 Power Scheme

The power scheme is shown in Figure 2-3 ESP32-C3 Power Scheme.

The components on the chip are powered via voltage regulators.

Table 2-9. Voltage Regulators

Voltage Regulator	Output	Power Supply
Digital	1.1 V	Digital power domain
Low-power	1.1 V	RTC power domain

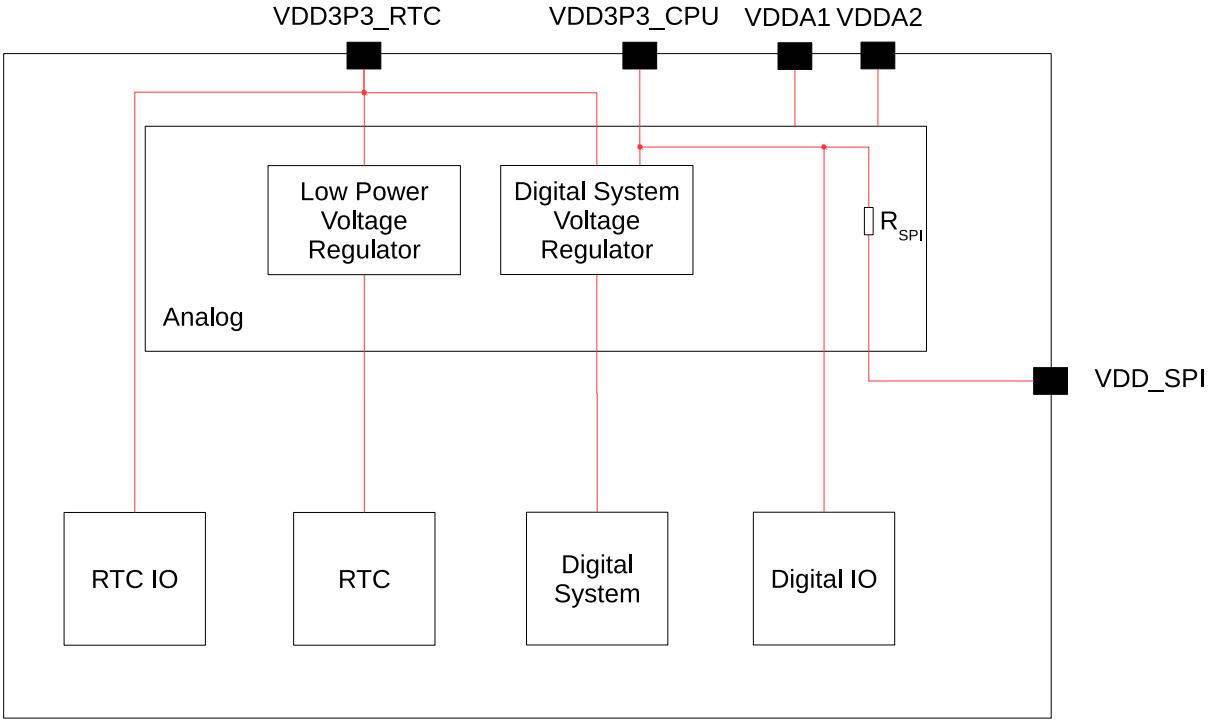


Figure 2-3. ESP32-C3 Power Scheme

2.5 Chip Power-up and Reset

Once the power is supplied to the chip, its power rails ne pin used for power-up and reset – is pulled high to activa power-up and reset timing parameters in Table 2-10 and Figure 2-4.

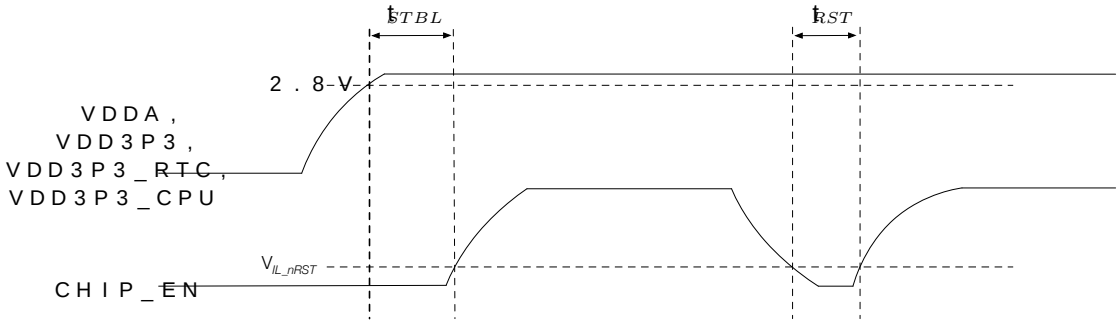


Figure 2-4. Visualization of Timing Parameter

Table 2-10. Description of Timing Parameters f

Param	Description	Min(µs)
t_{STBL}	Time reserved for the power rails of VDD VDD3P3_RTC, and VDD3P3_CPU to stabilize before pin is pulled high to activate the chip	50
t_{RST}	Time reserved for CHIP_EN to reset the chip (see Table 5-4)	50

2.6 Pin Mapping Between Chip and Flash

Table 2-11 lists the pin mapping between the chip and fash for a

For chip variants with in-package flash (see Table 1-1 Comparison), the pins allocated fo in-package fash can be identifed depending on the SPI moc

For off-package fash, these are the recommended pin mapp

For more information on SPI controllers, see also Section 4.2 SPI Controller

Notice:

It is not recommended to use the pins connected to fash for any

Table 2-11. Pin Mapping Between Chip and In-p

Pin No.	Pin Name	Single Flash	Dual Flash	Quad SPI / QPI Flash
22	SPICLK	CLK	CLK	CLK
21	SPICS0[1]	CS#	CS#	CS#
23	SPID	DI	DI	DI
24	SPIQ	DO	DO	DO
20	SPIWP	WP#	WP#	WP#
19	SPIHD	HOLD#	HOLD#	HOLD#

[1] CS0 is for in-package fash

3 Boot Confgurations

The chip allows for confguring the following boot parame
power-up or a hardware reset, without microcontroller in

- Chip boot mode
  - Strapping pins: GPIO2, GPIO8, and GPIO9
- ROM message printing
  - Strapping pin: GPIO8
  - eFuse parameters: EFUSE_UART_PRINT_CONTROL and EF

The default values of all the above eFuse bits are 0, which
one-time programmable, once an eFuse bit is programmed t
program eFuse bits, refer to ESP32-C3 Technical Reference Manual > Chapter eFuse Controller.

The default values of the strapping pins, namely the logi
pull-up/pull-down resistors at reset if the pins are not
high-impedance circuit.

Table 3-1. Default Confguration of Strapp

Strappi	Default Con	Bit Value
GPIO2	Floating	–
GPIO8	Floating	–
GPIO9	Weak pull-up	1

To change the bit values, the strapping pins should be con
the ESP32-C3 is used as a device by a host MCU, the strappi
the host MCU.

All strapping pins have latches. At system reset, the lat
pins and store them until the chip is powered down or shut
any other way. It makes the strapping pin values availabl
freed up to be used as regular IO pins after reset.

The timing of signals connected to these strapping pins should meet the requirements listed in the specifcations in Table 3-2 and Figure 3-1.

Table 3-2. Description of Timing Parameters fo

Param	Description	Min (ms)
t_{SU}	Setup time is the time reserved for the power rails before the CHIP_EN pin is pulled high to activat	0
t_H	Hold time is the time reserved for the chip to read pin values after CHIP_EN is already high and start operating as regular IO pins.	3

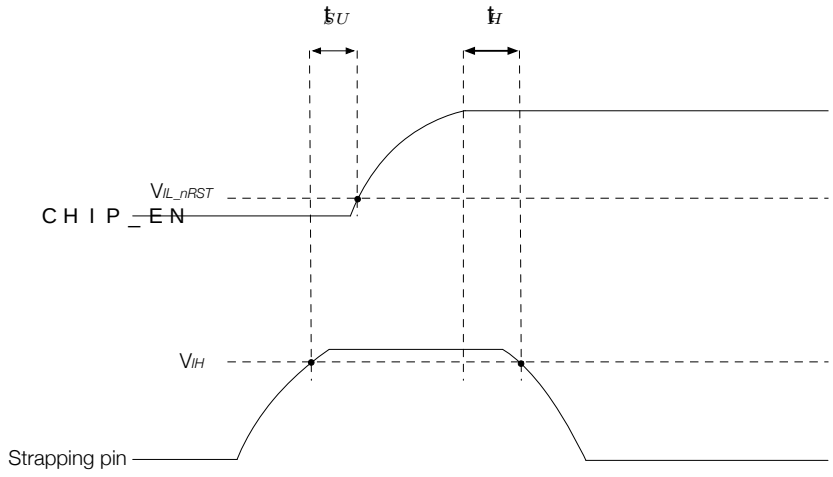


Figure 3-1. Visualization of Timing Parameter

3.1 Chip Boot Mode Control

GPIO2, GPIO8, and GPIO9 control the boot mode 3-Chip Boot Mode Control.

Table 3-3. Chip Boot Mode Control

Boot Mode	GPIO2[2]	GPIO8	GPIO9
SPI Boot	1	Any value	1
Joint Download Boot[3]	1	1	0

[1] Bold marks the default value and configuration
[2] GPIO2 actually does not determine SPI Boot Download Boot mode, but it is recommended this pin up due to glitches.
[3] Joint Download Boot mode supports the following download methods:
- USB-Serial-JTAG Download Boot
- UART Download Boot

In SPI Boot mode, the ROM bootloader loads and executes the system.

In Joint Download Boot mode, users can download binary files also possible to download binary files into SRAM and execute

In addition to SPI Boot and Joint Download Boot modes, ESP For details see Section ESP32-C3 Technical Reference Manual > Chapter Boot Control.

3.2 ROM Messages Printing Control

During the boot process, the messages by the ROM code can

- (Default) UART0 and USB Serial/JTAG controller

- UART0
- USB Serial/JTAG controller

EFUSE_UART_PRINT_CONTROL and GPIO8 could be used to control whether to print UART0 ROM messages. The UART0 ROM message printing is managed by EFUSE_UART_PRINT_CONTROL and GPIO8 as shown in Table 3-4 UART0 ROM Message Printing Control.

Table 3-4. UART0 ROM Message Printing Control

UART0 ROM Code Printing	EFUSE_UART_PRINT_CONTROL	GPIO8
Enabled	0	Ignored
	1	0
	2	1
Disabled	1	1
	2	0
	3	Ignored

[1] Bold marks the default value and configuration.

EFUSE_USB_PRINT_CHANNEL could be used to control whether to print USB Serial/JTAG messages. The USB Serial/JTAG ROM message printing is managed by EFUSE_USB_PRINT_CHANNEL and EFUSE_DIS_USB_SERIAL_JTAG as shown in Table 3-5 USB Serial/JTAG ROM Message Printing Control.

Table 3-5. USB Serial/JTAG ROM Message Printing Control

USB Serial/JTAG ROM Code Printing	EFUSE_DIS_USB_SERIAL_JTAG[2]	EFUSE_USB_PRINT_CHANNEL
Enabled	0	0
Disabled	0	1
	1	Ignored

[1] Bold marks the default value and configuration.

[2] EFUSE_DIS_USB_SERIAL_JTAG controls whether to di

4 Functional Description

4.1 System

This section describes the core of the chip's operation, system components, and security features.

4.1.1 Microprocessor and Master

This subsection describes the core processing units with

4.1.1.1 High-Performance CPU

ESP32-C3 has a low-power 32-bit RISC-V single-core micr

- four-stage pipeline that supports a clock frequency o
- RV32IMC ISA
- 32-bit multiplier and 32-bit divider
- up to 32 vectored interrupts at seven priority levels
- up to 8 hardware breakpoints/watchpoints
- up to 16 PMP regions
- JTAG for debugging

For details, see ESP32-C3 Technical Reference Manual > Chapter High-Performance CPU

4.1.1.2 GDMA Controller

ESP32-C3 has a general DMA controller (GDMA) with six inc and three receive channels. These six channels are share controller implements a fixed-priority scheme among thes

The GDMA controller controls data transfer using linked memory-to-memory data transfer at a high speed. All chan

Peripherals on ESP32-C3 with DMA feature are SPI2, UHCI0

For details, see ESP32-C3 Technical Reference Manual > Chapter GDMA Controller (DMA)

4.1.2 Memory Organization

This subsection describes the memory arrangement to exp for efficient operation.

Figure 4-1 illustrates the address mapping structure of ESP32

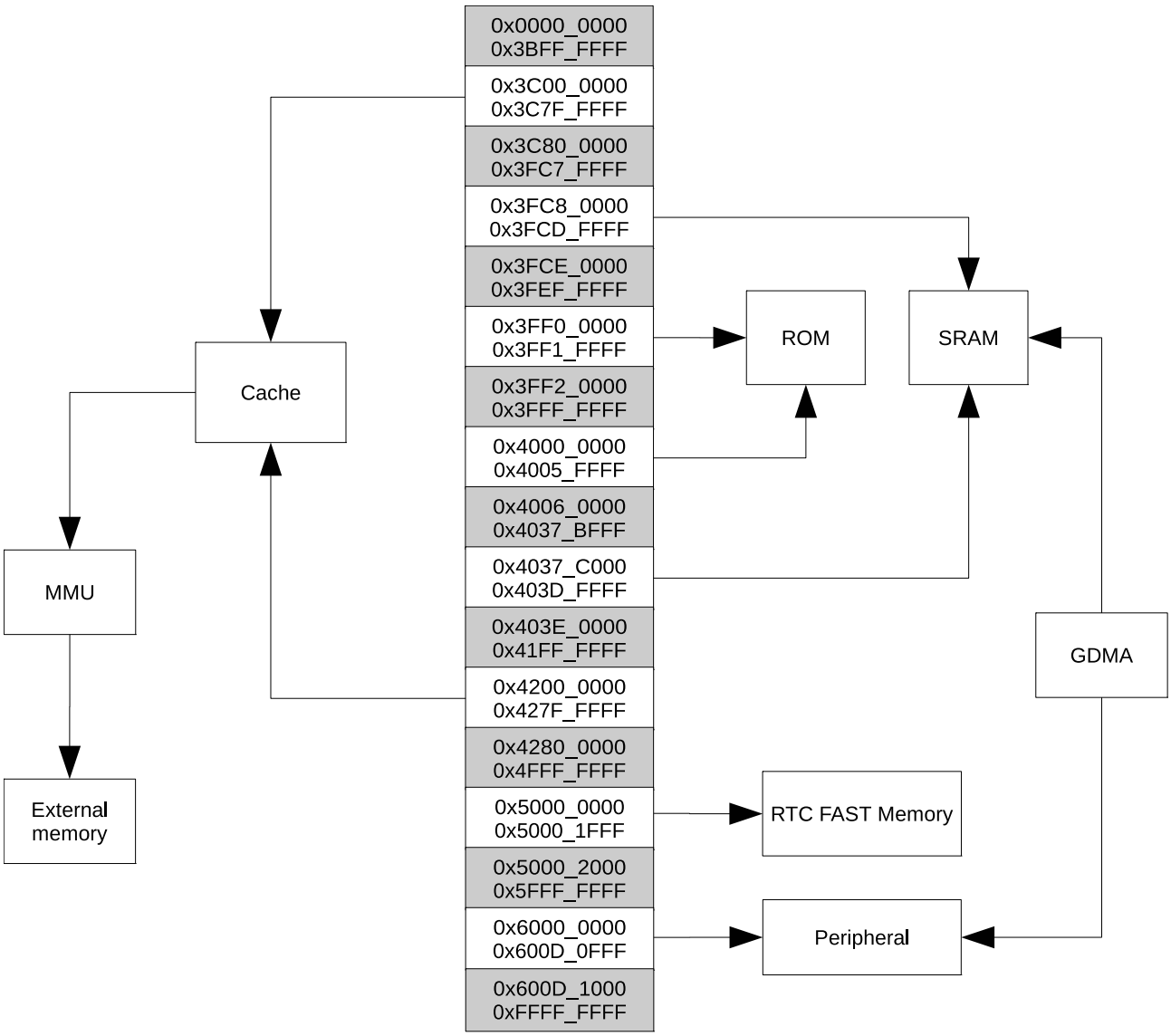


Figure 4-1. Address Mapping Structure

Note:
The memory space with gray background is not available for use

4.1.2 Internal Memory

ESP32-C3's internal memory includes:

- 384 KB of ROM for booting and core functions
- 400 KB of on-chip SRAM for data and instructions, running at a MHz. Of the 400 KB SRAM, 16 KB is confgured for cache
- RTC FAST memory of 8 KB of SRAM that can be accessed by the main Deep-sleep mode
- 4 Kbit of eFuse bits are reserved for your data, such as

- In-package fash
  - See fash size in ESP32-C3 Series Comparison
  - More than 100,000 program/erase cycles
  - More than 20 years of data retention time
  - Clock frequency up to 80 MHz by default

For details, see ESP32-C3 Technical Reference Manual > Chapter System and Memory.

4.1.2 Off-package Flash

ESP32-C3 supports SPI, Dual SPI, Quad SPI, and QPI interf fash, i.e. fash outside the chip's pacakge.

CPU's instruction memory space and read-only data memor ESP32-C3, whose size can be 16 MB at most. ESP32-C3 suppo XTS-AES to protect developers' programs and data in fash

Through high-speed caches, ESP32-C3 can support at a tim

- 8 MB of instruction memory space which can map into fas and 32-bit reads are supported.
- 8 MB of data memory space which can map into fash as ind 32-bit reads are supported.

> Note:
> After ESP32-C3 is initialized, software can customize the map

For details, see ESP32-C3 Technical Reference Manual > Chapter System and Memory.

4.1.3 Cache

ESP32-C3 has an eight-way set associative cache. This ca features:

- size: 16 KB
- block size: 32 bytes
- pre-load function
- lock function
- critical word frst and early restart

For details, see ESP32-C3 Technical Reference Manual > Chapter System and Memory.

4.1.4 eFuse Controller

The eFuse memory is a one-time programmable memory that s controller of ESP32-C3 is used to program and read this eF

Feature List

- Configurable write protection
- Configurable read protection
- Various hardware encoding schemes against data corru

For details, see Chapter Flash Memory Controller in ESP32-C3 Technical Reference Manual.

4.1 System Components

This subsection describes the essential components that the system.

4.1.1 IO MUX and GPIO Matrix

ESP32-C3 has 22 or 16 GPIO pins which can be assigned vari registers. Besides digital signals, some GPIOs can be al

All GPIOs have selectable internal pull-up or pull-down, are configured as an input, the input value can be read by s be set to generate edge-triggered or level-triggered CPU non-inverting and tristate, including input and output b multiplexed with other functions, such as the UART, SPI, to holding state.

The IO MUX and the GPIO matrix are used to route signals fr provide highly configurable I/O. Using GPIO Matrix, perip while peripheral output signals can be configured to any I

For details, see Chapter IO MUX and GPIO Matrix in ESP32-C3 Technical Reference Manual.

4.1.2 Reset

The ESP32-C3 chip provides four types of reset that occur System Reset, and Chip Reset. Except for Chip Reset, all r memory.

Feature List

- Support four reset levels:
  - CPU Reset: Only resets CPU core. Once such reset is r vector will be executed
  - Core Reset: Resets the whole digital system except R Bluetooth® LE, and digital GPIOs
  - System Reset: Resets the whole digital system, incl
  - Chip Reset: Resets the whole chip
- Support software reset and hardware reset:

– Software Reset : The CPU can trigger a software rese

– Hardware Reset : Hardware reset is directly trigger

For deta ESP32-C3 Technical Reference Manual > Chapter Reset and Clock

4.1.3 Clock

For deta ESP32-C3 Technical Reference Manual > Chapter Reset and Clock

CPU Clock

The CPU clock has three possible sources :

- external main crystal clock
- fast RC oscillator (typically about 17.5 MHz , and adju
- PLL clock

The application can select the clock source from the thre the CPU clock directly, or after division, depending on t clock source would be the external main crystal clock div

> Note:
> ESP32-C3 is unable to operate without an external main crysta

RTC Clock

The RTC slow clock is used for RTC counter, RTC watchdog ar sources :

- external low-speed (32 kHz) crystal clock
- internal slow RC oscillator (typically about 136 kHz ,
- internal fast RC oscillator divided clock (derived fr

The RTC fast clock is used for RTC peripherals and sensor

- external main crystal clock divided by 2
- internal fast RC oscillator divide-by-N clock (typic

4.1.3 Interrupt Matrix

The Interrupt Matrix in the ESP32-C3 chip independently CPU's peripheral interrupts, to timely inform CPU to pro

Feature List

- Accept 62 peripheral interrupt sources as input
- Generate 31 CPU peripheral interrupts to CPU as output
- Query current interrupt status of peripheral interru

- Configure priority, type, threshold, and enable signa

For details, see ESP32-C3 Technical Reference Manual > Chapter Interrupt Matrix

4.1.3.5 System Timer

ESP32-C3 integrates a 52-bit system timer, which has two
timer has the following features:

- counters with a fixed clock frequency of 16 MHz
- three types of independent interrupts generated acco
- two alarm modes: target mode and period mode
- 52-bit target alarm value and 26-bit periodic alarm va
- automatic reload of counter value
- counters can be stalled if the CPU is stalled or in OCD r

For details, see ESP32-C3 Technical Reference Manual > Chapter System Timer

4.1.3.6 Power Management Unit

The ESP32-C3 has an advanced Power Management Unit (PMU)
different power domains of the chip to achieve the best ba
consumption, and wakeup latency.

Configuring the PMU is a complex procedure. To simplify po
the following predefined power modes that power up different combinations

- **Active mode** – The CPU, RF circuits, and all peripherals are
  transmit, and listen.
- **Modem-sleep mode** – The CPU is on, but the clock frequency can b
  connections can be configured to remain active as RF ci
  required.
- **Light-sleep mode** – The CPU stops running, and can be optionally
  up via all wake up mechanisms: MAC, RTC timer, or exter
  active. Some groups of digital peripherals can be opt
- **Deep-sleep mode** – Only RTC is powered on. Wireless connection

For power consumption in different power modes, see Section 5.6 Current Consumption

Figure 4-2 Components and Power Domains and the following Table 4-1 show the distributi
components power domain and power subdomains.

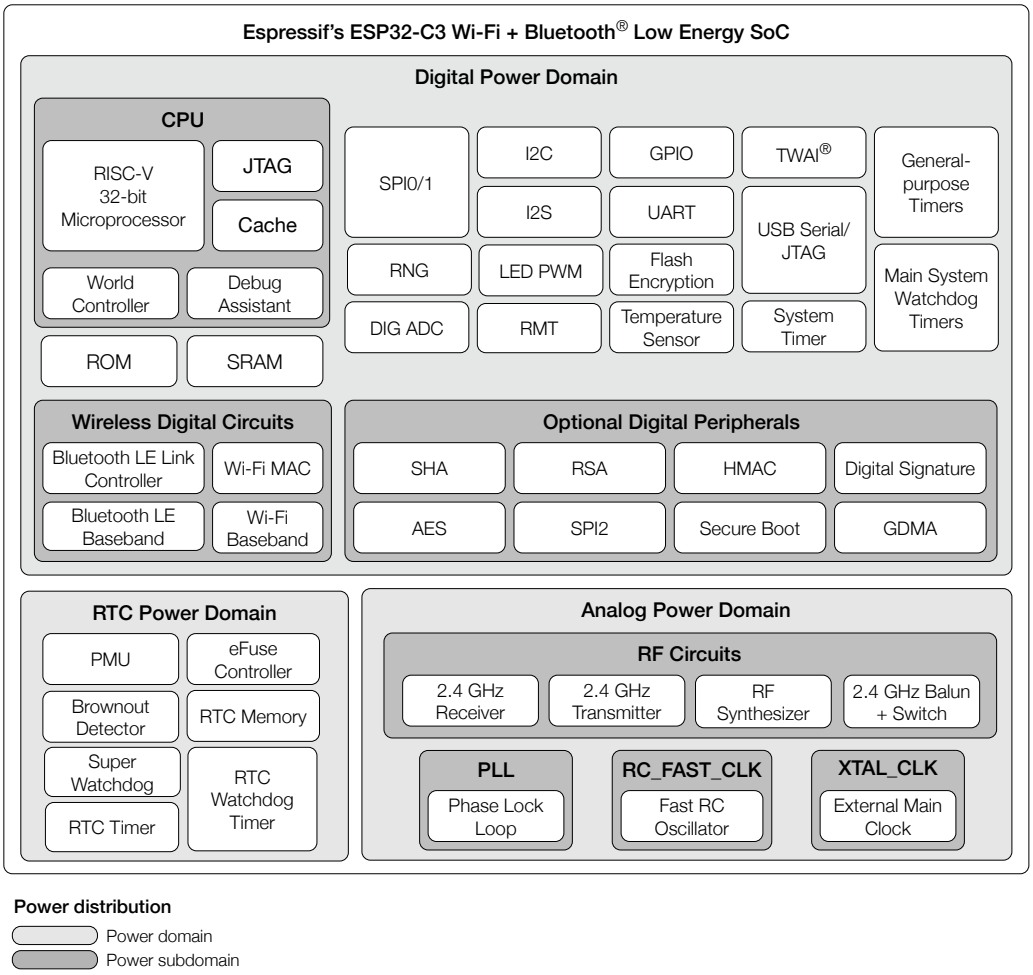


Figure 4-2. Components and Power Domains

Table 4-1. Components and Power Domains

Power Domain / Power Mode	RTC	Digital				Analog				
		CPU	Optional Digital Peripherals	Wireless Digital Circuits		FOSC_CLK	XTAL_CLK	PLL	RF Circuits
Active	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
Modem-sleep	ON	ON	ON	ON	ON[1]	ON	ON	ON	ON	OFF[2]
Light-sleep	ON	ON	OFF[1]	ON[1]	OFF[1]	ON	OFF	OFF	OFF	OFF[2]
Deep-sleep	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF

[1] Configurable, see the TRM.

[2] If Wireless Digital Circuits are on, RF circuits are period to keep active wireless connections running.

For detailed ESP32-C3 Technical Reference Manual Management (R

4.1.3 Timer Group

ESP32-C3 has two 54-bit general-purpose timers, which a auto-reload-capable up/down-timers.

The timers' features are summarized as follows:

- a 16-bit clock prescaler, from 1 to 65536
- a 54-bit time-base counter programmable to be increme
- able to read real-time value of the time-base counter
- halting and resuming the time-base counter
- programmable alarm generation
- level interrupt generation

For deta ESP32-C3 Technical Reference Manual > Chapter Timer Group (TIMG)

4.1.4 Watchdog Timers

For deta ESP32-C3 Technical Reference Manual > Chapter Watchdog Timers

Digital Watchdog Timers

ESP32-C3 contains three digital watchdog timers: one in Watchdog Timers, or MWDT) and one in the RTC module (calle

During the fash boot process, RWDT and the MWDT in timer g order to detect and recover from booting errors.

Digital watchdog timers have the following features:

- four stages, each with a programmable timeout value. E disabled separately
- interrupt, CPU reset, or core reset for MWDT upon expi or system reset for RWDT upon expiry of each stage
- 32-bit expiry counter
- write protection, to prevent RWDT and MWDT confgurati
- fash boot protection
  If the boot process from an SPI fash does not complete w watchdog will reboot the entire main system.

Analog Watchdog Timer

ESP32-C3 also has one analog watchdog timer: RTC super wa circuit in analog domain that helps to prevent the system system if required.

SWD has the following features:

- Ultra-low power

- Interrupt to indicate that the SWD timeout period is c
- Various dedicated methods for software to feed SWD, wh of the whole operating system

4.1.2 Permission Control

ESP32-C3 includes a Permission Controller (PMS), which peripherals) to two isolated environments, thereby real environments.

Feature List

- Independent access management in a privileged enviro
- Independent access management to internal memory, in
  - CPU access to internal memory
  - GDMA access to internal memory
- Independent access management to external memory, in
  - CPU to external memory via SPI1
  - CPU to external memory via Cache
- Independent access management to peripheral regions
  - CPU access to peripheral regions
  - Interrupt upon unsupported access alignment
- Address splitting for more flexible access management
- Register locks to secure the integrity of access manag
- Interrupt upon unauthorized access

For details, see Chapter 13 Permission Control (PMS in ESP32-C3 Technical Reference Manual.

4.1.3 System Registers

The System Registers in the ESP32-C3 chip are used to conf

Feature List

- Control system and memory
- Control clock
- Control software interrupt
- Control low-power management
- Control peripheral clock gating and reset

For details, see Chapter 14 System Registers (HP_SY in ESP32-C3 Technical Reference Manual.

4.1. Debug Assistant

The Debug Assistant provides a set of functions to help lo
offers various monitoring capabilities and logging feat
effciently.

Feature List

- Read/write monitoring: Monitors whether the CPU bus has read from
space. A detected read or write will trigger an interru
- Stack pointer (SP) monitoring: Monitors whether the SP exceeds the sp
bounds violation will trigger an interrupt.
- Program counter (PC) logging: Logs PC value. The developer can ge
recent CPU reset.
- Bus access: Records the information about bus access. W
specifed value, the Debug Assistant module will recor
and push the data to the SRAM.

For details, see Chapter 14 Debug Assistant (ASSIST
ESP32-C3 Technical Reference Manual).

4.1 Cryptography and Security Component

This subsection describes the security features incorpo
operations.

4.1.1 AES Accelerator

ESP32-C3 integrates an Advanced Encryption Standard (AE
speeds up computation using AES algorithm significantly,
software. The AES accelerator integrated in ESP32-C3 has
DMA-AES.

Feature List

- Typical AES working mode
  - AES-128/AES-256 encryption and decryption
- DMA-AES working mode
  - AES-128/AES-256 encryption and decryption
  - Block cipher mode
    * ECB (Electronic Codebook)
    * CBC (Cipher Block Chaining)
    * OFB (Output Feedback)
    * CTR (Counter)
    * CFB8 (8-bit Cipher Feedback)

* CFB128 (128-bit Cipher Feedback)

– Interrupt on completion of computation

For details, see Chapter AES Accelerator (AES) of ESP32-C3 Technical Reference Manual.

4.1.4 HMAC Accelerator

The HMAC Accelerator (HMAC) module is designed to comput the SHA-256 Hash algorithm and keys as described in RFC 2 computations, significantly reducing software complexi

Feature List

- Standard HMAC-SHA-256 algorithm
- Hash result only accessible by configurable hardware p
- Compatible to challenge-response authentication alg
- Generates required keys for the Digital Signature (DS
- Re-enables soft-disabled JTAG (in downstream mode)

For details, see Chapter HMAC Accelerator (HMAC) of ESP32-C3 Technical Reference Manual.

4.1.5 RSA Accelerator

The RSA accelerator provides hardware support for high-p asymmetric cipher algorithms, significantly improving t Compared with RSA algorithms implemented solely in soft algorithms significantly.

Feature List

- Large-number modular exponentiation with two option 3072 bits
- Large-number modular multiplication, operands width
- Large-number multiplication, operands width up to 15
- Operands of different widths
- Interrupt on completion of computation

For details, see Chapter RSA Accelerator (RSA) of ESP32-C3 Technical Reference Manual.

4.1.6 SHA Accelerator

The SHA Accelerator (SHA) is a hardware device that speed algorithm implemented solely in software. The SHA accel modes, which are Typical SHA and DMA-SHA.

Feature List

- The following hash algorithms are supported: SHA-1, SHA-224 and SHA-256 introduced in FIPS PUB 180-4.
  - SHA-1
  - SHA-224
  - SHA-256
- Two working modes
  - Typical SHA
  - DMA-SHA
- Interleaved function when working in Typical SHA work
- Interrupt function when working in DMA-SHA working mo

For more details, please see Chapter 20 SHA Accelerator (SH

4.1.20 Digital Signature

The Digital Signature (DS) module in the ESP32-C3 chip ge
hardware acceleration.

Feature List

- RSA digital signatures with key length up to 3072 bits
- Encrypted private key data, only decryptable by DS moc
- SHA-256 digest to protect private key data against tam

For more details, please see Chapter 21 Digital Signature

4.1.21 External Memory Encryption and Decryption

The External Memory Encryption and Decryption (XTS_AES)
for users' application code and data stored in the extern

Feature List

- General XTS_AES algorithm, compliant with IEEE Std 16
- Software-based manual encryption
- High-speed auto decryption, without software's part
- Encryption and decryption functions jointly determi
  and boot mode

For more details, please see Chapter 22 External Memory En
Decryption (XTS_AES)

4.1.14 Random Number Generator

The Random Number Generator (RNG) in the ESP32-C3 is a tru
32-bit random numbers for cryptographic operations from

Feature List

- RNG entropy source
  - Thermal noise from high-speed ADC or SAR ADC
  - An asynchronous clock mismatch

For more details about the Random Number Generator, see
Chapter Random Number Generator (RNG) in ESP32-C3 Technical Ref

4.2 Peripherals

This section describes the chip's peripheral capabiliti
that extend its functionality.

4.2.1 Connectivity Interface

This subsection describes the connectivity interfaces o
with external devices and networks.

4.2.1.1 UART Controller

ESP32-C3 has two UART interfaces, i.e. UART0 and UART1, w
communication (RS232 and RS485) at a speed of up to 5 Mbps
control (CTS and RTS signals) and software fow control (X
GDMA via UHCI0, and can be accessed by the GDMA controller

For detailed specifications of the UART Controller, see ESP32-C3 Technical Reference Manual.

Pin Assignment

The pins connected to transmit and receive UART signals (U0TXD and U0RXD) by default are GPIO21 ~ GPIO20 via IOMUX. Other signals can be routed to any available GPIO pins via GPIO Matrix.

For more information about the pin assignment, see Section 2.3.1 IO MUX and GPIO Matrix in ESP32-C3 Technical Reference Manual.

4.2.1.2 SPI Controller

ESP32-C3 has the following SPI interfaces:

- SPI0 used by ESP32-C3's GDMA controller and cache to acc
- SPI1 used by the CPU to access in-package or off-package
- SPI2 is a general purpose SPI controller with access to a

Features of SPI0 and SPI1

- Supports Single SPI, Dual SPI, and Quad SPI, QPI modes
- Configurable clock frequency with a maximum of 120 MHz
- Data transmission is in bytes

Features of SPI2

- Supports operation as a master or slave
- Connects to a DMA channel allocated by the GDMA contro
- Supports Single SPI, Dual SPI, and Quad SPI, QPI
- Configurable clock polarity (CPOL) and phase (CPHA)

- Configurable clock frequency
- Data transmission is in bytes
- Configurable read and write data bit order: most-signi
  first
- As a master
  - Supports 2-line full-duplex communication with cl
  - Supports 1-, 2-, 4-line half-duplex communication
  - Provides six SPI_CS pins for connection with six in
  - Configurable CS setup time and hold time
- As a slave
  - Supports 2-line full-duplex communication with cl
  - Supports 1-, 2-, 4-line half-duplex communication

For detailed information, see ESP32-C3 Technical Reference Manual > Chapter SPI Controller (SPI).

Pin Assignment

For SPI0/1, the pins are multiplexed with GPIO12 ~ GPIO17

For SPI2, the pins are multiplexed with GPIO2, GPIO4 ~ GP
MUX.

For more information about the pin assignment, see Secti
ESP32-C3 Technical Reference Manual > Chapter IO MUX and GPIO Matrix.

4.2.12 I2C Controller

ESP32-C3 has an I2C bus interface which is used for I2C ma
configuration. The I2C interface supports:

- standard mode (100 Kbit/s)
- fast mode (400 Kbit/s)
- up to 800 Kbit/s (constrained by SCL and SDA pull-up st
- 7-bit and 10-bit addressing mode
- double addressing mode
- 7-bit broadcast address

For detailed information, see ESP32-C3 Technical Reference Manual > Chapter I2C Controller (I2C).

Pin Assignment

The pins for I2C can be chosen from any GPIOs via the GPIO M

For more information about the pin assignment, see Secti
ESP32-C3 Technical Reference Manual > Chapter IO MUX and GPIO Matrix.

4.2.12 I2S Controller

ESP32-C3 includes a standard I2S interface. This interf
mode or half-duplex mode, and can be confgured for 8-bit,
clock frequency, from 10 kHz up to 40 MHz, is supported.

The I2S interface connects to the GDMA controller. The in
TDM standard, and PDM standard.

For deta ESP32-C3 Technical Reference Manual > Chapter I2S Controller (I2S)

Pin Assignment

The pins for the I2S Controller can be chosen from any GPI

For more information about the pin assignment, see Secti
ESP32-C3 Technical Reference Manual > Chapter IO MUX and GPIO Matrix

4.2.13 USB Serial/JTAG Controller

ESP32-C3 integrates a USB Serial/JTAG controller. This c

- CDC-ACM virtual serial port and JTAG adapter function
- USB 2.0 full speed compliant, capable of up to 12 Mbit/
  not support the faster 480 Mbit/s high-speed transfer
- programming in-package/off-package fash
- CPU debugging with compact JTAG instructions
- a full-speed USB PHY integrated in the chip

For deta ESP32-C3 Technical Reference Manual > Chapter USB Serial/JTAG Control
(USB_SERIAL_JTAG)

Pin Assignment

The pins for the USB Serial/JTAG Controller are multiple

For more information about the pin assignment, see Secti
ESP32-C3 Technical Reference Manual > Chapter IO MUX and GPIO Matrix

4.2.14 Two-wire Automotive Interface

ESP32-C3 has a TWAI® controller with the following features:

- compatible with ISO 11898-1 protocol (CAN Specifcati
- standard frame format (11-bit ID) and extended frame f
- bit rates from 1 Kbit/s to 1 Mbit/s
- multiple modes of operation: Normal, Listen Only, and
- 64-byte receive FIFO

- acceptance filter (single and dual filter modes)
- error detection and handling: error counters, configu arbitration lost capture

For deta ESP32-C3 Technical Reference Manual Chapter Two-wire Automotive Int

Pin Assignment

The pins for the Two-wire Automotive Interface can be cho

For more information about the pin assignment, see Secti ESP32-C3 Technical Reference Manual Chapter IO MUX and GPIO Matrix

4.2.11 LED PWM Controller

The LED PWM controller can generate independent digital controller:

- Can generate digital waveform with configurable perio can be up to 14 bits.
- Has multiple clock sources, including APB clock and e
- Can operate when the CPU is in Light-sleep mode.
- Supports gradual increase or decrease of duty cycle, w generator.

For deta ESP32-C3 Technical Reference Manual Chapter LED PWM Controller

Pin Assignment

The pins for the LED PWM Controller can be chosen from any

For more information about the pin assignment, see Secti ESP32-C3 Technical Reference Manual Chapter IO MUX and GPIO Matrix

4.2.12 Remote Control Peripheral

The Remote Control Peripheral (RMT) supports two channe channels of infrared remote reception. By controlling p infrared and other single-wire protocols. All four chann or receive waveform.

For more de ESP32-C3 Technical Reference Manual Chapter Remote Control Perip

Pin Assignment

The pins for the Remote Control Peripheral can be chosen f

For more information about the pin assignment, see Secti ESP32-C3 Technical Reference Manual Chapter IO MUX and GPIO Matrix

4.2 Analog Signal Processing

This subsection describes components on the chip that se

4.2.1 SAR ADC

ESP32-C3 integrates two 12-bit SAR ADCs.

- ADC1 supports measurements on 5 channels, and is facto
- ADC2 supports measurements on 1 channel, and is not fa

> Note:
> ADC2 of some chip revisions is not operational. See ESP32-C3 Series Errata for details.

For ADC characteristics, please refer to Table ADC Characteristics.

For more details, see ESP32-C3 Technical Reference Manual > Chapter On-Chip Sensors and Analog Signal Processing.

Pin Assignment

The pins for the SAR ADC are multiplexed with GPIO0 ~ GPIO external crystal or oscillator.

For more information about the pin assignment, see Section 2.3 IO Pins and ESP32-C3 Technical Reference Manual > Chapter IO MUX and GPIO Matrix.

4.2.2 Temperature Sensor

The temperature sensor generates a voltage that varies w via an ADC into a digital value.

The temperature sensor can output a range of temperature changes inside the chip. The temperature value depends o I/O load. Generally, the chip's internal temperature is

For more details, see ESP32-C3 Technical Reference Manual > Chapter On-Chip Sensors and Analog Signal Processing.

4.3 Wireless Communication

This section describes the chip's wireless communicatio
Bluetooth, and 802.15.4.

4.3.1 Radio

This subsection describes the fundamental radio technol
communication and data exchange. ESP32-C3 radio consist

- 2.4 GHz receiver
- 2.4 GHz transmitter
- bias and regulators
- balun and transmit-receive switch
- clock generator

4.3.2.1 2.4 GHz Receiver

The 2.4 GHz receiver demodulates the 2.4 GHz RF signal to c
to the digital domain with two high-resolution, high-spe
conditions, ESP32-C3 integrates RF filters, Automatic Ga
baseband filters.

4.3.2.2 2.4 GHz Transmitter

The 2.4 GHz transmitter modulates the quadrature baseban
antenna with a high-powered CMOS power amplifer. The use
of the power amplifer.

Additional calibrations are integrated to cancel any rad

- carrier leakage
- I/Q amplitude/phase matching
- baseband nonlinearities
- RF nonlinearities
- antenna matching

These built-in calibration routines reduce the cost, tim
testing.

4.3.3 Clock Generator

The clock generator produces quadrature clock signals of
components of the clock generator are integrated into the
regulators and dividers.

The clock generator has built-in calibration and self-t
are optimized on chip with patented calibration algorit
and the transmitter.

4.3 Wi-Fi

This subsection describes the chip's Wi-Fi capabilities
rate.

4.3.1 Wi-Fi Radio and Baseband

ESP32-C3 Wi-Fi radio and baseband support the following

- 802.11b/g/n
- 802.11n MCS0-7 that supports 20 MHz and 40 MHz bandwid
- 802.11n MCS32
- 802.11n 0.4 μs guard interval
- data rate up to 150 Mbps
- RX STBC (single spatial stream)
- adjustable transmitting power
- antenna diversity
  ESP32-C3 supports antenna diversity with an external
  more GPIOs, and used to select the best antenna to mini

4.3.2 Wi-Fi MAC

ESP32-C3 implements the full 802.11b/g/n Wi-Fi MAC prot
and SoftAP operations under the Distributed Control Fun
automatically with minimal host interaction to minimize

ESP32-C3 Wi-Fi MAC applies the following low-level prot

- 4 × virtual Wi-Fi interfaces
- infrastructure BSS in Station mode, SoftAP mode, Stat
- RTS protection, CTS protection, Immediate Block ACK
- fragmentation and defragmentation
- TX/RX A-MPDU, TX/RX A-MSDU
- transmit opportunity (TXOP)
- Wi-Fi multimedia (WMM)
- GCMP, CCMP, TKIP, WAPI, WEP, BIP, WPA2-PSK/WPA2-Enter
- automatic beacon monitoring (hardware TSF)
- 802.11mc FTM

4.3.2 Networking Features

Espressif provides libraries for TCP/IP networking, ESP protocols over Wi-Fi. TLS 1.0, 1.1 and 1.2 is also support

4.3 Bluetooth LE

This subsection describes the chip's Bluetooth capabili low-power, short-range applications. ESP32-C3 include hardware link layer controller, an RF/modem block and a f core features of Bluetooth 5 and Bluetooth mesh.

4.3.1 Bluetooth LE PHY

Bluetooth Low Energy radio and PHY in ESP32-C3 support:

- 1 Mbps PHY
- 2 Mbps PHY for higher data rates
- coded PHY for longer range (125 Kbps and 500 Kbps)
- HW Listen before talk (LBT)

4.3.2 Bluetooth LE Link Controller

Bluetooth Low Energy Link Layer Controller in ESP32-C3 s

- LE advertising extensions, to enhance broadcasting c
- multiple advertisement sets
- simultaneous advertising and scanning
- multiple connections in simultaneous central and per
- adaptive frequency hopping and channel assessment
- LE channel selection algorithm #2
- connection parameter update
- high duty cycle non-connectable advertising
- LE privacy 1.2
- LE data packet length extension
- link layer extended scanner filter policies
- low duty cycle directed advertising
- link layer encryption
- LE Ping

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Stresses above those listed in Table 5-1 Absolute Maximum Ratings may cause permanent dan
device. These are stress ratings only and normal operati
beyond those indicated in Section 5.2 Recommended Operating Conditions is not implied. Ex
absolute-maximum-rated conditions for extended period

Table 5-1. Absolute Maximum Ratings

Parameter	Description	Min	Max	Unit
Input power pins[1]	Allowed input voltage	0	3.6	V
I_{output}[2]	Cumulative IO output current	–	1000	mA
T_{STORE}	Storage temperature	-40	150	°C

[1] For more information on input power pins, see Section 2.4 Power Supply.
[2] The product proved to be fully functional after
while being connected to ground for 24 consecuti
ature of 25 °C.

5.2 Recommended Operating Conditions

For recommended ambient temperature of ESP32-C3 series, see Section 1 Comparison

Table 5-2. Recommended Operating Conditi

Parameter[1]	Description	Min	Typ	Max	Unit
VDDA, VDD3P3, VDD3P3_RTC	Recommended input voltage	3.0	3.3	3.6	V
VDD3P3_CPU[2][3]	Recommended input voltage	3.0	3.3	3.6	V
VDD_SPI (as input)		3.0	3.3	3.6	V
I_{VDD}	Cumulative input current	0.5	–	–	A

[1] See in conjunction with Section 2.4 Power Supply.
[2] If writing to eFuses, the voltage on VDD3P3_CPU sho
responsible for burning eFuses are sensitive to hig
[3] If VDD3P3_CPU is used to power VDD_SPI (see Section 2.5.2 VDD_SPI Power Source), the
drop on R_{SPI} should be accounted for. See also Section 5.3.3 VDD_SPI Output Characteristics.

5.3 VDD_SPI Output Characteristics

Table 5-3. VDD_SPI Internal and Output Char

Param	Description[1]	Typ	Unit
R_{SPI}	VDD_SPI powered by VDD3P3_CPU via R_{SPI} for 3.3 V flash_CPU[2]	7.5	Ω

[1] See in conjunction with 2.5.2 Power Scheme.

[2] VDD3P3_CPU must be > VDD_flash_min + $I_{flash\_max} * R_{SPI}$, where

- VDD_flash_min – minimum operating voltage of flash_
- I_flash_max – maximum operating current of flash_CI

5.4 DC Characteristics (3.3 V, 25 °C)

Table 5-4. DC Characteristics (3.3 V, 25

Param	Description	Min	Typ	Max	Unit
C_{IN}	Pin capacitance	—	2	—	pF
V_{IH}	High-level input voltage	0.75 × VDD[1]	—	VDD[1] + 0.3	V
V_{IL}	Low-level input voltage	0.3	—	0.25 × VDD[1]	V
I_{IH}	High-level input current	—	—	50	nA
I_{IL}	Low-level input current	—	—	50	nA
V_{OH}[2]	High-level output voltage	0.8 × VDD[1]	—	—	V
V_{OL}[2]	Low-level output voltage	—	—	0.1 × VDD[1]	V
I_{OH}	High-level source current (VDD[1] = 3.3 V, V_{OH} >= 2.64 V, PAD_DRIVER = 3)	—	40	—	mA
I_{OL}	Low-level sink current (VDD[1] = 3.3 V, V_{OL} = 0.495 V, PAD_DRIVER = 3)	—	28	—	mA
R_{PU}	Internal weak pull-up resistor	—	45	—	kΩ
R_{PD}	Internal weak pull-down resistor	—	45	—	kΩ
V_{IH_nRST}	Chip reset release voltage (CHIP_EN voltage is within the specifed range)	0.75 × VDD[1]	—	VDD[1] + 0.3	V
V_{IL_nRST}	Chip reset voltage (CHIP_EN voltage is within the specifed range)	0.3	—	0.25 × VDD[1]	V

[1] VDD – voltage from a power pin of a respective power doma

[2] V_{OH} and V_{OL} are measured using high-impedance load.

5.5 ADC Characteristics

Table 5-5. ADC Characteristics

Symbol	Parameter	Min	Max	Unit
DNL (Differential nonlinearity)[1]	ADC connected to an external 100 nF capacitor; DC signal input; Ambient temperature at 25 °C; Wi-Fi off	7	7	LSB
INL (Integral nonlinearity)		12	12	LSB
Sampling rate	—	—	100	kSPS[2]

[1] To get better DNL results, you can sample multiple ti
value.

[2] kSPS means kilo samples-per-second.

The calibrated ADC results after hardware calibration and software calibration are shown in Table 5-6. For higher accuracy, you may implement your own calibration

Table 5-6. ADC Calibration Results

Parameter	Description	Min	Max	Unit
Total error	ATTEN0, effective measurement range of 0 ~ 750	10	10	mV
	ATTEN1, effective measurement range of 0 ~ 1050	10	10	mV
	ATTEN2, effective measurement range of 0 ~ 1300	10	10	mV
	ATTEN3, effective measurement range of 0 ~ 2500	35	35	mV

5.6 Current Consumption

5.6.1 RF Current Consumption in Active Mode

The current consumption measurements are taken with a 3.
RF port. All transmitters' measurements are based on a 10

Table 5-7. Wi-Fi Current Consumption Dependi

Work Mode[1]	Description		Peak (mA)
Active (RF working)	TX	802.11b, 1 Mbps, @21 dBm	335
		802.11g, 54 Mbps, @19 dBm	285
		802.11n, HT20, MCS7, @18.5 dBm	276
		802.11n, HT40, MCS7, @18.5 dBm	278
	RX	802.11b/g/n, HT20	84
		802.11n, HT40	87

5.6. Current Consumption in Other Modes

Table 5-8. Current Consumption in Modem-sle

Mode	CPU Frequency (MHz)	Description	Typ All Peripherals Disabled	Typ All Peripherals Enabled[1] (mA)
Modem-sleep[2][3]	160	CPU is running	23	28
		CPU is idle	16	21
	80	CPU is running	17	22
		CPU is idle	13	18

[1] In practice, the current consumption might be differen
[2] In Modem-sleep mode, Wi-Fi is clock gated.
[3] In Modem-sleep mode, the consumption might be higher w 80 Mbit/s, in SPI 2-line mode the consumption is 10 mA.

Table 5-9. Current Consumption in Low-Power

Mode	Description	Typ (μA)
Light-sleep	VDD_SPI and Wi-Fi are powered down, and a 13 GPIO	
Deep-sleep	RTC timer + RTC memory	5
Power off	CHIP_EN is set to low level, the chip is powered o	1

5.7. Reliability

Table 5-10. Reliability Qualifcations

Test Item	Test Conditions	Test Standard
HTOL (High Temperature Operating Life)	125 °C, 1000 hours	JESD22-A108
ESD (Electro-Static Discharge Sensitivity)	HBM (Human Body Model)[1] ± 2000 V	JS-001
	CDM (Charged Device Model)[2] ± 1000 V	JS-002
Latch up	Current trigger ± 200 mA	JESD78
	Voltage trigger $1.5 \times V_{DD\,max}$	
Precondition	Bake 24 hours @125 °C Moisture soak (level 3: 192 hours @30 °C, 60 IR reflow solder: 260 + 0 °C, 20 seconds, thre	J-STD-020, JES JESD22-A113
TCT (Temperature Cycling Test)	65 °C / 150 °C, 500 cycles	JESD22-A104
uHAST (Highly Accelerated Stress Test, unbiased)	130 °C, 85% RH, 96 hours	JESD22-A118
HTSL (High Temperature Storage Life)	150 °C, 1000 hours	JESD22-A103

Cont'd on ne

Table 5-10 – cont'd from previous page

Test Item	Test Conditions	Test Standard
LTSL (Low Temperature Storage Life)	40 °C, 1000 hours	JESD22-A119

[1] JEDEC document JEP155 states that 500 V HBM allows safe mar
[2] JEDEC document JEP157 states that 250 V CDM allows safe mar

6 RF Characteristics

This section contains tables with RF characteristics of

The RF data is measured at the antenna port, where RF cabl
front-end circuit is 0

Devices should operate in the center frequency range all
center frequency range and the target transmit power in
Test Guide for instructions.

Unless otherwise stated, the RF tests are conducted with

6.1 Wi-Fi Radio

Table 6-1. Wi-Fi Frequency

Parameter	Min (MHz)	Typ (MHz)	Max (MHz)
Center frequency of operating channel	2412	—	2484

6.1.1 Wi-Fi RF Transmitter (TX) Characteristics

Table 6-2. TX Power with Spectral Mask and EVM Mee

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	21.0	—
802.11b, 11 Mbps	—	21.0	—
802.11g, 6 Mbps	—	21.0	—
802.11g, 54 Mbps	—	19.0	—
802.11n, HT20, MCS0	—	20.0	—
802.11n, HT20, MCS7	—	18.5	—
802.11n, HT40, MCS0	—	20.0	—
802.11n, HT40, MCS7	—	18.5	—

Table 6-3. TX EVM Test

Rate	Min (dBm)	Typ (dBm)	SL[1] (dB)
802.11b, 1 Mbps, @21 dBm	—	24.5	10
802.11b, 11 Mbps, @21 dBm	—	25.0	10
802.11g, 6 Mbps, @21 dBm	—	23.0	5
802.11g, 54 Mbps, @19 dBm	—	27.5	25
802.11n, HT20, MCS0, @20 dBm	—	22.5	5

Cont'd on next page

Table 6-3 – cont'd from previous page

Rate	Min (dB	Typ (dB	SL[1] (dB)
802.11n, HT20, MCS7, @18	—	5	0 27
802.11n, HT40, MCS0, @20	—	dB	2 5 5
802.11n, HT40, MCS7, @18	—	5	0 27

[1] SL stands for standard limit value.

6.1 Wi-Fi RF Receiver (RX) Characteristics

Table 6-4. RX Sensitivity

Rate	Min (dBr	Typ (dBr	Max (dBm)
802.11b, 1 Mbps	—	98.4	—
802.11b, 2 Mbps	—	96.0	—
802.11b, 5.5 Mbps	—	93.0	—
802.11b, 11 Mbps	—	88.6	—
802.11g, 6 Mbps	—	93.8	—
802.11g, 9 Mbps	—	92.2	—
802.11g, 12 Mbps	—	91.0	—
802.11g, 18 Mbps	—	88.4	—
802.11g, 24 Mbps	—	85.8	—
802.11g, 36 Mbps	—	82.0	—
802.11g, 48 Mbps	—	78.0	—
802.11g, 54 Mbps	—	76.6	—
802.11n, HT20, MCS0	—	93.6	—
802.11n, HT20, MCS1	—	90.8	—
802.11n, HT20, MCS2	—	88.4	—
802.11n, HT20, MCS3	—	85.0	—
802.11n, HT20, MCS4	—	81.8	—
802.11n, HT20, MCS5	—	77.8	—
802.11n, HT20, MCS6	—	76.0	—
802.11n, HT20, MCS7	—	74.8	—
802.11n, HT40, MCS0	—	90.0	—
802.11n, HT40, MCS1	—	88.0	—
802.11n, HT40, MCS2	—	85.2	—
802.11n, HT40, MCS3	—	82.0	—
802.11n, HT40, MCS4	—	78.8	—
802.11n, HT40, MCS5	—	74.6	—
802.11n, HT40, MCS6	—	73.0	—
802.11n, HT40, MCS7	—	71.4	—

Table 6-5. Maximum RX Level

Rate	Min (dBr	Typ (dBr	Max (dBm)
802.11b, 1 Mbps	—	5	—
802.11b, 11 Mbps	—	5	—
802.11g, 6 Mbps	—	5	—
802.11g, 54 Mbps	—	0	—
802.11n, HT20, MCS0	—	5	—
802.11n, HT20, MCS7	—	0	—
802.11n, HT40, MCS0	—	5	—
802.11n, HT40, MCS7	—	0	—

Table 6-6. RX Adjacent Channel Rejectio

Rate	Min (dB	Typ (dB	Max (dB)
802.11b, 1 Mbps	—	35	—
802.11b, 11 Mbps	—	35	—
802.11g, 6 Mbps	—	31	—
802.11g, 54 Mbps	—	20	—
802.11n, HT20, MCS0	—	31	—
802.11n, HT20, MCS7	—	16	—
802.11n, HT40, MCS0	—	25	—
802.11n, HT40, MCS7	—	11	—

6.2 Bluetooth 5 (LE) Radio

Table 6-7. Bluetooth LE Frequency

Parameter	Min (MHz	Typ (MHz	Max (MHz)
Center frequency of operating channel	2402	—	2480

6.2.1 Bluetooth LE RF Transmitter (TX) Characteri

Table 6-8. Transmitter Characteristics - Bl

Parameter	Description	Min	Typ	Max	Unit
RF transmit power	RF power control range	-24.00	0	20.00	dBm
	Gain control step	—	3.00	—	dB
Carrier frequency offset and drift	Max $\lvert f_n \rvert_{n=0,\,1,\,2,\,..k}$	—	17.00	—	kHz
	Max $\lvert f_0 - f_n \rvert$	—	1.75	—	kHz
	Max $\lvert f_n - f_{n-5} \rvert$	—	1.46	—	kHz

Cont'd on nex

Table 6-8 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
	$\lvert f_1 - f_0 \rvert$	—	0.80	—	kHz
Modulation characteristics	$\Delta f1_{avg}$	—	250.00	—	kHz
	Min $\Delta f2_{max}$ (for at least 99.9% of all $\Delta f2_{max}$)	—	190.00	—	kHz
	$\Delta f2_{avg} / \Delta f1_{avg}$	—	0.83	—	—
In-band spurious emissions	± 2 MHz offset	—	37.62	—	dBm
	± 3 MHz offset	—	41.95	—	dBm
	> ± 3 MHz offset	—	44.48	—	dBm

Table 6-9. Transmitter Characteristics - Blu

Parameter	Description	Min	Typ	Max	Unit
RF transmit power	RF power control range	0	20.00		dBm
	Gain control step	—	3.00	—	dB
Carrier frequency offset and drift	Max $\lvert f_n \rvert_{n=0, 1, 2, ..k}$	—	20.80	—	kHz
	Max $\lvert f_0 - f_n \rvert$	—	1.30	—	kHz
	Max $\lvert f_n - f_{n-5} \rvert$	—	1.33	—	kHz
	$\lvert f_1 - f_0 \rvert$	—	0.70	—	kHz
Modulation characteristics	$\Delta f1_{avg}$	—	498.00	—	kHz
	Min $\Delta f2_{max}$ (for at least 99.9% of all $\Delta f2_{max}$)	—	430.00	—	kHz
	$\Delta f2_{avg} / \Delta f1_{avg}$	—	0.93	—	—
In-band spurious emissions	± 4 MHz offset	—	43.55	—	dBm
	± 5 MHz offset	—	45.26	—	dBm
	> ± 5 MHz offset	—	45.26	—	dBm

Table 6-10. Transmitter Characteristics - Bl

Parameter	Description	Min	Typ	Max	Unit
RF transmit power	RF power control range	0	20.00		dBm
	Gain control step	—	3.00	—	dB
Carrier frequency offset and drift	Max $\lvert f_n \rvert_{n=0, 1, 2, ..k}$	—	17.50	—	kHz
	Max $\lvert f_0 - f_n \rvert$	—	0.45	—	kHz
	$\lvert f_n - f_{n-3} \rvert$	—	0.70	—	kHz
	$\lvert f_0 - f_3 \rvert$	—	0.30	—	kHz
Modulation characteristics	$\Delta f1_{avg}$	—	250.00	—	kHz
	Min $\Delta f1_{max}$ (for at least 99.9% of all $\Delta f2_{max}$)	—	235.00	—	kHz
In-band spurious emissions	± 2 MHz offset	—	37.90	—	dBm
	± 3 MHz offset	—	41.00	—	dBm
	> ± 3 MHz offset	—	42.50	—	dBm

Table 6-11. Transmitter Characteristics - Bl

Parameter	Description	Min	Typ	Max	Unit
RF transmit power	RF power control range	-24.00	0	20.00	dBm
	Gain control step	—	3.00	—	dB
Carrier frequency offset and drift	Max $\lvert f_n \rvert_{n=0,1,2,..k}$	—	17.00	—	kHz
	Max $\lvert f_0 - f_n \rvert$	—	0.88	—	kHz
	$\lvert f_n - f_{n-3} \rvert$	—	1.00	—	kHz
	$\lvert f_0 - f_3 \rvert$	—	0.20	—	kHz
Modulation characteristics	$\Delta f2_{avg}$	—	208.00	—	kHz
	Min $\Delta f2_{max}$ (for at least 99.9% of $\Delta f2_{all}$)	—	190.00	—	kHz
In-band spurious emissions	± 2 MHz offset	—	37.90	—	dBm
	± 3 MHz offset	—	41.30	—	dBm
	> ± 3 MHz offset	—	42.80	—	dBm

6.2. Bluetooth LE RF Receiver (RX) Characterist

Table 6-12. Receiver Characteristics - Blue

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	-97	—	dBm
Maximum received signal @30.8% PER	—	—	5	—	dBm
Co-channel C/I	—	—	8	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	3	—	dB
	F = F0 – 1 MHz	—	4	—	dB
	F = F0 + 2 MHz	—	29	—	dB
	F = F0 – 2 MHz	—	31	—	dB
	F = F0 + 3 MHz	—	33	—	dB
	F = F0 – 3 MHz	—	27	—	dB
	F ≥ F0 + 4 MHz	—	29	—	dB
	F ≤ F0 – 4 MHz	—	38	—	dB
Image frequency	—	—	29	—	dB
Adjacent channel to image frequency	$F = F_{image} + 1$ MHz	—	41	—	dB
	$F = F_{image} - 1$ MHz	—	33	—	dB
Out-of-band blocking performance	30 MHz–2000 MHz	—	-5	—	dBm
	2003 MHz–2399 MHz	—	-18	—	dBm
	2484 MHz–2997 MHz	—	-15	—	dBm
	3000 MHz–12.75 GHz	—	-5	—	dBm
Intermodulation	—	—	-30	—	dBm

Table 6-13. Receiver Characteristics - Blue

Parameter	Description	Min	Typ	Max	Unit
Sensitivity@30.8% PER	—	—	-93	—	dBm
Maximum received signal@30.8% PER	—	—	3	—	dBm
Co-channel C/I	—	—	10	—	dB
Adjacent channel selectivity C/I	F = F0 + 2 MHz	—	7	—	dB
	F = F0 – 2 MHz	—	7	—	dB
	F = F0 + 4 MHz	—	28	—	dB
	F = F0 – 4 MHz	—	26	—	dB
	F = F0 + 6 MHz	—	26	—	dB
	F = F0 – 6 MHz	—	27	—	dB
	F ≥ F0 + 8 MHz	—	29	—	dB
	F ≤ F0 – 8 MHz	—	28	—	dB
Image frequency	—	—	28	—	dB
Adjacent channel to image frequency	$F = F_{image}$ + 2 MHz	—	26	—	dB
	$F = F_{image}$ – 2 MHz	—	7	—	dB
Out-of-band blocking performance	30 MHz–2000 MHz	—	-5	—	dBm
	2003 MHz–2399 MHz	—	-19	—	dBm
	2484 MHz–2997 MHz	—	-16	—	dBm
	3000 MHz–12.75 GHz	—	-5	—	dBm
Intermodulation	—	—	-29	—	dBm

Table 6-14. Receiver Characteristics - Blue

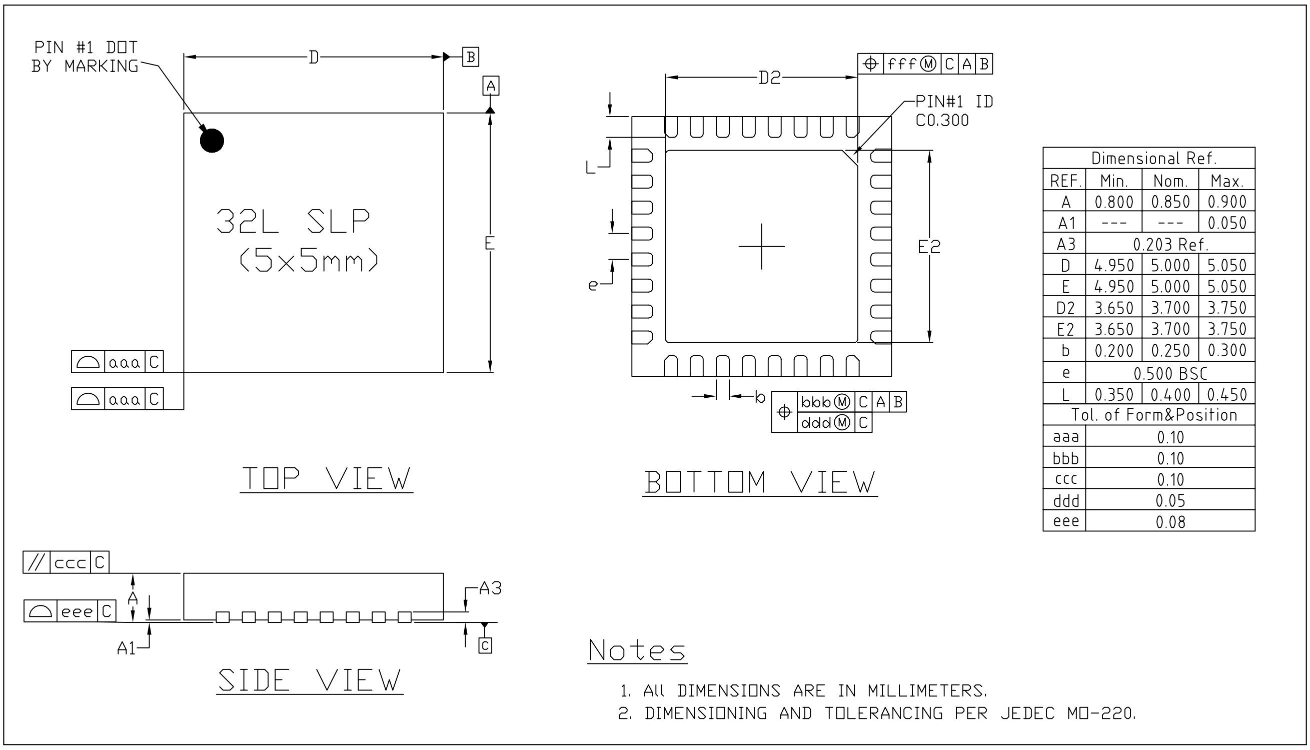
Parameter	Description	Min	Typ	Max	Unit
Sensitivity@30.8% PER	—	—	-105	—	dBm
Maximum received signal@30.8% PER	—	—	5	—	dBm
Co-channel C/I	—	—	3	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	6	—	dB
	F = F0 – 1 MHz	—	6	—	dB
	F = F0 + 2 MHz	—	33	—	dB
	F = F0 – 2 MHz	—	43	—	dB
	F = F0 + 3 MHz	—	37	—	dB
	F = F0 – 3 MHz	—	47	—	dB
	F ≥ F0 + 4 MHz	—	40	—	dB
	F ≤ F0 – 4 MHz	—	50	—	dB
Image frequency	—	—	40	—	dB
Adjacent channel to image frequency	$F = F_{image}$ + 1 MHz	—	50	—	dB
	$F = F_{image}$ – 1 MHz	—	37	—	dB

Table 6-15. Receiver Characteristics - Bluet

Parameter	Description	Min	Typ	Max	Unit
Sensitivity@30.8% PER	—	—	100	—	dBm
Maximum received signal@30.8% PER	—	—	5	—	dBm
Co-channel C/I	—	—	3	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	2	—	dB
	F = F0 – 1 MHz	—	3	—	dB
	F = F0 + 2 MHz	—	32	—	dB
	F = F0 – 2 MHz	—	33	—	dB
	F = F0 + 3 MHz	—	23	—	dB
	F = F0 – 3 MHz	—	40	—	dB
	F≥ F0 + 4 MHz	—	34	—	dB
	F≤ F0 – 4 MHz	—	44	—	dB
Image frequency	—	—	34	—	dB
Adjacent channel to image frequency	$F = F_{image}$ + 1 MHz	—	46	—	dB
	$F = F_{image}$ – 1 MHz	—	23	—	dB

7 Packaging

- For information about tape, reel and chip marking, please refer to ESP32-C3 Chip Packaging Information.
- The pins of the chip are numbered in anti-clockwise order … For pin numbers and pin names, see also Figure 2-1 ESP32-C3 Series Pin Layout … FH4, and ESP32-C … (Top View).
- The recommended land pattern source file (dxf) is available for download. You can view it with Autodesk Viewer.
- For reference PCB layout, please refer to ESP32-C3 Hardware Design Guidelines.



Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.800	0.850	0.900
A1	---	---	0.050
A3	0.203 Ref.		
D	4.950	5.000	5.050
E	4.950	5.000	5.050
D2	3.650	3.700	3.750
E2	3.650	3.700	3.750
b	0.200	0.250	0.300
e	0.500 BSC		
L	0.350	0.400	0.450
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

Figure 7-1. QFN32 (5×5 mm) Package

Appendix A – ESP32-C3 Consolidated Pin Overview

Pin No	Pin Name	Pin Type	Pin Providing Power	Pin Setting		Analog Function		IOMUX Function					
				At Reset	After Reset	0	1	0	Type	1	Type	2	Type
1	LNA_IN	Analog											
2	VDD3P3	Power											
3	VDD3P3	Power											
4	XTAL_32K_P	IO	VDD3P3_RTC			XTAL_32K_P	ADC1_CH0	GPIO0	I/O/T	GPIO0	I/O/T		
5	XTAL_32K_N	IO	VDD3P3_RTC			XTAL_32K_N	ADC1_CH1	GPIO1	I/O/T	GPIO1	I/O/T		
6	GPIO2	IO	VDD3P3_RTC	IE	IE		ADC1_C	GPIO	I/O	GPIO	I/O	FSPIQ	I1/O/T
7	CHIP_EN	Analog											
8	GPIO3	IO	VDD3P3_RTC	IE	IE		ADC1_CH3	GPIO3	I/O/T	GPIO3	I/O/T		
9	MTMS	IO	VDD3P3_RTC		IE		ADC1_C	MTMS	I1	GPIO	I/O	FSPIH	I1/O/T
10	MTDI	IO	VDD3P3_RTC		IE		ADC2_C	MTDI	I1	GPIO	I/O	FSPIW	I1/O/T
11	VDD3P3_RTC	Power											
12	MTCK	IO	VDD3P3_CPU		IE			MTCK	I1	GPIO	I/O	FSPIC	I1/O/T
13	MTDO	IO	VDD3P3_CPU		IE			MTDO	O/T	GPIO	I/O	FSPID	I1/O/T
14	GPIO8	IO	VDD3P3_CPU	IE	IE			GPIO	I/O	GPIO	I/O		
15	GPIO9	IO	VDD3P3_CPU	IE, WPU	IE, WPU			GPIO	I/O	GPIO	I/O		
16	GPIO10	IO	VDD3P3_CPU		IE			GPIO	I0/O/T	GPIO	I0/O/T	FSPICS0	I1/O/T
17	VDD3P3_CPU	Power											
18	VDD_SPI	Power	VDD3P3_CPU					GPIO	I1/O/T	GPIO	I1/O/T		
19	SPIHD	IO	VDD_SPI / VDD3P3_CPU	WPU	IE, WPU			SPIHD	I1/O/T	GPIO	I/O		
20	SPIWP	IO	VDD_SPI / VDD3P3_CPU	WPU	IE, WPU			SPIWP	I1/O/T	GPIO	I/O		
21	SPICS0	IO	VDD_SPI / VDD3P3_CPU	WPU	IE, WPU			SPICS0	O/T	GPIO	I/O		
22	SPICLK	IO	VDD_SPI / VDD3P3_CPU	WPU	IE, WPU			SPICLK	O/T	GPIO	I/O		
23	SPID	IO	VDD_SPI / VDD3P3_CPU	WPU	IE, WPU			SPID	I1/O/T	GPIO	I/O		
24	SPIQ	IO	VDD_SPI / VDD3P3_CPU	WPU	IE, WPU			SPIQ	I1/O/T	GPIO	I/O		
25	GPIO18	IO	VDD3P3_CPU			USB_D-		GPIO	I/O	GPIO	I/O		
26	GPIO19	IO	VDD3P3_CPU			USB_D+		GPIO	I/O	GPIO	I/O		
27	U0RXD	IO	VDD3P3_CPU		IE, WPU			U0RXD	I1	GPIO	I/O		
28	U0TXD	IO	VDD3P3_CPU		WPU			U0TXD	O	GPIO	I/O		
29	XTAL_N	Analog											
30	XTAL_P	Analog											
31	VDDA	Power											
32	VDDA	Power											
33	GND	Power											

* For details, see Section 2.3.3 Restrictions for GPIOs

Related Documentation and Resou

Related Documentation

- ESP32-C3 Technical Reference Manual – Detailed information on how to use the erals.
- ESP32-C3 Hardware Design Guidelines – Guidelines on how to integrate the ESI uct.
- ESP32-C3 Series SoC Errata – Descriptions of known errors in ESP32-C3 se
- Certifcates
  https://espressif.com/en/support/documents/certif
- ESP32-C3 Product/Process Change Notifcations (PCN)
  https://espressif.com/en/support/documents/pcns?l
- ESP32-C3 Advisories – Information on security, bugs, compatibility,
  https://espressif.com/en/support/documents/advisc
- Documentation Updates and Update Notifcation Subscri
  https://espressif.com/en/support/download/documer

Developer Zone

- ESP-IDF Programming Guide for ESP32-C3 – Extensive documentation for the ESI
- ESP-IDF and other development frameworks on GitHub.
  https://github.com/espressif
- ESP32 BBS Forum – Engineer-to-Engineer (E2E) Community for Espre
  share knowledge, explore ideas, and help solve problems wit
  https://esp32.com/
- The ESP Journal – Best Practices, Articles, and Notes from Espress
  https://blog.espressif.com/
- See the SDKs and Demos, APPs, Tools, AT Firmware
  https://espressif.com/en/support/download/sdks-de

Products

- ESP32-C3 Series SoCs – Browse through all ESP32-C3 SoCs.
  https://espressif.com/en/products/socs?id=ESP32-C
- ESP32-C3 Series Modules – Browse through all ESP32-C3-based modules.
  https://espressif.com/en/products/modules?id=ESP3
- ESP32-C3 Series DevKits – Browse through all ESP32-C3-based devkits.
  https://espressif.com/en/products/devkits?id=ESP3
- ESP Product Selector – Find an Espressif hardware product suitable fo
  https://products.espressif.com/#/product-selecto

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Revision History

Date	Versi	Release notes
2024-09	v1.9	Updated pin layout and the number of GPIOs PCN20240702 Upgrade ESP32-C3FH4X Product
2024-07	v1.8	• Removed the ESP32-C3FH4XAZ variant and Compatib Advisory for ESP32-C3 Chip Revision v1.1 in Chapter 1 ESP32-C3 Se Comparison • Updated the default driving s 2.1 Pin Overview > Note 4 • Added flash erase cycles, retention tim Section 4.1.2.1 Internal Memory • Improved the formatting, structure, an – Section 2 Pins – Section 3 Boot Configu (used to be named as Pins") – Section 4 Functional Description • Other minor updates
2024-04	v1.7	• Marked the ESP32-C3FN4 variant as end o • Marked the ESP32-C3FH4AZ variant as NRND • Marked the ESP32-C3FH4X variant as rec
2024-01	v1.6	• Added the new ESP32-C3FH4X and ESP32-C to 1 ESP32-C3 Series Comparison • Corrected the PWM duty resolution to 4.2.1.4 LED PWM Controller

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Date	Version	Release notes
2023-08	v1.5	• Marked ESP32-C3FN4 as NRND • Improved the content in the following s – Section 1 Product Overview – Section 2 Pins – Section 4.1.3.6 Power Management Unit – Section 4.2.1.2 SPI Controller – Section 5.1 Absolute Maximum Ratings – Section 5.2 Recommended Operating Condit – Section 5.3 VDD_SPI Output Characteristic – Section 5.5 ADC Characteristics • Added Appendix A • Updated the maximum value of "RF power Section 6.2 Bluetooth 5 (LE) Radio • Other minor updates
2022-12	v1.4	• Deleted feature "Antenna diversity" fr 4.3.1.1 • Deleted feature "Supports external pow • Updated the glitch type of GPIO18 to h Pin Overview
2022-11	v1.3	• Updated notes in Pin Overview Table • Added links to the Technical Reference figurations in Chapter 4 Functional Description • Added a note about ADC2 erratum in Section 4.2.2.1 ADC • Updated Section 4.1.3.8 Watchdog Timers • Added Table ADC Characteristics • Updated Section 5.6.2 Current Consumption in Othe • Updated RF transmit power in Section 6.2 Bluetooth 5 (LE) R • Updated the typical ... in Section 7 Packaging • Updated Chapter Related Documentation and Res
2022-04	v1.2	• Added a new chip variant ESP32-C3FH4AZ • Updated Figure ESP32-C3 Functional Block Diag • Added the wakeup source for Deep-sleep in Section 4.1.3.6 Power Management Unit

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Date	Version	Release notes
2021-10-26	v1.1	• Updated Figure 1 ESP32-C3 Functional Block Diagram to show power modes; • Added CoreMark score in Features; • Updated Table Pin Description to show d... • Updated Figure ESP32-C3 Power Scheme and the related descr... • Added Table SPI Signals; • Added note 3 to Table Recommended Operating Cond...; • Other updates to wording.
2021-05-28	v1.0	• Updated power modes; • Updated Section 3 Boot Configurations; • Updated some clock names and their f... 4.1.3 ... Clock; • Added clarifcation about ADC1 and ADC2 ... 4.2.1 SAR ADC; • Updated the default configuration of U0... Table IO MUX; • Updated sampling ... in Table ADC Characteristics; • Updated Table Reliability; • Added the link to recommended PCB land pattern in 7 Package ...
2021-04-23	v0.8	Updated Wi-Fi Radio and Bluetooth 5 (LE) Radio.
2021-04-07	v0.7	• Updated information about USB Serial/JTAG Controll...; • Added GPIO2 to Section 3 Boot Configurations; • Updated Figure Address Mapping Structure; • Added Table IO MUX and Table ... in Section 4.1.3 IO MUX and GPIO Matrix; • Updated information about SPI2 in Section 4.2.1 ...; • Updated fixed-priority channel ... in 4.1.1 GDMA Controller; • Updated Table Reliability.
2021-01-18	v0.6	• Clarifed that of the 400 KB SRAM, 16 KB i... • Updated maximum value to standard ... Wi-Fi RF Transmitter (TX) Characteristics in Section 6.1 Wi-Fi RF Transmitter Characteristics.

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Date	Versi	Release notes
2021-01-15	v1.0 3.5	• Updated information about Wi-Fi; • Added connection between in-package fa notes in Section Pin Definitions; • Updated ESP32-C3 Power Consumption in Modem-sleep Mode, added Figure Typical Timing Parameters for Power Saving Mode (Light-sleep), and added Table Description of Timing Parameters for Power Saving Mode (Light-sleep) in Section Low-Power Mode; • Added Figure Visualization of Timing Parameters for Power-down Boot and Table Description of Timing Parameters for Power-down Boot in Section Boot Configurations; • Updated Table Peripheral Pin Configurations; • Added Chapter Electrical Characteristics; • Added Chapter Packaging.
2020-11-27	v0.4	Preliminary version.

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