Experiment: 6 FIR Filter

Objective:

1. Draw a neat hardware architecture diagram for an 8-tap FIR filter using the following information

$$y(n) = a_0 \cdot x(n) + a_1 \cdot x(n-1) + a_2 \cdot x(n-2) + \cdots + a_7 \cdot x(n-7)$$

   a. Use Q4.12 fixed point representation for the 16-bit input/output samples.
   b. The 8 filter coefficients are $a_0 = -0.0841$, $a_1 = -0.0567$, $a_2 = 0.1826$, $a_3 = 0.4086$, $a_4 = 0.4086$, $a_5 = 0.1826$, $a_6 = -0.0567$, and $a_7 = -0.0841$
2. Implement the hardware architecture using Verilog. To perform the simulation, read the input samples from the file “input.txt” uploaded.
3. Use MATLAB / Python to plot the input and output samples and verify the Verilog simulation output.