FIR Filter

Objective:

1. Draw a neat hardware architecture diagram for an 8-tap FIR filter using the equation:

$y(n) = a_0 \cdot x(n) + a_1 \cdot x(n-1) + a_2 \cdot x(n-2) + \cdots + a_7 \cdot x(n-7)$

- Specifications:
- Use Q4.12 fixed-point representation for the 16-bit input and output samples.
- The 8 filter coefficients are:
    - $a_0 = -0.0841$
    - $a_1 = -0.0567$
    - $a_2 = 0.1826$
    - $a_3 = 0.4086$
    - $a_4 = 0.4086$
    - $a_5 = 0.1826$
    - $a_6 = -0.0567$
    - $a_7 = -0.0841$

1. 2. Implement the hardware architecture using Verilog.

- Use shift registers, fixed-point multipliers, and an adder tree to implement the architecture.
- Simulate the design using test inputs read from “input.txt” (already provided).

2. 3. Verify the simulation output using MATLAB or Python.

- Plot both the input and output signals using MATLAB/Python.
- Compare and analyze the plots to ensure the FIR filter is working as expected.