Process Fabrication for μDBS

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Abstract

The following content outlines the fabrication steps done in the Utah NanoFab Lab to build the μDBS. The purpose of this lab is to establish working recipes for the process and to keep track of past failures.

1 Design Process Overview

1.1 Design Architecture

The fabrication of the μDBS begins with design in Cadence through the X-FAB XC06 design package. The design is sent to X-FAB Foundry (Erfurt, GE) for fabrication. The chips that are returned must undergo metal plating for the contacts and the bond pads, a parylene coating, dicing, wire bonding, and assembly. The design architecture can be found in Figure A.1

2 General Instructions to Make a Mask

2.1 Lithography

1. Use the Heidelberg MicroPG 101
2. Click and follow instructions under the photolithography exposure wizard.
3. Record Size, Offset, Power (12 mW), Energy Mode (1/1).
4. To make a positive mask, **uncheck** inverted.

2.2 Exposure for mask

1. AZ developer 1:1
2. Develop for 1 min, the run under rinse water
3. DI rinse - hit run

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Table 4.1: 5" Wafer Thickness Measurements for Five Positions

	Wafer Thickness (mm)					
	Trial 1	**Trial 2**	**Trial 3**	**Trial 4**	**Mean**	**SD**
Position 1	0.676	0.652	0.746	0.716	0.698	0.0417
Position 2	0.677	0.669	0.703	0.698	0.687	0.0163
Position 3	0.698	0.682	0.682	0.693	0.689	0.00806
Position 4	0.689	0.685	0.682	0.703	0.690	0.00929
Position 5	0.678	0.691	0.684	0.691	0.686	0.00627

4. Dip for 3.5 min in Cr 14-S chromium etch
5. Rinse in DI for 2 min
6. Run in spin dryer (put in last spot)

3 General Instructions for Developing Photoresist

3.1 Applying Photoresist AZ 9260

1. CEE 100 Spinner
2. Spin at 2500 rpm, 60 Seconds
3. Bake at 110 C for 2+ Minutes

3.2 Exposing Photoresist AZ 9260

1. Use the EV 420 Aligner
2. 45 second exposure
3. 1:3.5 ratio of AZ 400K:DI water
4. 7 minute development
5. (FRESH BATCH EVERY TIME!!!!)

4 Creation of a Chip Tray

4.1 Measurements

Thickness measurements were taken of a 5" wafer using the Mitutoyo Dial Indicator Probe. Results can be found in Table 4.1.

Table 4.2: Proximal Length and Width Measurements

Proximal Length and Width Measurements (μm)								
	Chip 1	**Chip 2**	**Chip 3**	**Chip 4**	**Chip 5**	**Mean**	**SD**	**Mean + SD**
Position A	1488	1490	1488	1490	1490	1489.2	1.10	1490.30
Position B	1490	1492	1489	1488	1494	1490.6	2.41	1493.01
Position C	1490	1489	1490	1488	1489	1489.2	0.84	1490.04
Position D	10221	10224	10222	10218	10220	10221	2.24	10223.24

Table 4.3: Distal Length and Width Measurements

Distal Length and Width Measurements (μm)								
	Chip 1	**Chip 2**	**Chip 3**	**Chip 4**	**Chip 5**	**Mean**	**SD**	**Mean + SD**
Position A	1493	1496	1495	1495	1494	1494.6	1.14	1495.74
Position B	1494	1492	1494	1494	1492	1493.2	1.10	1494.30
Position C	1495	1494	1492	1495	1495	1494.2	1.30	1495.50
Position D	10220	10216	10217	10224	10221	10219.6	3.21	10222.81

Measurements of 5 Proximal and 5 Distal chips were taken on the Nikon V12A microscope. Results can be found in Table 4.2 and Table 4.3.

Length and width measurements can be found in Table 4.4.

Overall length and width measurements can be found in Table 4.5.

4.2 Mask Design

Run parameters for Tray Mask can be found in Table 4.6.

A Appendix 1

Table 4.4: Length and Width Measurements for Proximal and Distal Chips

Proximal				**Distal**			
	Mean	**SD**	**Mean + SD**		**Mean**	**SD**	**Mean + SD**
Width	1489.67	1.63	1491.30	**Width**	1494	1.25	1495.25
Length	10221	2.24	10223.24	**Length**	10219.6	3.21	10222.81

Table 4.5: Overall Length and Width Measurements for Proximal and Distal Chips

	Overall Mean	**Overall SD**	**Mean + SD**
Width	1491.83	2.63	1494.46
Length	10220.3	2.71	10223.01

Table 4.6: Run Parameters for Tray Mask

Heidelberg MicroPG 101 3 μm	
Run Parameters	
Design	Tray_Mask.gds
Type / Scale	gdsii / 1
Size X / Y (μm)	106667.9 / 106660.3
Offset X / Y (μm)	145 / 9.75
Power	12 mW
Exposure Level	50%
Energy Mode	1x1
Inverted	Uncheck
Automatic Centering	Check
Auto Unload	Check
Stripes	13334

Table 4.7: My caption

	Measurement
A	1.464
B	1.469
C	1.467
D	10.193

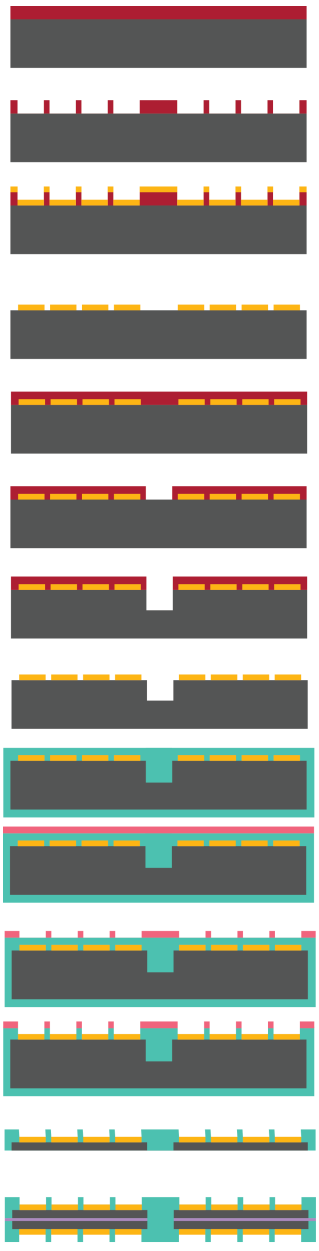

Figure A.1: Design Architecture