# Pipeline

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1. What is a FIR filter
   1. Taps and frequency cutoff
2. UART protocol
   1. Receiver
   2. Transmitter
3. Our implementation in VHDL
   1. Testbench waves
4. The generation of the signal
5. Set up of the FIR filter
6. FIR filter in python: what to expect
7. Data conversion
   1. Q approximation
   2. Signed to double and reverse
8. Script for the interface with FPGA
   1. Problems and solutions?
9. Comparison results