

Mohammed Ali-Khan

1001722553

Maa2553

25 April 2025

CSE 5357 Advanced Digital Logic Design

Spring Semester 2025

Term Project

Half-Precision Floating-Point Adder Subtractor

Requirements Summary

This lab demonstrates the use of a 4x4 keypad to input half-precision floating point numbers displayed in 16 bit binary display and adds the two numbers onto an LCD display.

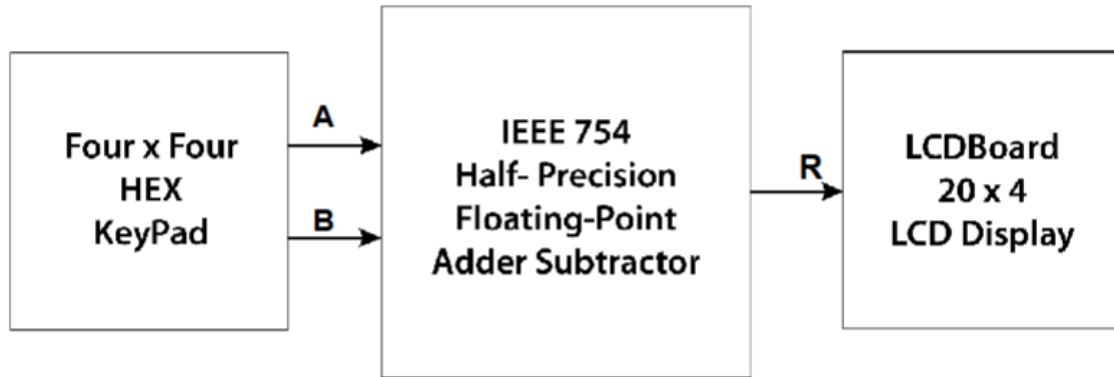


Figure 1 – Floating-Point Adder Subtractor with KeyPad and LCDBoard

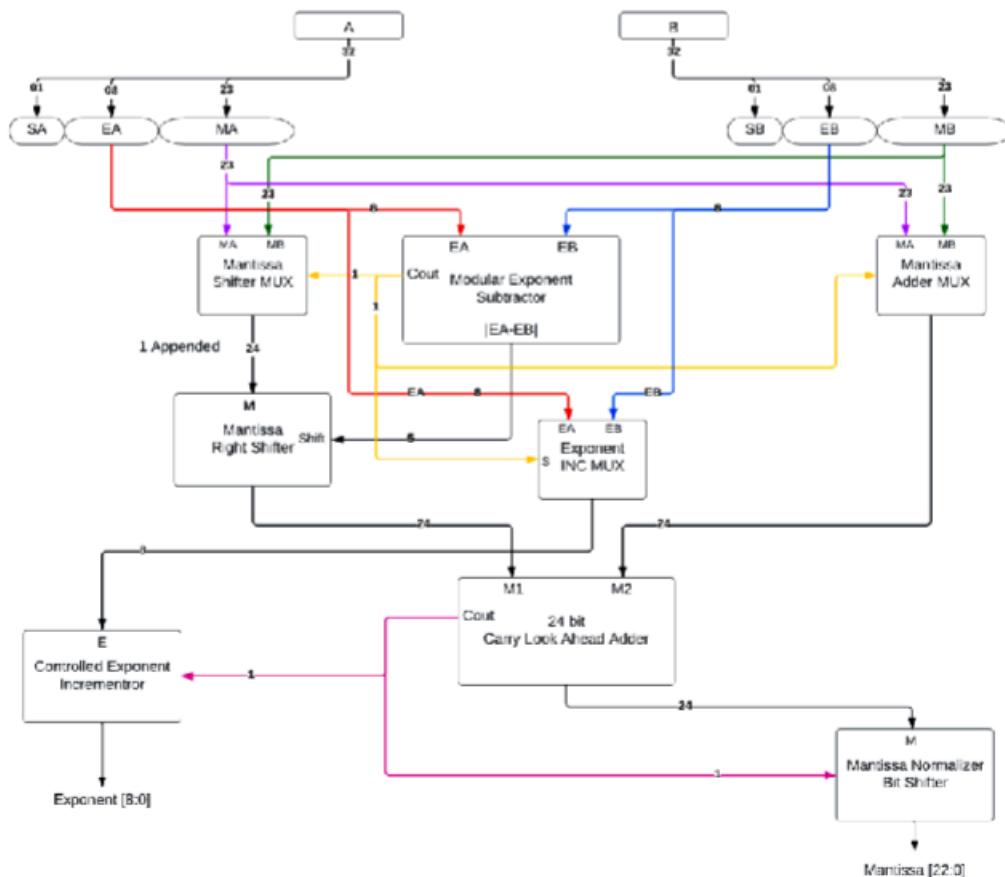
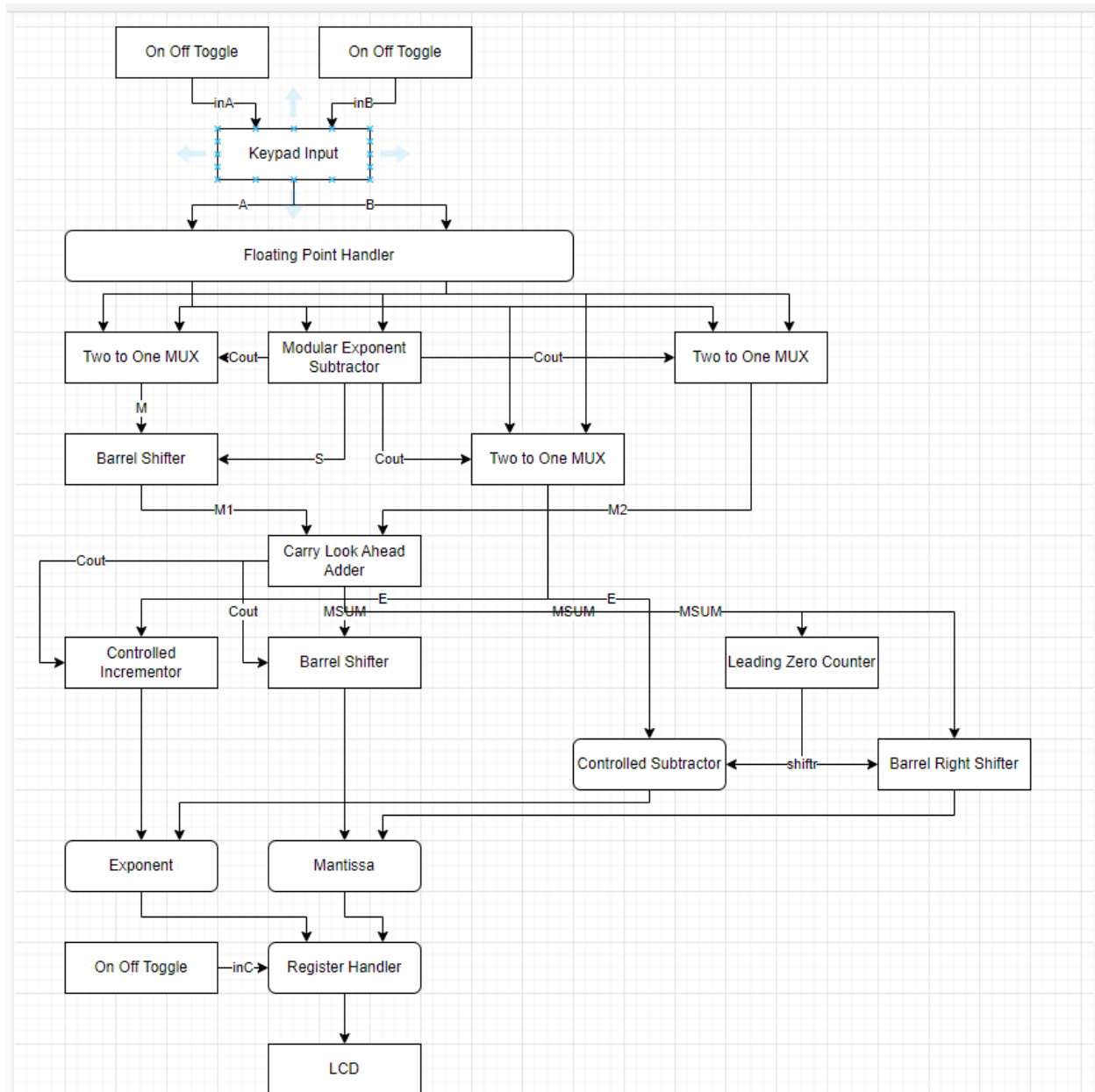


Figure 2 – Half-Precision Floating-Point Adder

Organization Diagram



Test Results

Summary

Compilation Report - CSE5357TP

Table of Contents

Flow Summary

Flow Settings

Flow Non-Default Glo

Flow Elapsed Time

Flow OS Summary

Flow Log

Analysis & Synthesis

Fitter

Flow Messages

Flow Suppressed Mes

Assembler

Timing Analyzer

Flow Summary

<<Filter>>

Flow Status

Successful - Fri Apr 25 17:17:57 2025

Quartus Prime Version

23.1std.1 Build 993 05/14/2024 SC Lite Edition

Revision Name

CSE5357TP

Top-level Entity Name

TopLevel

Family

MAX 10

Device

10M50DAF484C6GES

Timing Models

Preliminary

Total logic elements

704 / 49,760 (1 %)

Total registers

218

Total pins

31 / 360 (9 %)

Total virtual pins

0

Total memory bits

0 / 1,677,312 (0 %)

Embedded Multiplier 9-bit elements

0 / 288 (0 %)

Total PLLs

0 / 4 (0 %)

UFM blocks

0 / 1 (0 %)

ADC blocks

0 / 2 (0 %)

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	Strict Preservation
clear	Input	PIN_F15	7	B7_NO	PIN_F15	2.5 V		12mA (default)			
clearA	Input	PIN_B14	7	B7_NO	PIN_B14	2.5 V		12mA (default)			
clearB	Input	PIN_A14	7	B7_NO	PIN_A14	2.5 V		12mA (default)			
clk	Input	PIN_P11	3	B3_NO	PIN_P11	2.5 V		12mA (default)			
col[3]	Output	PIN_AB9	3	B3_NO	PIN_AB9	2.5 V		12mA (default)	2 (default)		
col[2]	Output	PIN_Y10	3	B3_NO	PIN_Y10	2.5 V		12mA (default)	2 (default)		
col[1]	Output	PIN_AA11	4	B4_NO	PIN_AA11	2.5 V		12mA (default)	2 (default)		
col[0]	Output	PIN_AA12	4	B4_NO	PIN_AA12	2.5 V		12mA (default)	2 (default)		
flagA	Output	PIN_A9	7	B7_NO	PIN_A9	2.5 V		12mA (default)	2 (default)		
flagB	Output	PIN_A10	7	B7_NO	PIN_A10	2.5 V		12mA (default)	2 (default)		
flagC	Output	PIN_B10	7	B7_NO	PIN_B10	2.5 V		12mA (default)	2 (default)		
keyA	Input	PIN_V8	3	B3_NO	PIN_V8	2.5 V		12mA (default)			
keyB	Input	PIN_AA5	3	B3_NO	PIN_AA5	2.5 V		12mA (default)			
keyC	Input	PIN_Y3	3	B3_NO	PIN_Y3	2.5 V		12mA (default)			
lcd_data[7]	Output	PIN_AA8	3	B3_NO	PIN_AA8	2.5 V		12mA (default)	2 (default)		
lcd_data[6]	Output	PIN_AA9	3	B3_NO	PIN_AA9	2.5 V		12mA (default)	2 (default)		
lcd_data[5]	Output	PIN_AB10	4	B4_NO	PIN_AB10	2.5 V		12mA (default)	2 (default)		
lcd_data[4]	Output	PIN_AB11	4	B4_NO	PIN_AB11	2.5 V		12mA (default)	2 (default)		
lcd_data[3]	Output	PIN_AB12	4	B4_NO	PIN_AB12	2.5 V		12mA (default)	2 (default)		
lcd_data[2]	Output	PIN_AB13	4	B4_NO	PIN_AB13	2.5 V		12mA (default)	2 (default)		
lcd_data[1]	Output	PIN_W12	4	B4_NO	PIN_W12	2.5 V		12mA (default)	2 (default)		
lcd_data[0]	Output	PIN_W13	4	B4_NO	PIN_W13	2.5 V		12mA (default)	2 (default)		
lcd_e	Output	PIN_AA14	4	B4_NO	PIN_AA14	2.5 V		12mA (default)	2 (default)		
lcd_rs	Output	PIN_W5	3	B3_NO	PIN_W5	2.5 V		12mA (default)	2 (default)		
lcd_rw	Output	PIN_AA15	4	B4_NO	PIN_AA15	2.5 V		12mA (default)	2 (default)		
op	Input	PIN_C10	7	B7_NO	PIN_C10	2.5 V		12mA (default)			
reset	Input	PIN_C12	7	B7_NO	PIN_C12	2.5 V		12mA (default)			

op	Input	PIN_C10	7	B7_NO	PIN_C10	2.5 V		12mA (default)			
reset	Input	PIN_C12	7	B7_NO	PIN_C12	2.5 V		12mA (default)			
row[3]	Input	PIN_AB5	3	B3_NO	PIN_AB5	2.5 V		12mA (default)			
row[2]	Input	PIN_AB6	3	B3_NO	PIN_AB6	2.5 V		12mA (default)			
row[1]	Input	PIN_AB7	3	B3_NO	PIN_AB7	2.5 V		12mA (default)			
row[0]	Input	PIN_AB8	3	B3_NO	PIN_AB8	2.5 V		12mA (default)			
inA	Unknown	PIN_C11	7	B7_NO		2.5 V (default)		12mA (default)			
inB	Unknown	PIN_D12	7	B7_NO		2.5 V (default)		12mA (default)			
<<new node>>											

Demonstration

The following link is to the demo video from my personal google drive. Cuts were made to facilitate keypad inputs (keypresses on same column are hard to register). Additionally, pictures have also been provided showcasing each test case.

<https://drive.google.com/file/d/1WyDM4RBCj7rQ4dV-JmP8vEceatxAiJ/view?usp=sharing>

1. $3.75 + 5.125$



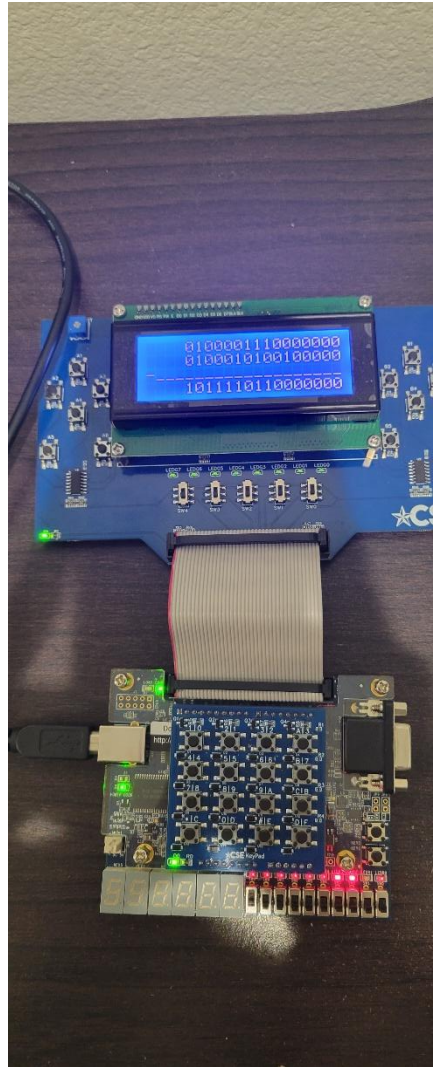
a.

2. $3.75 + -5.125$

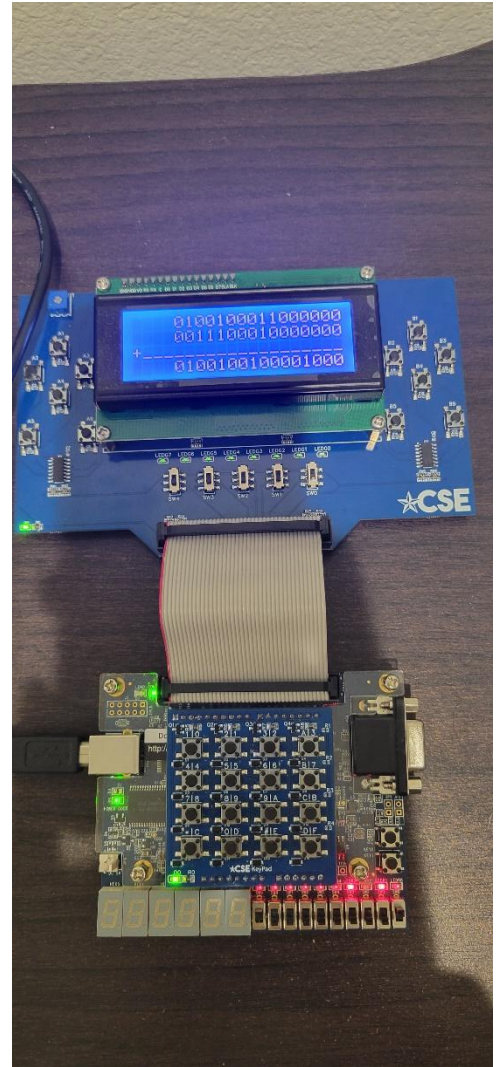


a.

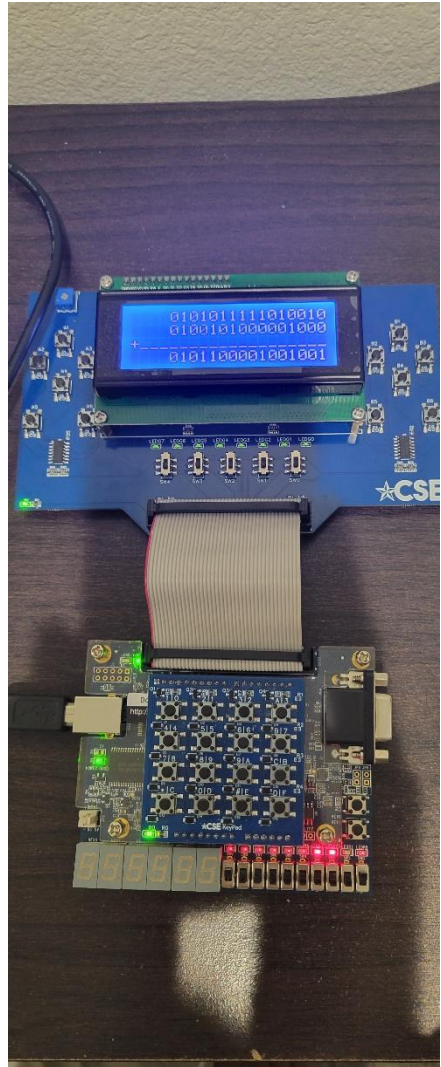
3. $3.75 - 5.125$



a.
4. $9.5 + 0.5625$



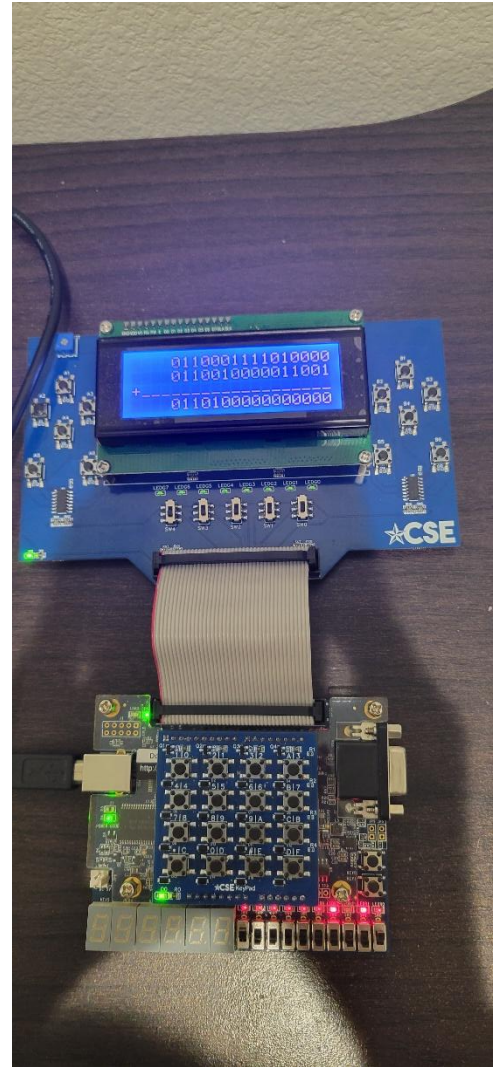
a.
5. $125.125 + 12.0625$



a.

6. $1000 + 1049$

b.



a.

Verilog Code

Top Level shown below. Minor changes, if any, are made to other modules. LeadingZeroCounter and BarrelRightShifter added for handling subtraction. Changes made to CarryLookAheadAdder to allow for 11 bit addition.

```

CSE5357P > @ TopLevel.sv > ...
1  module TopLevel (
2      input clk,
3      input reset,
4      input op,
5      input Clear,
6      input keyA, keyB, keyC,
7      input clearA, clearB,
8      input [3:0] row,
9      output flagA, flagB, flagC,
10     output [3:0] col,
11     output [7:0] lcd_data,
12     output lcd_rs,
13     output lcd_rw,
14     output lcd_e
15 );
16
17     // input button handler
18     logic inA, inB, inC;
19
20     // input logic reg
21     reg [15:0] A;
22     reg [15:0] B;
23     reg [15:0] C;
24     wire [1:0] Operation;
25     wire [15:0] keypad_out;
26     wire [3:0] keypad_value;
27     wire trig;
28
29     // output logic reg
30     reg [31:0] opA, opB;
31     reg [4:0] Exponent;
32     reg [10:0] Mantissa;
33
34     // floating point internal reg
35     reg SA, SB;
36     reg [4:0] EA, EB;
37     reg [9:0] MA, MB;
38
39     // exponent sub reg
40     reg [3:0] shift;
41     reg S;
42
43     // CLA adder reg
44     reg [10:0] M, M1, M2, MSUM;
45     reg [4:0] E;
46     reg Cout;
47
48     // reg for subtraction or negative
49     reg [10:0] M3;
50     reg [3:0] shiftr;
51     reg [4:0] dec, exp;
52     reg [10:0] minused, maxused;

```

```

CSE5357P > @ TopLevel.sv > ...
1  module TopLevel (
54     // assign plus or minus
55     assign Operation = op ? 2'b01 : 2'b10;
56
57     // split floating point
58     assign SA = A[15];
59     assign SB = B[15] ^ ~op;
60     assign EA = A[14:10];
61     assign EB = B[14:10];
62     assign MA = A[9:0];
63     assign MB = B[9:0];
64
65     // button handlers
66     OnOffToggle input_a (
67         .OnOff(keyA),
68         .IN(1'b1),
69         .OUT(inA)
70     );
71
72     OnOffToggle input_b (
73         .OnOff(keyB),
74         .IN(1'b1),
75         .OUT(inB)
76     );
77
78     OnOffToggle input_c (
79         .OnOff(keyC),
80         .IN(1'b1),
81         .OUT(inC)
82     );
83
84     // subtract exponents
85     ModularExponentSubtractor #(.N(5)) modular_exponent_subtractor (
86         .A(EA),
87         .B(EB),
88         .Out(shift),
89         .C(S)
90     );
91
92     // shift mantissa
93     Two2OneMux #(.N(11)) mantissa_shifter_mux (
94         .R({1'b1, MB}),
95         .B({1'b1, MA}),
96         .Cout(S),
97         .Out(M)
98     );
99
100    // select higher mantissa
101    Two2OneMux #(.N(11)) mantissa_adder_mux (
102        .R({1'b1, MA}),
103        .B({1'b1, MB}),
104        .Cout(S),
105        .Out(M2)
106    );
107

```


CSE5357P > TopLevel.sv > ...

```
1 module TopLevel (  
108     // select exponent  
109     TwoOneMux #(N(5)) exponent_inc_mux (  
110         .R(EA),  
111         .B(EB),  
112         .Cout(S),  
113         .Out(E)  
114     );  
115  
116     // shift lower mantissa  
117     BarrelShifter mantissa_right_shifter(  
118         .A(M),  
119         .B(shift[3:0]),  
120         .Y(M1)  
121     );  
122  
123     // handle negative addition  
124     assign M3 = (SA ^ SB) ? ~M1 + 1 : M1;  
125  
126     // add mantissas  
127     CarryLookAheadAdder CLAA(  
128         .A(M3),  
129         .B(M2),  
130         .c_in(1'b0), // optional, usually 0  
131         .S(MSUM),  
132         .c_out(Cout)  
133     );  
134  
135     // count leading zero for subtraction  
136     LeadingZeroCounter #(N(11)) zero_counter (  
137         .A(MSUM),  
138         .Count(shifttr)  
139     );  
140  
141     // increment exponent  
142     ControlledIncrementor controlled_exponent_incr(  
143         .A(E),  
144         .Select(Cout),  
145         .S(exp)  
146     );  
147  
148     // adjust exponent for subtraction  
149     assign dec = E - {1'b0, shifttr};  
150  
151     // adjust mantissa for addition  
152     BarrelShifter mantissa_normalizer_bit_shifter(  
153         .A(MSUM),  
154         .B(Cout),  
155         .Y(maxused)  
156     );  
157
```

CSE5357P > TopLevel.sv > ...

```
1 module TopLevel (  
157     // adjust mantissa for subtraction  
158     BarrelRightShifter mantissa_normalizer_right_shifter(  
159         .A(MSUM),  
160         .B(shifttr),  
161         .Y(minused)  
162     );  
163  
164     // output assignment  
165     assign Exponent = (SA ^ SB) ? dec : exp;  
166     assign Mantissa = (SA ^ SB) ? minused : maxused;  
167  
168     // input from keypad  
169     KeypadInput #(DIGITS(4)) keypad (  
170         .clk(clk),  
171         .reset(Clear),  
172         .row(row),  
173         .col(col),  
174         .out(keypad_out),  
175         .value(keypad_value),  
176         .trig(trig)  
177     );  
178  
179     // logic for input output reg  
180     reg [15:0] regA, regB, regC;  
181  
182     always @(posedge clk) begin  
183         if (reset) begin  
184             regA <= 0;  
185             regB <= 0;  
186             regC <= 0;  
187         end else begin  
188             if (clearA)  
189                 regA <= 0;  
190             else if (inA)  
191                 regA <= keypad_out;  
192  
193             if (clearB)  
194                 regB <= 0;  
195             else if (inB)  
196                 regB <= keypad_out;  
197  
198             if (!inC)  
199                 regC <= 0;  
200             else if (inC)  
201                 regC <= {(SA ^ SB), Exponent, Mantissa[9:0]};  
202         end  
203     end  
204  
205     assign A = regA;  
206     assign B = regB;  
207     assign C = regC;  
208
```

```

209
210     assign flagA = inA;
211     assign flagB = inB;
212     assign flagC = inC;
213
214     // send data to LCD
215     LCD #(
216         .WIDTH(16),
217         .DIGITS(5),
218         .FLOAT(0),
219         .MODE(1),
220         .LINES(4),
221         .CHARS(20)
222     ) lcd_unit (
223         .clk(clk),
224         .lcd_data(lcd_data),
225         .lcd_rs(lcd_rs),
226         .lcd_rw(lcd_rw),
227         .lcd_e(lcd_e),
228         .lcd_reset(reset),
229         .A(A),
230         .B(B),
231         .C(C),
232         .Operation(Operation)
233     );
234
235 endmodule
236

```

```

CSE5357P > @ LeadingZeroCounter.sv > ...
1  module LeadingZeroCounter #(parameter N = 11)(
2      input wire [N-1:0] A,
3      output reg [3:0] Count
4  );
5      integer i;
6      reg found;
7
8      always @(*) begin
9          Count = 0;
10         found = 0;
11         for (i = N-1; i >= 0; i = i - 1) begin
12             if (!found && A[i] == 1'b1) begin
13                 Count = N - 1 - i;
14                 found = 1;
15             end
16         end
17     end
18 endmodule
19

```

```

CSE5357P > @ BarrelRightShifter.sv > @ BarrelRightShifter
1  module BarrelRightShifter(
2      input [10:0] A,
3      input [3:0] B,
4      output [10:0] Y
5  );
6
7      wire [10:0] shift8, shift4, shift2, shift1;
8
9      Two2OneMuxAB shiftEight (
10         .Sel(B[3]),
11         .A({A[2:0], 8'b0}),
12         .B(A),
13         .Out(shift8)
14     );
15
16     Two2OneMuxAB shiftFour (
17         .Sel(B[2]),
18         .A({shift8[4:0], 4'b0}),
19         .B(shift8),
20         .Out(shift4)
21     );
22
23     Two2OneMuxAB shiftTwo (
24         .Sel(B[1]),
25         .A({shift4[8:0], 2'b0}),
26         .B(shift4),
27         .Out(shift2)
28     );
29
30     Two2OneMuxAB shiftOne (
31         .Sel(B[0]),
32         .A({shift2[9:0], 1'b0}),
33         .B(shift2),
34         .Out(shift1)
35     );
36
37     assign Y = shift1;
38
39 endmodule

```

```

CSE5357P > @ CarryLookAheadAdder.sv > CarryLookAheadAdder
1  module CarryLookAheadAdder(
2      input  logic [10:0] A,
3      input  logic [10:0] B,
4      input  logic      c_in,
5      output logic [10:0] S,
6      output logic      c_out
7  );
8
9      wire [3:0] S0, S1;
10     wire [2:0] S2;
11     wire      c4, c8;
12     wire      G0, P0, G1, P1, G2, P2;
13
14     CLA_4bit cla0 (
15         .A(A[3:0]), .B(B[3:0]), .c_in(c_in),
16         .S(S0), .c_out(c4), .G_out(G0), .P_out(P0)
17     );
18
19     CLA_4bit cla1 (
20         .A(A[7:4]), .B(B[7:4]), .c_in(c4),
21         .S(S1), .c_out(c8), .G_out(G1), .P_out(P1)
22     );
23
24     CLA_3bit cla2 (
25         .A(A[10:8]), .B(B[10:8]), .c_in(c8),
26         .S(S2), .c_out(c_out), .G_out(G2), .P_out(P2)
27     );
28
29     assign S = {S2, S1, S0};
30
31 endmodule
32

```