

graph_color.v3 (extract)	24	48.00	24	48.00	3050.25	0.02
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File Edit View Compile Simulate Add Transcript Tools Layout Bookmarks Window Help



ColumnLayout AllColumns

sim - Default

Instance

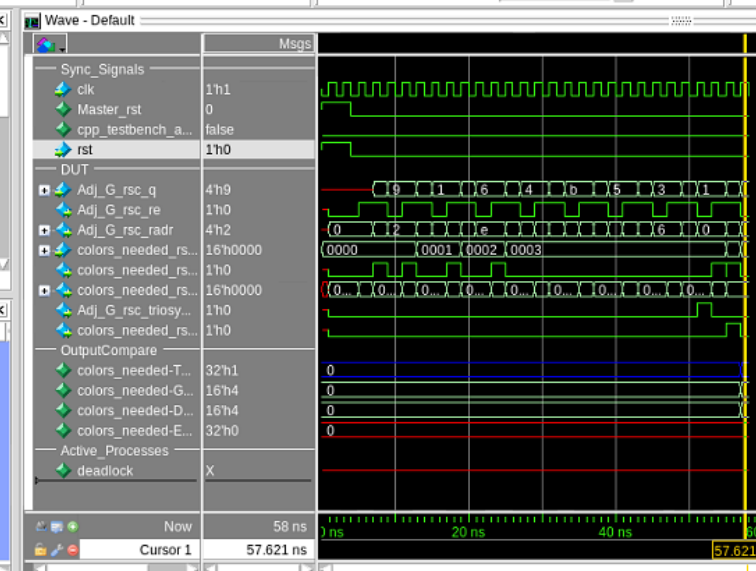
- scverify_top
 - rst_driver
 - rtl
 - Adj_G_rsc
 - colors_needed_rsc
 - trios_monitor_Adj_G_rsc_trios_lz_INS...
 - transactor_Adj_G
 - trios_monitor_colors_needed_rsc_trios...
 - transactor_colors_needed
 - user_tb
 - sync_generator
 - Monitor
 - ccs_probe_monitor
 - trios_observer_for_colors_needed_rsc
 - TLS_rst_method
 - max_sim_time_notify
 - generate_reset
 - deadlock_watch
 - deadlock_notify
 - #vsm_capacity#

Objects

Name	Value	KI	57621 ps
max_sim_time_event	Not Lo...	ScEv...	Internal
deadlock_event	Not Lo...	ScEv...	Internal
generate_reset_event	Not Lo...	ScEv...	Internal
rst	0	ScPri...	Internal
rst_n	Not Lo...	ScPri...	Internal
SIG_SC_LOGIC_0	Not Lo...	ScPri...	Internal
SIG_SC_LOGIC_1	Not Lo...	ScPri...	Internal
TLS_design_is_idle	Not Lo...	ScPri...	Internal
TLS_design_is_idle_r...	Not Lo...	ScPri...	Internal
clk	Not Lo...	ScPri...	Internal
TLS_rst	Not Lo...	ScPri...	Internal

Processes (Active)

Name	Type (filtered)	State
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Transcript

```

#
# stdin: <EOF>
# VSIM 2> run -all
# SCVerify intercepting C++ function 'graph_color' for RTL block 'graph_color'
# Info: HW reset: TLS_rst active @ 0 s
# Graph | Colors Computed: 4
# Info: Execution of user-supplied C++ testbench 'main()' has completed with exit code = 0
#
# Info: Collecting data completed
#   captured 1 values of Adj_G
#   captured 1 values of colors_needed_IN
#   captured 1 values of colors_needed
# Info: scverify_top/user_tb: Simulation completed
#
# Checking results
# 'colors_needed'
#   capture count      = 1
#   comparison count   = 1
#   ignore count       = 0
#   error count        = 0
#   stuck in dut fifo  = 0
#   stuck in golden fifo = 0
#
# Info: scverify_top/user_tb: Simulation PASSED @ 58 ns

```

Now: 58 ns Delta: 2 sim/scverify_top - Limited Visibility Region