

ISE/iMPACT FLASH HOWTO

How to write the DarkRISCV on FPGA FLASH!

Marcelo Samsoniuk

ISE/iMPACT FLASH HOWTO

Before start...

- You need install Xilinx ISE 14.7
- You need install Vivado 2018.2 or better, in order to use modern JTAG device drivers (i.e. we will use Vivado drivers on ISE/iMPACT)
- A board with Xilinx FPGA + FLASH
- A JTAG adapter compatible w/ Xilinx tools

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Extra tips before start...

- Xilinx ISE/iMPACT is hard to make work on Windows, to the Linux version is recommended... case you have no Linux, you can use WSL1 on Windows.
- Vivado works correctly on both Windows and Linux.
- Identify the FLASH model and size before start, because you will need such information ahead!

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ISE/Vivado Environments

- Start two separated terminals and load the environment scripts for ISE (1) and Vivado (2) separately in each terminal
- Start the “hw_server” on the Vivado terminal and keep it running...

```
Brooke's Law:
Whenever a system becomes completely defined, some damn fool
discovers something which either abolishes the system or
expands it beyond recognition.

root@darkstar:~# . /opt/Xilinx/14.7/ISE_DS/settings64.sh
root@darkstar:~# . /home/marcelo/Documents/Work/Xilinx/14.7/ISE_DS/common/.settings64.sh /home/marcelo/Documents/Work/Xilinx/14.7/ISE_DS/common
root@darkstar:~# . /home/marcelo/Documents/Work/Xilinx/14.7/ISE_DS/EDK/.settings64.sh /home/marcelo/Documents/Work/Xilinx/14.7/ISE_DS/EDK
root@darkstar:~# . /home/marcelo/Documents/Work/Xilinx/14.7/ISE_DS/PlanAhead/.settings64.sh /home/marcelo/Documents/Work/Xilinx/14.7/ISE_DS/PlanAhead
root@darkstar:~# . /home/marcelo/Documents/Work/Xilinx/14.7/ISE_DS/ISE/.settings64.sh /home/marcelo/Documents/Work/Xilinx/14.7/ISE_DS/ISE
root@darkstar:~#
root@darkstar:~#

It's a dog-eat-dog world out there, and I'm wearing Milkbone
underwear."

root@darkstar:~# . /opt/Xilinx/Vivado/2018.2/settings64.sh
-bash: /opt/Xilinx/DocNav/.settings64-DocNav.sh: No such file or directory
root@darkstar:~#
root@darkstar:~# hw_server

***** Xilinx hw_server v2018.2
**** Build date : Jun 14 2018-20:18:37
** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

INFO: hw_server application started
INFO: Use Ctrl-C to exit hw_server application

INFO: To connect to this hw_server instance use url: TCP:darkstar:3121
```


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Preparing the FPGA image

- Start ISE w/ “ise” command on the ISE terminal, open your project on “File/Open Project” (1), click w/ left button on “Generate Programming File” (2) and click on “Run” (3)
- ISE will build your FPGA image...

The screenshot shows the ISE Project Navigator interface. The Design Summary window is open, displaying the Project Status and Device Utilization Summary. The Project Status table shows the project file, module name, target device, product version, design goal, design strategy, and environment. The Device Utilization Summary table shows the logic utilization, including the number of slices, slice flip flops, 4 input LUTs, bonded IOBs, BRAMs, and GCLKs. The Detailed Reports table shows the status of various reports, including the Synthesis Report, Translation Report, Map Report, Place and Route Report, Power Report, and Post-PA Static Timing Report.

darksocv Project Status			
Project File:	darksocv.xise	Parser Errors:	No Errors
Module Name:	darksocv	Implementation State:	Synthesized
Target Device:	xc6slx9-2csg324	• Errors:	No Errors
Product Version:	ISE 14.7	• Warnings:	142 Warnings (1 new)
Design Goal:	Timing Performance	• Routing Results:	
Design Strategy:	Performance without IOB Packing	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

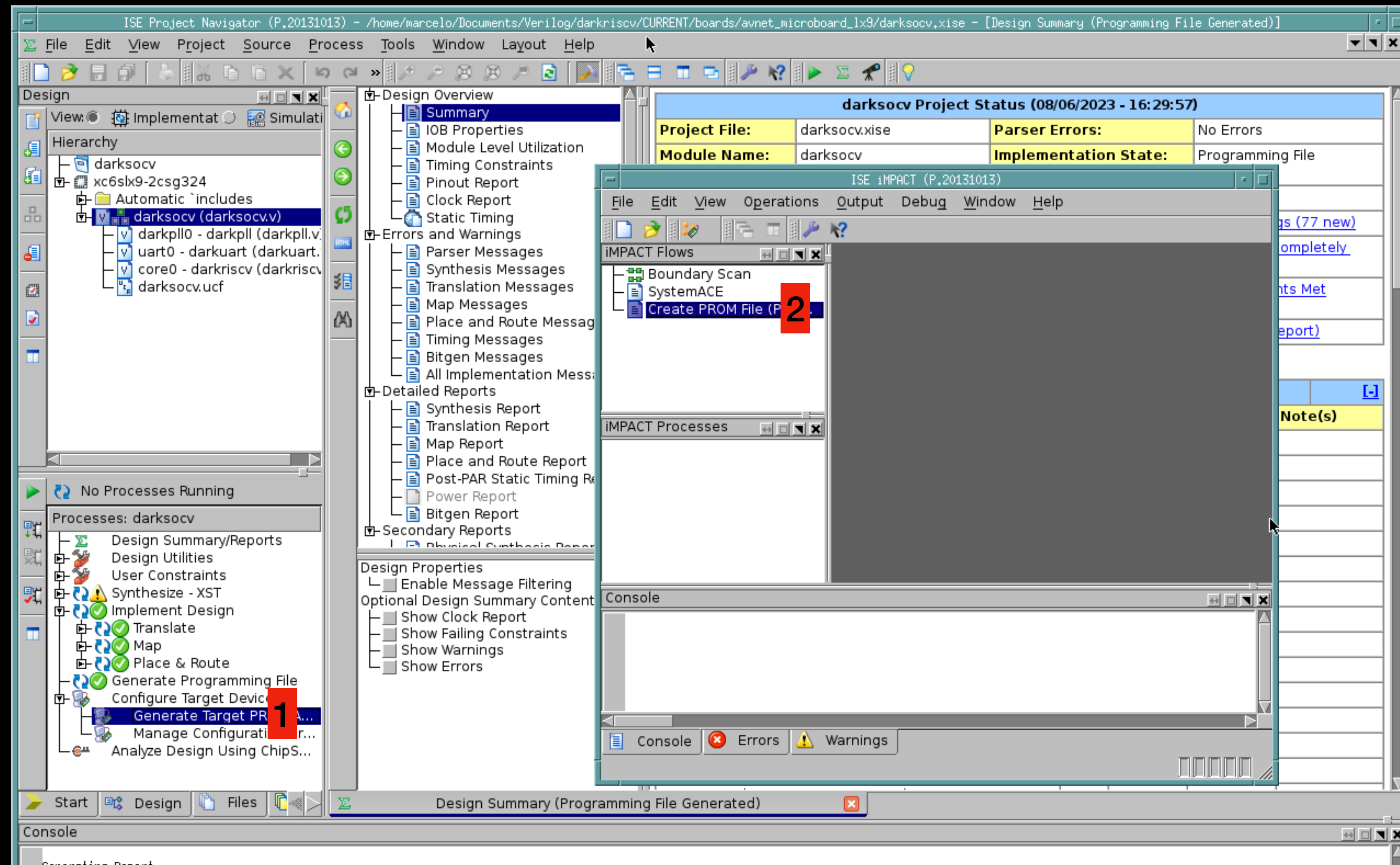
Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	971	960	101%
Number of Slice Flip Flops	427	1920	22%
Number of 4 input LUTs	1834	1920	95%
Number of bonded IOBs	12	66	18%
Number of BRAMs	2	4	50%
Number of GCLKs	1	24	4%

Detailed Reports					
Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Thu Aug 3 02:45:35 2023	0	142 Warnings (1 new)	24 Infos (0 new)
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PA Static Timing					

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Preparing the FLASH image

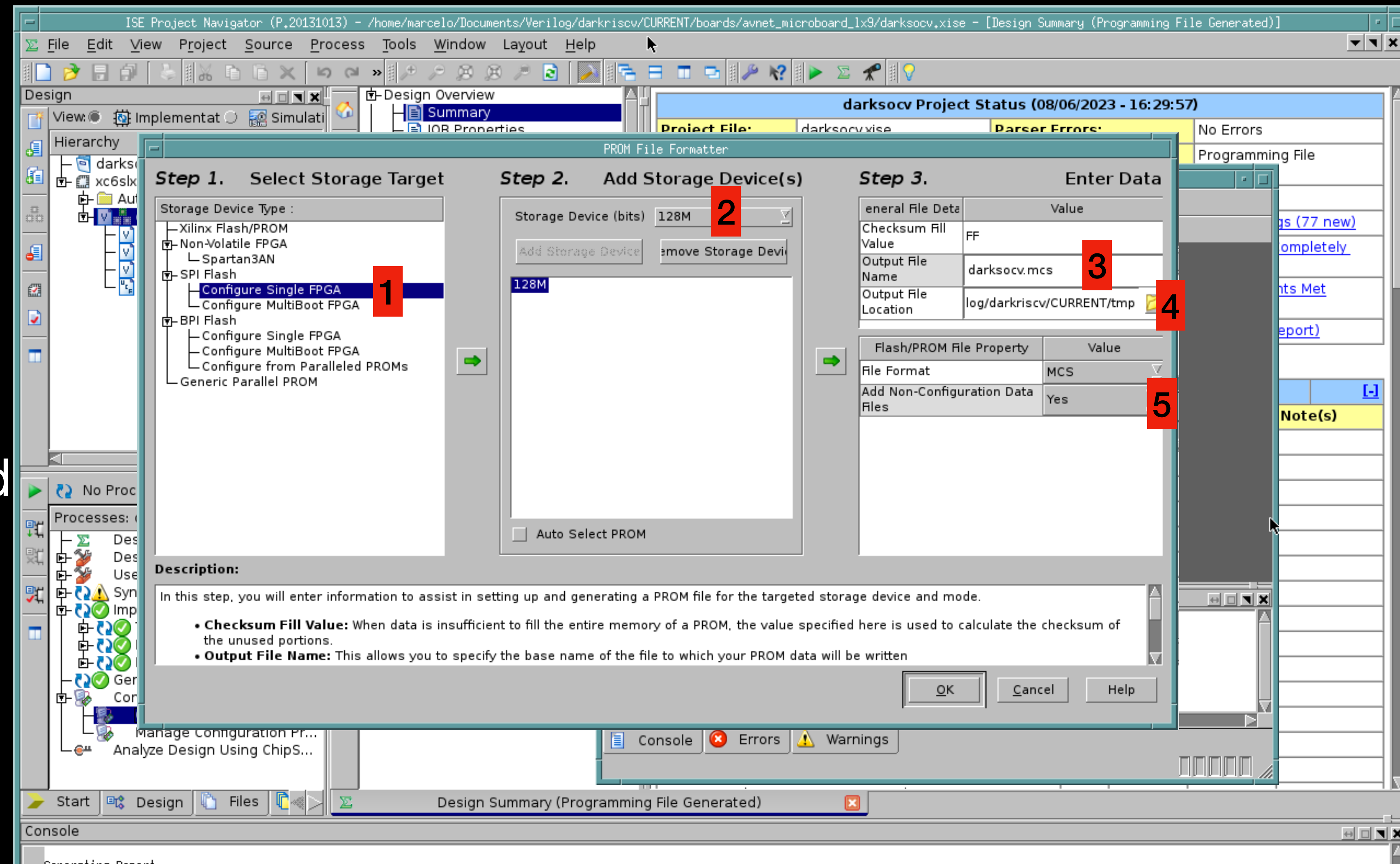
- After ISE concludes the FPGA build, open the option “Configure Target Device” and double-click on “Generate Target PROM” (1).
- It will open iMPACT, select “Create PROM File” (2)



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Preparing the FLASH image

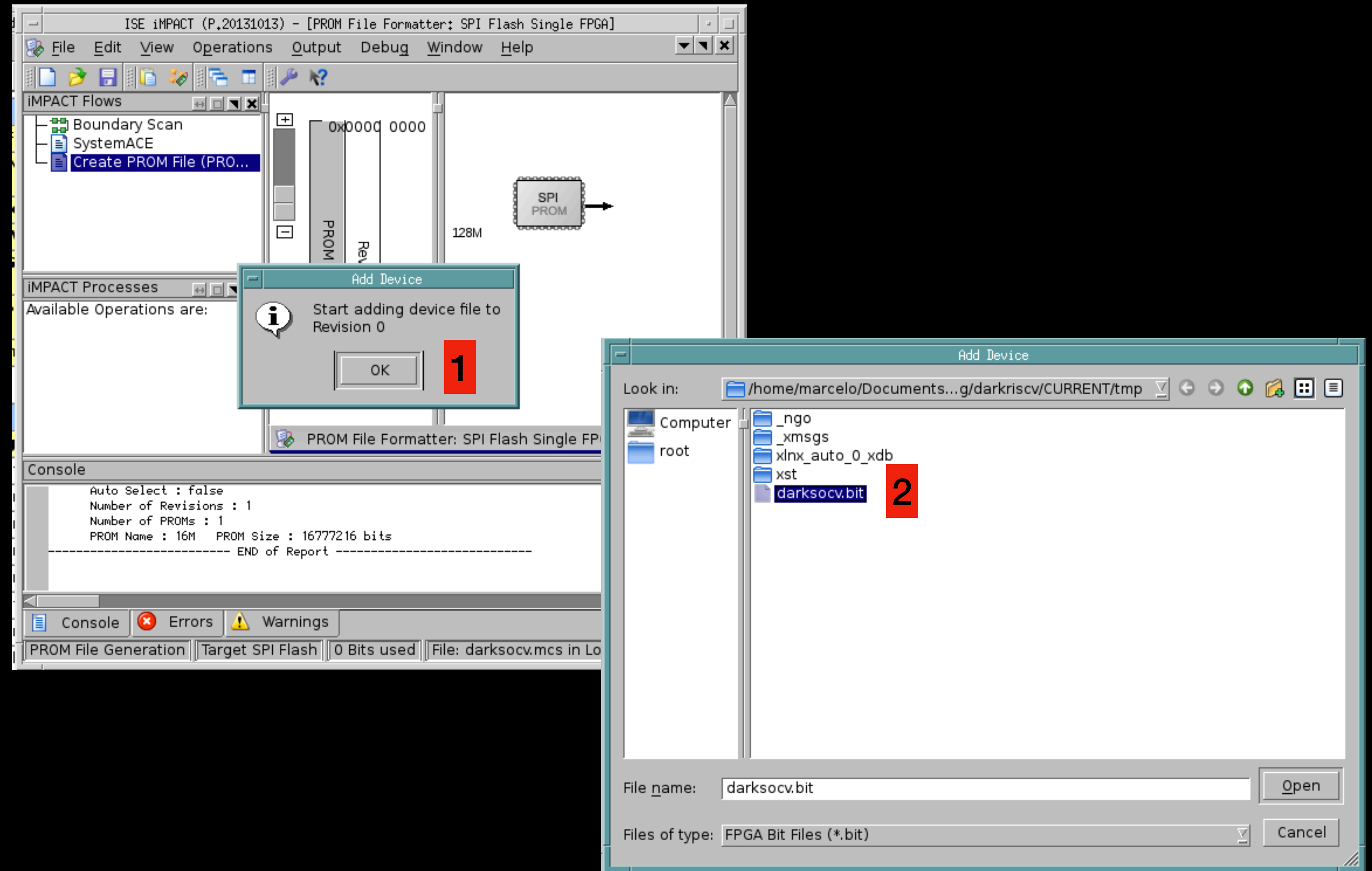
- Select “Configure Single FPGA”(1), select storage size, in this case 128Mbit (2), select the output name “darksocv.mcs” (3), the output path (4) and set the non-configuration files to “Yes” (5)



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Preparing the FLASH image

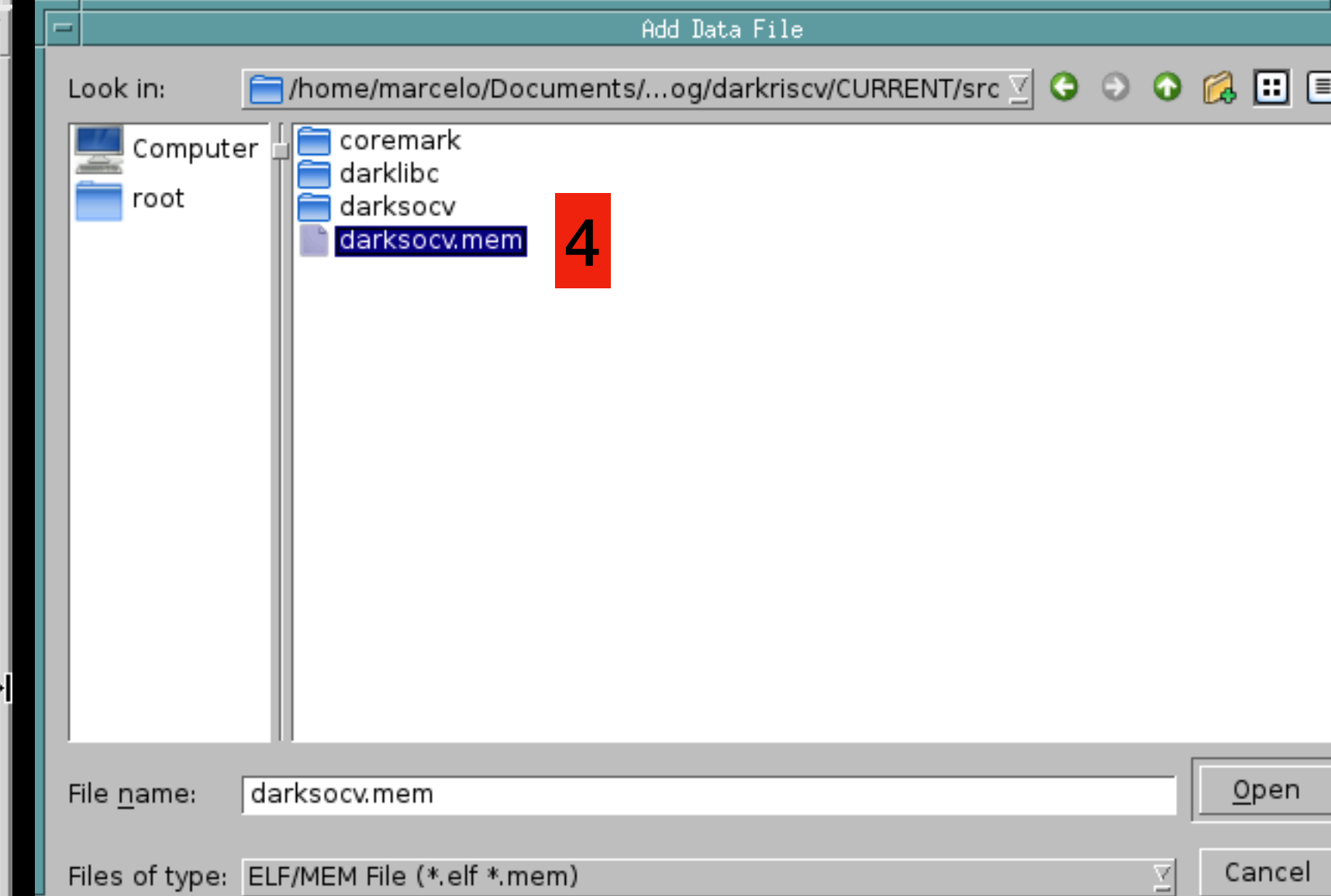
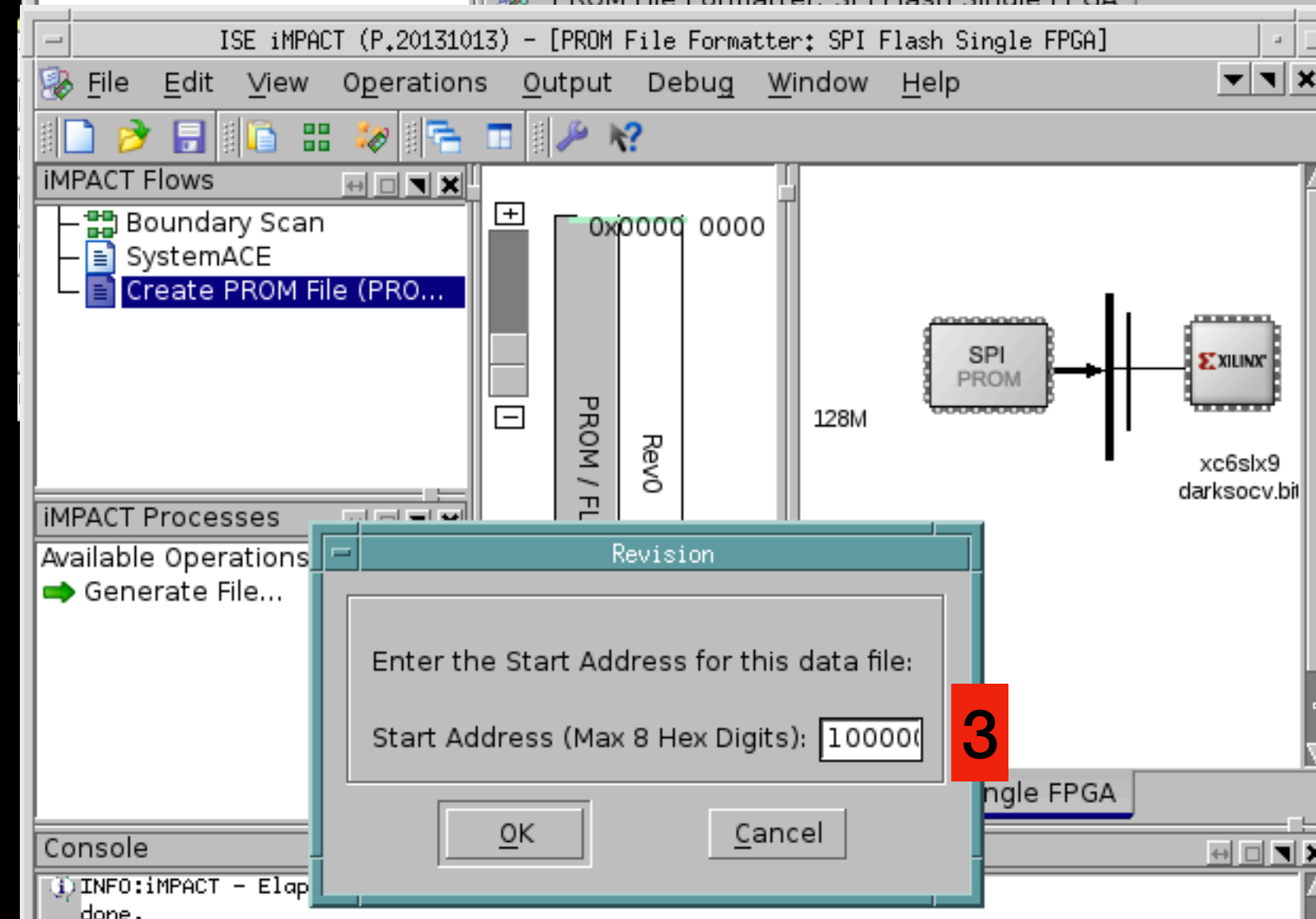
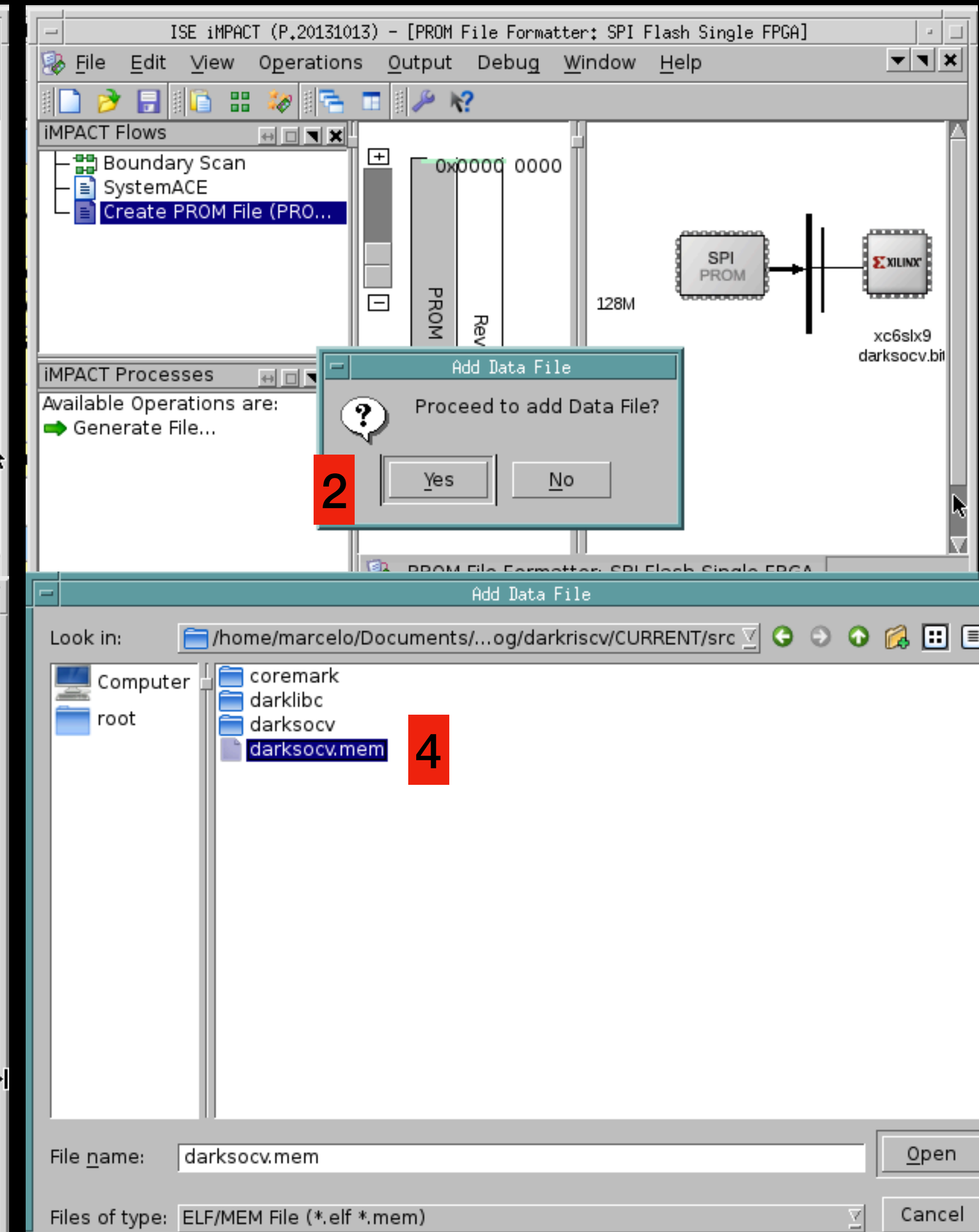
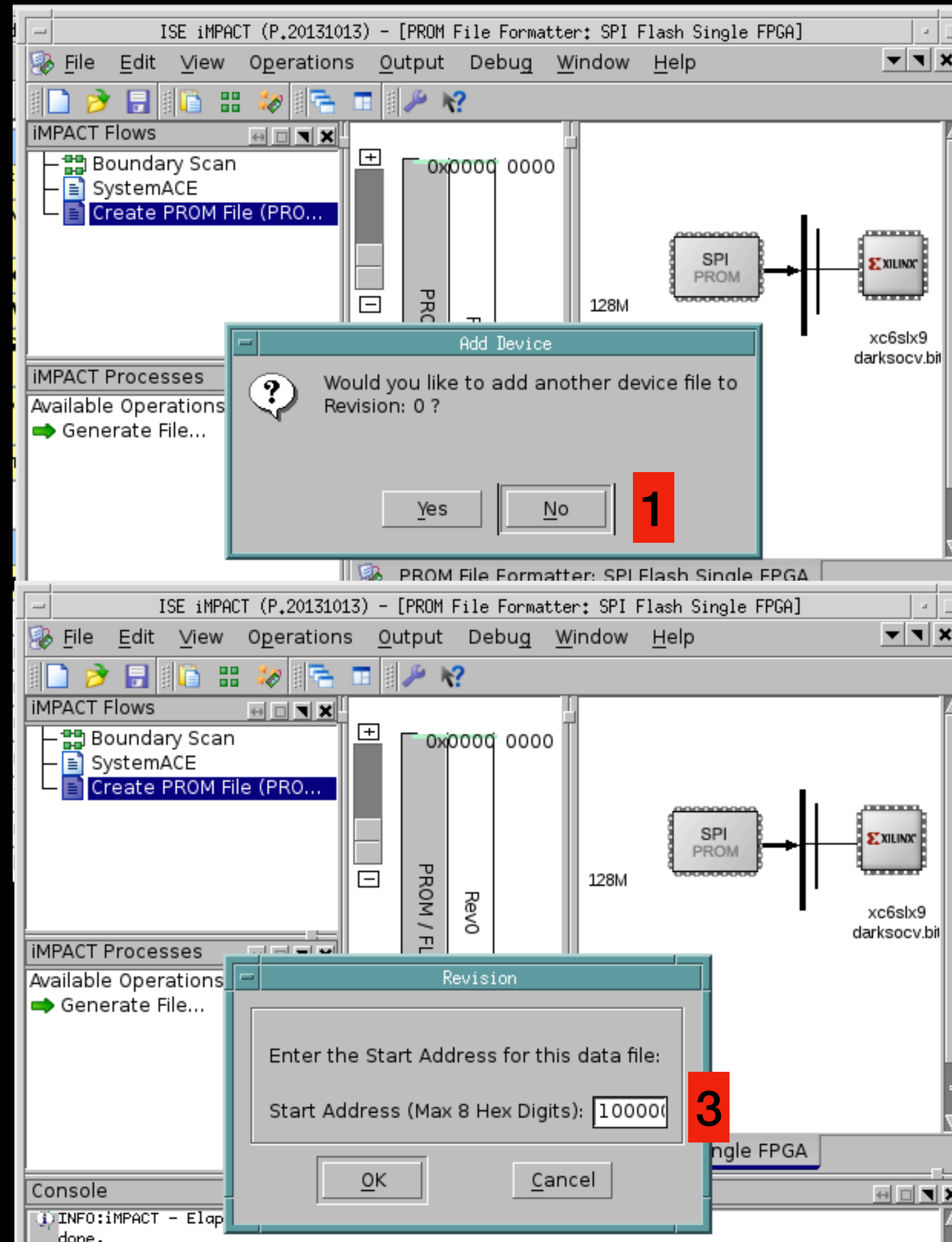
- Just click ok for the Revision 0 (1) and select the FPGA boot image (2), in this case, the darksocv.bit that we generated before



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Preparing the RISC-V image

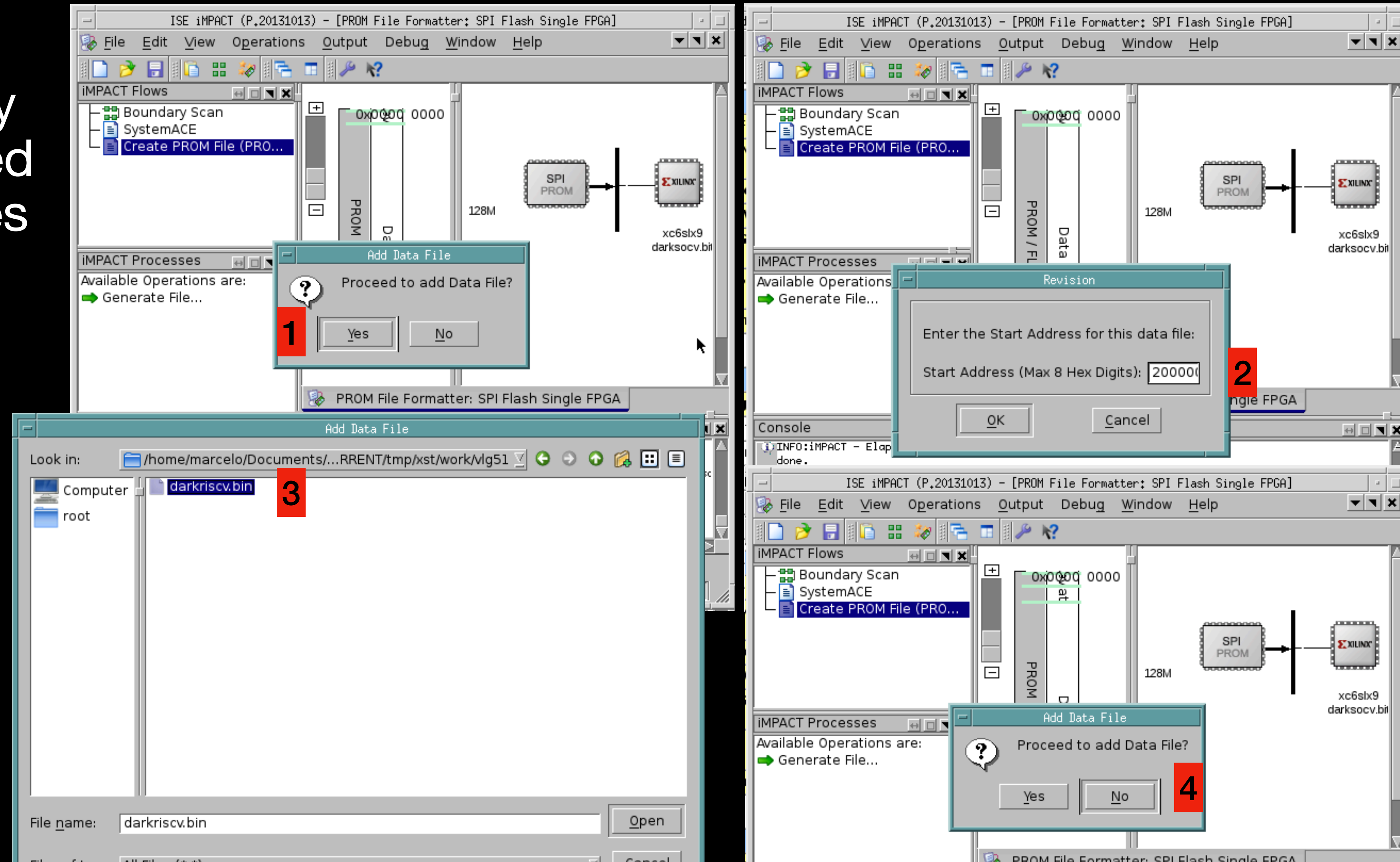
- Click on "No" to not add other boot FPGAs (1), click "Yes" to proceed to add data files (2), enter the data file start address (3), in this case 100000 means 1M and select the data file (4), in this case the darksocv.mem RISC-V image.



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Adding extra stuff (files, filesystem, etc)

- You can continuously click "Yes" to proceed to add more data files (1), incrementing the start address (2), selecting the file (3), etc...
- Case you need no more files, click "No" (4)



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FLASH Summary

- The tool will generate a summary, in a way you can review the file and offsets on the flash... case everything is ok, click “OK” (1) and double-click on “Generate File” (2) to generate the MCS file!

The image shows two windows from the ISE/iMPACT software. The left window is the 'Data File Assignment' dialog, and the right window is the 'PROM File Formatter: SPI Flash Single FPGA' window.

Data File Assignment Dialog:

Revision Start Address Assignment: (Only Revision 0 Start Address cannot be changed)

Revision	Start Address [Hex]	End Address [Hex]
0	0000	532C0

Non-Configuration Data File Assignment: (File and Start Address are allowed to change)

File Name	Start Address [Hex]	End Address [Hex]
ments/Verilog/darkiscv/CURRENT/src/darksocv.mem	100000	101E45
/darkiscv/CURRENT/tmp/xst/work/Vlg51/darkiscv.bin	200000	20A31C

Buttons: OK (1), Cancel, Update Address

PROM File Formatter: SPI Flash Single FPGA Window:

IMPACT Flows: Boundary Scan, SystemACE, Create PROM File (PRO...)

IMPACT Processes: Available Operations, Generate File... (2)

Diagram: SPI PROM (128M) connected to xc6slx9 darksocv.bit

Generate Succeeded

Console:

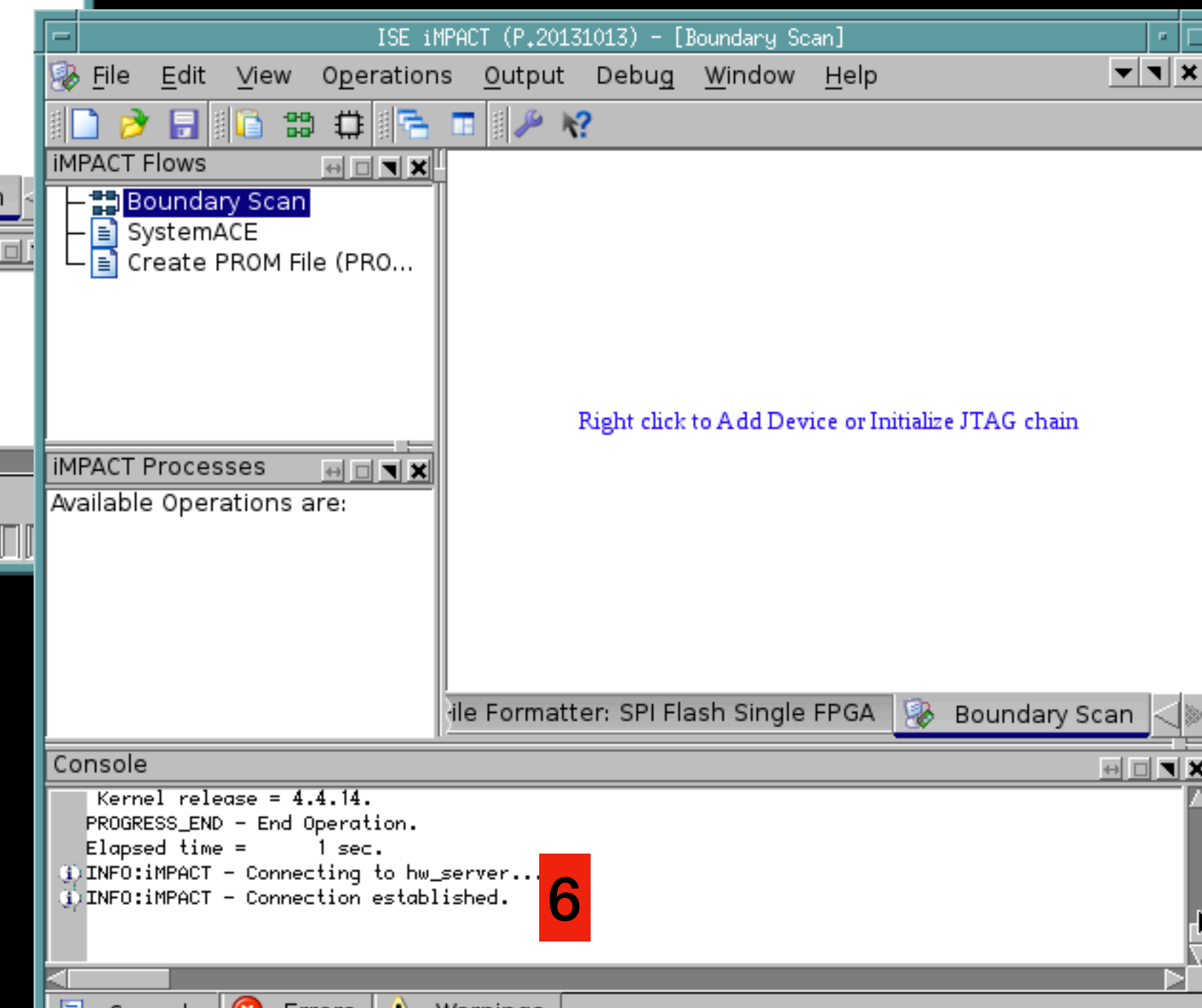
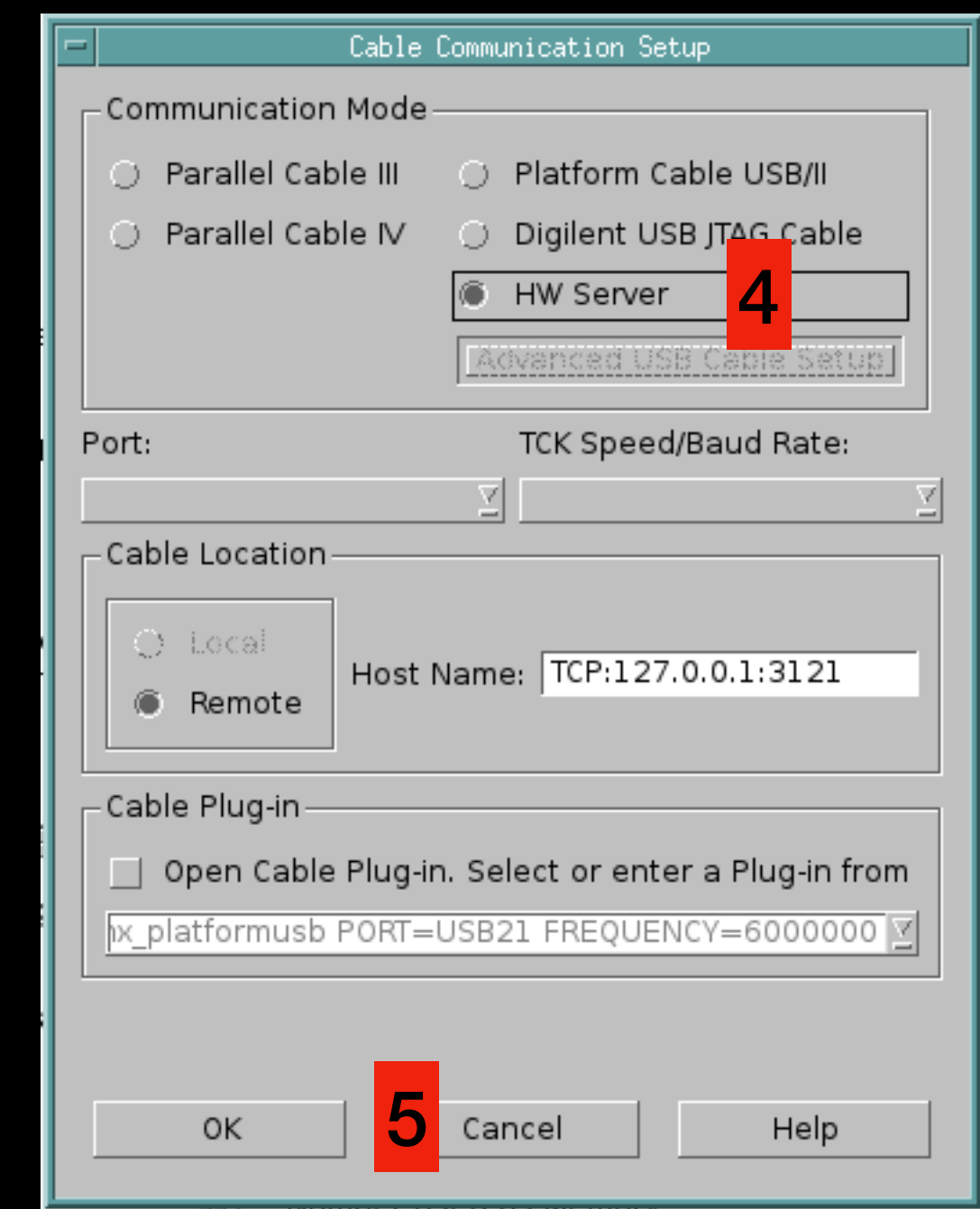
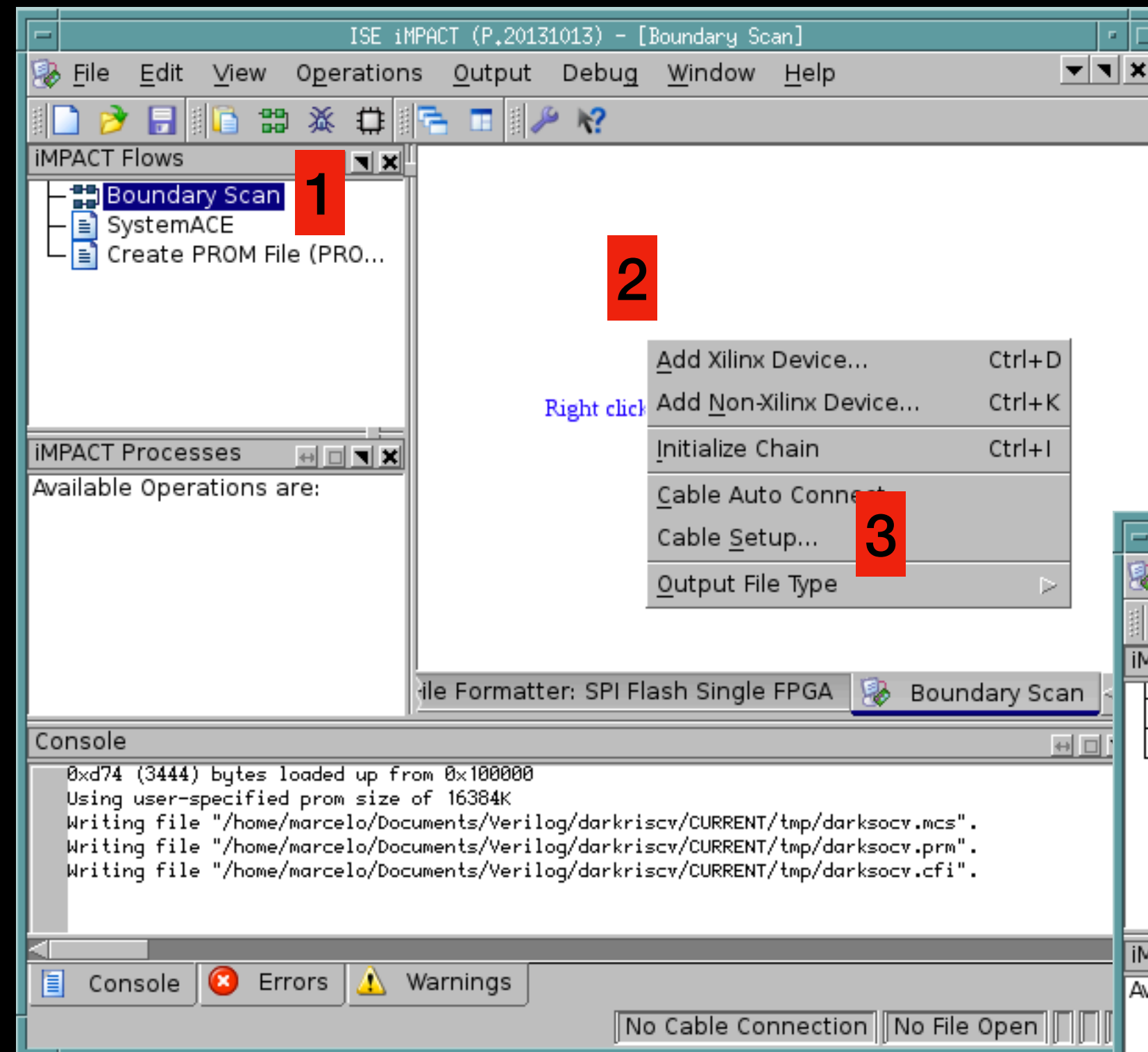
```
0xd74 (3444) bytes loaded up from 0x100000
Using user-specified prom size of 16384K
Writing file "/home/marcelo/Documents/Verilog/darkiscv/CURRENT/tmp/darksocv.mcs".
Writing file "/home/marcelo/Documents/Verilog/darkiscv/CURRENT/tmp/darksocv.prm".
Writing file "/home/marcelo/Documents/Verilog/darkiscv/CURRENT/tmp/darksocv.cfi".
```

Bottom status bar: PROM File Generation | Target SPI Flash | 2,724,832 Bits used | File: darksocv.mcs in Locati...

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Adding the JTAG adapter...

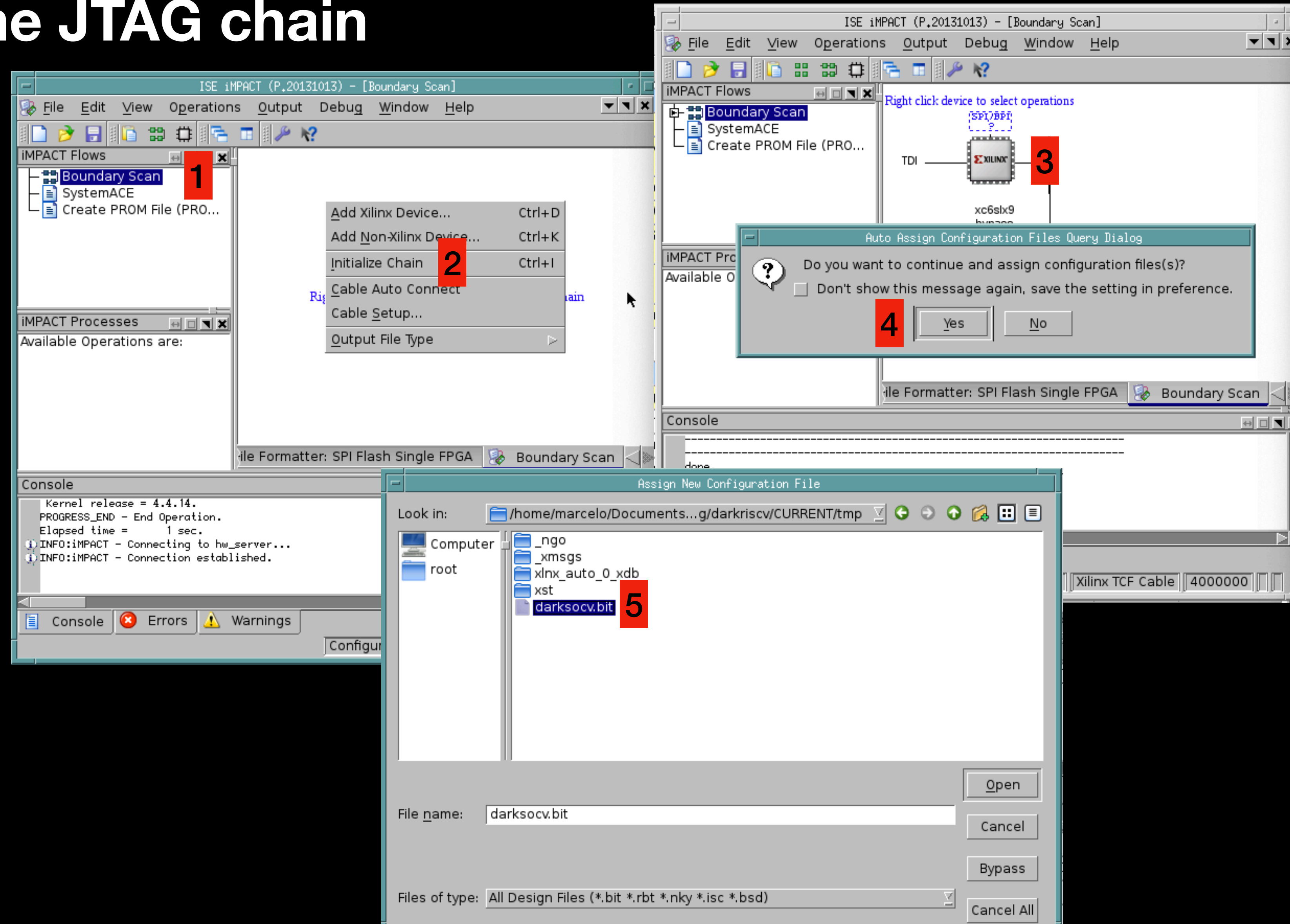
- Double-click on “Boundary Scan” (1), right click on blank space (2) and select “Cable Setup” (3).
- Select “HW Server” (4) to use the Vivado server and click “OK” (5), the Console must show “Connection established” (6)



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Adding the FPGA on the JTAG chain

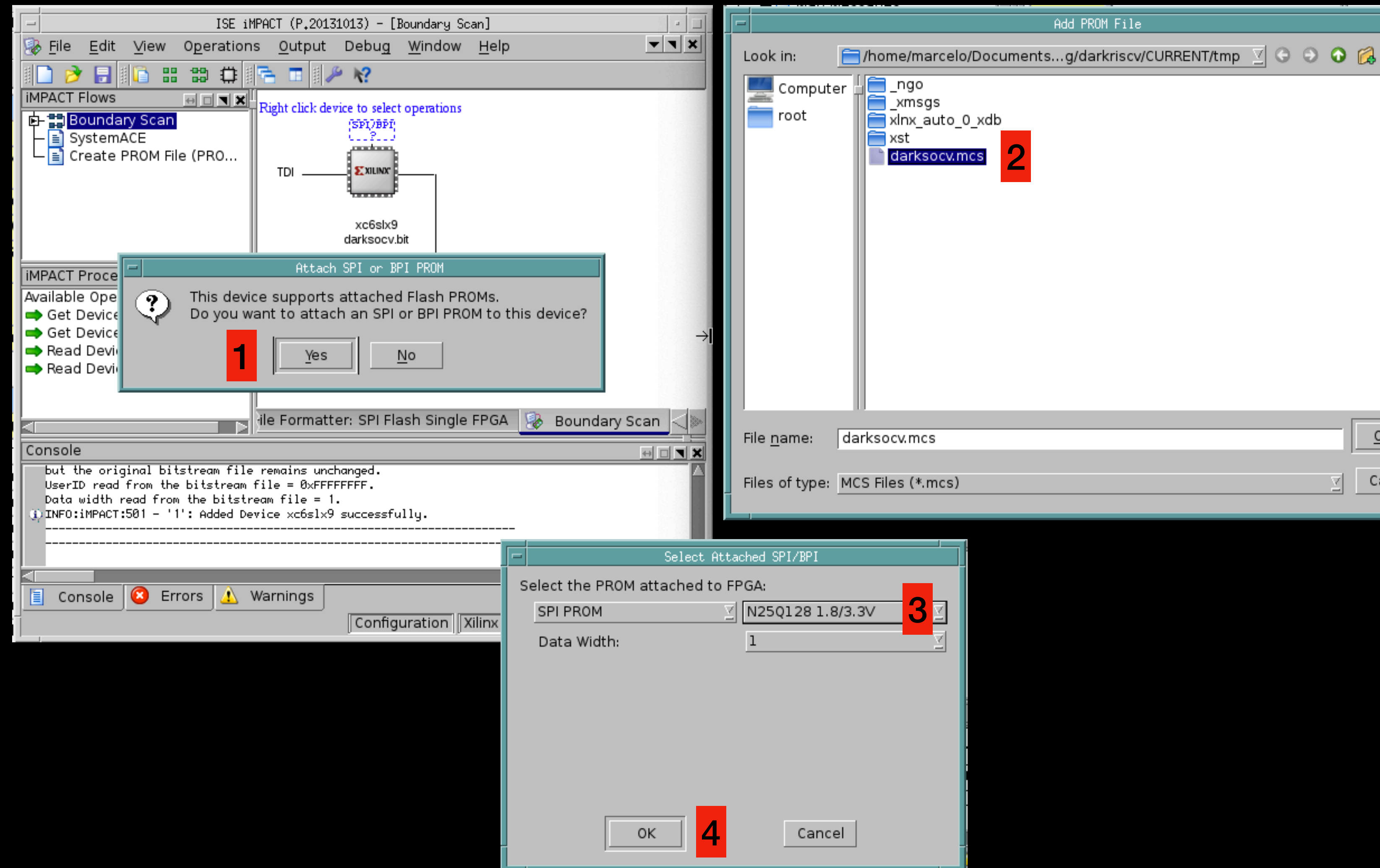
- Right click on blank area to open the menu (1) and select “Initialize Chain” (2), it will automatically identify the FPGA (3) and ask about a FPGA image, click “Yes” (4) and select the FPGA image that you generated moments before (5)



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Adding the FLASH on the JTAG chain

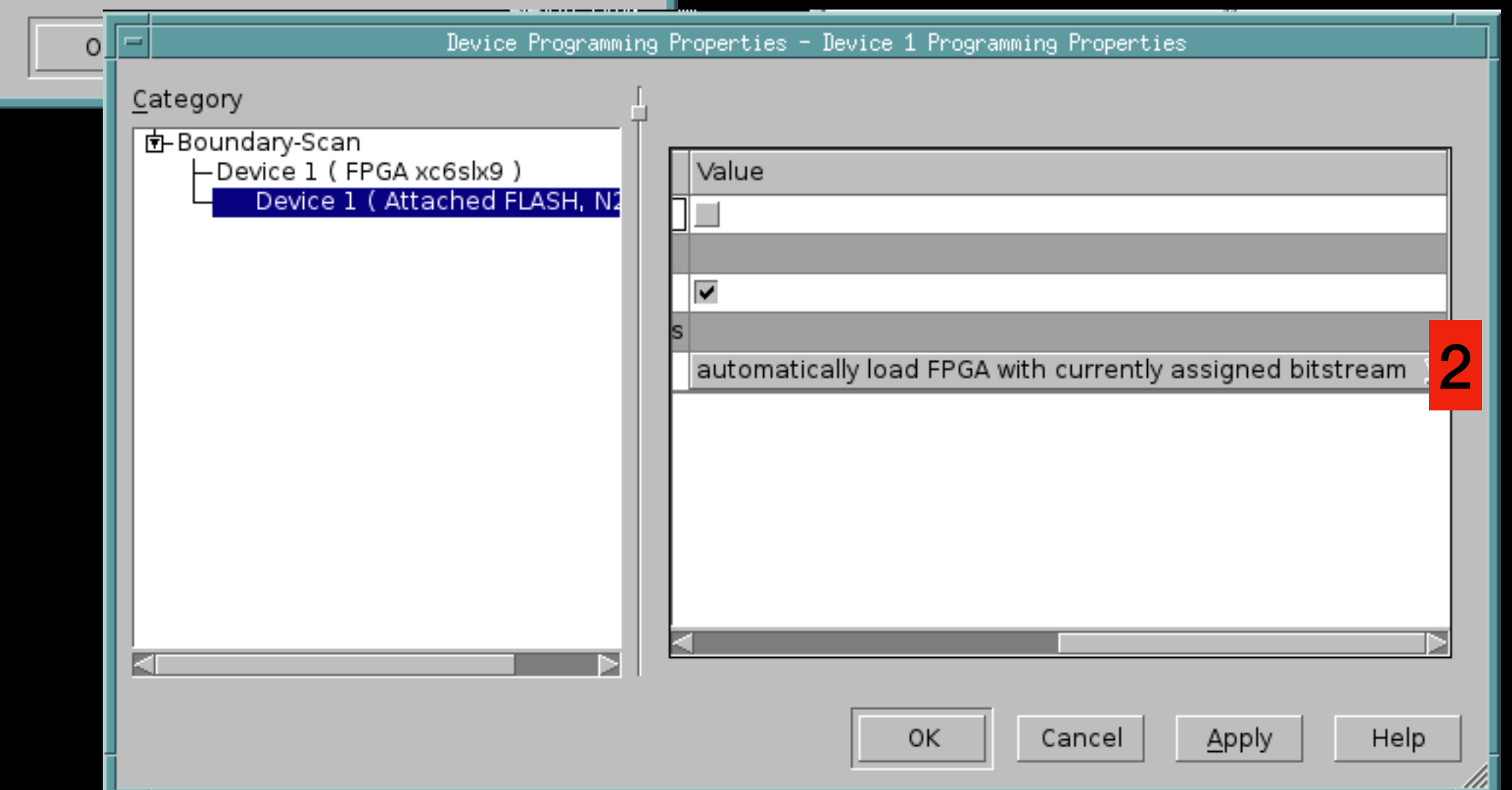
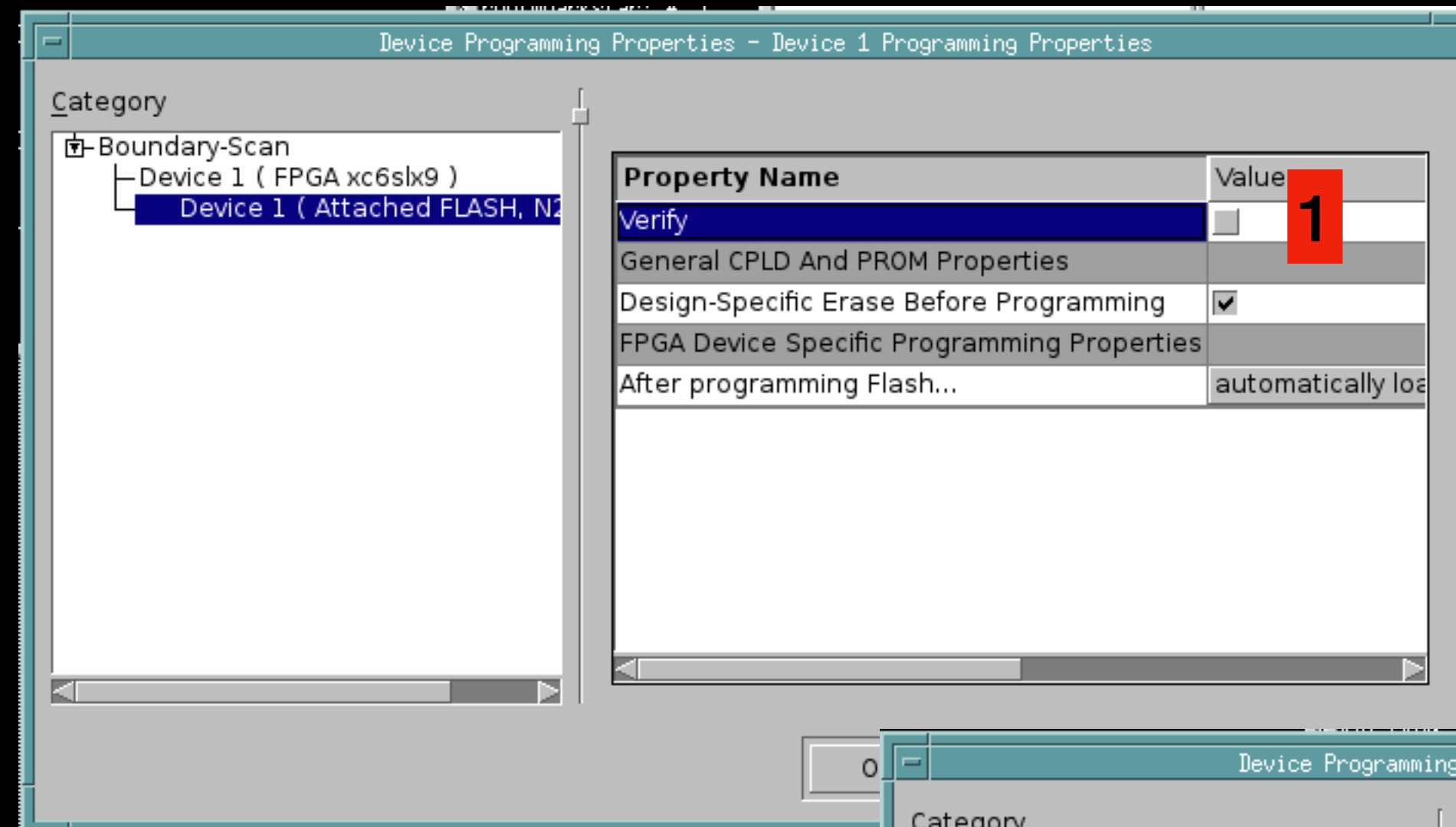
- The tool will ask about the FLASH, click “Yes” (1) and select the MCS file that you generated before (2)
- The tool will ask about the FLASH model (3), select the correct model and click “OK” (4)



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Adding the FLASH on the JTAG chain

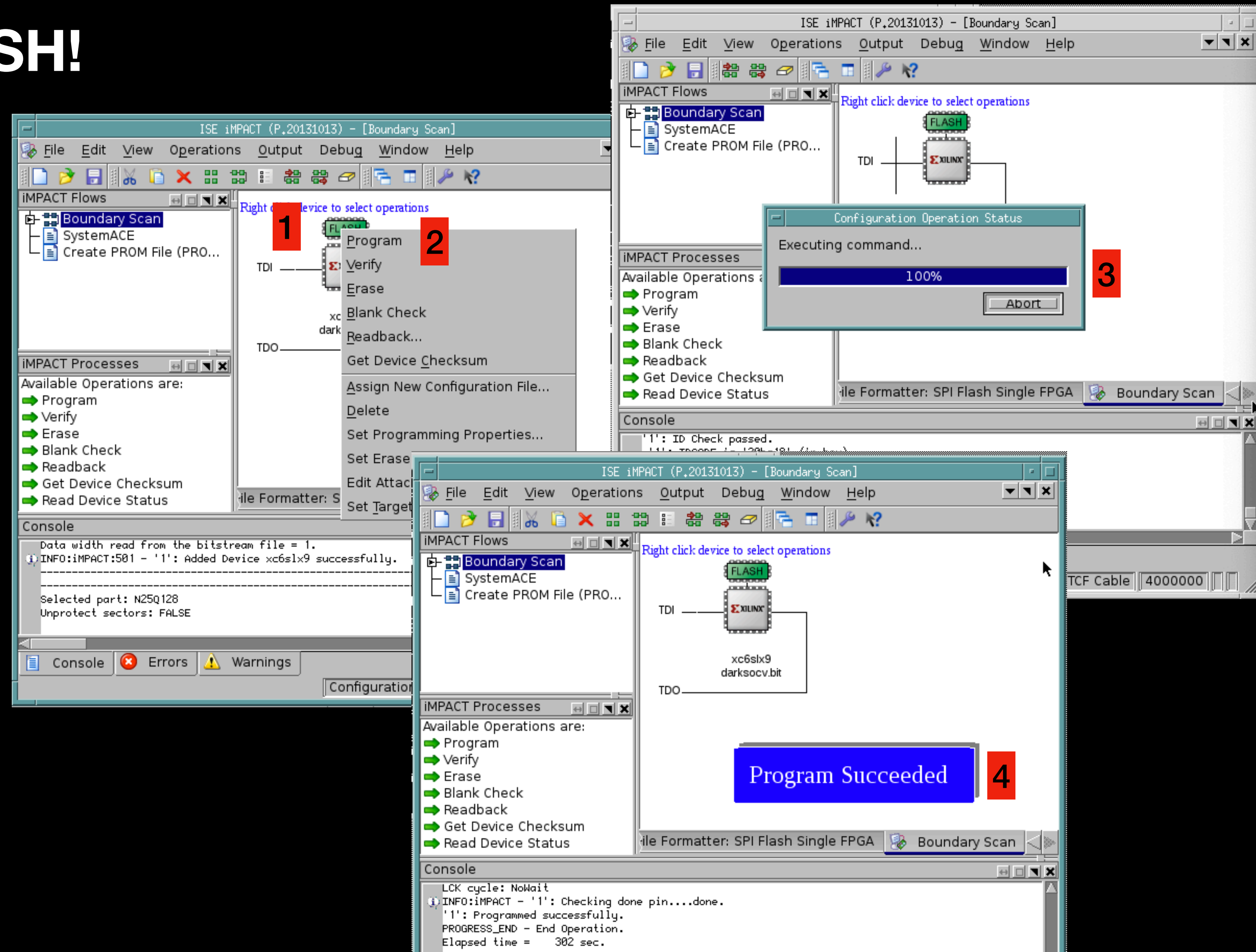
- The tool will ask about how to program the device, uncheck the “Verify” option (1) in order to make it work faster!
- You can also select to load the assigned bitstream after programming, also to make it faster (2)



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Programming the FLASH!

- Right click on the FLASH (1) to open the menu and click on “Program” (2).
- The tool will take a while to erase and program the FLASH (3)...
- When the tool is ready, it will show “Program Succeeded” (4)



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Checking the results...

- You can keep a terminal attached all time, so you can check before and after the programming...
- Just in case, reset or power cycle your board and check the compilation dates and good lucky!

Before: Nov 2021

[illegible]

After: Jul 2023

[illegible]