

MFWD

(R-Switch-3 GateWay Forwarding Engin)

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General precautions for handling of product

The following notes are applicable to entire CBIC with CPU core. For detailed usage notes, refer to the relevant sections of the manual. If the description under General precautions and in the body of the manual differs from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flow internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Regarding Clock

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized. When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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1. Overview

Forwarding engine is part of R-Switch system and aims at filtering, forwarding and routing the switch frames.

It snoops the frame information from fabric to redistribute them to the agent after filtering, forwarding and routing mechanisms.

1.1 Features

Forwarding engine Features are described in Table 1-1.

Table 1-1 Forwarding engine Feature List

Function	Details	
Overall function	Cut-through	Forwarding frames while receiving them depending on Layer 2
	Integrity check	Check frame format
	ACL filtering	Acceptance list filtering Block list filtering
	Direct forwarding	Forwarding frames coming from GWCAs by bypassing the forwarding engine [GWCA]
	Layer 3 forwarding	Forwarding frames based on a stream ID
	Layer 2 forwarding	Forwarding frames based on destination MAC addresses and VLAN
	Port based forwarding	Forwarding frames depending on source port
	L23U	Update of layer2 and Layer 3 depending on Layer 3 forwarding
	PSFP	PSFP filtering [PSFP] depending on Layer 3 forwarding
	ATS	ATS traffic shaping [ATS]
	FRER	FRER [FRER] depending on Layer 3 forwarding
Data provision	Ethernet Frames	Corresponds to the IEEE 802.3, 802.1Q and 802.1CB standards [802.3] [802.1Q] [802.1CB].
	Descriptors	Local Ethernet Descriptor, Local Direct Descriptor (Agents to Forwarding engine) Forwarding descriptor (Forwarding engine to Agents)

1.2 Forwarding Engine block diagram

Fig 1.1 shows Forwarding Engine block diagram.

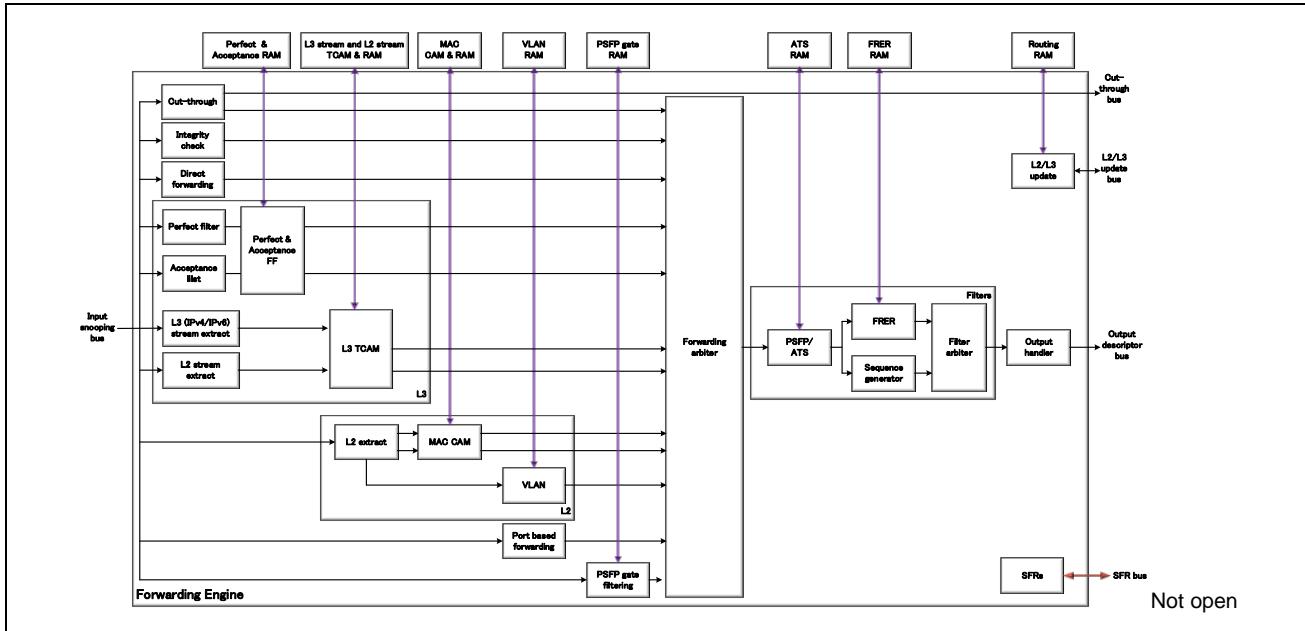


Fig 1.1: Forwarding Engine Block diagram

Table 1-2: Forwarding Engine Functional Blocks

Block name	Function
Cut-through	Filter frame L2 and send them to while receiving them.
Integrity check	Check frame formats.
Direct forwarding	Forward frames coming from a CPU with the forwarding information already present.
L3	L2~L4 Stream based forwarding/routing engine
L2	L2 switch
Port based forwarding	Source port-based forwarding
PSFP gate filtering	Gate filter for PSFP [802.1Qci]
Forwarding arbiter	Arbitrate between all the forwarding/ routing mechanisms
PSFP/ATS	Per stream filtering and policing [802.1Qci] and asynchronous traffic shaping [802.1Qcr]
FRER	Frame Replication and Elimination for Reliability [802.1CB]
Sequence generator	Sequence number generation for FRER proxy functionality [802.1CB]
Filter arbiter	Arbitrate between forwarding results and filtering results.
Output handler	Copy and send descriptors to targets. Manage overflow and security error recovery.

2. Parameter list

Forwarding Engine global parameter list is shown in Table 2-1.

Forwarding Engine local parameter list is shown in Table 2-2

Table 2-1 Global parameter list

Parameter Name	RSW3	Explanation
SFRs		
PADDR_NBR_FWD	110,592/4	Number of addresses used by Forwarding Engine SFRs[FWD] divided by 4 (bytes)
AXI master [GWCA]		
AXI_CHAIN_N	128	AXI Descriptor Chain number
Port Number [TOP]		
PORT_TSNA_N	13	TSN Agent Number [TSNA]
PORT_GWCA_N	2	CPU Agent Number [GWCA]
Local RAM [FAB]		
LCL_RAM_SZ	1024	Local RAM size in Kbytes
LCL_RAM_BSZ	128	Local RAM block size (A pointer will always link to a LOCAL_RAM_BSZ byte block size in the local RAM)
LCL_RAM_DW	512	Local RAM data bit width
LCL_DATA_SIZE	6	Local RAM data size width in byte
Frame		
FRM_TPL_W	16	Frame TPL (Total payload length) Width
FRM_PRIO_N	8	Frame priority
FRM_VCTRL_W	3	Frame VLAN control width
gPTP timer		
PTP_TN	2	gPTP timer number connected to the switch
Cut-through		
CT_CRULE_N	8	Cut-through rule number
Perfect filter		
PFL_TWBF_N	512	Two-byte filter number
PFL_THBF_N	128	Three-byte filter number
PFL_FOBF_N	512	Four-byte filter number
PFL_RAGF_N	128	Range-byte filter number
PFL_CADF_N	512	Cascade filter number
PFL_CFMF_N	7	Cascade filter mapped filter number
PFL_SID_W	135	Cascade filter stream ID
Layer3 forwarding		
LTH_STREAM_N	1024	L3 table number
TCAM_DATA_W	135	L3 TCAM data width
Routing		

Parameter Name	RSW3	Explanation
LTH_RRULE_N	2048	L3 rule number (routing number)
LTH_REMAP_N	32	L3 rule remapping number
Sequence generation [802.1CB]		
LTH_SEQGN_N	32	L3 sequence generation rule number
Hash		
LTH_RSLICE_WR_N	0	L3 hash write register slice number
LTH_RSLICE_RD_N	1	L3 hash read register slice number
PSFP[802.1Qci]		
PSFP_MSDU_N	16	PSFP MSDU filter number
PSFP_GATE_N	8	PSFP gate number
PSFP_DMTR_N	104	PSFP double bucket meter number
PSFP_SMTR_N	0	PSFP single bucket meter number
ATS[802.1Qcr]		
ATS_DESCR_N	16	Descriptor queue depth per meter in ATS table
FRER[802.1CB]		
FRER_RECE_N	128	FRER recovery entry number
FRER_HIST_LEN	14	FRER history length
FRER_RSLICE_WR_N	0	FRER write register slice number
FRER_RSLICE_RD_N	1	FRER read register slice number
Gate filter [802.1Qci]		
GATE_RAM_DP	256	PSFP gate filter RAM depth
Layer 2 forwarding		
MAC_ENTRY_N	2048	MAC table entry number
MAC_RSLICE_WR_N	0	MAC hash write register slice number
MAC_RSLICE_RD_N	1	MAC hash read register slice number
MAC_HW_LRN_N	8	MAC hardware leaning number (Number of MAC addresses that can be stored for HW learning before failing)
CAM_DATA_W	48	MAC TCAM data width
VLAN_RSLICE_WR_N	0	VLAN table write register slice number
VLAN_RSLICE_RD_N	1	VLAN table read register slice number
Counter		
COUNT_LOW_W	32	Low size Counter width
COUNT_MED_W	32	Medium size Counter width
Integrity		
INTG_ETYPE_N	8	Ether Type Filtering Number per Port
INTG_FILT_SIPA_N	1	IP Address Filtering Number per Port

Table 2-2 Local parameter list

Parameter Name	RSW3 Value	Explanation
SFRs		
PADDR_NBR_FWD_W	15	Number of addresses used by Forwarding Engine SFRs bus width [FWD]
AXI master		
AXI_CHAIN_W	7	AXI descriptor chain width
Port Number		
PORT_N	15	Port number on the switch
PORT_W	4	Port number on the switch bus width
PORT_TIME_N	13	Number of time critical ports on the switch (plugged to the Fabric time arbiter [FAB])
PORT_TIME_W	4	Time critical port number on the switch bus width
PORT_SLOW_N	2	Number of non-time critical ports on the switch (plugged to the Fabric LRU arbiter [FAB])
PORT_SLOW_W	1	Non-time critical port number on the switch bus width
PORT_FSRC_N	29	Forwarding source number
PORT_FSRC_W	5	Forwarding source number bus width
PORT_FTSRC_N	26	Forwarding time-critical source number
PORT_FTSRC_W	5	Forwarding time-critical source number bus width
Local RAM		
LCL_PTR_N	8192	Pointer number to address local RAM
LCL_PTR_W	13	Pointer width
Frame		
FRM_TIME_W	26	Cut-Through Maximum time setting (for TAS) bit width
FRM_MTN_W	5	Port number on the switch bus width
gPTP timer		
PTP_TN_W	1	gPTP timer number connected to the switch bus width
Cut-through		
CT_CRULE_W	3	Cut-through rule number bus width
CT_MTN_N	18	Cut-through multicast number
CT_MTN_W	5	Cut-through multicast number bus width
Perfect filter		
PFL_CADF_W	9	Cascade filter number bus width
PFL_TFIL_N	2560	Total filter number
PFL_TFIL_W	12	Total filter number bus width
Layer3 forwarding		
LTH_STREAM_W	10	L3 table number bus width
Routing		
LTH_RRULE_W	11	L3 rule number (routing number) bus width

Parameter Name	RSW3 Value	Explanation
PSFP[802.1Qci]		
PSFP_MSDU_W	4	PSFP MSDU filter number bus width
PSFP_GATE_W	3	PSFP gate number bus width
PSFP_MTR_N	104	PSFP meter number
PSFP_MTR_W	7	PSFP meter number bus width
PSFP_GENTRY_N	16	Maximum entry number for a gate for a running schedule
PSFP_GENTRY_W	4	Maximum entry number for a gate for a running schedule bus width
PSFP_GENTRY_W1	5	Maximum entry number for a gate for a running schedule +1 bus width
ATS[802.1Qcr]		
ATS_DESCR_W	4	Descriptor queue depth per meter in ATS table bus width
ATS_DESCR_W1	5	Descriptor queue depth per meter in ATS table +1 bus width
FRER[802.1CB]		
FRER_RECE_W	7	FRER recovery entry number bus width
FRER_HIST_LEN1	15	FRER history length + 1
FRER_HIST_LEN_W	4	FRER history length bus width
FRER_HIST_LEN_W1	4	FRER history length + 1 bus width
LTH_META_INFO_W	74	Layer 3 meta info width
LTH_RAM_DW	97	Layer 3 RAM data width
ATS_RAM_DW	199	ATS RAM data width
ATS_RAM_AW	11	ATS RAM address width
FRER_RAM_DW	64	FRER RAM data width
Gate filter[802.1Qci]		
GATE_RAM_AW	8	PSFP gate filter RAM address width
RAMs		
MAC_ENTRY_W	11	MAC table entry number bus width
MAC_META_INFO_W	78	MAC table meta width
VLAN_META_INFO_W	90	VLAN table meta width
MAC_RAM_DW	106	MAC table data width
VLAN_RAM_DW	117	VLAN table data width
L23U_RAM_DW	110	Layer2/Layer3 update table data width
PFL_META_INFO_W	90	Perfect filter meta info width
PFL_RAM_DW	116	Perfect filter RAM data width

3. Register

3.1 Register attributes

The register attribute defines what kind of access a register supports. Per one register, there are always two attributes, a register access attribute which define what kind of accesses a register supports and, a register security attribute which define what accesses can perform the unsecure APB [APB] in the register access attribute depending on the security setting in security registers.

“Representation of register access attributes” describes register access attributes and “Representation of register security attributes” describes register security attributes. Attributes are given to a register field in Register detailed explanation section by specifying the attribute symbols in the R/W-P column.

Table 3-1: Register access attributes

Symbol	Meaning	Impact on accesses	
		Write access	Read access
RW	Read write	Write value is written	Written value is read
R!=W	Read different than write	Write access happens	Read value differs from written value
R	Read only	Write value is ignored	Read access happens
R0	Only Read 0	Write value is ignored	Always read '0'
R1	Only Read 1	Write value is ignored	Always read '1'
R0W	Read 0 write	Write access happens	Always read as '0'
R1W	Read 1 write	Write access happens	Always read as '1'
RC	Read clear	Write value is ignored	Read access happens Read access clears the register

Table 3-2: Register security attributes (For R-Car products only)

Symbol	Meaning	Impact on accesses	
		Write access	Read access
U	Unprotected	Write access happens for unsecure APB	Read access happens for unsecure APB
P	Protected	A security register should be set to authorize write access by the unsecure APB.	A security register should be set to authorize read access by the unsecure APB
RU	Read-Unprotected	Write value ignored for unsecure APB	Read access happens for unsecure APB
RP	Read-Protected	Write value ignored for unsecure APB	A security register should be set to authorize read access by the unsecure APB
D	Duplicated	Write access happens for unsecure APB to a duplicated and independent register	Read access happens for unsecure APB to a duplicated and independent register
F	Forbidden	Write value ignored for unsecure APB	Read value ignored for unsecure APB
S	Switch	A security register should be set to authorize write access by the unsecure APB. A security register should be set to unauthorized write access by the secure APB.	A security register should be set to authorize read access by the unsecure APB

3.2 Register list

The Forwarding Engine register list is described in Table 3-3. FWRO (Forwarding Engine Register Offset) indicates base address of address space allocated to Forwarding Engine by the system. All registers representations are done with the default values of the section 2. If the Forwarding Engine is not use with default parameters, it should be taken in account by the user while reading the SFR representation.

Notes:

- A register can have two addresses. The address preceded by "E:" correspond to an emulation address which allows to read a register without modifying its content.

Table 3-3: List of MFWD registers

Offset/Address	Register name	Abbreviation
FWRO + 0000H	Forwarding Engine General Configuration	FWGC
FWRO + 0010H	Forwarding Engine TAG TPID Configuration 0	FWTTC0
FWRO + 0014H	Forwarding Engine TAG TPID Configuration 1	FWTTC1
FWRO + 0020H	Forwarding Engine CPU Exceptional Path Target Configuration	FWCEPTC
FWRO + 0024H	Forwarding Engine CPU Exceptional Path Reason Configuration 0	FWCEPRC0
FWRO + 0028H	Forwarding Engine CPU Exceptional Path Reason Configuration 1	FWCEPRC1
FWRO + 002CH	Forwarding Engine CPU Exceptional Path Reason Configuration 2	FWCEPRC2
FWRO + 0030H	Forwarding Engine CPU Learning Path Target Configuration	FWCLPTC
FWRO + 0034H	Forwarding Engine CPU Learning Path Reason Configuration	FWCLPRC
FWRO + 0040H	Forwarding Engine CPU Mirroring Path Target Configuration	FWCMPTC
FWRO + 0044H	Forwarding Engine CPU Mirroring Path Layer2/Layer3 Update Rule Configuration	FWCMPL23URC
FWRO + 0048H	Forwarding Engine Ethernet Mirroring Path Target Configuration	FWEMPTC
FWRO + 004CH	Forwarding Engine Ethernet Mirroring Path Layer2/Layer3 Update Rule Configuration	FWEMPL23URC
FWRO + 0050H	Forwarding Engine Source-Destination Mirroring Path Target Configuration	FWSDMPTC
FWRO + 0054H	Forwarding Engine Source-Destination Mirroring Path Vector Configuration	FWSDMPVC
FWRO + 0058H	Forwarding Engine Source-Destination Mirroring Path Layer2/Layer3 Update Rule Configuration	FWSDMPL23URC
FWRO + 0060H	Forwarding Engine Source Mirroring Path Target Configuration	FWSMPTC
FWRO + 0064H	Forwarding Engine Source Mirroring Path Vector Configuration	FWSMPVC
FWRO + 0068H	Forwarding Engine Source Mirroring Path Layer2/Layer3 Update Rule Configuration	FWSMPL23URC
FWRO + 0080H + 4H*i	Forwarding Engine Level Based WaterMark Configuration i (i=0..PORT_N-1)	FWLBWMCI
FWRO + 00C0H	Forwarding Engine IPV Based WaterMark Configuration	FWIBWMC
FWRO + 0100H + 10H*i	Forwarding Engine Port Configuration 0 i (i=0..PORT_N-1)	FWPC0i
FWRO + 0104H + 10H*i	Forwarding Engine Port Configuration 1 i (i=0..PORT_N-1)	FWPC1i
FWRO + 0108H + 10H*i	Forwarding Engine Port Configuration 2 i (i=0..PORT_N-1)	FWPC2i
FWRO + 010CH + 10H*i	Forwarding Engine Port Configuration 3 i (i=0..PORT_N-1)	FWPC3i
FWRO + 0200H + 20H*i + 4H*j	Forwarding Engine Port i and IPV j Filtering Priority and Information i (i=0..PORT_N-1) (j=0..FRM_PRIO_N-1)	FWPIFPIlj
FWRO + 0400H + 70H*i	Forwarding Engine Cut-Through General Configuration 0 i (i=0..CT_CRULE_N-1)	FWCTGC0i
FWRO + 0404H + 70H*i	Forwarding Engine Cut-Through General Configuration 1 i (i=0..CT_CRULE_N-1)	FWCTGC1i
FWRO + 0408H + 70H*i	Forwarding Engine Cut-Through Target Configuration 0 i (i=0..CT_CRULE_N-1)	FWCTTC0i
FWRO + 040CH + 70H*i	Forwarding Engine Cut-Through Target Configuration 1 i (i=0..CT_CRULE_N-1)	FWCTTC1i
FWRO + 0410H + 70H*i + 4H*j	Forwarding Engine Cut-Through Target Configuration 2 j i (j=0..PORT_GWCA_N-1) (i=0..CT_CRULE_N-1)	FWCTTC2ji
FWRO + 0450H + 70H*i	Forwarding Engine Cut-Through Separation Configuration 0 i (i=0..CT_CRULE_N-1)	FWCTSC0i
FWRO + 0454H + 70H*i	Forwarding Engine Cut-Through Separation Configuration 1 i (i=0..CT_CRULE_N-1)	FWCTSC1i
FWRO + 0458H + 70H*i	Forwarding Engine Cut-Through Separation Configuration 2 i (i=0..CT_CRULE_N-1)	FWCTSC2i
FWRO + 045CH + 70H*i	Forwarding Engine Cut-Through Separation Configuration 3 i (i=0..CT_CRULE_N-1)	FWCTSC3i

Offset/Address	Register name	Abbreviation
FWRO + 0460H + 70H*i	Forwarding Engine Cut-Through Separation Configuration 4 i (i= 0..CT_CRULE_N-1)	FWCTSC4i
FWRO + 0800H + 40H*i	Forwarding Engine Integrity Check Ethernet Type Configuration 1 i (i=0..PORT_N-1)	FWICETC1i
FWRO + 0804H + 40H*i	Forwarding Engine Integrity Check IPv4 Configuration i (i=0..PORT_N-1)	FWICIP4Ci
FWRO + 0808H + 40H*i	Forwarding Engine IPv4 Address Configuration i (i=0..PORT_N-1)	FWIP4ACi
FWRO + 080CH + 40H*i	Forwarding Engine Integrity Check IPv6 Configuration i (i=0..PORT_N-1)	FWICIP6Ci
FWRO + 0810H + 40H*i	Forwarding Engine IPv6 Address Configuration 0 i (i=0..PORT_N-1)	FWIP6AC0i
FWRO + 0814H + 40H*i	Forwarding Engine IPv6 Address Configuration 1 i (i=0..PORT_N-1)	FWIP6AC1i
FWRO + 0818H + 40H*i	Forwarding Engine IPv6 Address Configuration 2 i (i=0..PORT_N-1)	FWIP6AC2i
FWRO + 081CH + 40H*i	Forwarding Engine IPv6 Address Configuration 3 i (i=0..PORT_N-1)	FWIP6AC3i
FWRO + 0820H + 40H*i	Forwarding Engine IPv4 IP Address Prefix Configuration i (i=0..PORT_N-1)	FWIP4APCi
FWRO + 0824H + 40H*i	Forwarding Engine IPv6 IP Address Prefix Configuration i (i=0..PORT_N-1)	FWIP6APCi
FWRO + 1000H + 200H*i	Forwarding Engine Integrity Check Ethernet Type Configuration 2 i (i=0..PORT_N-1)	FWICETC2i
FWRO + 1010H + 200H*i + 4H*j	Forwarding Engine Integrity Check Ethernet Type Configuration 3 i j (i=0..PORT_N-1) (j=0..INTGETYPE_N/2-1)	FWICETC3ij
FWRO + 1050H + 200H*i + 4H*j	Forwarding Engine IPv4 Filtering Address Configuration i j (i=0..PORT_N-1) (j=0..INTGFILT_SIPA_N-1)	FWIP4FACij
FWRO + 1070H + 200H*i + 4H*j	Forwarding Engine IPv4 Specified Filter Configuration i j (i=0..PORT_N-1) (j=0..INTGFILT_SIPA_N-1)	FWIP4SFCij
FWRO + 1090H + 200H*i + 4H*j	Forwarding Engine IPv6 Filtering Address Configuration 0 i j (i=0..PORT_N-1) (j=0..INTGFILT_SIPA_N-1)	FWIP6FAC0ij
FWRO + 10B0H + 200H*i + 4H*j	Forwarding Engine IPv6 Filtering Address Configuration 1 i j (i=0..PORT_N-1) (j=0..INTGFILT_SIPA_N-1)	FWIP6FAC1ij
FWRO + 10D0H + 200H*i + 4H*j	Forwarding Engine IPv6 Filtering Address Configuration 2 i j (i=0..PORT_N-1) (j=0..INTGFILT_SIPA_N-1)	FWIP6FAC2ij
FWRO + 10F0H + 200H*i + 4H*j	Forwarding Engine IPv6 Filtering Address Configuration 3 i j (i=0..PORT_N-1) (j=0..INTGFILT_SIPA_N-1)	FWIP6FAC3ij
FWRO + 1110H + 200H*i + 4H*j	Forwarding Engine IPv6 Specified Filter Configuration i j (i=0..PORT_N-1) (j=0..INTGFILT_SIPA_N-1)	FWIP6SFCij
FWRO + 1130H + 200H*i	Forwarding Engine Ipv4 Total Length Check Configuration i (i=0..PORT_N-1)	FWIP4TLCCI
FWRO + 1134H + 200H*i	Forwarding Engine Ipv6 Payload Length Check Configuration i (i=0..PORT_N-1)	FWIP6PLCCI
FWRO + 1140H + 200H*i	Forwarding Engine Integrity Check Layer 4 Configuration i (i=0..PORT_N-1)	FWICL4Ci
FWRO + 1144H + 200H*i	Forwarding Engine Integrity Check Layer 4 TCP Header Length Configuration i (i=0..PORT_N-1)	FWICL4THLCi
FWRO + 4008H	Forwarding Engine IPv4 Stream Configuration	FWIP4SC
FWRO + 4018H	Forwarding Engine IPv6 Stream Configuration	FWIP6SC
FWRO + 401CH	Forwarding Engine IPv6 Offset Configuration	FWIP6OC
FWRO + 4020H	Forwarding Engine Layer 2 Stream Configuration	FWL2SC
FWRO + 4030H	Forwarding Engine Stream Filter Hash Equation Configuration	FWSFHEC
FWRO + 4040H	Forwarding Engine Software Hash Calculation Request 0	FWSHCR0
FWRO + 4044H	Forwarding Engine Software Hash Calculation Request 1	FWSHCR1
FWRO + 4048H	Forwarding Engine Software Hash Calculation Request 2	FWSHCR2
FWRO + 404CH	Forwarding Engine Software Hash Calculation Request 3	FWSHCR3
FWRO + 4050H	Forwarding Engine Software Hash Calculation Request 4	FWSHCR4
FWRO + 4054H	Forwarding Engine Software Hash Calculation Request 5	FWSHCR5
FWRO + 4058H	Forwarding Engine Software Hash Calculation Request 6	FWSHCR6
FWRO + 405CH	Forwarding Engine Software Hash Calculation Request 7	FWSHCR7
FWRO + 4060H	Forwarding Engine Software Hash Calculation Request 8	FWSHCR8
FWRO + 4064H	Forwarding Engine Software Hash Calculation Request 9	FWSHCR9
FWRO + 4068H	Forwarding Engine Software Hash Calculation Request 10	FWSHCR10
FWRO + 406CH	Forwarding Engine Software Hash Calculation Request 11	FWSHCR11
FWRO + 4070H	Forwarding Engine Software Hash Calculation Request 12	FWSHCR12
FWRO + 4074H	Forwarding Engine Software Hash Calculation Request 13	FWSHCR13
FWRO + 4078H	Forwarding Engine Software Hash Calculation Request Result	FWSHCR
FWRO + 4090H	Forwarding Engine L3 Table Entry Configuration 0	FWLTHTEC0
FWRO + 4094H	Forwarding Engine L3 Table Entry Configuration 1	FWLTHTEC1
FWRO + 40A0H	Forwarding Engine L3 Table Learn 0	FWLHTHLO

Offset/Address	Register name	Abbreviation
FWRO + 40A4H	Forwarding Engine L3 Table Learn 1	FWLTHTL1
FWRO + 40A8H	Forwarding Engine L3 Table Learn 2	FWLTHTL2
FWRO + 40A8CH	Forwarding Engine L3 Table Learn 3	FWLTHTL3
FWRO + 40B0H	Forwarding Engine L3 Table Learn 4	FWLTHTL4
FWRO + 40B4H	Forwarding Engine L3 Table Learn 5	FWLTHTL5
FWRO + 40B8H	Forwarding Engine L3 Table Learn 6	FWLTHTL6
FWRO + 40BCH	Forwarding Engine L3 Table Learn 7	FWLTHTL7
FWRO + 40C0H	Forwarding Engine L3 Table Learn 8	FWLTHTL8
FWRO + 40C4H	Forwarding Engine L3 Table Learn 9	FWLTHTL9
FWRO + 40C8H	Forwarding Engine L3 Table Learn 10	FWLTHTL10
FWRO + 40CCH	Forwarding Engine L3 Table Learn 11	FWLTHTL11
FWRO + 40D0H	Forwarding Engine L3 Table Learn 12	FWLTHTL12
FWRO + 40D4H + 4H*i	Forwarding Engine L3 Table Learn 13 i (i=0..PORT_GWCA_N-1)	FWLTHTL13i
FWRO + 4114H	Forwarding Engine L3 Table Learn 14	FWLTHTL14
FWRO + 4118H	Forwarding Engine L3 Table Learn 15	FWLTHTL15
FWRO + 411CH	Forwarding Engine L3 Table Learn Result	FWLTHTLR
FWRO + 4120H	Forwarding Engine L3 Table Initialization Monitoring	FWLTHTIM
FWRO + 4124H	Forwarding Engine L3 Table Entry Monitoring 0	FWLTHTEMO
FWRO + 4128H	Forwarding Engine L3 Table Entry Monitoring 1	FWLTHTEM1
FWRO + 4130H	Forwarding Engine L3 Table Search 0	FWLHTS0
FWRO + 4134H	Forwarding Engine L3 Table Search 1	FWLHTS1
FWRO + 4138H	Forwarding Engine L3 Table Search 2	FWLHTS2
FWRO + 413CH	Forwarding Engine L3 Table Search 3	FWLHTS3
FWRO + 4140H	Forwarding Engine L3 Table Search 4	FWLHTS4
FWRO + 4144H	Forwarding Engine L3 Table Search 5	FWLHTS5
FWRO + 4148H	Forwarding Engine L3 Table Search 6	FWLHTS6
FWRO + 4150H	Forwarding Engine L3 Table Search Result 0	FWLHTSR0
FWRO + 4154H	Forwarding Engine L3 Table Search Result 1	FWLHTSR1
FWRO + 4158H	Forwarding Engine L3 Table Search Result 2	FWLHTSR2
FWRO + 415CH	Forwarding Engine L3 Table Search Result 3	FWLHTSR3
FWRO + 4160H + 4H*i	Forwarding Engine L3 Table Search Result 4 i (i=0..PORT_GWCA_N-1)	FWLHTSR4i
FWRO + 41A0H	Forwarding Engine L3 Table Search Result 5	FWLHTSR5
FWRO + 41A4H	Forwarding Engine L3 Table Search Result 6	FWLHTSR6
FWRO + 41A8H	Forwarding Engine L3 Table Search Result 7	FWLHTSR7
FWRO + 41B0H	Forwarding Engine L3 Table Read	FWLHTTR
FWRO + 41B4H	Forwarding Engine L3 Table Read Result 0	FWLHTRR0
FWRO + 41B8H	Forwarding Engine L3 Table Read Result 1	FWLHTRR1
FWRO + 41BCH	Forwarding Engine L3 Table Read Result 2	FWLHTRR2
FWRO + 41C0H	Forwarding Engine L3 Table Read Result 3	FWLHTRR3
FWRO + 41C4H	Forwarding Engine L3 Table Read Result 4	FWLHTRR4
FWRO + 41C8H	Forwarding Engine L3 Table Read Result 5	FWLHTRR5
FWRO + 41CCH	Forwarding Engine L3 Table Read Result 6	FWLHTRR6
FWRO + 41D0H	Forwarding Engine L3 Table Read Result 7	FWLHTRR7
FWRO + 41D4H	Forwarding Engine L3 Table Read Result 8	FWLHTRR8
FWRO + 41D8H	Forwarding Engine L3 Table Read Result 9	FWLHTRR9
FWRO + 41DCH	Forwarding Engine L3 Table Read Result 10	FWLHTRR10
FWRO + 41E0H	Forwarding Engine L3 Table Read Result 11	FWLHTRR11

Offset/Address	Register name	Abbreviation
FWRO + 41E4H	Forwarding Engine L3 Table Read Result 12	FWLTHTRR12
FWRO + 41E8H + 4Hi	Forwarding Engine L3 Table Read Result 13 i (i=0..PORT_GWCA_N-1)	FWLTHTRR13i
FWRO + 4218H	Forwarding Engine L3 Table Read Result 14	FWLTHTRR14
FWRO + 421CH	Forwarding Engine L3 Table Read Result 15	FWLTHTRR15
FWRO + 4300H	Forwarding Engine L3 REcovery US Prescaler Configuration	FWLTHREUSPC
FWRO + 4304H	Forwarding Engine L3 REcovery Configuration	FWLTHREC
FWRO + 4308H	Forwarding Engine L3 REcovery Monitoring	FWLTHREM
FWRO + 4600H	Forwarding Engine MAC Table Entry Configuration 0	FWMACTEC0
FWRO + 4610H	Forwarding Engine MAC Table Learn 0	FWMACTL0
FWRO + 4614H	Forwarding Engine MAC Table Learn 1	FWMACTL1
FWRO + 4618H	Forwarding Engine MAC Table Learn 2	FWMACTL2
FWRO + 461CH	Forwarding Engine MAC Table Learn 3	FWMACTL3
FWRO + 4620H	Forwarding Engine MAC Table Learn 4	FWMACTL4
FWRO + 4624H	Forwarding Engine MAC Table Learn 5	FWMACTL5
FWRO + 4628H	Forwarding Engine MAC Table Learn 6	FWMACTL6
FWRO + 462CH + 4Hi	Forwarding Engine MAC Table Learn 7 i (i=0..PORT_GWCA_N-1)	FWMACTL7i
FWRO + 466CH	Forwarding Engine MAC Table Learn 8	FWMACTL8
FWRO + 4670H	Forwarding Engine MAC Table Learn Result	FWMACTLR
FWRO + 4680H	Forwarding Engine MAC Table Initialization Monitoring	FWMACTIM
FWRO + 4684H	Forwarding Engine MAC Table Entry Monitoring	FWMACTEM
FWRO + 4690H	Forwarding Engine MAC Table Search 0	FWMACTS0
FWRO + 4694H	Forwarding Engine MAC Table Search 1	FWMACTS1
FWRO + 4698H	Forwarding Engine MAC Table Search 2	FWMACTS2
FWRO + 469CH	Forwarding Engine MAC Table Search 3	FWMACTS3
FWRO + 46A0H	Forwarding Engine MAC Table Search Result 0	FWMACTSR0
FWRO + 46A4H	Forwarding Engine MAC Table Search Result 1	FWMACTSR1
FWRO + 46A8H + 4Hi	Forwarding Engine MAC Table Search Result 2 i (i=0..PORT_GWCA_N-1)	FWMACTSR2i
FWRO + 46E8H	Forwarding Engine MAC Table Search Result 3	FWMACTSR3
FWRO + 46F0H	Forwarding Engine MAC Table Search Result 4	FWMACTSR4
FWRO + 46F4H	Forwarding Engine MAC Table Search Result 5	FWMACTSR5
FWRO + 46F8H	Forwarding Engine MAC Table Search Result 6	FWMACTSR6
FWRO + 4700H	Forwarding Engine MAC Table Read	FWMACTR
FWRO + 4710H	Forwarding Engine MAC Table Read Result 0	FWMACTRR0
FWRO + 4714H	Forwarding Engine MAC Table Read Result 1	FWMACTRR1
FWRO + 4718H	Forwarding Engine MAC Table Read Result 2	FWMACTRR2
FWRO + 471CH	Forwarding Engine MAC Table Read Result 3	FWMACTRR3
FWRO + 4720H	Forwarding Engine MAC Table Read Result 4	FWMACTRR4
FWRO + 4724H	Forwarding Engine MAC Table Read Result 5	FWMACTRR5
FWRO + 4728H	Forwarding Engine MAC Table Read Result 6	FWMACTRR6
FWRO + 472CH + 4Hi	Forwarding Engine MAC Table Read Result 7 i (i=0..PORT_GWCA_N-1)	FWMACTRR7i
FWRO + 476CH	Forwarding Engine MAC Table Read Result 8	FWMACTRR8
FWRO + 4800H	Forwarding Engine MAC Table HW Learning Configuration 0	FWMACHWLCO
FWRO + 4804H	Forwarding Engine MAC Table HW Learning Configuration 1	FWMACHWLCL
FWRO + 4810H + 4Hi	Forwarding Engine MAC Table HW Learning Configuration 2 i (i=0..PORT_N -1)	FWMACHWLCL2i
FWRO + 4880H	Forwarding Engine MAC AGing US Prescaler Configuration	FWMACAGUSPC
FWRO + 4884H	Forwarding Engine MAC AGing Configuration	FWMACAGC
FWRO + 4888H	Forwarding Engine MAC AGing Monitoring 0	FWMACAGM0

Offset/Address	Register name	Abbreviation
FWRO + 488CH	Forwarding Engine MAC AGing Monitoring 1	FWMACAGM1
FWRO + 4890H	Forwarding Engine MAC REcovery US Prescaler Configuration	FWMACREUSPC
FWRO + 4894H	Forwarding Engine MAC REcovery Configuration	FWMACREC
FWRO + 4898H	Forwarding Engine MAC REcovery Monitoring	FWMACREM
FWRO + 4900H	Forwarding Engine VLAN Table Entry Configuration	FWVLANTEC
FWRO + 4910H	Forwarding Engine VLAN Table Learn 0	FWVLANTL0
FWRO + 4914H	Forwarding Engine VLAN Table Learn 1	FWVLANTL1
FWRO + 4918H	Forwarding Engine VLAN Table Learn 2	FWVLANTL2
FWRO + 491CH	Forwarding Engine VLAN Table Learn 3	FWVLANTL3
FWRO + 4920H	Forwarding Engine VLAN Table Learn 4	FWVLANTL4
FWRO + 4924H	Forwarding Engine VLAN Table Learn 5	FWVLANTL5
FWRO + 4928H + 4H*i	Forwarding Engine VLAN Table Learn 6 i (i=0..PORT_GWCA_N-1)	FWVLANTL6i
FWRO + 4968H	Forwarding Engine VLAN Table Learn 7	FWVLANTL7
FWRO + 496CH	Forwarding Engine VLAN Table Learn Result	FWVLANTLR
FWRO + 4970H	Forwarding Engine VLAN Table Initialization Monitoring	FWVLANTIM
FWRO + 4974H	Forwarding Engine VLAN Table Entry Monitoring	FWVLANTEM
FWRO + 4980H	Forwarding Engine VLAN Table Search	FWVLANTS
FWRO + 4984H	Forwarding Engine VLAN Table Search Result 0	FWVLANTSRO
FWRO + 4988H	Forwarding Engine VLAN Table Search Result 1	FWVLANTSRI
FWRO + 498CH	Forwarding Engine VLAN Table Search Result 2	FWVLANTSRI2
FWRO + 4990H	Forwarding Engine VLAN Table Search Result 3	FWVLANTSRI3
FWRO + 4994H	Forwarding Engine VLAN Table Search Result 4	FWVLANTSRI4
FWRO + 4998H + 4H*i	Forwarding Engine VLAN Table Search Result 5 i (i=0..PORT_GWCA_N-1)	FWVLANTSRI5i
FWRO + 49C8H	Forwarding Engine VLAN Table Search Result 6	FWVLANTSRI6
FWRO + 4A00H + 10H*i	Forwarding Engine Port Based Forwarding Configuration 0 i (i=0..PORT_N)	FWPBFC0i
FWRO + 4A04H + 10H*i	Forwarding Engine Port Based Forwarding Configuration 1 i (i=0..PORT_N)	FWPBFC1i
FWRO + 4B00H + 20H*i + 4H*j [note] PORT_GWCA_N was limited by j=8.	Forwarding Engine Port Based Forwarding CSD Configuration j i (j=0..PORT_GWCA_N-1) (i=0..PORT_N-1)	FWPBFCSDCji
FWRO + 4E00H	Forwarding Engine Layer2/Layer3 Update Rule Learn 0	FWL23URL0
FWRO + 4E04H	Forwarding Engine Layer2/Layer3 Update Rule Learn 1	FWL23URL1
FWRO + 4E08H	Forwarding Engine Layer2/Layer3 Update Rule Learn 2	FWL23URL2
FWRO + 4E0CH	Forwarding Engine Layer2/Layer3 Update Rule Learn 3	FWL23URL3
FWRO + 4E10H	Forwarding Engine Layer2/Layer3 Update Rule Learn Result	FWL23URLR
FWRO + 4E20H	Forwarding Engine Layer2/Layer3 Update Table Initialization Monitoring	FWL23UTIM
FWRO + 4E30H	Forwarding Engine Layer2/Layer3 Update Rule Read	FWL23URR
FWRO + 4E34H	Forwarding Engine Layer2/Layer3 Update Rule Read Result 0	FWL23URRR0
FWRO + 4E38H	Forwarding Engine Layer2/Layer3 Update Rule Read Result 1	FWL23URRR1
FWRO + 4E3CH	Forwarding Engine Layer2/Layer3 Update Rule Read Result 2	FWL23URRR2
FWRO + 4E40H	Forwarding Engine Layer2/Layer3 Update Rule Read Result 3	FWL23URRR3
FWRO + 4F00H + 4H*i	Forwarding Engine Layer2/Layer3 Update ReMapping Configuration i (i=0..LTH_REMAP_N)	FWL23URMCi
FWRO + 5000H + 4H*i	Forwarding Engine PSFP MSDU Filter Global Configuration i (i=0..PSFP_MSDU_N-1)	FWPMFGCi
FWRO + 5100H + 40H*i	Forwarding Engine PSFP Gate Filter Configuration i (i=0..PSFP_GATE_N-1)	FWPGFCi
FWRO + 5104H + 40H*i	Forwarding Engine PSFP Gate Filter Initial Gate State Configuration i (i=0..PSFP_GATE_N-1)	FWPGFIGSci
FWRO + 5108H + 40H*i	Forwarding Engine PSFP Gate Filter Entry Number Configuration i (i=0..PSFP_GATE_N-1)	FWPGFENCI
FWRO + 510CH + 40H*i	Forwarding Engine PSFP Gate Filter Entry Number Monitoring i (i=0..PSFP_GATE_N-1)	FWPGFENMI
FWRO + 5110H + 40H*i	Forwarding Engine PSFP Gate Filter Cycle Start Time Configuration 0 i (i=0..PSFP_GATE_N-1)	FWPGFCSTC0i
FWRO + 5114H + 40H*i	Forwarding Engine PSFP Gate Filter Cycle Start Time Configuration 1 i (i=0..PSFP_GATE_N-1)	FWPGFCSTC1i

Offset/Address	Register name	Abbreviation
FWRO + 5118H + 40H*i	Forwarding Engine PSFP Gate Filter Cycle Start Time Monitoring 0 i (i=0..PSFP_GATE_N-1)	FWPGFCSTM0i
FWRO + 511CH + 40H*i	Forwarding Engine PSFP Gate Filter Cycle Start Time Monitoring 1 i (i=0..PSFP_GATE_N-1)	FWPGFCSTM1i
FWRO + 5120H + 40H*i	Forwarding Engine PSFP Gate Filter Cycle Time Configuration i (i=0..PSFP_GATE_N-1)	FWPGFCTCi
FWRO + 5124H + 40H*i	Forwarding Engine PSFP Gate Filter Cycle Time Monitoring i (i=0..PSFP_GATE_N-1)	FWPGFCTMi
FWRO + 5128H + 40H*i	Forwarding Engine PSFP Gate Filter Hardware Calibration Configuration i (i=0..PSFP_GATE_N-1)	FWPGFHCCI
FWRO + 512CH + 40H*i	Forwarding Engine PSFP Gate Filter Status Monitoring i (i=0..PSFP_GATE_N-1)	FWPGFSMi
FWRO + 5130H + 40H*i	Forwarding Engine PSFP Gate Filter Global Configuration i (i=0..PSFP_GATE_N-1)	FWPGFGCi
FWRO + 5500H	Forwarding Engine PSFP Gate Filter Gate Learn 0	FWPGFGL0
FWRO + 5504H	Forwarding Engine PSFP Gate Filter Gate Learn 1	FWPGFGL1
FWRO + 5508H	Forwarding Engine PSFP Gate Filter Gate Learn Result	FWPGFGLR
FWRO + 5510H	Forwarding Engine PSFP Gate Filter Gate Read	FWPGFGR
FWRO + 5514H	Forwarding Engine PSFP Gate Filter Read Result 0	FWPGFRR0
FWRO + 5518H	Forwarding Engine PSFP Gate Filter Read Result 1	FWPGFRR1
FWRO + 5520H	Forwarding Engine PSFP Gate Filter RAM Initialization Monitoring	FWPGFRIM
FWRO + 1_8000H + 20H*i	Forwarding Engine PSFP MeTeR Filter Configuration i (i=0..PSFP_MTR_N-1)	FWPMTRFCi
FWRO + 1_8004H + 20H*i	Forwarding Engine PSFP MeTeR CBS Configuration i (i=0..PSFP_MTR_N-1)	FWPMTRCBSci
FWRO + 1_8008H + 20H*i	Forwarding Engine PSFP MeTeR CIR Configuration i (i=0..PSFP_MTR_N-1)	FWPMTRCIRCi
FWRO + 1_800CH + 20H*i	Forwarding Engine PSFP MeTeR EBS Configuration i (i=0..PSFP_DMTR_N-1)	FWPMTREBSci
FWRO + 1_8010H + 20H*i	Forwarding Engine PSFP MeTeR EIR Configuration i (i=0..PSFP_DMTR_N-1)	FWPMTREIRCi
FWRO + 1_8014H + 20H*i	Forwarding Engine PSFP MeTeR Filter Monitoring i (i=0..PSFP_MTR_N-1)	FWPMTRFMI
FWRO + 6000H	Forwarding Engine FRER Table Learn 0	FWFTL0
FWRO + 6004H	Forwarding Engine FRER Table Learn 1	FWFTL1
FWRO + 6008H	Forwarding Engine FRER Table Learn Result	FWFTLR
FWRO + 6010H	Forwarding Engine FRER TimeOut Configuration	FWFTOC
FWRO + 6014H	Forwarding Engine FRER TimeOut Prescaler Configuration	FWFTOPC
FWRO + 6020H	Forwarding Engine FRER Table Initialization Monitoring	FWFTIM
FWRO + 6030H	Forwarding Engine FRER Table Read	FWFTR
FWRO + 6034H	Forwarding Engine FRER Table Read Result 0	FWFTRR0
FWRO + 6038H	Forwarding Engine FRER Table Read Result 1	FWFTRR1
FWRO + 603CH	Forwarding Engine FRER Table Read Result 2	FWFTRR2
FWRO + 6100H + 8H*i	Forwarding Engine SEQuence Number Generation Configuration i (i=0.. LTH_SEQGN_N-1)	FWSEQNGCi
FWRO + 6104H + 8H*i	Forwarding Engine SEQuence Number Generation Monitoring i (i=0.. LTH_SEQGN_N-1)	FWSEQNGMi
FWRO + 6200H	Forwarding Engine SEQuence Number Reset Configuration	FWSEQNRC
FWRO + 6300H + 20H*i E: FWRO + 6E00H + 20H*i	Forwarding Engine Cut-Through Forwarded Descriptor CouNter i (i=0..PORT_TIME_N-1)	FWCTFDCNi
FWRO + 6300H + 20H*(i + PORT_TIME_N) E: FWRO + 6E00H + 20H*(i + PORT_TIME_N)	Forwarding Engine Direct Descriptor Forwarded Descriptor CouNter i (i=0..PORT_SLOW_N-1)	FWDDFDCNi
FWRO + 6304H + 20H*i E: FWRO + 6E04H + 20H*i	Forwarding Engine Layer 3 Forwarded Descriptor CouNter i (i=0..PORT_N-1)	FWLTHFDCNi
FWRO + 630CH + 20H*i E: FWRO + 6E0CH + 20H*i	Forwarding Engine Layer 2 Forwarded Descriptor CouNter i (i=0..PORT_N-1)	FWLTWFDCNi
FWRO + 6310H + 20H*i E: FWRO + 6E10H + 20H*i	Forwarding Engine Port Based Forwarded Descriptor CouNter i (i=0..PORT_N-1)	FWPBFDCNi
FWRO + 6314H + 20H*i E: FWRO + 6E14H + 20H*i	Forwarding Engine MAC Hardware Learn CouNter i (i=0..PORT_N-1)	FWMHLCNi

Offset/Address	Register name	Abbreviation
FWRO + 6500H + 20H*i E: FWRO + 7000H + 20H*i	Forwarding Engine Integrity Check Rejected Descriptor CouNter i (i=0..PORT_N-1)	FWICRDCNi
FWRO + 6504H + 20H*i E: FWRO + 7004H + 20H*i	Forwarding Engine WaterMark Rejected Descriptor CouNter i (i=0..PORT_N-1)	FWWMRDCNi
FWRO + 6508H + 20H*i E: FWRO + 7008H + 20H*i	Forwarding Engine Cut-Through Rejected Descriptor CouNter i (i=0..PORT_TIME_N-1)	FWCTRDCNi
FWRO + 6508H + 20H*(i + PORT_TIME_N) E: FWRO + 7008H + 20H*(i + PORT_TIME_N)	Forwarding Engine Direct Descriptor Rejected Descriptor CouNter i (i=0..PORT_SLOW_N-1)	FWDDRDCNi
FWRO + 650CH + 20H*i E: FWRO + 700CH + 20H*i	Forwarding Engine Layer 3 Rejected Descriptor CouNter i (i=0..PORT_N-1)	FWLTHRDCNi
FWRO + 6514H + 20H*i E: FWRO + 7014H + 20H*i	Forwarding Engine Layer 2 Rejected Descriptor CouNter i (i=0..PORT_N-1)	FWLTLRDCNi
FWRO + 6518H + 20H*i E: FWRO + 7018H + 20H*i	Forwarding Engine Port Based Rejected Descriptor CouNter i (i=0..PORT_N-1)	FWPBRCNi
FWRO + 6700H + 4H*i E: FWRO + 7200H + 4H*i	Forwarding Engine PSFP MSDU Filtered Descriptor CouNter i (i=0..PSFP_MSDU_N-1)	FWPMFDCNi
FWRO + 6780H + 4H*i E: FWRO + 7280H + 4H*i	Forwarding Engine PSFP Gate Filtered Descriptor CouNter i (i=0..PSFP_GATE_N-1)	FWPGFDCNi
FWRO + 1_9000H + 20H*i E: FWRO + 1_A000H + 20H*i	Forwarding Engine PSFP Meter Green Descriptor CouNter i (i=0..PSFP_MTR_N-1)	FWPMGDCNi
FWRO + 1_9004H + 20H*i E: FWRO + 1_A004H + 20H*i	Forwarding Engine PSFP Meter Yellow Descriptor CouNter i (i=0..PSFP_DMTR_N-1)	FWPMYDCNi
FWRO + 1_9008H + 20H*i E: FWRO + 1_A008H + 20H*i	Forwarding Engine PSFP Meter Red Descriptor CouNter i (i=0..PSFP_MTR_N-1)	FWPMRDCNi
FWRO + 6A00H + 8H*i E: FWRO + 7500H + 8H*i	Forwarding Engine FRER Passed Packet CouNter i (i=0..FRER_RECE_N-1)	FWFRPPCNi
FWRO + 6A04H + 8H*i E: FWRO + 7504H + 8H*i	Forwarding Engine FRER Discarded Packet CouNter i (i=0..FRER_RECE_N-1)	FWFRDPCNi
FWRO + 1_6000H + 20H*i E: FWRO + 1_7000H + 20H*i	Forwarding Engine Block List Filtering CouNter i (i=0..PORT_N-1)	FWBLFCNi
FWRO + 1_600CH + 20H*i E: FWRO + 1_700CH + 20H*i	Forwarding Engine Acceptance List Filtering CouNter i (i=0..PORT_N-1)	FWALFCNi
FWRO + 7900H + 10H*i	Forwarding Engine Error Interrupt Status 0 i (i=0..PORT_N)	FWEIS0i
FWRO + 7904H + 10H*i	Forwarding Engine Error Interrupt Enable 0 i (i=0..PORT_N)	FWEIE0i
FWRO + 7908H + 10H*i	Forwarding Engine Error Interrupt Disable 0 i (i=0..PORT_N)	FWEID0i
FWRO + 7A00H	Forwarding Engine Error Interrupt Status 1	FWEIS1
FWRO + 7A04H	Forwarding Engine Error Interrupt Enable 1	FWEIE1
FWRO + 7A08H	Forwarding Engine Error Interrupt Disable 1	FWEID1
FWRO + 7A10H	Forwarding Engine Error Interrupt Status 2	FWEIS2
FWRO + 7A14H	Forwarding Engine Error Interrupt Enable 2	FWEIE2
FWRO + 7A18H	Forwarding Engine Error Interrupt Disable 2	FWEID2
FWRO + 7A20H	Forwarding Engine Error Interrupt Status 3	FWEIS3
FWRO + 7A24H	Forwarding Engine Error Interrupt Enable 3	FWEIE3
FWRO + 7A28H	Forwarding Engine Error Interrupt Disable 3	FWEID3
FWRO + 7A30H	Forwarding Engine Error Interrupt Status 4	FWEIS4

Offset/Address	Register name	Abbreviation
FWRO + 7A34H	Forwarding Engine Error Interrupt Enable 4	FWEIE4
FWRO + 7A38H	Forwarding Engine Error Interrupt Disable 4	FWEID4
FWRO + 7A40H	Forwarding Engine Error Interrupt Status 5 0	FWEIS50
FWRO + 7A44H	Forwarding Engine Error Interrupt Enable 5 0	FWEIE50
FWRO + 7A48H	Forwarding Engine Error Interrupt Disable 5 0	FWEID50
FWRO + 7A50H	Forwarding Engine Error Interrupt Status 5 1	FWEIS51
FWRO + 7A54H	Forwarding Engine Error Interrupt Enable 5 1	FWEIE51
FWRO + 7A58H	Forwarding Engine Error Interrupt Disable 5 1	FWEID51
FWRO + 7A60H	Forwarding Engine Error Interrupt Status 5 2	FWEIS52
FWRO + 7A64H	Forwarding Engine Error Interrupt Enable 5 2	FWEIE52
FWRO + 7A68H	Forwarding Engine Error Interrupt Disable 5 2	FWEID52
FWRO + 7A70H	Forwarding Engine Error Interrupt Status 5 3	FWEIS53
FWRO + 7A74H	Forwarding Engine Error Interrupt Enable 5 3	FWEIE53
FWRO + 7A78H	Forwarding Engine Error Interrupt Disable 5 3	FWEID53
FWRO + 7A80H	Forwarding Engine Error Interrupt Status 6 0	FWEIS60
FWRO + 7A84H	Forwarding Engine Error Interrupt Enable 6 0	FWEIE60
FWRO + 7A88H	Forwarding Engine Error Interrupt Disable 6 0	FWEID60
FWRO + 7A90H	Forwarding Engine Error Interrupt Status 6 1	FWEIS61
FWRO + 7A94H	Forwarding Engine Error Interrupt Enable 6 1	FWEIE61
FWRO + 7A98H	Forwarding Engine Error Interrupt Disable 6 1	FWEID61
FWRO + 7AA0H	Forwarding Engine Error Interrupt Status 6 2	FWEIS62
FWRO + 7AA4H	Forwarding Engine Error Interrupt Enable 6 2	FWEIE62
FWRO + 7AA8H	Forwarding Engine Error Interrupt Disable 6 2	FWEID62
FWRO + 7AB0H	Forwarding Engine Error Interrupt Status 6 3	FWEIS63
FWRO + 7AB4H	Forwarding Engine Error Interrupt Enable 6 3	FWEIE63
FWRO + 7AB8H	Forwarding Engine Error Interrupt Disable 6 3	FWEID63
FWRO + 7AC0H	Forwarding Engine Error Interrupt Status 7 0	FWEIS70
FWRO + 7AC4H	Forwarding Engine Error Interrupt Enable 7 0	FWEIE70
FWRO + 7AC8H	Forwarding Engine Error Interrupt Disable 7 0	FWEID70
FWRO + 7AD0H	Forwarding Engine Error Interrupt Status 7 1	FWEIS71
FWRO + 7AD4H	Forwarding Engine Error Interrupt Enable 7 1	FWEIE71
FWRO + 7AD8H	Forwarding Engine Error Interrupt Disable 7 1	FWEID71
FWRO + 7AE0H	Forwarding Engine Error Interrupt Status 7 2	FWEIS72
FWRO + 7AE4H	Forwarding Engine Error Interrupt Enable 7 2	FWEIE72
FWRO + 7AE8H	Forwarding Engine Error Interrupt Disable 7 2	FWEID72
FWRO + 7AF0H	Forwarding Engine Error Interrupt Status 7 3	FWEIS73
FWRO + 7AF4H	Forwarding Engine Error Interrupt Enable 7 3	FWEIE73
FWRO + 7AF8H	Forwarding Engine Error Interrupt Disable 7 3	FWEID73
FWRO + 7B00H	Forwarding Engine Error Interrupt Status 8 0	FWEIS80
FWRO + 7B04H	Forwarding Engine Error Interrupt Enable 8 0	FWEIE80
FWRO + 7B08H	Forwarding Engine Error Interrupt Disable 8 0	FWEID80
FWRO + 7B10H	Forwarding Engine Error Interrupt Status 8 1	FWEIS81
FWRO + 7B14H	Forwarding Engine Error Interrupt Enable 8 1	FWEIE81
FWRO + 7B18H	Forwarding Engine Error Interrupt Disable 8 1	FWEID81
FWRO + 7B20H	Forwarding Engine Error Interrupt Status 8 2	FWEIS82
FWRO + 7B24H	Forwarding Engine Error Interrupt Enable 8 2	FWEIE82
FWRO + 7B28H	Forwarding Engine Error Interrupt Disable 8 2	FWEID82

Offset/Address	Register name	Abbreviation
FWRO + 7B30H	Forwarding Engine Error Interrupt Status 8 3	FWEIS83
FWRO + 7B34H	Forwarding Engine Error Interrupt Enable 8 3	FWEIE83
FWRO + 7B38H	Forwarding Engine Error Interrupt Disable 8 3	FWEID83
FWRO + 7C00H	Forwarding Engine Monitoring Interrupt Status 0	FWMIS0
FWRO + 7C04H	Forwarding Engine Monitoring Interrupt Enable 0	FWMIE0
FWRO + 7C08H	Forwarding Engine Monitoring Interrupt Disable 0	FWMID0
FWRO + 7D00H	Forwarding Engine Security Configuration Register 0	FWSCR0
FWRO + 7D04H	Forwarding Engine Security Configuration Register 1	FWSCR1
FWRO + 7D08H	Forwarding Engine Security Configuration Register 2	FWSCR2
FWRO + 7D0CH	Forwarding Engine Security Configuration Register 3	FWSCR3
FWRO + 7D10H	Forwarding Engine Security Configuration Register 4	FWSCR4
FWRO + 7D54H	Forwarding Engine Security Configuration Register 21	FWSCR21
FWRO + 7D58H	Forwarding Engine Security Configuration Register 22	FWSCR22
FWRO + 7D5CH	Forwarding Engine Security Configuration Register 23	FWSCR23
FWRO + 7D60H	Forwarding Engine Security Configuration Register 24	FWSCR24
FWRO + 7D64H	Forwarding Engine Security Configuration Register 25	FWSCR25
FWRO + 7D68H	Forwarding Engine Security Configuration Register 26	FWSCR26
FWRO + 7D6CH	Forwarding Engine Security Configuration Register 27	FWSCR27
FWRO + 7D70H	Forwarding Engine Security Configuration Register 28	FWSCR28
FWRO + 7D74H	Forwarding Engine Security Configuration Register 29	FWSCR29
FWRO + 7D78H	Forwarding Engine Security Configuration Register 30	FWSCR30
FWRO + 7D7CH	Forwarding Engine Security Configuration Register 31	FWSCR31
FWRO + 7D80H	Forwarding Engine Security Configuration Register 32	FWSCR32
FWRO + 7D84H	Forwarding Engine Security Configuration Register 33	FWSCR33
FWRO + 7D88H	Forwarding Engine Security Configuration Register 34	FWSCR34
FWRO + 7D8CH	Forwarding Engine Security Configuration Register 35	FWSCR35
FWRO + 7D90H	Forwarding Engine Security Configuration Register 36	FWSCR36
FWRO + 7D94H	Forwarding Engine Security Configuration Register 37	FWSCR37
FWRO + 7D98H	Forwarding Engine Security Configuration Register 38	FWSCR38
FWRO + 7D9CH	Forwarding Engine Security Configuration Register 39	FWSCR39
FWRO + 7DA0H	Forwarding Engine Security Configuration Register 40	FWSCR40
FWRO + 7DA4H	Forwarding Engine Security Configuration Register 41	FWSCR41
FWRO + 7DA8H	Forwarding Engine Security Configuration Register 42	FWSCR42
FWRO + 7DACH	Forwarding Engine Security Configuration Register 43	FWSCR43
FWRO + 7DB0H	Forwarding Engine Security Configuration Register 44	FWSCR44
FWRO + 7DB4H	Forwarding Engine Security Configuration Register 45	FWSCR45
FWRO + 7DB8H	Forwarding Engine Security Configuration Register 46	FWSCR46
FWRO + 7DBCH	Forwarding Engine Security Configuration Register 47	FWSCR47
FWRO + 7DC0H	Forwarding Engine Security Configuration Register 48	FWSCR48
FWRO + 7DC4H	Forwarding Engine Security Configuration Register 49	FWSCR49
FWRO + 7E00H + 4H*i	Forwarding Engine Security Configuration Register Two byte filter i. (i=0..PFL_TWBF_N/32-1)	FWSCRTOi
FWRO + 7E40H + 4H*i	Forwarding Engine Security Configuration Register THree byte filter i. (i=0..PFL_THBF_N/32-1)	FWSCRTHi
FWRO + 7E80H + 4H*i	Forwarding Engine Security Configuration Register FOur byte filter i. (i=0..PFL_FOBF_N/32-1)	FWSCRFOi
FWRO + 7EC0H + 4H*i	Forwarding Engine Security Configuration Register RAnge filter i. (i=0..PFL_RAGF_N/32-1)	FWSCRRAi
FWRO + 7F00H + 4H*i	Forwarding Engine Security Configuration Register CAscade filter i. (i=0..PFL_CADF_N/32-1)	FWSCRCAi
FWRO + 8000H + 10H*i	ForWarding engine TWo Byte Filter Configuration i (i=0..PFL_TWBF_N-1)	FWTWBFCi
FWRO + 8004H + 10H*i	ForWarding engine TWo Byte Filter Value Configuration i (i=0..PFL_TWBF_N-1)	FWTWBFCVi

Offset/Address	Register name	Abbreviation
FWRO + A000H + 10H*i	ForWarding engine THree Byte Filter Configuration i (i=0..PFL_THBF_N-1)	FWTHBFCi
FWRO + A004H + 10H*i	ForWarding engine THree Byte Filter Value Configuration 0 i (i=0..PFL_THBF_N-1)	FWTHBFV0Ci
FWRO + A008H + 10H*i	ForWarding engine THree Byte Filter Value Configuration 1 i (i=0..PFL_THBF_N-1)	FWTHBFV1Ci
FWRO + B000H + 10H*i	ForWarding engine FOur Byte Filter Configuration i (i=0..PFL_FOBF_N-1)	FWFOBFCi
FWRO + B004H + 10H*i	ForWarding engine FOur Byte Filter Value 0 Configuration i (i=0..PFL_FOBF_N-1)	FWFOBFV0Ci
FWRO + B008H + 10H*i	ForWarding engine FOur Byte Filter Value 1 Configuration i (i=0..PFL_FOBF_N-1)	FWFOBFV1Ci
FWRO + D000H + 10H*i	ForWarding engine Range Filter Configuration i (i=0..PFL_RAGF_N-1)	FWRFCi
FWRO + D004H + 10H*i	Forwarding Engine Range Filter Start Value Configuration i (i=0..PFL_RAGF_N-1)	FWRFSVCi
FWRO + D008H + 10H*i	Forwarding Engine Range Filter End Value Configuration i (i=0..PFL_RAGF_N-1)	FWRFEVCi
FWRO + E000H + 40H*i ... + 1_5FC0H	Forwarding Engine Cascade Filter Configuration i (i=0..PFL_CADF_N-1)	FWCFCi
FWRO + E004H + 40H*i + 4H*j ... + 1_5FC0H + 4H*j	Forwarding Engine Cascade Filter Mapping Configuration i j (i=0..PFL_CADF_N-1) (j=0..PFL_CFMF_N-1)	FWCFMCij

Restrictions:

- If nothing specified, a register need an authorization from secured APB interface to be accessed by unsecured APB interface. This applies for Read and Write accesses. Any exception to this rule will be specified under “Security restrictions” or “Security un-restrictions” labels.

3.3 Register detailed explanation

This section describes SFR details.

3.3.1 Forwarding Engine Function registers

This section describes Forwarding Engine function registers.

For Forwarding Engine function procedure details, refer to section 4.1.

3.3.1.1 General function registers

(1) FWGC

Forwarding Engine General Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FPM	RSV								LTWUFRP[3:0]				LTHUFRP[3:0]		
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV														SVM[1:0]	

Bits	Bit name	RW-P	Initial value	Function description
31	FPM	RW-P	0H	<p>Filtering Priority Mode</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Filtering Info (PSFP) is selected by Filtering Priority [RSW3 Mode] - 1'b1: Filtering Info (PSFP) is selected by Routing Priority [RSW2 Compatibility Mode] <p>All of FP (Filtering Priority) will be invalid.</p> <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If FWGC.FPM = 1'b1, FWPIFPlj is not used. <p>Notes:</p> <ul style="list-style-type: none"> - This configuration will be used to select PSFP filtering parameters based on FP/RP. If FWGC.FPM = 1'b0 and a frame finds a match in multiple routing tables with highest RP and FP is from different routing tables, the PSFP rule with the highest FP in the hit table (Perf, L3S, L2S, VLAN, MAC, FWPIFPlj) is selected.
30:24	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
23:20	LTWUFRP	RW-P	0B	<p>Layer 2 Unknown (and Source Source Port) Filtering Routing Priority</p> <p>Functions:</p> <ul style="list-style-type: none"> - Routing Priority will be fixed this value for follow filtering conditions. - "Source Source Port Filtering (Layer 2 Source MAC address)" - "VLAN Unknown Filtering" - "Source MAC Unknown Filtering" - "Destination MAC Unknown Filtering"
19:16	LTHUFRP	RW-P	0B	<p>Layer 3 Unknown Filtering Routing Priority</p> <p>Functions:</p> <ul style="list-style-type: none"> - Routing Priority will be fixed this value for follow filtering condition. - "Layer 3 Unknown Filtering"
15:2	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.

1:0	SVM	RW-P	0H	<p>Switch VLAN Mode</p> <p>Values:</p> <ul style="list-style-type: none">- 2'b00: No VLAN mode (VLAN not used for forwarding)- 2'b01: C-TAG mode (C-TAG used for forwarding)- 2'b10: SC-TAG mode (S-TAG used for forwarding)- 2'b11: Reserved <p>Functions:</p> <ul style="list-style-type: none">- For more details, refer to R-Switch TOP specification [TOP]- HW: If FWGC.SVM is set to 2'b00, incoming packet PCP and DEI fields will be considered as 0 by Forwarding Engine.- For more details, refer to section 5.1.2
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(2) FWTTTC0

Forwarding Engine TAG TPID Configuration 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STT[15:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTT[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:16	STT	RW-P	88A8H	<p>S-TAG TPID [801.2Q] Functions: - Configure the S-TAG TPID. Restrictions: - SW: FWTTTC0.CTT, FWTTTC0.STT and FWTTTC1.RTT registers should always be set to different values. - SW: This register cannot be set to 0H~05FFH, 0800H nor 86DDH</p>
15:0	CTT	RW-P	8100H	<p>C-TAG TPID [801.2Q] Functions: - Configure the C-TAG TPID. Restrictions: - SW: FWTTTC0.CTT, FWTTTC0.STT and FWTTTC1.RTT registers should always be set to different values. - SW: This register cannot be set to 0H~05FFH, 0800H nor 86DDH</p>

(3) FWTTTC1

Forwarding Engine TAG TPID Configuration 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTT[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
15:0	RTT	RW-P	F1C1H	<p>R-TAG TPID [801.2CB]</p> <p>Functions:</p> <ul style="list-style-type: none"> - Configure the R-TAG TPID. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: FWTTTC0.CTT, FWTTTC0.STT and FWTTTC1.RTT registers should always be set to different values. - SW: This register cannot be set to 0H~05FFH, 0800H nor 86DDH

(4) FWCEPTC

Forwarding Engine CPU Exceptional Path Target Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV							EPSL	RSV							EPICS [PORT_SLOW_W-1:0]
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV	EPIPV[2:0]			RSV / EPCSD[AXI_CHAIN_W-1:0]											

Bits	Bit name	RW-P	Initial value	Function description
31:25	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
24	EPSL	RW-RP	0H	Exceptional Path Security Level Functions: - Configures descriptor security level for exceptional path.
23: PORT_SLOW_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_SLOW_W+15:16	EPICS	RW-P	0H	Exceptional Path CPU Select Functions: - Configures CPU to which exceptional frames will be sent. - Refer to Fabric specification for port mapping [FAB]. Restrictions: - SW: This register should not be set to a value bigger than PORT_SLOW_N-1
15	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
14:12	EPIPV	RW-P	0H	Exceptional Path Internal Priority Value Functions: - Configures the priority to which exceptional frames will be sent.
11: AXI_CHAIN_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
AXI_CHAIN_W-1:0	EPCSD	RW-P	0H	Exceptional Path CPU Sub Destination Functions: - Configures the CPU sub destination to which exceptional frames will be sent.

(5) FWCEPRC0

Forwarding Engine CPU Exceptional Path Reason Configuration 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICL4fef	ICIP6FEF F	ICIP4FE F	ICTfef	RSV	DDFSFE F	DDFEef	DDEEf	RSV	GCKSEE F	GDNEEF	GTFEF	RSV	GSEQEE F	GAXEEF	GAREEE F
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV	EMACSE EF	ECKSEE F	ETFEF	EOEEF	EUEEF	EBOEEF	ERPOO EF	ERFFEF	ECFFCE EF	ECFSEE F	EFFMEE F	EFCSEE F	ENIBEEF EF	EPCRCE EF	EPHYEE F

Bits	Bit name	RW-P	Initial value	Function description
31	ICL4fef	RW-P	0H	Integrity Check Layer 4 Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered Integrity Check Layer 4 Filtering are discarded. - 1'b1: Frames filtered Integrity Check Layer 4 Filtering are forwarded to exceptional path.
30	ICIP6FEF	RW-P	0H	Integrity Check IPv6 Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered Integrity Check IPv6 Filtering are discarded. - 1'b1: Frames filtered Integrity Check IPv6 Filtering are forwarded to exceptional path.
29	ICIP4FEF	RW-P	0H	Integrity Check IPv4 Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered Integrity Check IPv4 Filtering are discarded. - 1'b1: Frames filtered Integrity Check IPv4 Filtering are forwarded to exceptional path.
28	ICTfef	RW-P	0H	Integrity Check Type Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered Integrity Check Type Filtering are discarded. - 1'b1: Frames filtered Integrity Check Type Filtering are forwarded to exceptional path.
27	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
26	DDFSFEF	RW-P	0H	Direct Descriptor Format Security Filtering Exceptional Forwarding Values: - 1'b0: Frames with Direct Descriptor Format Security Error are discarded. - 1'b1: Frames with Direct Descriptor Format Security Error are forwarded to exceptional path.
25	DDFEef	RW-P	0H	Direct Descriptor Format Error Exceptional Forwarding Values: - 1'b0: Frames with Direct Descriptor Format Error are discarded. - 1'b1: Frames with Direct Descriptor Format Error are forwarded to exceptional path.
24	DDEEf	RW-P	0H	Direct Descriptor Error Exceptional Forwarding Values: - 1'b0: Frames with Direct Descriptor Error are discarded. - 1'b1: Frames with Direct Descriptor Error are forwarded to exceptional path.
23	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
22	GCKSEEf	RW-P	0H	GWCA CheckSum Error Exceptional Forwarding Values: - 1'b0: Frames received with CheckSum Error flag are discarded. - 1'b1: Frames received with CheckSum Error flag are forwarded to exceptional path.

21	GDNEEF	RW-P	0H	GWCA Descriptor Number Error Exceptional Forwarding Values: - 1'b0: Frames received with Descriptor Number Error are discarded. - 1'b1: Frames received with Descriptor Number Error are forwarded to exceptional path.
20	GTFEF	RW-P	0H	GWCA TAG Filtering Exceptional Forwarding Values: - 1'b0: Frames received with TAG Filtering flag are discarded. - 1'b1: Frames received with TAG Filtering flag are forwarded to exceptional path.
19	RSV	R0-U	0H	- Reserved area. On read, 0 will be returned.
18	GSEQEEF	RW-P	0H	GWCA Sequence Error Exceptional Forwarding Values: - 1'b0: Frames received with Sequence Error are discarded. - 1'b1: Frames received with Sequence Error are forwarded to exceptional path.
18	GAXEEF	RW-P	0H	GWCA AXI Error Exceptional Forwarding Values: - 1'b0: Frames received with AXI Error are discarded. - 1'b1: Frames received with AXI Error are forwarded to exceptional path.
16	GAREEEF	RW-P	0H	GWCA AXI RAM ECC Error Exceptional Forwarding Values: - 1'b0: Frames received with AXI RAM ECC Error are discarded. - 1'b1: Frames received with AXI RAM ECC Error are forwarded to exceptional path.
15	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
14	EMACSEEF	RW-P	0H	Ethernet MACsec Error Exceptional Forwarding Values: - 1'b0: Frames received with MACsec Error flag are discarded. - 1'b1: Frames received with MACsec Error flag are forwarded to exceptional path.
13	ECKSEEF	RW-P	0H	Ethernet CheckSum Error Exceptional Forwarding Values: - 1'b0: Frames received with CheckSum Error flag are discarded. - 1'b1: Frames received with CheckSum Error flag are forwarded to exceptional path.
12	ETFEF	RW-P	0H	Ethernet TAG Filtering Exceptional Forwarding Values: - 1'b0: Frames received with TAG Filtering flag are discarded. - 1'b1: Frames received with TAG Filtering flag are forwarded to exceptional path.
11	EOEEF	RW-P	0H	Ethernet Oversize Error Exceptional Forwarding Values: - 1'b0: Frames received with Oversize Error are discarded. - 1'b1: Frames received with Oversize Error are forwarded to exceptional path.
10	EUEEF	RW-P	0H	Ethernet Undersize Error Exceptional Forwarding Values: - 1'b0: Frames received with Undersize Error are discarded. - 1'b1: Frames received with Undersize Error are forwarded to exceptional path.
9	EBOEEF	RW-P	0H	Ethernet Buffer Overflow Error Exceptional Forwarding Values: - 1'b0: Frames received with Buffer Overflow Error are discarded. - 1'b1: Frames received with Buffer Overflow Error are forwarded to exceptional path.

8	ERPOOEF	RW-P	0H	Ethernet Reception Partially Out of Operation Exceptional Forwarding Values: - 1'b0: Frames received with Reception Partially Out of Operation flag are discarded. - 1'b1: Frames received with Reception Partially Out of Operation flag are forwarded to exceptional path.
7	ERFFEF	RW-P	0H	Ethernet RMAC Frame Filtered Exceptional Forwarding Values: - 1'b0: Frames received with RMAC Frame Filtered flag are discarded. - 1'b1: Frames received with RMAC Frame Filtered flag are forwarded to exceptional path.
6	ECFFCEEF	RW-P	0H	Ethernet C-Fragment FRAG_COUNT Error Exceptional Forwarding Values: - 1'b0: Frames received with C-Fragment FRAG_COUNT Error are discarded. - 1'b1: Frames received with C-Fragment FRAG_COUNT Error are forwarded to exceptional path.
5	ECFSEEF	RW-P	0H	Ethernet C-Fragment SMD Error Exceptional Forwarding Values: - 1'b0: Frames received with C-Fragment SMD Error are discarded. - 1'b1: Frames received with C-Fragment SMD Error are forwarded to exceptional path.
4	EFFMEEF	RW-P	0H	Ethernet Final Fragment Missing Error Exceptional Forwarding Values: - 1'b0: Frames received with Final Fragment Missing Error are discarded. - 1'b1: Frames received with Final Fragment Missing Error are forwarded to exceptional path.
3	EFCSEEF	RW-P	0H	Ethernet FCS Error Exceptional Forwarding Values: - 1'b0: Frames received with FCS Error are discarded. - 1'b1: Frames received with FCS Error are forwarded to exceptional path.
2	ENIBEEF	RW-P	0H	Ethernet Nibble Error Exceptional Forwarding Values: - 1'b0: Frames received with Nibble Error are discarded. - 1'b1: Frames received with Nibble Error are forwarded to exceptional path.
1	EPCRCEEF	RW-P	0H	Ethernet PCH CRC Error Exceptional Forwarding Values: - 1'b0: Frames received with PCH CRC Error are discarded. - 1'b1: Frames received with PCH CRC Error are forwarded to exceptional path.
0	EPHYEEF	RW-P	0H	Ethernet PHY Error Exceptional Forwarding Values: - 1'b0: Frames received with PHY Error are discarded. - 1'b1: Frames received with PHY Error are forwarded to exceptional path.

Notes:

- For ethernet error/flag explanations, refer to Ethernet agent specification document [TSNA].
- For GWCA error/flag explanations, refer to GWCA specification document [GWCA].

(6) FWCEPRC1

Forwarding Engine CPU Exceptional Path Reason Configuration 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
RSV														FBLFEF	FALFEF	
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
RSV						FSFFEF	FIFFEF	RSV						FMTRFE	FGATEF	FMSDUF
														F	EF	EF

Bits	Bit name	RW-P	Initial value	Function description
31:18	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
17	FBLFEF	RW-P	0H	Forwarding engine Block List Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered by Block List are discarded. - 1'b1: Frames filtered by Block List are forwarded to exceptional path.
16	FALFEF	RW-P	0H	Forwarding engine Acceptance List Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered by Acceptance List are discarded. - 1'b1: Frames filtered by Acceptance List are forwarded to exceptional path.
151:10	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
9	FSFFEF	RW-P	0H	Forwarding engine Sequence FRER Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered by FRER Sequence recovery are discarded. - 1'b1: Frames filtered by FRER Sequence recovery are forwarded to exceptional path.
8	FIFFEF	RW-P	0H	Forwarding engine Individual FRER Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered by FRER individual recovery are discarded. - 1'b1: Frames filtered by FRER individual recovery are forwarded to exceptional path.
7:3	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
2	FMTRFEF	RW-P	0H	Forwarding engine MeTeR Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered by PSFP Meter filter are discarded. - 1'b1: Frames filtered by PSFP Meter filter are forwarded to exceptional path.
1	FGATEFEEF	RW-P	0H	Forwarding engine GATE Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered by PSFP Gate filter are discarded. - 1'b1: Frames filtered by PSFP Gate filter are forwarded to exceptional path.
0	FMSDUFEEF	RW-P	0H	Forwarding engine MSDU Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered by PSFP MSDU filter are discarded. - 1'b1: Frames filtered by PSFP MSDU filter are forwarded to exceptional path.

(7) FWCEPRC2

Forwarding Engine CPU Exceptional Path Reason Configuration 2

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV			FPBFSF EF	FTWFSF EF	FWMFEF	RSV	FLTHFS FEF	RSV		FVLANS LFEF	FSMACS LFEF	FDMACS LFEF	RSV		FLTHSL FEF
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV			FPBNTF EF	FLTWN FEF	RSV	FLTHNT FEF	FDDNTF EF	RSV		FVLANU FEF	FSMACU FEF	FDMACU FEF	RSV		FLTHUF EF

Bits	Bit name	RW-P	Initial value	Function description
31:27	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
28	FPBFSFEF	RW-P	0H	Forwarding engine Port Based Format Security Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered are discarded because Port based format security filtering. - 1'b1: Frames filtered are forwarded to exceptional path because Port based format security filtering.
27	FTWFSFEF	RW-P	0H	Forwarding engine Layer 2 Format Security Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered are discarded because L2 format security filtering. - 1'b1: Frames filtered are forwarded to exceptional path because L2 format security filtering.
26	FWMFEF	RW-P	0H	Forwarding engine WaterMark Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered because of watermark are discarded. - 1'b1: Frames filtered because of watermark are forwarded to exceptional path.
25	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
24	FLTHFSFEF	RW-P	0H	Forwarding engine Layer 3 Format Security Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered because stream ID corresponding descriptor is unsecure and MSDU filter, Gate filter, Meter filter, FRER rule number or routing rule number is secure are discarded. - 1'b1: Frames filtered because stream ID corresponding descriptor is unsecure and MSDU filter, Gate filter, Meter filter, FRER rule number or routing rule number is secure are forwarded to exceptional path.
23:22	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
21	FVLANSLFEF	RW-P	0H	Forwarding Engine VLAN Source Lock Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered because of VLAN source lock are discarded. - 1'b1: Frames filtered because of VLAN source lock are forwarded to exceptional path.
20	FSMACSLFEF	RW-P	0H	Forwarding Engine Source MAC Source Lock Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered because of Source MAC source lock are discarded. - 1'b1: Frames filtered because of Source MAC source lock are forwarded to exceptional path.
19	FDMACSLFEF	RW-P	0H	Forwarding Engine Destination MAC Source Lock Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered because of Destination MAC source lock are discarded. - 1'b1: Frames filtered because of Destination MAC source lock are forwarded to exceptional path.
18:17	RSV	R0-U	0H	- Reserved area. On read, 0 will be returned.

16	FLTHSLFEF	RW-P	0H	Forwarding Engine Layer 3 Source Lock Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered because of Layer 3 source lock are discarded. - 1'b1: Frames filtered because of Layer 3 source lock are forwarded to exceptional path.
15:13	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
12	FPBNTFEF	RW-P	0H	Forwarding engine Port Based No Target Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered because no target during Port Based forwarding is detected are discarded. - 1'b1: Frames filtered because no target during Port Based forwarding is detected are forwarded to exceptional path.
11	FLTWNTEF	RW-P	0H	Forwarding engine Layer 2 No Target Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered because the combination on VLAN destination vector and destination MAC destination vector is null are discarded. - 1'b1: Frames filtered because the combination on VLAN destination vector and destination MAC destination vector is null are forwarded to exceptional path.
10	RSV	R0-U	0H	- Reserved area. On read, 0 will be returned.
9	FLTHNTFEF	RW-P	0H	Forwarding engine Layer 3 No Target Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered because no target during Layer 3 forwarding is detected are discarded. - 1'b1: Frames filtered because no target during Layer 3 forwarding is detected are forwarded to exceptional path.
8	FDDNTFEF	RW-P	0H	Forwarding engine Direct Descriptor No Target Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered because no target during direct forwarding is detected are discarded. - 1'b1: Frames filtered because no target during direct forwarding is detected are forwarded to exceptional path.
7:6	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
5	FVLANUEF	RW-P	0H	Forwarding engine VLAN Unknown Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered because their VLAN is unknown are discarded. - 1'b1: Frames filtered because their VLAN is unknown are forwarded to exceptional path.
4	FSMACUFEF	RW-P	0H	Forwarding engine Source MAC Unknown Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered because their Source MAC is unknown are discarded. - 1'b1: Frames filtered because their Source MAC is unknown are forwarded to exceptional path.
3	FDMACUFEF	RW-P	0H	Forwarding engine Destination MAC Unknown Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered because their Destination MAC is unknown are discarded. - 1'b1: Frames filtered because their Destination MAC is unknown are forwarded to exceptional path.
2:1	RSV	R0-U	0H	- Reserved area. On read, 0 will be returned.
0	FLTHUFEF	RW-P	0H	Forwarding engine Layer 3 Unknown Filtering Exceptional Forwarding Values: - 1'b0: Frames filtered because their stream ID is unknown are discarded. - 1'b1: Frames filtered because their stream ID is unknown are forwarded to exceptional path.

(8) FWCLPTC

Forwarding Engine CPU Learning Path Target Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV							LPSL	RSV						LPCS	
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV	LPIPV[2:0]			RSV / LPCSD[AXI_CHAIN_W-1:0]										[PORT_SLOW_W-1:0]	

Bits	Bit name	RW-P	Initial value	Function description
31:25	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
24	LPSL	RW-RP	0H	Learning Path Security Level Functions: - Configures descriptor security level for Learning path.
23: PORT_SLOW_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_SLOW_W+15:16	LPCS	RW-P	0H	Learning Path CPU Select Functions: - Configures CPU to which Learning frames will be sent. - Refer to Fabric specification for port mapping [FAB]. Restrictions: - SW: This register should not be set to a value bigger than PORT_SLOW_N-1
15	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
14:12	LPIPV	RW-P	0H	Learning Path Internal Priority Value Functions: - Configures the priority to which Learning frames will be sent.
11: AXI_CHAIN_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
AXI_CHAIN_W-1:0	LPCSD	RW-P	0H	Learning Path CPU Sub Destination Functions: - Configures the CPU sub destination to which Learning frames will be sent.

(9) FWCLPRC

Forwarding Engine CPU Learning Path Reason Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV								UVLANL F	UPSMAC LF	USMACL F	UDMACL F	RSV			USIDL F

Bits	Bit name	RW-P	Initial value	Function description
31:8	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
7	UVLANLF	RW-P	0H	<p>Unknown VLAN Learning Forwarding</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Frames received with an unknown VLAN are not forwarded to Learning path. - 1'b1: Frames received with an unknown VLAN are forwarded to Learning path.
6	UPSMACLF	RW-P	0H	<p>Unknown Port for Source MAC Learning Forwarding</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Frames received with an unknown port for Source MAC are not forwarded to Learning path. - 1'b1: Frames received with an unknown port for Source MAC are forwarded to Learning path.
5	USMACLF	RW-P	0H	<p>Unknown Source MAC Learning Forwarding</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Frames received with an unknown Source MAC are not forwarded to Learning path. - 1'b1: Frames received with an unknown Source MAC are forwarded to Learning path.
4	UDMACLF	RW-P	0H	<p>Unknown Destination MAC Learning Forwarding</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Frames received with an unknown destination MAC address are not forwarded to Learning path. - 1'b1: Frames received with an unknown destination MAC address are forwarded to Learning path.
3:1	RSV	R0-U	0H	<ul style="list-style-type: none"> - Reserved area. On read, 0 will be returned.
0	USIDL F	RW-P	0H	<p>Unknown Stream ID Learning Forwarding</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Frames received with an unknown stream ID are not forwarded to Learning path. - 1'b1: Frames received with an unknown stream ID are forwarded to Learning path.

(10) FWCMPTC

Forwarding Engine CPU Mirroring Path Target Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV							CMPSL	RSV / CMPCS[PORT_SLOW_W-1:0]							
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMPIPU	CMPIPV[2:0]		RSV / CMPCSD[AXI_CHAIN_W-1:0]												

Bits	Bit name	RW-P	Initial value	Function description
31:25	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
24	CMPSL	RW-RP	0H	<p>CPU Mirroring Path Security Level</p> <p>Functions:</p> <ul style="list-style-type: none"> - Configures descriptor security level for CPU mirroring path.
23: PORT_SLOW_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_SLOW_W+15:16	CMPCS	RW-P	0H	<p>CPU Mirroring Path CPU Select</p> <p>Functions:</p> <ul style="list-style-type: none"> - Configures CPU to which CPU mirroring frames will be sent. - Refer to Fabric specification for port mapping [FAB]. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: This register should not be set to a value bigger than PORT_SLOW_N-1
15	CMPIPU	RW-P	0H	<p>CPU Mirroring Path Internal Priority Update</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Frames mirrored to CPU path are sent with the same priority as for forwarding. - 1'b1: Frames mirrored to CPU path are sent with FWCMPTC.CMPIPV priority.
14:12	CMPIPV	RW-P	0H	CPU Mirroring Path Internal Priority Value
11: AXI_CHAIN_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
AXI_CHAIN_W-1:0	CMPCSD	RW-P	0H	<p>CPU Mirroring Path CPU Sub Destination</p> <p>Functions:</p> <ul style="list-style-type: none"> - Configures the CPU sub destination to which CPU mirroring frames will be sent.

(11) FWCML23URC

Forwarding Engine CPU Mirroring Path Layer2/3 Update Rule Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMRV[1:0]	RSV / CMRN[LTH_RRULE_W-1:0]														

Bits	Bit name	RW-P	Initial value	Function description
31:16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
15:14	CMRV	RW-P	0H	<p>CPU Mirroring Routing Valid</p> <p>Functions:</p> <ul style="list-style-type: none"> - Configures enabling the L23 update function for the mirroring frame. (not affected original frame) - 2'b00: The mirroring frame will be applied L23 update of original frame. - 2'b01: The mirroring frame will be disabled L23 update. (Even if original frame is enabled L23 update) - 2'b10: The mirroring frame will be applied L23 update of FWCMPL23URC.CMRV. - The update rule applied here is outside the scope of Format Security Filtering. - 2'b11: Reserved. <p>Restrictions:</p> <ul style="list-style-type: none"> - When Cut-through forwarding mirroring, this value have to set to 2'b00.
13:LTH_RRULE_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
LTH_RRULE_W-1:0	CMRN	RW-P	0H	<p>CPU Mirroring Routing Number</p> <p>Values:</p> <ul style="list-style-type: none"> - If FWCMPL23URC.CMRV set to 2'b10, FDESCR.RN will be updated this value for the mirroring frame.

(12) FWEMPTC

Forwarding Engine Ethernet Mirroring Path Target Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV							EMPSL	RSV / EMPPS[PORT_TIME_W-1:0]							
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EMPIPU	EMPIPV[2:0]			RSV											

Bits	Bit name	RW-P	Initial value	Function description
31:25	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
24	EMPSL	RW-RP	0H	Ethernet Mirroring Path Security Level Functions: - Configures descriptor security level for Ethernet mirroring path.
23: PORT_TIME_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_TIME_W+15:16	EMPPS	RW-P	0H	Ethernet Mirroring Path Port Select Functions: - Configures port to which Ethernet mirroring frames will be sent. - Refer to Fabric specification for port mapping [FAB]. Restrictions: - SW: This register should not be set to a value bigger than PORT_TIME_N-1
15	EMPIPU	RW-P	0H	Ethernet Mirroring Path Internal Priority Update Values: - 1'b0: Frames mirrored to Ethernet path are sent with the same priority as for forwarding. - 1'b1: Frames mirrored to Ethernet path are sent with FWEMPTC.EMPIPV priority.
14:12	EMPIPV	RW-P	0H	Ethernet Mirroring Path Internal Priority Value
11:0	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.

(13) FWEMPL23URC

Forwarding Engine Ethernet Mirroring Path Layer2/3 Update Rule Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EMRV[1:0]	RSV / EMRN[LTH_RRULE_W-1:0]														

Bits	Bit name	RW-P	Initial value	Function description
31:16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
15:14	EMRV	RW-P	0H	<p>Ether Mirroring Routing Valid</p> <p>Functions:</p> <ul style="list-style-type: none"> - Configures enabling the L23 update function for the mirroring frame. (not affected original frame) - 2'b00: The mirroring frame will be applied L23 update of original frame. - 2'b01: The mirroring frame will be disabled L23 update. (Even if original frame is enabled L23 update) - 2'b10: The mirroring frame will be applied L23 update of FWEMPL23URC.EMRN. The update rule applied here is outside the scope of Format Security Filtering. - 2'b11: Reserved. <p>Restrictions:</p> <ul style="list-style-type: none"> - When Cut-through forwarding mirroring, this value have to set to 2'b00.
13:LTH_RRULE_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
LTH_RRULE_W-1:0	EMRN	RW-P	0H	<p>Ether Mirroring Routing Number</p> <p>Values:</p> <ul style="list-style-type: none"> - If FWEMPL23URC.EMRV set to 2'b10, FDESCR.RN will be updated this value for the mirroring frame.

(14) FWSDMPTC

Forwarding Engine Source-Destination Mirroring Path Target Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV							SDMPSL	RSV / SDMPPS[PORT_W-1:0]							
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDMPIPU	SDMPIPV[2:0]			RSV / SDMPCSD[AXI_CHAIN_W-1:0]											

Bits	Bit name	RW-P	Initial value	Function description
31:25	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
24	SDMPSL	RW-RP	0H	<p>Source-Destination Mirroring Path Security Level</p> <p>Functions:</p> <ul style="list-style-type: none"> - Configures descriptor security level for Source-Destination mirroring path.
23: PORT_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_W+15:16	SDMPPS	RW-P	0H	<p>Source-Destination Mirroring Path destination Port Select</p> <p>Functions:</p> <ul style="list-style-type: none"> - Configures Port to which Source-Destination mirroring frames will be sent. - Refer to Fabric specification for port mapping [FAB]. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: This register should not be set to a value bigger than PORT_N-1
15	SDMPIPU	RW-P	0H	<p>Source-Destination Mirroring Path Internal Priority Update</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Frames mirrored to Source-Destination path are sent with the same priority as for forwarding. - 1'b1: Frames mirrored to Source-Destination path are sent with FWSDMPTC.SDMPIPV priority.
14:12	SDMPIPV	RW-P	0H	Source-Destination Mirroring Path Internal Priority Value
11: AXI_CHAIN_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
AXI_CHAIN_W-1:0	SDMPCSD	RW-P	0H	<p>Source-Destination Mirroring Path CPU Sub Destination</p> <p>Functions:</p> <ul style="list-style-type: none"> - Configures the CPU sub destination to which Source-Destination mirroring frames will be sent.

(15) FWSDMPVC

Forwarding Engine Source-Destination Mirroring Path Vector Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV / SDMSV[PORT_N-1:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / SDMDV[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: PORT_N+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_N+15:16	SDMSV	RW-P	0H	<p>Source-Destination Mirroring Source Vector</p> <p>Functions:</p> <ul style="list-style-type: none"> - Frames coming from a port set in FWSDMPVC.SDMSV register and sent to a port set in FWSDMPVC.SDMDV register is also duplicated to Source-Destination mirroring path. - Setting this register to 0 disable Source-Destination mirroring path.
15: PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_N-1:0	SDMDV	RW-P	0H	<p>Source-Destination Mirroring Destination Vector</p> <p>Functions:</p> <ul style="list-style-type: none"> - Frames coming from a port set in FWSDMPVC.SDMSV register and sent to a port set in FWSDMPVC.SDMDV register is also duplicated to Source-Destination mirroring path. - Setting this register to 0 disable Source-Destination mirroring path.

(16) FWSDMPL23URC

Forwarding Engine Source-Destination Mirroring Path Layer2/3 Update Rule Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDMRV[1:0]	RSV / SDMRN[LTH_RRULE_W-1:0]														

Bits	Bit name	RW-P	Initial value	Function description
31:16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
15:14	SDMRV	RW-P	0H	<p>Source-Destination Mirroring Routing Valid</p> <p>Functions:</p> <ul style="list-style-type: none"> - Configures enabling the L23 update function for the mirroring frame. (not affected original frame) - 2'b00: The mirroring frame will be applied L23 update of original frame. - 2'b01: The mirroring frame will be disabled L23 update. (Even if original frame is enabled L23 update) - 2'b10: The mirroring frame will be applied L23 update of FWSDMPL23URC.SDMRN. The update rule applied here is outside the scope of Format Security Filtering. - 2'b11: Reserved <p>Restrictions:</p> <ul style="list-style-type: none"> - When Cut-through forwarding mirroring, this value have to set to 2'b00.
13:LTH_RRULE_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
LTH_RRULE_W -1:0	SDMRN	RW-P	0H	<p>Source-Destination Mirroring Routing Number</p> <p>Values:</p> <ul style="list-style-type: none"> - If FWSDMPL23URC.SDMRV set to 2'b10, FDESCR.RN will be updated this value for the mirroring frame.

(17) FWSMPTC

Forwarding Engine Source Mirroring Path Target Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV							SMPSL	RSV / SMPPS[PORT_W-1:0]							
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMPIPU	SMPIPV[2:0]		RSV / SMPCSRD[AXI_CHAIN_W-1:0]												

Bits	Bit name	RW-P	Initial value	Function description
31:25	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
24	SMPSL	RW-RP	0H	<p>Source Mirroring Path Security Level</p> <p>Functions:</p> <ul style="list-style-type: none"> - Configures descriptor security level for Source mirroring.
23: PORT_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORt_W+15:16	SMPPS	RW-P	0H	<p>Source Mirroring Path destination Port Select</p> <p>Functions:</p> <ul style="list-style-type: none"> - Configures Destination Port to which Source mirroring frames will be sent. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: This register should not be set to a value bigger than PORT_N-1
15	SMPIPU	RW-P	0H	<p>Source Mirroring Path Internal Priority Update</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Frames mirrored to Source are sent with the same priority as for forwarding. - 1'b1: Frames mirrored to Source are sent with FWSMPTC.SMPIPV priority.
14:12	SMPIPV	RW-P	0H	Source Mirroring Path Internal Priority Value
11: AXI_CHAIN_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
AXI_CHAIN_W-1:0	SMPCSRD	RW-P	0H	<p>Source Mirroring Path CPU Sub Destination</p> <p>Functions:</p> <ul style="list-style-type: none"> - Configures the CPU sub destination to which Source mirroring frames will be sent.

(18) FWSMPVC

Forwarding Engine Source Mirroring Path Vector Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV / SMSV[PORT_N-1:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV															

Bits	Bit name	RW-P	Initial value	Function description
31: PORT_N+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_N+15:16	SMSV	RW-P	0H	<p>Source Mirroring Source Vector</p> <p>Functions:</p> <ul style="list-style-type: none"> - Frames coming from a port set in FWSMPVC.SSMSV register is also duplicated to Source mirroring path. - Setting this register to 0 disable Source mirroring path.
15:0	RSV	R0-U	0H	- Reserved area. On read, 0 will be returned.

(19) FWSMPL23URC

Forwarding Engine Source Mirroring Path Layer2/3 Update Rule Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMRV[1:0]	RSV / SMRN[LTH_RRULE_W-1:0]														

Bits	Bit name	RW-P	Initial value	Function description
31:16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
15:14	SMRV	RW-P	0H	<p>Source Mirroring Routing Valid</p> <p>Functions:</p> <ul style="list-style-type: none"> - Configures enabling the L23 update function for the mirroring frame. (not affected original frame) - 2'b00: The mirroring frame will be applied L23 update of original frame. - 2'b01: The mirroring frame will be disabled L23 update. (Even if original frame is enabled L23 update) - 2'b10: The mirroring frame will be applied L23 update of FWSMPL23URC.SMRN. The update rule applied here is outside the scope of Format Security Filtering. - 2'b11: Reserved. <p>Restrictions:</p> <ul style="list-style-type: none"> - When Cut-through forwarding mirroring, this value have to set to 2'b00.
13:LTH_RRULE_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
LTH_RRULE_W-1:0	SMRN	RW-P	0H	<p>Source Mirroring Routing Number</p> <p>Values:</p> <ul style="list-style-type: none"> - If FWSMPL23URC.SMRV set to 2'b10, FDESCR.RN will be updated this value for the mirroring frame.

(20) FWIBWMC

Forwarding Engine IPV Based WaterMark Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV / IBSWMR[PORT_N-1:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / IBUWMR[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: PORT_N+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_N+15:16	IBSWMR	RW-P	0H	<p>IPV Based Secure WaterMark Rejected</p> <p>Only frames with a secure descriptor coming from port i that are lower IPV than the IPV defined by COMA water mark are rejected.</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Above water mark operation is done regardless DEI value. - 1'b1: Above water mark operation is done if DEI only value of 1.
15: PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_N-1:0	IBUWMR	RW-P	0H	<p>IPV Based Unsecure WaterMark Rejected</p> <p>Only frames with a unsecure descriptor coming from port i that are lower IPV than the IPV defined by COMA water mark are rejected.</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Above water mark operation is done regardless DEI value. - 1'b1: Above water mark operation is done if only DEI value of 1.

(21) FWLBWMCi (i=0..PORT_N-1)

Forwarding Engine Level Based WaterMark Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WMFLPRI[15:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WMCLPRI[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:16	WMFLPRI	RW-P	0H	<p>WaterMark Flush Level Priority Rejected i</p> <p>Values:</p> <ul style="list-style-type: none"> Bit j set to 1'b0: Frames coming for port i and that should be forwarded with {DEI,IPV} equal to j are forwarded. Bit j set to 1'b1: Frames coming for port i and that should be forwarded with {DEI,IPV} equal to j are discarded when watermark flush level is set for port i (WM.FLUSH[i] is set [COMA]). <p>Notes:</p> <ul style="list-style-type: none"> {DEI,IPV} refers to the bit association {DEI,IPV[2:0]}, so in decimal it can be written 8*DEI+IPV
15:0	WMCLPRI	RW-P	0H	<p>WaterMark Critical Level Priority Rejected i</p> <p>Values:</p> <ul style="list-style-type: none"> Bit j set to 1'b0: Frames coming for port i and that should be forwarded with {DEI,IPV} equal to j are forwarded. Bit j set to 1'b1: Frames coming for port i and that should be forwarded with {DEI,IPV} equal to j are discarded when watermark critical level is set for port i (WM.CRITICAL[i] is set [COMA]). <p>Notes:</p> <ul style="list-style-type: none"> {DEI,IPV} refers to the bit association {DEI,IPV[2:0]}, so in decimal it can be written 8*DEI+IPV

(22) FWPC0i (i=0..PORT_N-1)

Forwarding Engine Port Configuration 0 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VLANSL VFEi	VLANRU Si	VLANRU i	VLANSAi	MACHM Ai	MACHLA i	MACRU SSAi	MACRU SAi	MACSSA i	MACRU DSAi	MACRU DAi	MACDSA i	RSV			LHTDD Mi
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV						L2SEi	IP6OEi	IP6TEi	IP6UEi	IP4OEi	IP4TEi	IP4UEi	LTHRUS Si	LTHRUSi	LTHTAi

Bits	Bit name	RW-P	Initial value	Function description
31	VLANSLVFEi	RW-P	0B	<p>VLAN Source Lock Vector Force Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: No functions. - 1'b1: VLAN.SLV[i] of all entries will be forced to 1'b1. <p>Details:</p> <ul style="list-style-type: none"> - For IEEE 802.1D 8.6.2 Ingress: If set to 1'b1 = "The default value for this parameter", disable ingress filtering (VLAN Source Port Filtering) for per ports.
30	VLANRUSi	RW-F	0B	<p>VLAN Reject Unknown Secure i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Unknown secure VLAN coming from source port i are not rejected. - 1'b1: Unknown secure VLAN coming from source port i are rejected. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: This bit should be set to 1'b0 if FWGC.SVM is set to 2'b00.
29	VLANRUi	RW-P	0B	<p>VLAN Reject Unknown i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Unknown VLAN coming from source port i are not rejected. - 1'b1: Unknown VLAN coming from source port i are rejected. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: This bit should be set to 1'b0 if FWGC.SVM is set to 2'b00.
28	VLANSAi	RW-P	0B	<p>VLAN Search Active i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: VLAN search is disabled for source port i. - 1'b1: VLAN search is enabled for source port i. <p>Functions:</p> <ul style="list-style-type: none"> - HW: If VLAN Destination search is disable for port i, all frames coming from port i are considered as unknown for VLAN search. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: This bit should be set to 1'b0 if FWGC.SVM is set to 2'b00.

27	MACHMAi	RW-P	0B	<p>MAC Hardware Migration Active i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Known unicast MAC Source addresses coming from source port i with a wrong source port in MAC.DV are not overwritten. - 1'b1: Known unicast MAC Source addresses coming from source port i with a wrong source port in MAC.DV are overwritten. - SW: Do not set this register to 1'b1 if i is greater than or equal to PORT_TSNA_N. (HW migration of Source MAC for frames sent from the CPU port is prohibited.)
26	MACHLAI	RW-P	0B	<p>MAC Hardware Learning Active i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Unknown unicast MAC Source addresses coming from source port i are not added to the MAC table. - 1'b1: Unknown unicast MAC Source addresses coming from source port i are added to the MAC table. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: Do not set this register to 1'b1 if i is greater than or equal to PORT_TSNA_N. (HW learning of Source MAC for frames sent from the CPU port is prohibited.)
25	MACRUSSAi	RW-F	0B	<p>MAC Reject Unknown Source Secure Addresses i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Unknown secure MAC Source addresses coming from source port i are not rejected. - 1'b1: Unknown secure MAC Source addresses coming from source port i are rejected.
24	MACRUSAi	RW-P	0B	<p>MAC Reject Unknown Source Addresses i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Unknown MAC Source addresses coming from source port i are not rejected. - 1'b1: Unknown MAC Source addresses coming from source port i are rejected.
23	MACSSAi	RW-P	0B	<p>MAC Source Search Active i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: MAC Source search is disabled for source port i. - 1'b1: MAC Source search is enabled for source port i.
22	MACRUDSAi	RW-F	0B	<p>MAC Reject Unknown Destination Secure Addresses i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Unknown secure MAC Destination addresses coming from source port i are not rejected. - 1'b1: Unknown secure MAC Destination addresses coming from source port i are rejected.
21	MACRUDAi	RW-P	0B	<p>MAC Reject Unknown Destination Addresses i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Unknown MAC Destination addresses coming from source port i are not rejected. - 1'b1: Unknown MAC Destination addresses coming from source port i are rejected.
20	MACDSAi	RW-P	0B	<p>MAC Destination Search Active i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: MAC Destination search is disabled for source port i. - 1'b1: MAC Destination search is enabled for source port i.
19:17	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
16	LHTDDMi	RW-P	0B	<p>L3 Table Disable with Destination MAC check i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: No functions. - 1'b1: Frames received with a destination MAC address NOT equal to port MAC address assigned on [RMAC] and [GWCA], L3 stream (IPv4 or IPv6) will be disabled for source port i. (L2 stream will not be disabled.) In other words, only "when there is a match will destination MAC address" be recognized as an Layer 3 frame.
15:10	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.

9	L2SEi	RW-P	0H	<p>L2 Stream Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: L2 stream disabled for source port i. - 1'b1: L2 stream enabled for source port i.
8	IP6OEi	RW-P	0B	<p>IPv6 Other Enabled i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: non-TCP non-UDP IPv6 detection disabled for source port i. - 1'b1: non-TCP non-UDP IPv6 detection enabled for source port i.
7	IP6TEi	RW-P	0B	<p>IPv6 TCP Enabled i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: IPv6/TCP detection disabled for source port i. - 1'b1: IPv6/TCP detection enabled for source port i.
6	IP6UEi	RW-P	0B	<p>IPv6 UDP Enabled i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: IPv6/UDP detection disabled for source port i. - 1'b1: IPv6/UDP detection enabled for source port i.
5	IP4OEi	RW-P	0B	<p>IPv4 Other Enabled i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: non-TCP non-UDP IPv4 detection disabled for source port i. - 1'b1: non-TCP non-UDP IPv4 detection enabled for source port i.
4	IP4TEi	RW-P	0B	<p>IPv4 TCP Enabled i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: IPv4/TCP detection disabled for source port i. - 1'b1: IPv4/TCP detection enabled for source port i.
3	IP4UEi	RW-P	0B	<p>IPv4 UDP Enabled i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: IPv4/UDP detection disabled for source port i. - 1'b1: IPv4/UDP detection enabled for source port i.
2	LTHRUSSi	RW-F	0B	<p>L3 Reject Unknown Secure Streams i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Unknown secure streams coming from source port i are not rejected. - 1'b1: Unknown secure streams coming from source port i are rejected.
1	LTHRUSi	RW-P	0B	<p>L3 Reject Unknown Streams i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Unknown streams coming from source port i are not rejected. - 1'b1: Unknown streams coming from source port i are rejected.
0	LTHTAi	RW-P	0B	<p>L3 Table Active i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: L3 table is disabled for source port i. - 1'b1: L3 table is enabled for source port i.

(23) FWPC1i (i=0..PORT_N-1)

Forwarding Engine Port Configuration 1 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV / LTHFMI[PORT_N-1:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV	BLSLDi	BLEi	RSV	PFALSL Di	PFALEi[1:0]	RSV								DDSLi	DDEi

Bits	Bit name	RW-P	Initial value	Function description
31:PORT_N+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_N+15:16	LTHFMI	RW-P	1H << i (2 ⁱ)	<p>Layer THree Forwarding Mask i</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit j set to 1'b0: Frames forwarded by Layer 3 forwarding can be forwarded to port j. - Bit j set to 1'b1: Frames forwarded by Layer 3 forwarding cannot be forwarded to port j.
15:14	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
13	BLSLDi	RW-P	0H	<p>Block List Security Level Disable i</p> <p>Value:</p> <ul style="list-style-type: none"> - 1'b0: Block list control is only available if Security Level is secure (FDESCR.BL=1 and FDESCR.SL=1). - 1'b1: Block list control is available if Security Level is secure or unsecure(FDESCR.BL=1 and FDESCR.SL=*) <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: Setting this register to 1 is not recommended as it causes security issues.
12	BLEi	RW-P	0H	<p>Block List Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: No function. - 1'b1: Block List enabled.
11	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
10	PFALSLDi	RW-P	0H	<p>Perfect Filter Acceptance List Security Level Disable i</p> <p>Value:</p> <ul style="list-style-type: none"> - 1'b0: Acceptance list control is only available when acceptance list is configured by secure. - 1'b1: Acceptance list control is available when acceptance list is configured by secure or unsecure. <p>This register affects for overwrite functions enabling.</p> <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: Setting this register to 1 is not recommended as it causes security issues.

				Perfect Filter Acceptance List Enable i Values: <ul style="list-style-type: none">- 2'b00: Acceptance List disabled.- 2'b01: Acceptance List enabled inbound mode. Deny all frames from ingress port i. "Inbound acceptance filter" (L3(acceptance).SLV[source port number] == 1'b1) can accept frames forwarding.- 2'b10: Acceptance List enabled outbound mode. Deny all frames from ingress port i. "Outbound acceptance filter" (L3(acceptance).DLV[destination port number] == 1'b1) can accept frames forwarding.- 2'b11: Acceptance List enabled inbound/outbound mode. Deny all frames from ingress port i. "Inbound acceptance filter" (L3(acceptance).SLV[source port number] == 1'b1) and "Outbound acceptance filter" (L3(acceptance).DLV[destination port number] == 1'b1) can accept frames forwarding. Restrictions: <ul style="list-style-type: none">- If you were forwarding in the traditional way (after setting FWPC1i.PFALEi[1:0] to other than 2'b00), all frames would be filtered from source port i. (Because the Acceptance list table FDESCR.AL=1 is not set.)- This register DOES NOT affect for overwrite functions enabling.
7:2	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
1	DDSLi	RW-F	0H	Direct Descriptor Security Level i Values: <ul style="list-style-type: none">- 1'b0: Secured Direct Descriptor discarded for port i.- 1'b1: Secured Direct Descriptor forwarded for port i. Restrictions: <ul style="list-style-type: none">- HW: This bit exists only in i=PORT_TIME_N..PORT_N-1.
0	DDEi	RW-P	0H	Direct Descriptor Enable i Values: <ul style="list-style-type: none">- 1'b0: Direct Descriptor disabled for port i- 1'b1: Direct Descriptor enabled for port i Restrictions: <ul style="list-style-type: none">- HW: This bit exists only in i=PORT_TIME_N..PORT_N-1.

(24) FWPC2i (i=0..PORT_N-1)

Forwarding Engine Port Configuration 2 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV / LTWFMi[PORT_N-1:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV															

Bits	Bit name	RW-P	Initial value	Function description
31:PORT_N+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_N+15:16	LTWFMi	RW-P	1H << i (2 ⁱ)	<p>Layer Two Forwarding Mask i</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit j set to 1'b0: Frames forwarded by Layer 2 forwarding can be forwarded to port j. - Bit j set to 1'b1: Frames forwarded by Layer 2 forwarding cannot be forwarded to port j.
15:0	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.

(25) FWPC3i (i=0..PORT_N-1)

Forwarding Engine Port Configuration 3 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															L23UOEi
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / LTHFMDi[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:17	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
16	L23UOEi	RW-P	0H	<p>Layer2/Layer3 Update Overwrite Enable i</p> <p>Value:</p> <ul style="list-style-type: none"> - 0: No function - 1: When selected (by routing priority) layer3 forwarding rule with invalid layer2/layer3 update rule is used, invalid layer2/layer3 update rule is overwrite by not-selected (by routing priority) VLAN forwarding rule with valid layer2/layer3 update rule. <p>Restriction:</p> <ul style="list-style-type: none"> - When selected “invalid L23 update rule of secure layer3 forwarding” cannot overwrite “valid L23 update rule of unsecure VLAN forwarding”.
15:PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_N-1:0	LTHFMDi	RW-P	0H	<p>Layer THree Forwarding Mask Disable for L23U i</p> <p>Function:</p> <ul style="list-style-type: none"> - This register is used to disable forwarding mask functional (FWPC1i.LTHFMI) if forwarding frame was Layer2/Layer3 updated. <p>Values:</p> <ul style="list-style-type: none"> - Bit j set to 1'b0: No function. - Bit j set to 1'b1: Layer Three Forwarding Mask disabled if L23Update is valid. <p>Restriction</p> <ul style="list-style-type: none"> - Bit j is only available when FWPC1i.LTHFMI[j] is set. - Even if the L23 update of layer 3 forwarding is changed from invalid to valid by FWPC3i.L23UOEi, this function (FWPC3i.LTHFMDi) will not disable masking for layer 3 forwarding.

(26) FWPIFPIij (i=0..PORT_N-1) (j=0..FRM_PRIO_N-1)

Forwarding Engine Port i and IPV j Filtering Priority and Information

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PIFPij[3:0]				RSV			PIFISLij	PIFIGAVij	RSV				PIFIGANij[PSFP_GATE_W-1:0]		
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIFIMSVij	RSV			PIFIMSNij[PSFP_MSDU_W-1:0]				PIFIMEVij	PIFIMENij[PSFP_MTR_W-1:0]						

Bits	Bit name	RW-P	Initial value	Function description
31	PIFPij[3]	RW-RP	0H	Port i and IPV j Filtering Priority (MSB) Values: - Filtering priority value for Port i and IPV j Restrictions: - HW: If FWGC.FPM is 1'b1, this value is invalid. (not use Filtering Priority, use Routing Priority)
30:28	PIFPij[2:0]	RW-P	0H	Port i and IPV j Filtering Priority Values: - Filtering priority value for Port i and IPV j Restrictions: - HW: If FWGC.FPM is 1'b1, this value is invalid. (not use Filtering Priority, use Routing Priority)
27:25	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
24	PIFISLij	RW-RP	0H	Port i and IPV j Filtering Info Security Level Value - 1'b0: Port i and IPV j Filtering Info input is unsecure - 1'b1: Port i and IPV j Filtering Info input is secure Restrictions: - HW: If FWGC.FPM is 1'b1, this value is invalid.
23	PIFIGAVij	RW-P	0H	Port i and IPV j Filtering Info GATE Valid Value - 1'b0: No function. - 1'b1: PSFP GATE Valid for Port i and IPV j Restrictions: - HW: If FWGC.FPM is 1'b1, this value is invalid.
22:PSFP_GATE_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PSFP_GATE_W+15:16	PIFIGANij	RW-P	0H	Port i and IPV j Filtering Info GATE Number Value - PSFP GATE Number for Port i and IPV j Restrictions: - HW: If FWGC.FPM is 1'b1, this value is invalid.
15	PIFIMSVij	RW-P	0H	Port i and IPV j Filtering Info MSDU Valid Value - 1'b0: No function. - 1'b1: PSFP MSDU Valid for Port i and IPV j Restrictions:

				- HW: If FWGC.FPM is 1'b1, this value is invalid.
14:PSFP_MSDU_W+8	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PSFP_MSDU_W+7:8	PIFIMSNij	RW-P	0H	<p>Port i and IPV j Filtering Info MSDU Number</p> <p>Value:</p> <ul style="list-style-type: none"> - PSFP MSDU Number for Port i and IPV j <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If FWGC.FPM is 1'b1, this value is invalid.
7	PIFIMEVij	RW-P	0H	<p>Port i and IPV j Filtering Info METER Valid</p> <p>Value</p> <ul style="list-style-type: none"> - 1'b0: No function. - 1'b1: PSFP METER Valid for Port i and IPV j <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If FWGC.FPM is 1'b1, this value is invalid.
PSFP_MTR_W-1:0	PIFIMENij	RW-P	0H	<p>Port i and IPV j Filtering Info METER Number</p> <p>Value</p> <ul style="list-style-type: none"> - PSFP METER Number for Port i and IPV j <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If FWGC.FPM is 1'b1, this value is invalid.

3.3.1.2 Cut-through forwarding function registers

(1) FWCTGC0i (i= 0..CT_CRULE_N-1)

Forwarding Engine Cut-Through General Configuration 0 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV	CTRTGli	CTVCTRLi[1:0]	CTFli	RSV		CTETEi	CTSDEi	CTSPEi	CTSVEi	CTCDEi	CTCPEi	CTCVEi	CTMSEi	CTMDEi	

Bits	Bit name	RW-P	Initial value	Function description
31:15	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
14	CTRTGli	RW-F	0H	<p>Cut-through R-TaG In i [GWCA] [TSNA] Values: <ul style="list-style-type: none"> - 1'b0: R-TAG is not included in cut-through frame. - 1'b1: R-TAG is included in cut-through frame. Functions <ul style="list-style-type: none"> - This register is used as FDESCR.RTGI for cut-through. </p>
13:12	CTVCTRLi	RW-F	0H	<p>Cut-through VLAN ConTRoL i [GWCA] [TSNA] Values: <ul style="list-style-type: none"> - 2'b00: The ingress matching separation rule i frame is a No TAG frame - 2'b01: The ingress matching separation rule i frame is a C-TAG frame - 2'b10: The ingress matching separation rule i frame is a SC-TAG frame - 2'b11: The ingress matching separation rule i frame is a CoS TAG frame Functions <ul style="list-style-type: none"> - This register is used as FDESCR.VCTRL[1:0] for cut-through. </p>
11	CTFli	RW-F	0H	<p>Cut-Through FCS In i Values: <ul style="list-style-type: none"> - 1'b0: The frame matching separation rule i as no FCS included. - 1'b1: The frame matching separation rule i as an FCS included. Functions <ul style="list-style-type: none"> - This register is used as FDESCR.FI for cut-through. Restrictions: <ul style="list-style-type: none"> - SW: This bit should be set to the frame source port MRGC.RCPT (same) value [RMAC]. case.1 : CTFli=1, RCPT=1 and correct FCS frame incoming -> correct FCS frame forwarded (The FCS attached to the input frame is output as it is. If the tag is converted, the FCS value will be invalid.) case.2 : CTFli=1, RCPT=1 and incorrect FCS frame incoming -> incorrect FCS frame forwarded case.3 : CTFli=0, RCPT=0 and correct FCS frame incoming -> correct FCS frame forwarded case.4 : CTFli=0, RCPT=0 and incorrect FCS frame incoming -> correct FCS frame forwarded (The correct FCS will be added after the incorrect FCS.) </p>

10:9	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
8	CTETEi	RW-F	0H	<p>Cut-through Ethernet Type Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Ethernet Type not included in Cut-Through separation for separation rule i. - 1'b1: Ethernet Type included in Cut-Through separation for separation rule i.
7	CTSDEi	RW-F	0H	<p>Cut-through S-TAG DEI Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: S-TAG DEI not included in Cut-Through separation for separation rule i. - 1'b1: S-TAG DEI included in Cut-Through separation for separation rule i. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: This bit can be set to 1'b1 only if FWGC.SVM is set to 2'b10
6	CTSPEi	RW-F	0H	<p>Cut-through S-TAG PCP Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: S-TAG PCP not included in Cut-Through separation for separation rule i. - 1'b1: S-TAG PCP included in Cut-Through separation for separation rule i. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: This bit can be set to 1'b1 only if FWGC.SVM is set to 2'b10
5	CTSVEi	RW-F	0H	<p>Cut-through S-TAG VLAN Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: S-TAG VLAN not included in Cut-Through separation for separation rule i. - 1'b1: S-TAG VLAN included in Cut-Through separation for separation rule i. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: This bit can be set to 1'b1 only if FWGC.SVM is set to 2'b10
4	CTCDEi	RW-F	0H	<p>Cut-through C-TAG DEI Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: C-TAG DEI not included in Cut-Through separation for separation rule i. - 1'b1: C-TAG DEI included in Cut-Through separation for separation rule i. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: This bit can be set to 1'b1 only if FWGC.SVM is set to 2'b10 or 2'b01
3	CTCPEi	RW-F	0H	<p>Cut-through C-TAG PCP Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: C-TAG PCP not included in Cut-Through separation for separation rule i. - 1'b1: C-TAG PCP included in Cut-Through separation for separation rule i. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: This bit can be set to 1'b1 only if FWGC.SVM is set to 2'b10 or 2'b01
2	CTCVEi	RW-F	0H	<p>Cut-through C-TAG VLAN Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: C-TAG VLAN not included in Cut-Through separation for separation rule i. - 1'b1: C-TAG VLAN included in Cut-Through separation for separation rule i. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: This bit can be set to 1'b1 only if FWGC.SVM is set to 2'b10 or 2'b01
1	CTMSEi	RW-F	0H	<p>Cut-through MAC Source Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: MAC Source not included in Cut-Through separation for separation rule i. - 1'b1: MAC Source included in Cut-Through separation for separation rule i.
0	CTMDEi	RW-F	0H	<p>Cut-through MAC Destination Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: MAC destination not included in Cut-Through separation for separation rule i. - 1'b1: MAC destination included in Cut-Through separation for separation rule i.

(2) FWCTGC1i (i= 0..CT_CRULE_N-1)

Forwarding Engine Cut-Through General Configuration 1 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV / CTMTi[FRM_TIME_W-1:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTMTi[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: FRM_TIME_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
FRM_TIME_W-1:0	CTMTi	RW-F	0H	<p>Cut-Through Maximum time i</p> <p>Functions:</p> <ul style="list-style-type: none"> - Describes maximum time on the PHY in ns of frames matching separation rule i - This time should take in account the whole frame (including preamble, SFD, TAGs and FCS) and IFG. - And this value have to minus internal latency (10 clk_cycle. Exp 66ns if clk = 150MHz). - This size will be used for TAS calculations [TSNA] <p>Cautions:</p> <ul style="list-style-type: none"> - If this register does not have the correct value, some frames could cross a closed gate in TAS [TSNA]. - if TAS is enabled, sending frames smaller than this register value will decrease the PHY throughput because the frame time will be reserved at this register value [TSNA]. Therefore, TAS gate open time must be bigger than CTMTi value.

(3) FWCTTC0i (i= 0..CT_CRULE_N-1)

Forwarding Engine Cut-Through Target Configuration 0 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV / CTDFMi[PORT_TIME_N-1:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / CTDVi[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:PORT_TIME_N+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_TIME_N-1:0	CTDFMi	RW-F	0H	<p>Cut-through Destination Forwarding Mode i</p> <ul style="list-style-type: none"> - 1'b0: Frame is forwarded in Cut-through mode - 1'b1: Frame is forwarded in Store and forward mode <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: In Cut-through mode, a frame with an error cannot be rejected and is forwarded to its destination ports.
15:PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_N-1:0	CTDVi	RW-F	0H	<p>Cut-through Destination Vector i</p> <p>Functions:</p> <ul style="list-style-type: none"> - Select the ports to which the frames matching separation rule i will be sent. - Enables cut-through for separation rule i. <p>Restrictions:</p> <ul style="list-style-type: none"> - When cut-through is enabled for rule i, at least one bit set to 1'b1 in FWCTTC0i.CTDVi[PORT_TIME_N-1:0] and should be set FWCTTC0i.CTDFMi to 1'b0 for a cut-through able destination agent (when cut-through is enabled, at least one Ethernet destination port should use with cut-through mode)

(4) FWCTTC1i (i= 0..CT_CRULE_N-1)

Forwarding Engine Cut-Through Target Configuration 1 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															CTEMEi CTCMEi
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTIPUi	CTIPVi[2:0]		RSV												

Bits	Bit name	RW-P	Initial value	Function description
31:18	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
17	CTEMEi	RW-F	0H	Cut-through Ethernet Mirroring Enable Values: - 1'b0: Ethernet mirroring is disabled for frames matching separation rule i. - 1'b1: Ethernet mirroring is enabled for frames matching separation rule i.
16	CTCMEi	RW-F	0H	Cut-through CPU Mirroring Enable Values: - 1'b0: CPU mirroring is disabled for frames matching separation rule i. - 1'b1: CPU mirroring is enabled for frames matching separation rule i.
15	CTIPUi	RW-F	0H	Cut-through Internal Priority Update Values: - 1'b0: Use the output descriptor priority to forwarding frames matching separation rule i. - 1'b1: Use FWCTTC1i.CTIPVi priority to forwarding frames matching separation rule i.
14:12	CTIPVi	RW-F	0H	Cut-through Internal Priority Value
11:0	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.

(5) FWCTTC2ji (j= 0..PORT_GWCA_N-1) (i= 0..CT_CRULE_N-1)

Forwarding Engine Cut-Through Target Configuration 2 j i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / CTCSDji[AXI_CHAIN_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
12: AXI_CHAIN_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
AXI_CHAIN_W -1:0	CTCSDji	RW-F	0H	Cut-Through CPU Sub Destination Functions: - Configures the CPU sub destination to which frames matching separation rule i will go for slow port number j.

(6) FWCTSC0i (i=0..CT_CRULE_N-1)

Forwarding Engine Cut-Through Separation Configuration 0 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CTDMAUPI[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTDMAUPI [15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	CTDMAUPI	RW-F	0H	Cut-Through Destination MAC Address Upper Part i

(7) FWCTSC1i (i=0..CT_CRULE_N-1)

Forwarding Engine Cut-Through Separation Configuration 1 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CTDMADPi[15:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTSMAUPi [15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:16	CTDMADPi	RW-F	0H	Cut-Through Destination MAC Address Downer Part i
15:0	CTSMAUPi	RW-F	0H	Cut-Through Source MAC Address Upper Part i

(8) FWCTSC2i (i=0..CT_CRULE_N-1)

Forwarding Engine Cut-Through Separation Configuration 2 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CTSMADPi[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTSMADPi [15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	CTSMADPi	RW-F	0H	Cut-Through Source MAC Address Downer Part i

(9) FWCTSC3i (i=0..CT_CRULE_N-1)

Forwarding Engine Cut-Through Separation Configuration 3 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
CTSDi	CTSPi[2:0]		CTSVi[11:0]													
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
CTCDi	CTCPI[2:0]		CTCVi[11:0]													

Bits	Bit name	RW-P	Initial value	Function description
31	CTSDi	RW-F	0H	Cut-Through S-TAG DEI i
30:28	CTSPi	RW-F	0H	Cut-Through S-TAG PCP i
27:16	CTSVi	RW-F	0H	Cut-Through S-TAG VLAN i
15	CTCDi	RW-F	0H	Cut-Through C-TAG DEI i
14:12	CTCPI	RW-F	0H	Cut-Through C-TAG PCP i
11:0	CTCVi	RW-F	0H	Cut-Through C-TAG VLAN i

(10) FWCTSC4i (i=0..CT_CRULE_N-1)

Forwarding Engine Cut-Through Separation Configuration 4 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV / CTSPNi[PORT_TIME_W-1:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTETi[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:PORT_TIME_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_TIME_W+15:16	CTSPNi	RW-F	0H	Cut-Through Source Port Number i Restrictions: - HW: In Cut-through mode (not store and forward mode), this bit have to set smaller than PORT_TIME_N.
15:0	CTETi	RW-F	0H	Cut-Through Ethernet Type i

3.3.1.3 Integrity check function registers

(1) FWICETC1i (i=0..PORT_N-1)

Forwarding Engine Integrity Check Ethernet Type Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICDMi	RSV														
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OTFEi	PTPFEi	MSFEi	ECFEi	PPFEi	EOLFEi	ESPFEi	EFCFEi	IP6FEi	SRPFEi	AVTPFEi	WOLFEi	ARPFEi	IP4FEi	EUSFEi	ESFEi

Bits	Bit name	RW-P	Initial value	Function description
31	ICDMi	RW-P	0H	<p>Integrity Check Disable Mode for L3 and L4</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: No function. - 1'b1: Frames received with a destination MAC address NOT equal to port MAC address assigned on [RMAC] and [GWCA] will be disabled "L3/L4 integrity check functions". <p>Notes:</p> <ul style="list-style-type: none"> - "L3/L4 integrity check functions" means "All of 3.3.1.3 enabled settings excluding FWICETC1i and FWICETC2i".
30:16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
15	OTFEi	RW-P	0H	<p>Other Type Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: Frames received with a type different than all types described below (The specified by FWICETC1i[14:0] and FWICETC3ij(j=all) will be rejected. <p>Specified below and ETDFVij can be used by acceptance list.</p> <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If use this function, please set acceptable value for FWICETC3ij(j=all) (not use with initial value 0x00).
14	PTPFEi	RW-P	0H	<p>Precision Time Protocol Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: Frames received with a type equal to 16'h88F7 will be rejected. <p>Specified 0x88F7 can be used by block list.</p>
13	MSFEi	RW-P	0H	<p>MAC Security Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: Frames received with a type equal to 16'h88E5 will be rejected.
12	ECFEi	RW-P	0H	<p>EtherCat Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: Frames received with a type equal to 16'h88A4 will be rejected.

11	PPFEi	RW-P	0H	Profinet Protocol Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: Frames received with a type equal to 16'h8892 will be rejected.
10	EOLFEi	RW-P	0H	EAP Over LAN Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: Frames received with a type equal to 16'h888E will be rejected.
9	ESPFEi	RW-P	0H	Ethernet Slow Protocol Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: Frames received with a type equal to 16'h8809 will be rejected.
8	EFCFEi	RW-P	0H	Ethernet Flow Control Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: Frames received with a type equal to 16'h8808 will be rejected.
7	IP6FEi	RW-P	0H	IPv6 Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: Frames received with a type equal to 16'h86DD will be rejected.
6	SRPFEi	RW-P	0H	SRP Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: Frames received with a type equal to 16'h22EA will be rejected.
5	AVTPFEi	RW-P	0H	AVTP Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: Frames received with a type equal to 16'h22F0 will be rejected.
4	WOLFEi	RW-P	0H	Wake-On-Lan Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: Frames received with a type equal to 16'h0842 will be rejected.
3	ARPFEi	RW-P	0H	Address Resolution Protocol Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: Frames received with a type equal to 16'h0806 will be rejected.
2	IP4FEi	RW-P	0H	IPv4 Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: Frames received with a type equal to 16'h0800 will be rejected.
1	EUSFEi	RW-P	0H	Ethernet Undefined Size Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: Frames received with a type bigger or equal to 16'h05DD (16'd1501) and smaller or equal to 16'h05FF (16'd1535) will be rejected.
0	ESFEi	RW-P	0H	Ethernet Size Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: Frames received with a type smaller or equal to 16'h05DC (16'd1500) will be rejected.

(2) FWICIP4Ci (i=0..PORT_N-1)

Forwarding Engine Integrity Check IPv4 Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV	IP4LADCi	IP4WTLF	IP4OTLF	IP4UTLFI	IP4IFFFEi	IP4FFFFF	RSV	IP4WBH	IP4OLSA	IP4OWS	IP4SSDA	IP4OSAF	IP4LSAF	IP4USAFA	IP4BSAF
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP4MSA	IP4ODA	IP4LDAF	IP4UDAF	IP4BDAF	IP4MDA	IP4UUD	IP4OTHF	IP4ICMP	IP4UDPF	IP4TCPF	IP4TLNF	IP4MFFE	RSV	IP4WVF	IP4WHL
FEi	FEi	Ei	Ei	Ei	FEi	AFei	Ei	FEi	Ei	Ei	Ei	i	Ei	Ei	FEi

Bits	Bit name	RW-P	Initial value	Function description
31	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
30	IP4LADCi	RW-P	0H	IPv4 Loopback Address Definition Change i Values: - 1'b0: IPv4 Loopback IP address includes addresses from 127.0.0.0 to 127.255.255.255). - 1'b1: IPv4 Loopback IP address includes addresses from 127.0.0.1 to 127.255.255.254).
29	IP4WTLFi	RW-P	0H	IPv4 Wrong Total Length Filter i Values: - 1'b0: Not filtering. - 1'b1: IPv4 frames with a Total length field smaller than IHL*4 are rejected.
28	IP4OTLFI	RW-P	0H	IPv4 Over Total Length Filter i Values: - 1'b0: Not filtering. - 1'b1: IPv4 frames with the Total Length field is bigger than a received IP Packet Size (the real size of IP header and IP payload without FCS) are rejected.
27	IP4UTLFI	RW-P	0H	IPv4 Under Total Length Filter i Values: - 1'b0: Not filtering. - 1'b1: IPv4 frames with the Total Length field is smaller than a received IP Packet Size (the real size of IP header and IP payload without FCS) are rejected.
26	IP4IFFFEi	RW-P	0H	IPv4 Intermediate Fragment Frame Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: IPv4 frames received with "FragmentOffset != 0" are rejected.
25	IP4FFFFEi	RW-P	0H	IPv4 First Fragment Frame Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: IPv4 frames received with "MoreFragments == 1 and FragmentOffset == 0" are rejected.
24	RSV	RW-P	0H	Reserved area. On read, 0 will be returned.
23	IP4WBHLFEi	RW-P	0H	IPv4 Wrong Bigger Header Length Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: IPv4 frames with an IHL*4 field giving a bigger value than its real IP Packet Size (the real size of IP header and IP payload without FCS) are rejected.

22	IP4OLSAFEi	RW-P	0H	<p>IPv4 Off Link Source Address Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: IPv4 frames received with a source IP address which is different network address (the value of FWIP4ACi.IP4Ai range from MSB indicated by FWIP4APCi.IP4API) of received port are rejected. - Specified FWIP4AC<i>i</i> can used by acceptance list. <p>Restrictions:</p> <ul style="list-style-type: none"> - If FWIP4APCi.IP4API == 0, this bit have to set 1'b0.
21	IP4OWSAFEi	RW-P	0H	<p>IPv4 OWn Source Address Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: IPv4 frames received with a source IP address which is FWIP4ACi.IP4Ai are rejected. - Specified FWIP4AC<i>i</i> can used by block list.
20	IP4SSDAFEi	RW-P	0H	<p>IPv4 Same Source and Destination Address Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: IPv4 frames received with same source and destination IP address are rejected.
19	IP4OSAFEi	RW-P	0H	<p>IPv4 Other Source Address Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: Pv4 frames received with a Source IP address which is not unicast, multicast or broadcast are rejected.
18	IP4LSAFEi	RW-P	0H	<p>IPv4 Loopback Source Address Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: IPv4 frames received with a loopback source IP address are rejected (Loopback IP address includes addresses "from 127.0.0.0 to 127.255.255.255" or "from 127.0.0.1 to 127.255.255.254" defined by FWICIP4Ci.IP4LADCi).
17	IP4USAFei	RW-P	0H	<p>IPv4 Unspecified Source Address Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: IPv4 frames received with an Unspecified source IP address are rejected (Unspecified IP address includes address 0.0.0.0).
16	IP4BSAFEi	RW-P	0H	<p>IPv4 Broadcast Source Address Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: IPv4 frames received with a Broadcast source IP address are rejected (Broadcast IP address is address 255.255.255.255).
15	IP4MSAFEi	RW-P	0H	<p>IPv4 Multicast Source Address Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: IPv4 frames received with a multicast source IP address are rejected (Multicast IP address includes addresses from 224.0.0.0 to 239.255.255.255).
14	IP4ODAFEi	RW-P	0H	<p>IPv4 Other Destination Address Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: Pv4 frames received with a destination IP address which is not unicast, multicast, broadcast or unspecified are rejected.

13	IP4LDAFEi	RW-P	0H	IPv4 Loopback Destination Address Filtering Enable i Values: <ul style="list-style-type: none">- 1'b0: Not filtering.- 1'b1: IPv4 frames received with a loopback destination IP address are rejected (Loopback IP address includes addresses from 127.0.0.0 to 127.255.255.255 or “from 127.0.0.1 to 127.255.255.254” defined by FWICIP4Ci.IP4LADCi).
12	IP4UDAFEi	RW-P	0H	IPv4 Unspecified Destination Address Filtering Enable i Values: <ul style="list-style-type: none">- 1'b0: Not filtering.- 1'b1: IPv4 frames received with an unspecified destination IP address are rejected (Unspecified IP address includes address 0.0.0.0).
11	IP4BDAFEi	RW-P	0H	IPv4 Broadcast Destination Address Filtering Enable i Values: <ul style="list-style-type: none">- 1'b0: Not filtering.- 1'b1: IPv4 frames received with a Broadcast destination IP address are rejected (Broadcast IP address is address 255.255.255.255).
10	IP4MDAFEi	RW-P	0H	IPv4 Multicast Destination Address Filtering Enable i Values: <ul style="list-style-type: none">- 1'b0: Not filtering.- 1'b1: IPv4 frames received with a multicast destination IP address are rejected (Multicast IP address includes addresses from 224.0.0.0 to 239.255.255.255).
9	IP4UUDAFEi	RW-P	0H	IPv4 Unknown Unicast Destination Address Filtering Enable i Values: <ul style="list-style-type: none">- 1'b0: Not filtering.- 1'b1: IPv4 frames received with a unicast destination IP address which is not FWIP4ACi.IP4Ai are rejected (Unicast IP address includes addresses from 0.0.0.0 to 223.255.255.255 which are not Unspecified or Loopback addresses).
8	IP4OTHFEi	RW-P	0H	IPv4 OTHer Filtering Enable i Values: <ul style="list-style-type: none">- 1'b0: Not filtering.- 1'b1: IPv4 frames which are no TCP,UDP or ICMP are rejected.
7	IP4ICMPFEi	RW-P	0H	IPv4 ICMP Filtering Enable i Values: <ul style="list-style-type: none">- 1'b0: Not filtering.- 1'b1: IPv4/ICMP frames are rejected.
6	IP4UDPFEi	RW-P	0H	IPv4 UDP Filtering Enable i Values: <ul style="list-style-type: none">- 1'b0: Not filtering.- 1'b1: IPv4/UDP frames are rejected.
5	IP4TCPFEi	RW-P	0H	IPv4 TCP Filtering Enable i Values: <ul style="list-style-type: none">- 1'b0: Not filtering.- 1'b1: IPv4/TCP frames are rejected.
4	IP4TLNFEi	RW-P	0H	IPv4 Time to Live Null Filtering Enable i Values: <ul style="list-style-type: none">- 1'b0: Not filtering.- 1'b1: IPv4 frames with Time to Live field null are rejected.

3	IP4MFFEi	RW-P	0H	IPv4 More Fragment Filtering Enable i Values: <ul style="list-style-type: none">- 1'b0: Not filtering.- 1'b1: IPv4 frames with More Fragment Flag set in Flags field are rejected.
2	RSV	RW-P	0H	Reserved area. On read, 0 will be returned.
1	IP4WVFEi	RW-P	0H	IPv4 Wrong Version Filtering Enable i Values: <ul style="list-style-type: none">- 1'b0: Not filtering.- 1'b1: IPv4 frames with a Version field value different than 4 are rejected.
0	IP4WHLFEi	RW-P	0H	IPv4 Wrong Header Length Filtering Enable i Values: <ul style="list-style-type: none">- 1'b0: Not filtering.- 1'b1: IPv4 frames with an IHL field value smaller than 5 are rejected.

(3) FWIP4ACi (i=0..PORT_N-1)

Forwarding Engine IPv4 Address Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IP4Ai[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP4Ai[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	IP4Ai	RW-P	0H	IPv4 Address i Functions: - Set port i IPv4 address. Recommended setting the unicast address here.

(4) FWICIP6Ci (i=0..PORT_N-1)

Forwarding Engine Integrity Check IPv6 Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV								IP6OPLF E	IP6UPLF E	RSV	IP6OLSA FEi	IP6OWS AFEi	IP6SSDA FEi	IP6USA Ei	IP6LSAF Ei
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP6MSA FEi	IP6LLSA FEi	IP6ULSA FEi	IP6UDAF Ei	IP6LDAF Ei	IP6MDA FEi	IP6LLDA FEi	IP6ULDA FEi	IP6UUD AFEi	IP6OTHF Ei	IP6ICMP FEi	IP6UDPF Ei	IP6TCPF Ei	IP6HLNF Ei	RSV	IP6WVF Ei

Bits	Bit name	RW-P	Initial value	Function description
31:24	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
23	IP6OPLFE	RW-P	0H	<p>IPv6 Over Payload Length Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: IPv6 frames with the Payload Length field is bigger than a received IP Payload Size (the real size of IP payload without IP header and FCS) are rejected.
22	IP6UPLFE	RW-P	0H	<p>IPv6 Under Payload Length Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: IPv6 frames with the Payload Length field is smaller than a received IP Payload Size (the real size of IP payload without IP header and FCS) are rejected.
21	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
20	IP6OLSAFEi	RW-P	0H	<p>IPv6 Off Link Source Address Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: IPv6 frames received with a source IP address which is different network address (the value of {FWIP6AC0i.IP6AP0i, FWIP6AC1i.IP6AP1i, FWIP6AC2i.IP6AP2i, FWIP6AC3i.IP6AP3i} range from MSB indicated by FWIP6APCi.IP6APi) of received port are rejected. - Specified FWIP6AC<i>i</i> can be used by acceptance list. <p>Restrictions:</p> <ul style="list-style-type: none"> - If FWIP6APCi.IP6APi == 0, this bit must be set 1'b0.
19	IP6OWSAFEi	RW-P	0H	<p>IPv6 Own Source Address Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: IPv6 frames received with a source IP address which is {FWIP6AC0i.IP6AP0i, FWIP6AC1i.IP6AP1i, FWIP6AC2i.IP6AP2i, FWIP6AC3i.IP6AP3i} are rejected. - Specified FWIP6AC<i>i</i> can be used by block list.
18	IP6SSDAFei	RW-P	0H	<p>IPv6 Same Source and Destination Address Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: IPv6 frames received with same source and destination IP address are rejected.
17	IP6USAFei	RW-P	0H	<p>IPv6 Unspecified Source Address Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: IPv6 frames received with an Unspecified source IP address are rejected (Unspecified IP address includes ::/128 address).

16	IP6LSAFEi	RW-P	0H	IPv6 Loopback Source Address Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: IPv6 frames received with a Loopback source IP address are rejected (Loopback IP address includes ::1/128 address).
15	IP6MSAFEi	RW-P	0H	IPv6 Multicast Source Address Filtering Enable I Values: - 1'b0: Not filtering. - 1'b1: IPv6 frames received with a Multicast source IP address are rejected (Multicast IP address includes FF00::/8 addresses).
14	IP6LLSAFEi	RW-P	0H	IPv6 Link-Local Source Address Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: IPv6 frames received with a Link-Local source IP address are rejected (Link-Local IP address includes FE80::/10 addresses).
13	IP6ULSAFEi	RW-P	0H	IPv6 Unique Local Source Address Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: IPv6 frames received with a Unique Local source IP address are rejected (Unique Local IP address includes FC00::/7 addresses).
12	IP6UDAFEi	RW-P	0H	IPv6 Unspecified Destination Address Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: IPv6 frames received with an Unspecified destination IP address are rejected (Unspecified IP address includes ::/128 address).
11	IP6LDAFEi	RW-P	0H	IPv6 Loopback Destination Address Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: IPv6 frames received with a Loopback destination IP address are rejected (Loopback IP address includes ::1/128 address).
10	IP6MDAFEi	RW-P	0H	IPv6 Multicast Destination Address Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: IPv6 frames received with a Multicast destination IP address are rejected (Multicast IP address includes FF00::/8 addresses).
9	IP6LLDAFEi	RW-P	0H	IPv6 Link-Local Destination Address Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: IPv6 frames received with a Link-Local destination IP address are rejected (Link-Local IP address includes FE80::/10 addresses).
8	IP6ULDAFEi	RW-P	0H	IPv6 Unique Local Destination Address Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: IPv6 frames received with a Unique Local destination IP address are rejected (Unique Local IP address includes FC00::/7 addresses).

7	IP6UUDAFEi	RW-P	0H	IPv6 Unknown Unicast Destination Address Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: IPv6 frames received with a unicast destination IP address which is not {FWIP6AC0i.IP6AP0i, FWIP6AC1i.IP6AP1i, FWIP6AC2i.IP6AP2i, FWIP6AC3i.IP6AP3i} are rejected (Unicast IP address includes addresses which are not Unique Local unicast, Link-local unicast, Multicast, Loopback or Unspecified addresses).
6	IP6OTHFEi	RW-P	0H	IPv6 OTHER Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: IPv6 frames which are no TCP,UDP or ICMP are rejected.
5	IP6ICMPFEi	RW-P	0H	IPv6 ICMP Filtering Enable i Values: - 1'b0: I Not filtering. - 1'b1: IPv6/ICMP frames are rejected.
4	IP6UDPFEi	RW-P	0H	IPv6 UDP Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: IPv6/UDP frames are rejected.
3	IP6TCPFEi	RW-P	0H	IPv6 TCP Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: IPv6/TCP frames are rejected.
2	IP6HLNFEi	RW-P	0H	IPv6 HopLimit Null Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: IPv6 frames with HopLimit field null are rejected.
1	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
0	IP6WVFEi	RW-P	0H	IPv6 Wrong Version Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: IPv6 frames with a Version field value different than 6 are rejected. note: This IPv6 integrity check will happen based on ether type field and is irrespective of header length and TPL size (Even though the header length is smaller than minimum header length of corresponding frame type).

(5) FWIP6AC0i (i=0..PORT_N-1)

Forwarding Engine IPv6 Address Configuration 0 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IP6AP0i[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP6AP0i[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	IP6AP0i	RW-P	0H	<p>IPv6 Address Part 0 i</p> <p>Functions:</p> <ul style="list-style-type: none"> - Set port i IPv6 address. Recommended setting the unicast address here.

(6) FWIP6AC1i (i=0..PORT_N-1)

Forwarding Engine IPv6 Address Configuration 1 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IP6AP1i[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP6AP1i[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	IP6AP1i	RW-P	0H	<p>IPv6 Address Part 1 i</p> <p>Functions:</p> <ul style="list-style-type: none"> - Set port i IPv6 address. Recommended setting the unicast address here.

(7) FWIP6AC2i (i=0..PORT_N-1)

Forwarding Engine IPv6 Address Configuration 2 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IP6AP2i[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP6AP2i[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	IP6AP2i	RW-P	0H	<p>IPv6 Address Part 2 i</p> <p>Functions:</p> <ul style="list-style-type: none"> - Set port i IPv6 address. Recommended setting the unicast address here.

(8) FWIP6AC3i (i=0..PORT_N-1)

Forwarding Engine IPv6 Address Configuration 3 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IP6AP3i[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP6AP3i[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	IP6AP3i	RW-P	0H	<p>IPv6 Address Part 3 i</p> <p>Functions:</p> <ul style="list-style-type: none"> - Set port i IPv6 address. Recommended setting the unicast address here.

(9) FWIP4APCi (i=0..PORT_N-1)

Forwarding Engine IPv4 Address Prefix Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV												IP4APi[5:0]			

Bits	Bit name	RW-P	Initial value	Function description
31:6	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
5:0	IP4APi	RW-P	0H	IPv4 Address Prefix i Functions: Set port i IPv4 address prefix of FWIP4ACi

(10) FWIP6APCi (i=0..PORT_N-1)

Forwarding Engine IPv6 Address Prefix Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV								IP6APi[7:0]							

Bits	Bit name	RW-P	Initial value	Function description
31:8	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
7:0	IP6APi	RW-P	0H	IPv6 Address Prefix i Functions: Set port i IPv6 address prefix of FWIP6AC0-3i

(11) FWICETC2i (i=0..PORT_N-1)

Forwarding Engine Integrity Check Ethernet Type Configuration 2 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV								ETDFEi7	ETDFEi6	ETDFEi5	ETDFEi4	ETDFEi3	ETDFEi2	ETDFEi1	ETDFEi0

Bits	Bit name	RW-P	Initial value	Function description
31-INTGETYPE_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
INTGETYPE_N-1:0	ETDFEij	RW-P	0H	<p>Ether Type Directed Filtering Enable i j (j=0.. INTGETYPE_N-1) (Block list function)</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: Frames received with a type equal to FWICETC3i(j/2).ETDFVij will be rejected. <p>Specified ETDFVij can be used by block list.</p>

(12) FWICETC3ij (i=0..PORT_N-1) (j=0..INTGETYPE_N/2-1)

Forwarding Engine Integrity Check Ethernet Type Configuration 3 i j

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ETDFV i (j^*2+1) [15:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETDFV i (j^*2) [15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:16	ETDFVi(j^*2+1)	RW-P	0H	<p>Ether Type Directed Filtering Value i j^*2+1</p> <p>Values:</p> <ul style="list-style-type: none"> Specify the value of "Ether type" field used for specifying. <p>Restrictions:</p> <ul style="list-style-type: none"> SW: This register cannot be set to 0800H nor 86DDH (Setting these values will not blocklist rejections.)
15:0	ETDFVi(j^*2)	RW-P	0H	<p>Ether Type Directed Filtering Value i j^*2</p> <p>Values:</p> <ul style="list-style-type: none"> Specify the value of "Ether type" field used for specifying. <p>Restrictions:</p> <ul style="list-style-type: none"> SW: This register cannot be set to 0800H nor 86DDH (Setting these values will not blocklist rejections.)

(13) FWIP4FACij (i=0..PORT_N-1) (j=0..INTG_FILT_SIPA_N-1)

Forwarding Engine IPv4 Filtering Address Configuration i j

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IP4FAij[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP4FAij[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	IP4FAij	RW-P	0H	<p>IPv4 Filtering Address I j</p> <p>Functions:</p> <ul style="list-style-type: none"> - Set port i IPv4 address for filter j. Recommended setting the unicast address here.

(14) FWIP4SFCij (i=0..PORT_N-1) (j=0..INTG_FILT_SIPA_N-1)

Forwarding Engine IPv4 Specified Filter Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
RSV										IP4FAP[5:0]							
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
RSV										IP4SOLD	IP4SDBD	IP4SNDA	IP4SUDA	IP4SOLS	IP4SDBS	IP4NSNA	IP4SUSA
								AFEij	AFEij	FEij	FEij	AFEij	AFEij	FEij	FEij		

Bits	Bit name	RW-P	Initial value	Function description
31:22	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
21:16	IP4FAPij	RW-P	0H	<p>IPv4 Filtering Address Prefix i</p> <p>Functions:</p> <ul style="list-style-type: none"> - Set port i IPv4 filtering address prefix of FWIP4FACij
15:8	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
7	IP4SOLDAFEij	RW-P	0H	<p>IPv4 Specified Off Link Destination Address Filtering Enable i j</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: IPv4 frames received with a destination IP address which is not equal to network address represented by FWIP4FACij.IP4FAij and FWIP4SFCij.IP4FAPij are rejected. <p>Restrictions:</p> <ul style="list-style-type: none"> - If FWIP4SFCij.IP4FAPij == 0, this bit have to set 1'b0.
6	IP4SDBDAFEij	RW-P	0H	<p>IPv4 Specified Directed Broadcast Destination Address Filtering Enable i j</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: IPv4 frames received with a directed broadcast destination IP address which is network address represented by FWIP4FACij.IP4FAij and FWIP4SFCij.IP4FAPij are rejected.
5	IP4SNDAFEij	RW-P	0H	<p>IPv4 Specified Network Destination Address Filtering Enable i j</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: IPv4 frames received with a network destination IP address which is network address represented by FWIP4FACij.IP4FAij and FWIP4SFCij.IP4FAPij are rejected. <p>Notes:</p> <ul style="list-style-type: none"> - IPv4 network address includes "Network== any (based on the prefix value) : Host== all 0".
4	IP4SUDAFEij	RW-P	0H	<p>IPv4 Specified Unicast Destination Address Filtering Enable i j</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: IPv4 frames received with a unicast destination IP address which is FWIP4FACij.IP4FAij are rejected.
3	IP4SOLSAFEij	RW-P	0H	<p>IPv4 Specified Off Link Source Address Filtering Enable i j</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: IPv4 frames received with a source IP address which is not equal to network address represented by FWIP4FACij.IP4FAij and FWIP4SFCij.IP4FAPij are rejected. <p>Restrictions:</p> <ul style="list-style-type: none"> - If FWIP4SFCij.IP4FAPij == 0, this bit have to set 1'b0.

2	IP4SDBSAFEij	RW-P	0H	<p>IPv4 Specified Directed Broadcast Source Address Filtering Enable i j</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: IPv4 frames received with a directed broadcast source IP address which is network address represented by FWIP4FACij.IP4FAij and FWIP4SFCij.IP4FAPij are rejected.
1	IP4NSSAFEij	RW-P	0H	<p>IPv4 Specified Network Source Address Filtering Enable i j</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: IPv4 frames received with a network source IP address which is network address represented by FWIP4FACij.IP4FAij and FWIP4SFCij.IP4FAPij are rejected. <p>Notes:</p> <ul style="list-style-type: none"> - IPv4 network address includes "Network== any (based on the prefix value) : Host== all 0".
0	IP4SUSAFEij	RW-P	0H	<p>IPv4 Specified Unicast Source Address Filtering Enable i j</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: IPv4 frames received with a unicast source IP address which is FWIP4FACij.IP4FAij are rejected. If setting FWIPF4ACij.IP4FAij to something other than unicast (Example, multicast) frame, that can also be filtered.

(15) FWIP6FAC0ij (i=0..PORT_N-1) (j=0..INTG_FILT_SIPA_N-1)

Forwarding Engine IPv6 Filtering Address Configuration 0 i j

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IP6FAP0ij[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP6FAP0ij[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	IP6FAP0ij	RW-P	0H	IPv6 Filtering Address Part 0 i j Functions: Set port i IPv6 address for filtering j. Recommended setting the unicast address here.

(16) FWIP6FAC1ij (i=0..PORT_N-1) (j=0..INTG_FILT_SIPA_N-1)

Forwarding Engine IPv6 Filtering Address Configuration 1 i j

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IP6FAP1ij[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP6FAP1ij[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	IP6FAP1ij	RW-P	0H	IPv6 Filtering Address Part 1 i j Functions: Set port i IPv6 address for filtering j. Recommended setting the unicast address here.

(17) FWIP6FAC2ij (i=0..PORT_N-1) (j=0..INTG_FILT_SIPA_N-1)

Forwarding Engine IPv6 Filtering Address Configuration 2 i j

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IP6FAP2ij[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP6FAP2ij[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	IP6FAP2ij	RW-P	0H	<p>IPv6 Filtering Address Part 2 i j</p> <p>Functions:</p> <p>Set port i IPv6 address for filtering j. Recommended setting the unicast address here.</p>

(18) FWIP6FAC3ij (i=0..PORT_N-1) (j=0..INTG_FILT_SIPA_N-1)

Forwarding Engine IPv6 Filtering Address Configuration 3 i j

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IP6FAP3ij[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP6FAP3ij[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	IP6FAP3ij	RW-P	0H	IPv6 Filtering Address Part 3 i j Functions: Set port i IPv6 address for filtering j. Recommended setting the unicast address here.

(19) FWIP6SFCij (i=0..PORT_N-1) (j=0..INTG_FILT_SIPA_N-1)

Forwarding Engine IPv6 Specified Filter Configuration i j

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV								IP6FAP[7:0]							
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV								IP6SOLD _i AFEij	IP6SDBD _i AFEij	IP6SNDA _i FEij	IP6SUDA _i FEij	IP6SOLS _i AFEij	IP6SDBS _i AFEij	IP6NSA _i FEij	IP6SUSA _i FEij

Bits	Bit name	RW-P	Initial value	Function description
31:24	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
23:16	IP6FAP _{ij}	RW-P	0H	<p>IPv6 Filtering Address Prefix i Functions: Set port i IPv6 filtering address prefix of {FWIP6FAC0ij,IP6FAP0ij, FWIP6FAC1ij,IP6FAP1ij, FWIP6FAC2ij,IP6FAP2ij, FWIP6FAC3ij,IP6FAP3ij} and FWIP6SFCij,IP6FAPij are rejected.</p>
15:8	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
7	IP6SOLDAFE _{ij}	RW-P	0H	<p>IPv6 Specified Off Link Destination Address Filtering Enable i j Values: - 1'b0: Not filtering. - 1'b1: IPv6 frames received with a destination IP address which is not equal to network address represented by {FWIP6FAC0ij,IP6FAP0ij, FWIP6FAC1ij,IP6FAP1ij, FWIP6FAC2ij,IP6FAP2ij, FWIP6FAC3ij,IP6FAP3ij} and FWIP6SFCij,IP6FAPij are rejected. Restrictions: - If FWIP6SFCij,IP6FAPij == 0, this bit have to set 1'b0.</p>
6	IP6SDBDAFE _{ij}	RW-P	0H	<p>IPv6 Specified Directed Broadcast Destination Address Filtering Enable i j Values: - 1'b0: Not filtering. - 1'b1: IPv6 frames received with a directed broadcast destination IP address which is network address represented by {FWIP6FAC0ij,IP6FAP0ij, FWIP6FAC1ij,IP6FAP1ij, FWIP6FAC2ij,IP6FAP2ij, FWIP6FAC3ij,IP6FAP3ij} and FWIP6SFCij,IP6FAPij are rejected. (IPv6 Directed broadcast destination IP address includes "Network == any : Host == all 1")</p>
5	IP6SNDAFE _{ij}	RW-P	0H	<p>IPv6 Specified Network Destination Address Filtering Enable i j Values: - 1'b0: Not filtering. - 1'b1: IPv6 frames received with a network destination IP address which is network address represented by {FWIP6FAC0ij,IP6FAP0ij, FWIP6FAC1ij,IP6FAP1ij, FWIP6FAC2ij,IP6FAP2ij, FWIP6FAC3ij,IP6FAP3ij} and FWIP6SFCij,IP6FAPij are rejected. Notes: - IPv6 network address includes "Network== any (based on the prefix value) : Host== all 0".</p>
4	IP6SUDAFE _{ij}	RW-P	0H	<p>IPv6 Specified Unicast Destination Address Filtering Enable i j Values: - 1'b0: Not filtering. - 1'b1: IPv6 frames received with a unicast destination IP address which is {FWIP6FAC0ij,IP6FAP0ij, FWIP6FAC1ij,IP6FAP1ij, FWIP6FAC2ij,IP6FAP2ij, FWIP6FAC3ij,IP6FAP3ij} are rejected.</p>

3	IP6SOLSAFEij	RW-P	0H	<p>IPv6 Specified Off Link Source Address Filtering Enable i j</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: IPv6 frames received with a source IP address which is not equal to network address represented by {FWIP6FAC0ij.IP6FAP0ij, FWIP6FAC1ij.IP6FAP1ij, FWIP6FAC2ij.IP6FAP2ij, FWIP6FAC3ij.IP6FAP3ij} and FWIP6SFCij.IP6FAPij are rejected. <p>Restrictions:</p> <ul style="list-style-type: none"> - If FWIP6SFCij.IP6FAPij == 0, this bit have to set 1'b0.
2	IP6SDBSAFEij	RW-P	0H	<p>IPv6 Specified Directed Broadcast Source Address Filtering Enable i j</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: IPv6 frames received with a directed broadcast source IP address which is network address represented by {FWIP6FAC0ij.IP6FAP0ij, FWIP6FAC1ij.IP6FAP1ij, FWIP6FAC2ij.IP6FAP2ij, FWIP6FAC3ij.IP6FAP3ij} and FWIP6SFCij.IP6FAPij are rejected. (IPv6 Directed broadcast source IP address includes "Network == any : Host == all 1")
1	IP6NSSAFEij	RW-P	0H	<p>IPv6 Specified Network Source Address Filtering Enable i j</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: IPv6 frames received with a network source IP address which is network address represented by {FWIP6FAC0ij.IP6FAP0ij, FWIP6FAC1ij.IP6FAP1ij, FWIP6FAC2ij.IP6FAP2ij, FWIP6FAC3ij.IP6FAP3ij} and FWIP6SFCij.IP6FAPij are rejected. <p>Notes:</p> <ul style="list-style-type: none"> - IPv6 network address includes "Network== any (based on the prefix value) : Host== all 0".
0	IP6SUSAFeij	RW-P	0H	<p>IPv6 Specified Unicast Source Address Filtering Enable i j</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: IPv6 frames received with a unicast source IP address which is {FWIP6FAC0ij.IP6FAP0ij, FWIP6FAC1ij.IP6FAP1ij, FWIP6FAC2ij.IP6FAP2ij, FWIP6FAC3ij.IP6FAP3ij} are rejected. If setting {FWIP6FAC0ij.IP6FAP0ij, FWIP6FAC1ij.IP6FAP1ij, FWIP6FAC2ij.IP6FAP2ij, FWIP6FAC3ij.IP6FAP3ij} to something other than unicast (Example, multicast) frame, that can also be filtered.

(20) FWIP4TLCCi (i=0..PORT_N-1)

Forwarding Engine IPv4 Total Length Check Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IP4TLFMXVi[15:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP4TLFMVi[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:16	IP4TLFMXVi	RW-P	0H	<p>IPv4 Total Length Filtering MaXimum Value i</p> <p>Functions:</p> <ul style="list-style-type: none"> - All0: Not filtering. - Other: IPv4 frames with the Total Length field is bigger than this value are rejected.
15:0	IP4TLFMVi	RW-P	0H	<p>IPv4 Total Length Filtering Minimum Value i</p> <p>Functions:</p> <ul style="list-style-type: none"> - All0: Not filtering. - Other: IPv4 frames with the Total Length field is smaller than this value are rejected.

(21) FWIP6PLCCi (i=0..PORT_N-1)

Forwarding Engine IPv6 Payload Length Check Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IP6PLFMXVi[15:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP6PLFMVi[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:16	IP6PLFMXVi	RW-P	0H	<p>IPv6 Payload Length Filtering MaXimum Value i</p> <p>Functions:</p> <ul style="list-style-type: none"> - All0: Not filtering. - Other: IPv6 frames with the Payload Length field is bigger than this value are rejected.
15:0	IP6PLFMVi	RW-P	0H	<p>IPv6 Payload Length Filtering Minimum Value i</p> <p>Functions:</p> <ul style="list-style-type: none"> - All0: Not filtering. - Other: IPv6 frames with the Payload Length field is smaller than this value are rejected.

(22) FWICL4Ci (i=0..PORT_N-1)

Forwarding Engine Integrity Check Layer 4 Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
L4IPLFVi[15:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L4THLFVi[3:0]	RSV	L4N9FEi	L4N8FEi	L4N7FEi	L4N6FEi	L4N5FEi	L4N4FEi	L4N3FEi	L4N2FEi	L4N1FEi	L4N0FEi				

Bits	Bit name	RW-P	Initial value	Function description
31:16	L4IPLFVi	RW-P	0H	<p>Layer4 ICMPv4/ICMPv6 Payload Length Filtering Value i</p> <p>Values:</p> <ul style="list-style-type: none"> - IP Packet Size (the real size of IP header and IP payload without FCS) of Layer4-ICMPv4/Ping or Layer4-ICMPv6/Ping frame (having ICMPv4/ICMPv6 and "Type of ICMP header = 0x0 or 0x8" protocol in payload) used by FWICL4Ci.L4N9FEi bit.
15:12	L4THLFVi	RW-P	0H	<p>Layer4 TCP Header Length Filtering Value i</p> <p>Values:</p> <ul style="list-style-type: none"> - "TCP Header length field" of "IPv4-non-fragmented or IPv4-first-fragmented or IPv6 frame" used by FWICL4Ci.L4N6FEi bit.
11:10	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
9	L4N9FEi	RW-P	0H	<p>Layer 4 No.9 Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: Layer4-ICMPv4/Ping or Layer4-ICMPv6/Ping frames (having ICMPv4/v6 and "Type of ICMP header = 0x0 or 0x8" protocol in payload) received with a "IP Packet Size (the real size of IP header and IP payload without FCS) more than FWICL4Ci.L4IPLFVi" are rejected.
8	L4N8FEi	RW-P	0H	<p>Layer 4 No.8 Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: Layer4-ICMPv4 frames (having ICMPv4 protocol in payload) received with a "IPv4-fragmented frame" are rejected.
7	L4N7FEi	RW-P	0H	<p>Layer 4 No.7 Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: Layer4-TCP frames (having TCP protocol in payload) received with a "IPv4-fragmented frame" are rejected.
6	L4N6FEi	RW-P	0H	<p>Layer 4 No.6 Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Not filtering. - 1'b1: Layer4-TCP frames received with a "TCP Header length field smaller than FWICL4Ci.L4THLFVi" and " IPv4 frame or IPv6 frame" are rejected.

5	L4N5FEi	RW-P	0H	Layer 4 No.5 Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: Layer4-TCP frames received with a "SYN == 1, ACK == 0 and source port smaller than 1024" and " IPv4 frame or IPv6 frame" are rejected.
4	L4N4FEi	RW-P	0H	Layer 4 No.4 Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: Layer4-TCP frames received with a "SYN == 1 and FIN == 1" and " IPv4 frame or IPv6 frame" are rejected.
3	L4N3FEi	RW-P	0H	Layer 4 No.3 Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: Layer4-TCP frames received with a "Sequence_Number == 0 and FIN == 1 and URG == 1 and PSH == 1" and " IPv4 frame or IPv6 frame" are rejected.
2	L4N2FEi	RW-P	0H	Layer 4 No.2 Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: Layer4-TCP frames received with a "Sequence_Number == 0 and TCP_FLAGS == 0" and " IPv4 frame or IPv6 frame" are rejected.
1	L4N1FEi	RW-P	0H	Layer 4 No.1 Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1: Layer4-UDP frames received with a "Source Port == Destination Port" and " IPv4 frame or IPv6 frame" will be rejected.
0	L4N0FEi	RW-P	0H	Layer 4 No.0 Filtering Enable i Values: - 1'b0: Not filtering. - 1'b1 : Layer4-TCP frames received with a "Source Port == Destination Port" and "IPv4 frame or IPv6 frame" will be rejected.

Detail of " fragmented frame" means "(More Fragment FF[2] == 1'b1) or (Fragment Offset FO != All0)".

In other words, "non-fragmented frame" means "(More Fragment FF[2] == 1'b0) and (Fragment Offset FO == All0)"

By the way, "Don't Fragment FF[1]" is don't care.

IPv4 IP header	Version	IHL	ToS	Total Length	Identification	FF []	Fragment Offset	TTL	IP Protocol	Header Checksum	Source IP	Destination IP
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(23) FWICL4THLCi (i=0..PORT_N-1)

Forwarding Engine Integrity Check Layer 4 TCP Header Length Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV												L4THLFMXVi[3:0]			
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV												L4THLFMVi[3:0]			

Bits	Bit name	RW-P	Initial value	Function description
31:20	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
19:16	L4THLFMXVi	RW-P	0H	<p>Layer 4 TCP Header Length Filtering MaXimum Value i</p> <p>Functions:</p> <ul style="list-style-type: none"> - All0: Not filtering. - Other: Layer 4 TCP frames with the Header Length field is bigger than this value are rejected.
15:4	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
3:0	L4THLFMVi	RW-P	0H	<p>Layer 4 TCP Header Length Filtering Minimum Value i</p> <p>Functions:</p> <ul style="list-style-type: none"> - All0: Not filtering. - Other: Layer 4 TCP frames with the Header Length field is smaller than this value are rejected.

3.3.1.4 Layer 3 forwarding/routing/filtering perfect filter function registers

(1) FWTWBFCi (i=0..PFL_TWBF_N-1)

ForWarding engine TWo Byte Filter Configuration i.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
RSV								TWBF0Vi[7:0]									
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
RSV								TWBFI Mi	RSV								TWBFUMi [1:0]

Bits	Bit name	RW-P	Initial value	Function description
31:24	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
23:16	TWBFOVi	RW-P	0H	<p>TWo Byte Filter Offset Value i</p> <p>Functions:</p> <ul style="list-style-type: none"> If FWTWBFCi.TWBFI is 1'b0: Offset in byte where the filter i will start filtering the frame data. If FWTWBFCi.TWBFI is 1'b1: Offset in byte where the filter i will start filtering the frame TAGs. <p>Restrictions:</p> <ul style="list-style-type: none"> SW: If FWTWBFCi.TWBFI is set to 1'b1, this register should be set to 0 to filter S-TAG and set to 2 to filter C-TAG. SW: If FWTWBFCi.TWBFI is set to 1'b1 and FWGC.SVM is set to 2'b01 (C-TAG mode), this register shouldn't be set to 0.
15:9	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
8	TWBFI	RW-P	0H	<p>TWo Byte Filtering Mode i</p> <p>Values:</p> <ul style="list-style-type: none"> 1'b0: Offset filtering. 1'b1: VLAN TAG filtering. <p>Restrictions:</p> <ul style="list-style-type: none"> SW: This register shouldn't be set to 2'b1 if FWGC.SVM is set to 2'b00.
7:2	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
1:0	TWBFI[1:0]	RW-P	0H	<p>TWo Byte Filter Unit Mode i</p> <p>Values :</p> <ul style="list-style-type: none"> 2'b00: Mask mode 2'b01: Expand mode 2'b10: Precise mode 2'b11: Reserved <p>Restrictions:</p> <ul style="list-style-type: none"> SW: This register shouldn't be set to 2'b01 if FWTWBFCi.TWBFI is set to 1'b1.

(2) FWTWBFCi (i=0..PFL_TWBF_N-1)

ForWarding engine TWo Byte Filter Value Configuration i.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TWBFV1i[15:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TWBFV0i[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:16	TWBFV1i	R!=W-P	0H	<p>TWo Byte Filter Value 1 i.</p> <p>Functions:</p> <ul style="list-style-type: none"> If FWTWBFCi.TWBFDUMi is 2'b00: Used as a mask for FWTWBFCi.TWBFDV0i. If FWTWBFCi.TWBFDUMi is 2'b01: Used as an extension for FWTWBFCi.TWBFDV0i (Compare value is { FWTWBFCi.TWBFDV0i, FWTWBFCi.TWBFDV1i}). If FWTWBFCi.TWBFDUMi is 2'b10: Used as 2-byte filter value with a filter ID of $2^i + 1$. <p>Update conditions:</p> <ul style="list-style-type: none"> HW: Writing to FWTWBFCi register will update this register to the last value that has been written to any of the FWTWBFCj.TWBFDV1j registers by the same APB interface.
15:0	TWBFV0i	R!=W-P	0H	<p>TWo Byte Filter Value 0 i.</p> <p>Functions:</p> <ul style="list-style-type: none"> If FWTWBFCi.TWBFDUMi is 2'b00: Used as a 2-byte filter value masked by FWTWBFCi.TWBFDV1i with a filter ID of 2^i. If FWTWBFCi.TWBFDUMi is 2'b01: Used as the first 2-byte of a 4-byte filter extended by FWTWBFCi.TWBFDV1i with a filter ID of 2^i (Compare value is { FWTWBFCi.TWBFDV0i, FWTWBFCi.TWBFDV1i}). If FWTWBFCi.TWBFDUMi is 2'b10: Used as 2-byte filter value with a filter ID of 2^i. <p>Update conditions:</p> <ul style="list-style-type: none"> HW: Writing to FWTWBFCi register will update this register to the last value that has been written to any of the FWTWBFCj.TWBFDV0j registers by the same APB interface.

(3) FWTHBFCi (i=0..PFL_THBF_N-1)

ForWarding engine THree Byte Filter Configuration i.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV								THBFOVi[7:0]							
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV								THBFUMi [1:0]							

Bits	Bit name	RW-P	Initial value	Function description
31:24	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
23:16	THBFOVi	RW-P	0H	THree Byte Filter Offset Value i Functions: - Offset in byte where the filter i will start filtering the frame. (The offset ignores all TAGs)
15:2	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
1:0	THBFUMi[1:0]	RW-P	0H	THree Byte Filter Unit Mode i Values : - 2'b00: Mask mode - 2'b01: Expand mode - 2'b10: Precise mode - 2'b11: Reserved

(4) FWTHBFV0Ci (i=0..PFL_THBF_N-1)

ForWarding engine THree Byte Filter Value 0 Configuration i.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV								THBFV0i[23:16]							
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
THBFV0i[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:24	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
23:0	THBFV0i	R!=W-P	0H	<p>THree Byte Filter Value 0 i.</p> <p>Functions:</p> <ul style="list-style-type: none"> - If FWTHBFCi.THBFUMi is 2'b00: Used as a 3-byte filter value masked by FWTHBFV1Ci.THBFV1i with a filter ID of $2^*(i + \text{PFL_TWBF_N})$. - If FWTHBFCi.THBFUMi is 2'b01: Used as the first 3-byte of a 6-byte filter extended by FWTHBFV1Ci.THBFV1i with a filter ID of $2^*(i + \text{PFL_TWBF_N})$ (Compare value is {FWTHBFV0Ci.THBFV0i, FWTHBFV1Ci.THBFV1i}). - If FWTHBFCi.THBFUMi is 2'b10: Used as 3-byte filter value with a filter ID of $2^*(i + \text{PFL_TWBF_N})$. <p>Update conditions:</p> <ul style="list-style-type: none"> - HW: Writing to FWTHBFCi register will update this register to the last value that has been written to any of the FWTHBFV0Cj.THBFV0j registers by the same APB interface.

(5) FWTHBFV1Ci (i=0..PFL_THBF_N-1)

ForWarding engine THree Byte Filter Value 1 Configuration i.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV								THBFV1i[23:16]							
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
THBFV1i[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:24	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
23:0	THBFV1i	R!=W-P	0H	<p>THree Byte Filter Value 1 i.</p> <p>Functions:</p> <ul style="list-style-type: none"> - If FWTHBFCi.THBFUMi is 2'b00: Used as a mask for FWTHBFV0Ci.THBFV0i. - If FWTHBFCi.THBFUMi is 2'b01: Used as an extension for FWTHBFV0Ci.THBFV0i (Compare value is { FWTHBFV0Ci.THBFV0i, FWTHBFV1Ci.THBFV1i}). - If FWTHBFCi.THBFUMi is 2'b10: Used as 3-byte filter value with a filter ID of $2^*(i + PFL_TWBF_N) + 1$. <p>Update conditions:</p> <ul style="list-style-type: none"> - HW: Writing to FWTHBFCi register will update this register to the last value that has been written to any of the FWTHBFV1Cj.THBFV1j registers by the same APB interface.

(6) FWFOBFCi (i=0..PFL_FOBF_N-1)

ForWarding engine FOUr Byte Filter Configuration i.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV								FOBFVOi[7:0]							
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV								FOBFUMi [1:0]							

Bits	Bit name	RW-P	Initial value	Function description
31:24	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
23:16	FOBFVOi	RW-P	0H	FOUr Byte Filter Offset Value i Functions: - Offset in byte where the filter i will start filtering the frame. (The offset ignores all TAGs)
15:2	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
1:0	FOBFUMi[1:0]	RW-P	0H	FOUr Byte Filter Unit Mode i Values : - 2'b00: Mask mode - 2'b01: Expand mode - 2'b10: Precise mode - 2'b11: Reserved

(7) FWFOBFV0Ci (i=0..PFL_FOBF_N-1)

ForWarding engine FOur Byte Filter Value 0 Configuration i.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FOBFV0i[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOBFV0i[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	FOBFV0i	R!=W-P	0H	<p>FOUr Byte Filter Value 0 i.</p> <p>Functions:</p> <ul style="list-style-type: none"> If FWFOBFCi. FOBFUMi is 2'b00: Used as a 4-byte filter value masked by FWFOBFV1Ci. FOBFV1i with a filter ID of $2^*(i + PFL_TWBF_N + PFL_THBF_N)$. If FWFOBFCi. FOBFUMi is 2'b01: Used as the first 4-byte of a 8-byte filter extended by FWFOBFV1Ci. FOBFV1i with a filter ID of $2^*(i + PFL_TWBF_N + PFL_THBF_N)$ (Compare value is {FWFOBFV0Ci.FOBFV0i, FWFOBFV1Ci.FOBFV1i}). If FWFOBFCi. FOBFUMi is 2'b10: Used as 4-byte filter value with a filter ID of $2^*(i + PFL_TWBF_N + PFL_THBF_N)$. <p>Update conditions:</p> <ul style="list-style-type: none"> HW: Writing to FWFOBFCi register will update this register to the last value that has been written to any of the FWFOBFV0Cj. FOBFV0j registers by the same APB interface.

(8) FWFOBFV1Ci (i=0..PFL_FOBF_N-1)

ForWarding engine FOUr Byte Filter Value 1 Configuration i.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FOBFV1i[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOBFV1i[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:24	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
31:0	FOBFV1i	R!=W-P	0H	<p>FOUr Byte Filter Value 1 i.</p> <p>Functions:</p> <ul style="list-style-type: none"> - If FWFOBFCi. FOBFUMi is 2'b00: Used as a mask for FWFOBFV0Ci. FOBFV0i. - If FWFOBFCi. FOBFUMi is 2'b01: Used as an extension for FWFOBFV0Ci. FOBFV0i (Compare value is { FWFOBFV0Ci. FOBFV0i, FWFOBFV1Ci. FOBFV1i}). - If FWFOBFCi. FOBFUMi is 2'b10: Used as 4-byte filter value with a filter ID of 2*(i + PFL_TWBF_N + PFL_THBF_N) + 1. <p>Update conditions:</p> <ul style="list-style-type: none"> - HW: Writing to FWFOBFCi register will update this register to the last value that has been written to any of the FWFOBFV1Cj. FOBFV1j registers by the same APB interface.

(9) FWRFCi (i=0..PFL_RAGF_N-1)

ForWarding engine Range Filter Configuration i.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
RSV								RFOVi[7:0]									
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
RSV								RFEMi	RFOMi	RSV							

Bits	Bit name	RW-P	Initial value	Function description
31:24	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
23:16	RFOVi	RW-P	0H	<p>Range Filter Offset Value i</p> <p>Functions:</p> <ul style="list-style-type: none"> If FWRFCi.RFOMi is 1'b0: Offset in byte where the filter i will start filtering the frame data. If FWRFCi.RFOMi is 1'b1: Offset in byte where the filter i will start filtering the frame TAGs. <p>Restrictions:</p> <ul style="list-style-type: none"> SW: If FWRFCi.RFOMi is set to 1'b1, this register should be set to 0 (S-TAG filter) or 2 (C-TAG filter). SW: If FWRFCi.RFOMi is set to 1'b1 and FWGC.SVM is set to 2'b01 (C-TAG mode), this register shouldn't be set to 0.
15:10	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
9	RFEMi	RW-P	0H	<p>Range Filtering Extension Mode i</p> <p>Values:</p> <ul style="list-style-type: none"> 1'b0: Range Filtering Normal Mode. 1'b1: Range Filtering Extension Mode. <p>Restrictions:</p> <ul style="list-style-type: none"> SW: If FWRFCi.RFOMi is set to 1'b1, this register shouldn't be set to 1'b1 (this register is no valid).
8	RFOMi	RW-P	0H	<p>Range Filtering Offset Mode i</p> <p>Values:</p> <ul style="list-style-type: none"> 1'b0: Offset filtering. 1'b1: VLAN TAG filtering. <p>Restrictions:</p> <ul style="list-style-type: none"> SW: If FWGC.SVM is set to 2'b00, this register shouldn't be set to 1'b1. SW: If FWRFCi.RFEMi is set to 1'b1, this register shouldn't be set to 1'b1.
7:0	RSV	R0-U	0H	Reserved area. On read, 0 will be returned

(10) FWRFSCi (i=0..PFL_RAGF_N-1)

Forwarding Engine Range Filter Start Value Configuration i.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RFSV1i[15:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFSV0i[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:16	RFSV1i	R!=W-P	0H	<p>Range Filter Start Value 1 i.</p> <p>Functions:</p> <ul style="list-style-type: none"> If FWRFCi.RFEMi is 1'b0: Used has range filter start value with a filter ID of $2^*(i + PFL_TWBF_N + PFL_THBF_N + PFL_FOBF_N) + 1$ (Compare value is from FWRFSCi.RFSV1i to FWRFEVCi.RFEV1i). If FWRFCi.RFEMi is 1'b1: Used as an extension for FWRFSCi.RFSV0i (Compare value is from {FWRFSCi.RFSV1i, FWRFSCi.RFSV0i} to {FWRFEVCi.RFEV1i, FWRFEVCi.RFEV0i}). <p>Update conditions:</p> <ul style="list-style-type: none"> HW: Writing to FWRFCi register will update this register to the last value that has been written to any of the FWRFSCj.RFSV0j and FWRFEVCj.RFEV0j registers by the same APB interface. <p>Restrictions</p> <ul style="list-style-type: none"> SW: If FWRFCi.RFOMi is set to 1'b1, the value of FWRFSCi.RFSV1i[15:12] and FWRFSCi.RFEV1i[15:12] should be set to 0.
15:0	RFSV0i	R!=W-P	0H	<p>Range Filter Start Value 0 i.</p> <p>Functions:</p> <ul style="list-style-type: none"> If FWRFCi.RFEMi is 1'b0: Used has range filter start value with a filter ID of $2^*(i + 1 + PFL_TWBF_N + PFL_THBF_N + PFL_FOBF_N)$ (Compare value is from FWRFSCi.RFSV0i to FWRFEVCi.RFEV0i). If FWRFCi.RFEMi is 1'b1: Used as the first 2-byte of a 4-byte filter extended by FWRFSCi.RFSV1i (Compare value is from {FWRFSCi.RFSV1i, FWRFSCi.RFSV0i} to {FWRFEVCi.RFEV1i, FWRFEVCi.RFEV0i}). <p>Update conditions:</p> <ul style="list-style-type: none"> HW: Writing to FWRFCi register will update this register to the last value that has been written to any of FWRFSCj.RFSV0j and FWRFEVCj.RFEV0j registers by the same APB interface. <p>Restrictions</p> <ul style="list-style-type: none"> SW: If FWRFCi.RFOMi is set to 1'b1, the value of FWRFSCi.RFSV0i[15:12] and FWRFSCi.RFEV0i[15:12] should be set to 0.

(11) FWRFEVCi (i=0..PFL_RAGF_N-1)

Forwarding Engine Range Filter End Value Configuration i.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RFEV1i[15:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFEV0i[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:16	RFEV1i	R!=W-P	0H	<p>Range Filter End Value 1 i.</p> <p>Functions:</p> <ul style="list-style-type: none"> If FWRFCi.RFEMi is 1'b0: Used has range filter end value with a filter ID of $2*(i + PFL_TWBF_N + PFL_THBF_N + PFL_FOBF_N) + 1$ (Compare value is from FWRFSVCi.RFSV1i to FWRFEVCi.RFEV1i). If FWRFCi.RFEMi is 1'b1: Used as an extension for FWRFSVCi.RFEV0i (Compare value is from {FWRFSVCi.RFSV1i, FWRFSVCi.RFSV0i} to {FWRFEVCi.RFEV1i, FWRFEVCi.RFEV0i}). <p>Update conditions:</p> <ul style="list-style-type: none"> HW: Writing to FWRFCi register will update this register to the last value that has been written to any of the FWRFSVCj.RFSV0j and FWRFEVCj.RFEV0j registers by the same APB interface. <p>Restrictions</p> <ul style="list-style-type: none"> SW: If FWRFCi.RFOMi is set to 1'b1, the value of FWRFSVCi.RFSV1i[15:12] and FWRFSVCi.RFEV1i[15:12] should be set to 0.
15:0	RFEV0i	R!=W-P	0H	<p>Range Filter End Value 0 i.</p> <p>Functions:</p> <ul style="list-style-type: none"> If FWRFCi.RFEMi is 1'b0: Used has range filter end value with a filter ID of $2*(i + 1 + PFL_TWBF_N + PFL_THBF_N + PFL_FOBF_N)$ (Compare value is from FWRFSVCi.RFSV0i to FWRFEVCi.RFEV0i). If FWRFCi.RFEMi is 1'b1: Used as the first 2-byte of a 4-byte filter extended by FWRFSVCi.RFEV1i (Compare value is from {FWRFSVCi.RFSV1i, FWRFSVCi.RFSV0i} to {FWRFEVCi.RFEV1i, FWRFEVCi.RFEV0i}). <p>Update conditions:</p> <ul style="list-style-type: none"> HW: Writing to FWRFCi register will update this register to the last value that has been written to any of FWRFSVCj.RFSV0j and FWRFEVCj.RFEV0j registers by the same APB interface. <p>Restrictions</p> <ul style="list-style-type: none"> SW: If FWRFCi.RFOMi is set to 1'b1, the value of FWRFSVCi.RFSV0i[15:12] and FWRFSVCi.RFEV0i[15:12] should be set to 0.

(12) FWCF Ci (i=0..PFL_CADF_N-1)

Forwarding Engine Cascade Filter Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CFMMi	RSV / CFPFFVi[PORT_TSNA_N -1:0]														
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RSV / CFEFFVi[PORT_N-1:0]														

Bits	Bit name	RW-P	Initial value	Function description
31	CFMMi	RW-P	0H	Cascade Filter Match Mode i Values: - 1'b0: All (AND) Match Mode. - 1'b1: Partial (OR) Match Mode.
30: PORT_TSNA_N +16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PORT_TSNA_N +15:16	CFPFFVi	RW-P	0H	Cascade Filter P-Frame Filter Valid Value: - Bit j is 1'b0: Cascade filter i is disabled for port j p-frames. - Bit j is 1'b1: Cascade filter i is enabled for port j p-frames.
15:PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PORT_N-1:0	CFEFFVi	RW-P	0H	Cascade Filter E-Frame Filter Valid Value: - Bit j is 1'b0: Cascade filter i is disabled for port j e-frames (All slow ports frames are e-frames) [GWCA]. - Bit j is 1'b1: Cascade filter i is enabled for port j e-frames (All slow ports frames are e-frames) [GWCA].

(13) FWCFMCij (i=0..PFL_CADF_N-1) (j=0..PFL_CFMF_N-1)

Forwarding Engine Cascade Filter Mapping Configuration i j

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFFV ij	RSV / CFFNij[PFL_TFIL_W-1:0]														

Bits	Bit name	RW-P	Initial value	Function description
31:16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
15	CFFVij	R!=W-P	0B	<p>Cascade Filter Filter Valid i j</p> <p>Function:</p> <ul style="list-style-type: none"> - Enables FWCFMCij.CFFNij for cascade filter i. - If no one of the FWCFMCij.CFFVij is equal to 1, cascade filter i is disabled. <p>Update conditions:</p> <ul style="list-style-type: none"> - HW: Writing to FWCFCI register will update this register to the last value that has been written to FWCFMCkj.CFFVkj register (k can take any value) by the same APB interface. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: Be sure to specify the lowest address for j=0 among cascade filters. Filter of j=0 will be matched first, which helps reduce power consumption.
14:PFL_TFIL_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned

PFL_TFIL_W-1:0	CFFNij	R!=W-P	0B	<p>Cascade Filter Filter Number i j</p> <p>Function:</p> <ul style="list-style-type: none"> - Map filter number FWCFMCij.CFFNij to cascade filter number i. <p>Update conditions:</p> <ul style="list-style-type: none"> - HW: Writing to FWCFCi register will update this register to the last value that has been written to FWCFMCKj.CFFNkj register (k can take any value) by the same APB interface. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW&SW: This value have to set within the following range. If violate this restriction (set out of range), cascade filter (FWCFMFij.CFFVij) will be invalid. (x=0, 1, 2, 3) $(i=x*(PFL_CADF_N/4)-(x+1)*(PFL_CADF_N/4)-1)$ $PFL_TWBF_N*2^{(x/4)}$ $\leq \text{FWCFMFij.CFFNij}$ $\leq PFL_TWBF_N*2^{((x+1)/4)-1}$ OR $PFL_THBF_N*2^{(x/4)}+(PFL_TWBF_N)*2$ $\leq \text{FWCFMFij.CFFNij}$ $\leq PFL_THBF_N*2^{((x+1)/4)-1}+(PFL_TWBF_N)*2$ OR $PFL_FOBF_N*2^{(x/4)}+(PFL_TWBF_N+PFL_THBF_N)*2$ $\leq \text{FWCFMFij.CFFNij}$ $\leq PFL_FOBF_N*2^{((x+1)/4)-1}+(PFL_TWBF_N+PFL_THBF_N)*2$ OR $PFL_RAGF_N*2^{(x/4)}+(PFL_TWBF_N+PFL_THBF_N+ PFL_FOBF_N)*2$ $\leq \text{FWCFMFij.CFFNij}$ $\leq PFL_RAGF_N*2^{((x+1)/4)-1}+(PFL_TWBF_N+PFL_THBF_N+ PFL_FOBF_N)*2$ <p>[Example]</p> <p>{0, 1024, 1280, 2304} <= FWCFMC0-127j.CFFN0-127j <= {255, 1087, 1535, 2367} {256, 1088, 1536, 2368} <= FWCFMC128-255j.CFFN128-255j <= {511, 1151, 1791, 2431} {512, 1152, 1792, 2432} <= FWCFMC256-383j.CFFN256-383j <= {767, 1215, 2047, 2495} {768, 1216, 2048, 2496} <= FWCFMC384-511j.CFFN384-511j <= {1023, 1279, 2303, 2559}</p>
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3.3.1.5 Layer 3 forwarding/routing/filtering L3/L2 Stream hash ID function registers

(1) FWIP4SC

Forwarding Engine IPv4 Stream Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV							IP4IDP TS	IP4IID S	IP4IIS S	IP4ICD S	IP4ICP TS	IP4ICV S	IP4ISD S	IP4ISP S	IP4ISV S
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV			IP4IDP TH	IP4ISP TH	IP4IPH	IP4IID H	IP4IIS H	IP4ICD H	IP4ICP H	IP4ICV H	IP4ISD H	IP4ISP H	IP4ISV H	IP4IM SH	IP4IM DH

Bits	Bit name	RW-P	Initial value	Function description
31:25	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
24	IP4IDPTS	RW-RP	0B	<p>IPv4 Include Destination Port in Stream</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: TCP/UDP Destination port is not included in L3 IPv4 stream ID - 1'b1: TCP/UDP Destination port is included in L3 IPv4 stream ID
23	IP4IIDS	RW-RP	0B	<p>IPv4 Include IP Destination in Stream</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: IPv4 Destination IP address is not included in L3 IPv4 stream ID - 1'b1: IPv4 Destination IP address is included in L3 IPv4 stream ID
22	IP4IISS	RW-RP	0B	<p>IPv4 Include IP Source in Stream</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: IPv4 Source IP address is not included in L3 IPv4 stream ID - 1'b1: IPv4 Source IP address is included in L3 IPv4 stream ID
21	IP4ICDS	RW-RP	0B	<p>IPv4 Include C-TAG DEI in Stream</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: C-TAG DEI is not included in L3 IPv4 stream ID - 1'b1: C-TAG DEI is included in L3 IPv4 stream ID <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00, this register should be set to 0.
20	IP4ICPS	RW-RP	0B	<p>IPv4 Include C-TAG PCP in Stream</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: C-TAG PCP is not included in L3 IPv4 stream ID - 1'b1: C-TAG PCP is included in L3 IPv4 stream ID <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00, this register should be set to 0.
19	IP4ICVS	RW-RP	0B	<p>IPv4 Include C-TAG VLAN ID in Stream</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: C-TAG VLAN ID is not included in L3 IPv4 stream ID - 1'b1: C-TAG VLAN ID is included in L3 IPv4 stream ID <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00, this register should be set to 0.

18	IP4ISDS	RW-RP	0B	<p>IPv4 Include S-TAG DEI in Stream</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: S-TAG DEI is not included in L3 IPv4 stream ID - 1'b1: S-TAG DEI is included in L3 IPv4 stream ID <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00 or 2'b01, this register should be set to 0.
17	IP4ISPS	RW-RP	0B	<p>IPv4 Include S-TAG PCP in Stream</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: S-TAG PCP is not included in L3 IPv4 stream ID - 1'b1: S-TAG PCP is included in L3 IPv4 stream ID <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00 or 2'b01, this register should be set to 0.
16	IP4ISVS	RW-RP	0B	<p>IPv4 Include S-TAG VLAN ID in Stream</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: S-TAG VLAN ID is not included in L3 IPv4 stream ID - 1'b1: S-TAG VLAN ID is included in L3 IPv4 stream ID <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00 or 2'b01, this register should be set to 0.
15:13	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
12	IP4IDPTH	RW-RP	0B	<p>IPv4 Include Destination Port in Hash</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: TCP/UDP Destination port is not included in hash calculation - 1'b1: TCP/UDP Destination port is included in hash calculation
11	IP4ISPTH	RW-RP	0B	<p>IPv4 Include Source Port in Hash</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: TCP/UDP Source port is not included in hash calculation - 1'b1: TCP/UDP Source port is included in hash calculation
10	IP4IPH	RW-RP	0B	<p>IPv4 Include Protocol in Hash</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: IPv4 Protocol is not included in hash calculation - 1'b1: IPv4 Protocol is included in hash calculation
9	IP4IIDH	RW-RP	0B	<p>IPv4 Include IP Destination in Hash</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: IPv4 Destination IP address is not included in hash calculation - 1'b1: IP v4 Destination IP address is included in hash calculation
8	IP4IISH	RW-RP	0B	<p>IPv4 Include IP Source in Hash</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: IPv4 Source IP address is not included in hash calculation - 1'b1: IPv4 Source IP address is included in hash calculation
7	IP4ICDH	RW-RP	0B	<p>IPv4 Include C-TAG DEI in Hash</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: C-TAG DEI is not included in hash calculation - 1'b1: C-TAG DEI is included in hash calculation <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00, this register should be set to 0.

6	IP4ICPH	RW-RP	0B	<p>IPv4 Include C-TAG PCP in Hash</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: C-TAG PCP is not included in hash calculation - 1'b1: C-TAG PCP is included in hash calculation <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00, this register should be set to 0.
5	IP4ICVH	RW-RP	0B	<p>IPv4 Include C-TAG VLAN ID in Hash</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: C-TAG VLAN ID is not included in hash calculation - 1'b1: C-TAG VLAN ID is included in hash calculation <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00, this register should be set to 0.
4	IP4ISDH	RW-RP	0B	<p>IPv4 Include S-TAG DEI in Hash</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: S-TAG DEI is not included in hash calculation - 1'b1: S-TAG DEI is included in hash calculation <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00 or 2'b01, this register should be set to 0.
3	IP4ISPHE	RW-RP	0B	<p>IPv4 Include S-TAG PCP in Hash</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: S-TAG PCP is not included in hash calculation - 1'b1: S-TAG PCP is included in hash calculation <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00 or 2'b01, this register should be set to 0.
2	IP4ISVH	RW-RP	0B	<p>IPv4 Include S-TAG VLAN ID in Hash</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: S-TAG VLAN ID is not included in hash calculation - 1'b1: S-TAG VLAN ID is included in hash calculation <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00 or 2'b01, this register should be set to 0.
1	IP4IMSH	RW-RP	0B	<p>IPv4 Include MAC Source in Hash</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: MAC Source address is not included in hash calculation - 1'b1: MAC Source address is included in hash calculation
0	IP4IMDH	RW-RP	0B	<p>IPv4 Include MAC Destination in Hash</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: MAC Destination address is not included in hash calculation - 1'b1: MAC Destination address is included in hash calculation

(2) FWIP6SC

Forwarding Engine IPv6 Stream Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV							IP6IDP TS	IP6II1 S	IP6II0 S	IP6ICD S	IP6ICP S	IP6ICV S	IP6ISD S	IP6ISP S	IP6ISV S
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV			IP6IDP TH	IP6ISP TH	IP6IPH	IP6IID H	IP6IIS H	IP6ICD H	IP6ICP H	IP6ICV H	IP6ISD H	IP6ISP H	IP6ISV H	IP6IM SH	IP6IM DH

Bits	Bit name	RW-P	Initial value	Function description
31:25	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
24	IP6IDPTS	RW-RP	0B	<p>IPv6 Include Destination Port in Stream</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: TCP/UDP Destination port is not included in L3 IPv6 stream ID - 1'b1: TCP/UDP Destination port is included in L3 IPv6 stream ID
23	IP6II1S	RW-RP	0B	<p>IPv6 Include IP 1 in Stream</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: IPv6 IP address part 1 is not included in L3 IPv6 stream ID - 1'b1: IPv6 IP address part 1 is included in L3 IPv6 stream ID <p>Function:</p> <ul style="list-style-type: none"> - IPv6 IP address part 1 is a 4-byte byte length field extracted from the IP source or destination address depending on FWIP6OC configuration.
22	IP6II0S	RW-RP	0B	<p>IPv6 Include IP 0 in Stream</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: IPv6 IP address part 0 is not included in L3 IPv6 stream ID - 1'b1: IPv6 IP address part 0 is included in L3 IPv6 stream ID <p>Function</p> <ul style="list-style-type: none"> - IPv6 IP address part 0 is a 4-byte byte length field extracted from the IP source or destination address depending on FWIP6OC configuration.
21	IP6ICDS	RW-RP	0B	<p>IPv6 Include C-TAG DEI in Stream</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: C-TAG DEI is not included in L3 IPv6 stream ID - 1'b1: C-TAG DEI is included in L3 IPv6 stream ID <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00, this register should be set to 0.
20	IP6ICPS	RW-RP	0B	<p>IPv6 Include C-TAG PCP in Stream</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: C-TAG PCP is not included in L3 IPv6 stream ID - 1'b1: C-TAG PCP is included in L3 IPv6 stream ID <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00, this register should be set to 0.

19	IP6ICVS	RW-RP	0B	<p>IPv6 Include C-TAG VLAN ID in Stream</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: C-TAG VLAN ID is not included in L3 IPv6 stream ID - 1'b1: C-TAG VLAN ID is included in L3 IPv6 stream ID <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00, this register should be set to 0.
18	IP6ISDS	RW-RP	0B	<p>IPv6 Include S-TAG DEI in Stream</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: S-TAG DEI is not included in L3 IPv6 stream ID - 1'b1: S-TAG DEI is included in L3 IPv6 stream ID <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00 or 2'b01, this register should be set to 0.
17	IP6ISPS	RW-RP	0B	<p>IPv6 Include S-TAG PCP in Stream</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: S-TAG PCP is not included in L3 IPv6 stream ID - 1'b1: S-TAG PCP is included in L3 IPv6 stream ID <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00 or 2'b01, this register should be set to 0.
16	IP6ISVS	RW-RP	0B	<p>IPv6 Include S-TAG VLAN ID in Stream</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: S-TAG VLAN ID is not included in L3 IPv6 stream ID - 1'b1: S-TAG VLAN ID is included in L3 IPv6 stream ID <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00 or 2'b01, this register should be set to 0.
15:13	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
12	IP6IDPTH	RW-RP	0B	<p>IPv6 Include Destination Port in Hash</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: TCP/UDP Destination port is not included in hash calculation - 1'b1: TCP/UDP Destination port is included in hash calculation
11	IP6ISPTH	RW-RP	0B	<p>IPv6 Include Source Port in Hash</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: TCP/UDP Source port is not included in hash calculation - 1'b1: TCP/UDP Source port is included in hash calculation
10	IP6IPH	RW-RP	0B	<p>IPv6 Include Protocol in Hash (Next Header)</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: IPv6 Protocol is not included in hash calculation - 1'b1: IPv6 Protocol is included in hash calculation
9	IP6IIDH	RW-RP	0B	<p>IPv6 Include IP Destination in Hash</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: IPv6 Destination IP address is not included in hash calculation - 1'b1: IPv6 Destination IP address is included in hash calculation
8	IP6IISH	RW-RP	0B	<p>IPv6 Include IP Source in Hash</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: IPv6 Source IP address is not included in hash calculation - 1'b1: IPv6 Source IP address is included in hash calculation

7	IP6ICDH	RW-RP	0B	<p>IPv6 Include C-TAG DEI in Hash</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: C-TAG DEI is not included in hash calculation - 1'b1: C-TAG DEI is included in hash calculation <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00, this register should be set to 0.
6	IP6ICPH	RW-RP	0B	<p>IPv6 Include C-TAG PCP in Hash</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: C-TAG PCP is not included in hash calculation - 1'b1: C-TAG PCP is included in hash calculation <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00, this register should be set to 0.
5	IP6ICVH	RW-RP	0B	<p>IPv6 Include C-TAG VLAN ID in Hash</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: C-TAG VLAN ID is not included in hash calculation - 1'b1: C-TAG VLAN ID is included in hash calculation <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00, this register should be set to 0.
4	IP6ISDH	RW-RP	0B	<p>IPv6 Include S-TAG DEI in Hash</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: S-TAG DEI is not included in hash calculation - 1'b1: S-TAG DEI is included in hash calculation <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00 or 2'b01, this register should be set to 0.
3	IP6ISPH	RW-RP	0B	<p>IPv6 Include S-TAG PCP in Hash</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: S-TAG PCP is not included in hash calculation - 1'b1: S-TAG PCP is included in hash calculation <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00 or 2'b01, this register should be set to 0.
2	IP6ISVH	RW-RP	0B	<p>IPv6 Include S-TAG VLAN ID in Hash</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: S-TAG VLAN ID is not included in hash calculation - 1'b1: S-TAG VLAN ID is included in hash calculation <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00 or 2'b01, this register should be set to 0.
1	IP6IMSH	RW-RP	0B	<p>IPv6 Include MAC Source in Hash</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: MAC Source address is not included in hash calculation - 1'b1: MAC Source address is included in hash calculation
0	IP6IMDH	RW-RP	0B	<p>IPv6 Include MAC Destination in Hash</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: MAC Destination address is not included in hash calculation - 1'b1: MAC Destination address is included in hash calculation

(3) FWIP6OC

Forwarding Engine IPv6 Offset Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV								IP6IPO1[3:0]				RSV			IP6IPO M1
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV								IP6IPO0[3:0]				RSV			IP6IPO M0

Bits	Bit name	RW-P	Initial value	Function description
31:24	RSV	RO-U	0H	Reserved area. On read, 0 will be returned
23:20	IP6IPO1	RW-RP	0H	<p>IPv6 IP Offset 1</p> <p>Values:</p> <ul style="list-style-type: none"> - i: Byte [i:i+3] of selected IP address are used for IPv6 IP address part 1. <p>Restriction:</p> <ul style="list-style-type: none"> - SW: This register shouldn't be set to a value bigger than 12.
19:17	RSV	RO-U	0H	Reserved area. On read, 0 will be returned
16	IP6IPOM1	RW-RP	0B	<p>IPv6 IP Offset mode 1</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: IPv6 IP address part 1 is extracted from IP source address - 1'b1: IPv6 IP address part 1 is extracted from IP destination address
15:8	RSV	RO-U	0H	Reserved area. On read, 0 will be returned
7:4	IP6IPO0	RW-RP	0H	<p>IPv6 IP Offset 0</p> <p>Values:</p> <ul style="list-style-type: none"> - i: Byte [i:i+3] of selected IP address are used for IPv6 IP address part 0. <p>Restriction:</p> <ul style="list-style-type: none"> - SW: This register shouldn't be set to a value bigger than 12.
3:1	RSV	RO-U	0H	Reserved area. On read, 0 will be returned
0	IP6IPOM0	RW-RP	0B	<p>IPv6 IP Offset mode 0</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: IPv6 IP address part 0 is extracted from IP source address - 1'b1: IPv6 IP address part 0 is extracted from IP destination address

(4) FWL2SC

Forwarding Engine Layer 2 Stream Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV								L2ICD S	L2ICP S	L2ICV S	L2ISD S	L2ISP S	L2ISV S	L2IMS S	L2IMD S

Bits	Bit name	RW-P	Initial value	Function description
31:8	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
7	L2ICDS	RW-RP	0B	<p>Layer 2 Include C-TAG DEI in Stream</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: MAC C-TAG DEI is not included in L2 stream ID - 1'b1: MAC C-TAG DEI is included in L2 stream ID <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00, this register should be set to 0.
6	L2ICPS	RW-RP	0B	<p>Layer 2 Include C-TAG PCP ID in Stream</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: MAC C-TAG PCP is not included in L2 stream ID - 1'b1: MAC C-TAG PCP is included in L2 stream ID <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00, this register should be set to 0.
5	L2ICVS	RW-RP	0B	<p>Layer 2 Include C-TAG VLAN ID in Stream</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: MAC C-TAG VLAN ID is not included in L2 stream ID - 1'b1: MAC C-TAG VLAN ID is included in L2 stream ID <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00, this register should be set to 0.
4	L2ISDS	RW-RP	0B	<p>Layer 2 Include S-TAG DEI in Stream</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: MAC S-TAG DEI is not included in L2 stream ID - 1'b1: MAC S-TAG DEI is included in L2 stream ID <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00 or 2'b01, this register should be set to 0.
3	L2ISPS	RW-RP	0B	<p>Layer 2 Include S-TAG PCP ID in Stream</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: MAC S-TAG PCP is not included in L2 stream ID - 1'b1: MAC S-TAG PCP is included in L2 stream ID <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00 or 2'b01, this register should be set to 0.

2	L2ISVS	RW-RP	0B	<p>Layer 2 Include S-TAG VLAN ID in Stream</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: MAC S-TAG VLAN ID is not included in L2 stream ID - 1'b1: MAC S-TAG VLAN ID is included in L2 stream ID <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: If FWGC.SVM is set to 2'b00 or 2'b01, this register should be set to 0.
1	L2IMSS	RW-RP	0B	<p>Layer 2 Include MAC Source in Stream</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: MAC Source address is not included in L2 stream ID - 1'b1: MAC Source address is included in L2 stream ID
0	L2IMDS	RW-RP	0B	<p>Layer 2 Include MAC Destination in Stream</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: MAC Destination address is not included in L2 stream ID - 1'b1: MAC Destination address is included in L2 stream ID

(5) FWSFHEC

Forwarding Engine Stream Filter Hash Equation Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IP6HE[15:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP4HE[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:16	IP6HE	RW-F	1H	<p>Stream Filter Hash Equation</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit 0 is set: Hash equation $1+x^{17}$ is activated in Hash function for IPv6 Hash calculation. - Bit i ($i!=0$) is set: Hash equation $1+x^{i+1}+x^{17}$ is activated in Hash function for IPv6 Hash calculation <p>Function:</p> <ul style="list-style-type: none"> - If several Hash equations are activated, the result of all activated equation are XORed to give the final Hash ID.
15:0	IP4HE	RW-F	1H	<p>Stream Filter Hash Equation</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit 0 is set: Hash equation $1+x^{17}$ is activated in Hash function for IPv4 Hash calculation. - Bit i ($i!=0$) is set: Hash equation $1+x^{i+1}+x^{17}$ is activated in Hash function for IPv4 Hash calculation <p>Function:</p> <ul style="list-style-type: none"> - If several Hash equations are activated, the result of all activated equation are XORed to give the final Hash ID.

(6) FWSHCR0

Forwarding Engine Software Hash Calculation Request 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SHCMDP0[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHCMDP0[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	SHCMDP0	RW-D	0H	Software Hash Calculation MAC Destination Part 0 Functions: - SW: This register is used to accelerate hash calculation.

(7) FWSHCR1

Forwarding Engine Software Hash Calculation Request 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SHCMDP1[15:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHCMSP0[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:16	SHCMDP1	RW-D	0H	<p>Software Hash Calculation MAC Destination Part 1</p> <p>Functions:</p> <ul style="list-style-type: none"> - SW: This register is used to accelerate hash calculation.
15:0	SHCMSP0	RW-D	0H	<p>Software Hash Calculation MAC Source Part 0</p> <p>Functions:</p> <ul style="list-style-type: none"> - SW: This register is used to accelerate hash calculation.

(8) FWSHCR2

Forwarding Engine Software Hash Calculation Request 2

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SHCMSP1[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHCMSP1[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	SHCMSP1	RW-D	0H	<p>Software Hash Calculation MAC Source Part 1</p> <p>Functions:</p> <ul style="list-style-type: none"> - SW: This register is used to accelerate hash calculation.

(9) FWSHCR3

Forwarding Engine Software Hash Calculation Request 3

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SHCSP[2:0]			SHCS D	SHCSV[11:0]											
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHCCP[2:0]			SHCC D	SHCCV[11:0]											

Bits	Bit name	RW-P	Initial value	Function description
31:29	SHCSP	RW-D	0H	Software Hash Calculation S-TAG PCP Functions: - SW: This register is used to accelerate hash calculation.
28	SHCSD	RW-D	0H	Software Hash Calculation S-TAG DEI Functions: - SW: This register is used to accelerate hash calculation.
27:16	SHCSV	RW-D	0H	Software Hash Calculation S-TAG VLAN Functions: - SW: This register is used to accelerate hash calculation.
15:13	SHCCP	RW-D	0H	Software Hash Calculation C-TAG PCP Functions: - SW: This register is used to accelerate hash calculation.
12	SHCCD	RW-D	0H	Software Hash Calculation C-TAG DEI Functions: - SW: This register is used to accelerate hash calculation.
11:0	SHCCV	RW-D	0H	Software Hash Calculation C-TAG VLAN Functions: - SW: This register is used to accelerate hash calculation.

(10) FWSHCR4

Forwarding Engine Software Hash Calculation Request 4

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															SHCF F
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV								SHCP[7:0]							

Bits	Bit name	RW-P	Initial value	Function description
31:17	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
16	SHCFF	RW-D	0H	<p>Software Hash Calculation Frame Format</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: IPv4 Hash Calculation - 1'b1: IPv6 Hash Calculation <p>Functions:</p> <ul style="list-style-type: none"> - SW: This register is used to accelerate hash calculation.
15:8	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
7:0	SHCP	RW-D	0H	<p>Software Hash Calculation Protocol (NextHeader for IPv6)</p> <p>Functions:</p> <ul style="list-style-type: none"> - SW: This register is used to accelerate hash calculation.

(11) FWSHCR5

Forwarding Engine Software Hash Calculation Request 5

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SHCISP0[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHCISP0[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	SHCISP0	RW-D	0H	<p>Software Hash Calculation IP Source Part 0</p> <p>Functions:</p> <ul style="list-style-type: none"> - SW: This register is used to accelerate hash calculation. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: Should be set to 0 for IPv4 Hash calculation

(12) FWSHCR6

Forwarding Engine Software Hash Calculation Request 6

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SHCISP1[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHCISP1[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	SHCISP1	RW-D	0H	<p>Software Hash Calculation IP Source Part 1</p> <p>Functions:</p> <ul style="list-style-type: none"> - SW: This register is used to accelerate hash calculation. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: Should be set to 0 for IPv4 Hash calculation

(13) FWSHCR7

Forwarding Engine Software Hash Calculation Request 7

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SHCISP2[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHCISP2[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	SHCISP2	RW-D	0H	<p>Software Hash Calculation IP Source Part 2</p> <p>Functions:</p> <ul style="list-style-type: none"> - SW: This register is used to accelerate hash calculation. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: Should be set to 0 for IPv4 Hash calculation

(14) FWSHCR8

Forwarding Engine Software Hash Calculation Request 8

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SHCISP3[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHCISP3[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	SHCISP3	RW-D	0H	<p>Software Hash Calculation IP Source Part 3</p> <p>Functions:</p> <ul style="list-style-type: none"> - SW: This register is used to accelerate hash calculation. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: Should be set to IP source address for IPv4 Hash calculation

(15) FWSHCR9

Forwarding Engine Software Hash Calculation Request 9

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SHCIDP0[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHCIDP0[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	SHCIDP0	RW-D	0H	<p>Software Hash Calculation IP Destination Part 0</p> <p>Functions:</p> <ul style="list-style-type: none"> - SW: This register is used to accelerate hash calculation. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: Should be set to 0 for IPv4 Hash calculation

(16) FWSHCR10

Forwarding Engine Software Hash Calculation Request 10

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SHCIDP1[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHCIDP1[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	SHCIDP1	RW-D	0H	<p>Software Hash Calculation IP Source Destination Part 1</p> <p>Functions:</p> <ul style="list-style-type: none"> - SW: This register is used to accelerate hash calculation. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: Should be set to 0 for IPv4 Hash calculation

(17) FWSHCR11

Forwarding Engine Software Hash Calculation Request 11

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SHCIDP2[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHCIDP2[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	SHCIDP2	RW-D	0H	<p>Software Hash Calculation IP Destination Part 2</p> <p>Functions:</p> <ul style="list-style-type: none"> - SW: This register is used to accelerate hash calculation. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: Should be set to 0 for IPv4 Hash calculation

(18) FWSHCR12

Forwarding Engine Software Hash Calculation Request 12

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SHCIDP3[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHCIDP3[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	SHCIDP3	RW-D	0H	<p>Software Hash Calculation IP Destination Part 3</p> <p>Functions:</p> <ul style="list-style-type: none"> - SW: This register is used to accelerate hash calculation. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: Should be set to IP destination address for IPv4 Hash calculation

(19) FWSHCR13

Forwarding Engine Software Hash Calculation Request 13

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SHCSP[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHCDP[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:16	SHCSP	RW-D	0H	<p>Software Hash Calculation Source Port</p> <p>Functions:</p> <ul style="list-style-type: none"> - SW: This register is used to accelerate hash calculation.
15:0	SHCDP	RW-D	0H	<p>Software Hash Calculation Destination Port</p> <p>Functions:</p> <ul style="list-style-type: none"> - SW: This register is used to accelerate hash calculation.

(20) FWSHCRR

Forwarding Engine Software Hash Calculation Request Result

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SHC															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHCR[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31	SHC	R-D	0H	<p>Software Hash Calculation</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: Writing FWSHCRR13 register will set this bit. <p>Clear conditions:</p> <ul style="list-style-type: none"> - HW: This bit will be de-asserted when hash calculation is completed. <p>Functions:</p> <ul style="list-style-type: none"> - SW: This register is used to accelerate hash calculation.
30:16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
15:0	SHCR	R-D	0H	<p>Software Hash Calculation Result</p> <p>Update conditions:</p> <ul style="list-style-type: none"> - HW: FWSHCRR.SHC clear event. <p>Functions:</p> <ul style="list-style-type: none"> - SW: This register is used to accelerate hash calculation.

3.3.1.6 Layer 3 forwarding/routing/filtering table function registers

(1) FWLTHTEC0

Forwarding Engine L3 Table Entry Configuration 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
RSV																
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
RSV						PFFALA A	PFFALA[PFL_CADF_W-1:0]									

Bits	Bit name	RW-P	Initial value	Function description
31:PFL_CADF_W+1	RSV	R0-U	0H	- Reserved area. On read, 0 will be returned
PFL_CADF_W	PFFALAA	RW-F	0H	<p>Perfect Filter Forwarding Acceptance List Area All</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: No functions. - 1'b1: All areas serve as Acceptance List, ignoring the value of FWLTHTEC0.PFFALA.
PFL_CADF_W-1:0	PFFALA	RW-F	PFL_CADF_N - 1	<p>Perfect Filter Forwarding Acceptance List Area</p> <p>Functions:</p> <ul style="list-style-type: none"> - Value: Perfect filter table = 0x0 ~ this value - Acceptance list filter table = this value+1 ~ PFL_CADF_N-1 <p>Restrictions:</p> <ul style="list-style-type: none"> - Not all (PFL_CADF_N) can be Acceptance list filter table only this register. - All (PFL_CADF_N) can be Perfect filter table (if this value sets to PFL_CADF_N-1). - If FWLTHTEC0.PFFALAA == 1'b1, this register was invalid (this register was treated as -1.).

(2) FWLTHTEC1

Forwarding Engine L3 Table Entry Configuration 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV						LTHTUENC[LTH_STREAM_W-1:0]									

Bits	Bit name	RW-P	Initial value	Function description
31: LTH_STREAM_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
LTH_STREAM_W-1:0	LTHTUENC	RW-F	0H	<p>L3/L2 stream filter Table Unsecure Entry Number Configuration</p> <p>Functions:</p> <ul style="list-style-type: none"> - L3/L2 stream filter table unsecure entry number configuration. <p>Example:</p> <ul style="list-style-type: none"> - FWLTHEC1.LTHTUENC = 0: L3/L2 stream filter table all secure entry but none unsecure entry. - FWLTHEC1.LTHTUENC = 0x8: L3/L2 stream filter table able from 0 to 7 are unsecure entry and 8 ~ LTH_STREAM_N-1 are secure entry. - All entry cannot be unsecure.

(3) FWLTHTL0

Forwarding Engine L3 Table Learn 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV						LTHELA[LTH_STREAM_W-1:0]									

Bits	Bit name	RW-P	Initial value	Function description
31: LTH_STREAM_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
LTH_STREAM_W-1:0	LTHELA	RW-D	0H	<p>L3 Entry Learn Address</p> <ul style="list-style-type: none"> - The learning address (entry number) of L3 table. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: This is invalid if FWLTHTL1.LTHSLP0[0] == 1'b1 (Perfect filter was selected). - SW: Prohibits access outside of permitted areas by unsecure. Therefore, please register for Secure before registering for Unsecure.

(4) FWLTHTL1

Forwarding Engine L3 Table Learn 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHED	RSV								LTHFPL[3:0]			LTHRPL[3:0]			
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV		LTHBLL	RSV	LTHHLDL	RSV		LTHSLP0[7:0]								

Bits	Bit name	RW-P	Initial value	Function description
31	LTHED	RW-D	0B	<p>L3 Entry Delete</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Learn the set Layer 3 forwarding/routing/filtering entry in L3 table. - 1'b1: Delete the set Layer 3 forwarding/routing/filtering entry in L3 table.
30:24	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
23	LTHFPL[3]	RW-F	0B	<p>L3 Filtering Priority Learn (MSB)</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in L3 table.
22:20	LTHFPL[2:0]	RW-D	0B	<p>L3 Filtering Priority Learn</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in L3 table.
19	LTHRPL[3]	RW-F	0B	<p>L3 Routing Priority Learn (MSB)</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in L3 table.
18:16	LTHRPL[2:0]	RW-D	0B	<p>L3 Routing Priority Learn</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in L3 table.
15:3	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
12	LTHBLL	RW-D	0B	<p>L3 Block List Learn</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in L3 table.
11	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
10	LTHHLDL	RW-D	0B	<p>L3 (Source MAC) Hardware Learning Disable Learn</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in L3 table.
9:8	RSV	R0-U	0H	Reserved area. On read, 0 will be returned

7:0	LTHSLP0	RW-D	0B	<p>L3 table Stream Learn Part 0</p> <p>Functions:</p> <ul style="list-style-type: none">- Used for learning/overwriting an entry in L3 table.- L3 table ID correspond to {FWLTHTL1. LTHSLP0, FWLTHTL2. LTHSLP1, FWLTHTL3. LTHSLP2, FWLTHTL4. LTHSLP3, FWLTHTL5. LTHSLP4}. <p>Values:</p> <ul style="list-style-type: none">- [0]: Perfect table selected.- [1]: L3/L2 stream table selected and L3 stream (IPv4 Other) filter.- [2]: L3/L2 stream table selected and L3 stream (IPv4 TCP) filter.- [3]: L3/L2 stream table selected and L3 stream (IPv4 UDP) filter.- [4]: L3/L2 stream table selected and L3 stream (IPv6 Other) filter.- [5]: L3/L2 stream table selected and L3 stream (IPv6 TCP) filter.- [6]: L3/L2 stream table selected and L3 stream (IPv6 UDP) filter.- [7]: L3/L2 stream table selected and L2 stream filter. <p>Restrictions:</p> <ul style="list-style-type: none">- SW: To be set only one bit for [7:0]. (0x01, 0x02, 0x04, 0x08, 0x10 ,0x20, 0x40 or 0x80)
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(5) FWLTHTL2

Forwarding Engine L3 Table Learn 2

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHSLP1[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHSLP1[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	LTHSLP1	RW-D	0B	<p>L3 table Stream Learn Part 1</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in L3 table. - L3 table ID correspond to {FWLTHTL1.LTHSLP0, FWLTHTL2.LTHSLP1, FWLTHTL3.LTHSLP2, FWLTHTL4.LTHSLP3, FWLTHTL5.LTHSLP4}. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: {FWLTHTL2.LTHSLP1, FWLTHTL3.LTHSLP2, FWLTHTL4.LTHSLP3, FWLTHTL5.LTHSLP4} have to less than PFL_CADF_N, if FWLTHTL1.LTHSLP0[0] == 1'b1 (Perfect filter was selected). - SW: Set 0 to the masked bit for L3/L2 stream table(FWLTHTL1.LTHSLP0[0] != 1'b1).

(6) FWLTHTL3

Forwarding Engine L3 Table Learn 3

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHSLP2[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHSLP2[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	LTHSLP2	RW-D	0B	<p>L3 table Stream Learn Part 2</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in L3 table. - L3 table ID correspond to {FWLTHTL1.LTHSLP0, FWLTHTL2.LTHSLP1, FWLTHTL3.LTHSLP2, FWLTHTL4.LTHSLP3, FWLTHTL5.LTHSLP4}. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: {FWLTHTL2.LTHSLP1, FWLTHTL3.LTHSLP2, FWLTHTL4.LTHSLP3, FWLTHTL5.LTHSLP4} have to less than PFL_CADF_N, if FWLTHTL1.LTHSLP0[0] == 1'b1 (Perfect filter was selected). - SW: Set 0 to the masked bit for L3/L2 stream table(FWLTHTL1.LTHSLP0[0] != 1'b1).

(7) FWLHTL4

Forwarding Engine L3 Table Learn 4

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHSLP3[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHSLP3[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	LTHSLP3	RW-D	0B	<p>L3 table Stream Learn Part 3</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in L3 table. - L3 table ID correspond to {FWLTHTL1.LTHSLP0, FWLTHTL2.LTHSLP1, FWLTHTL3.LTHSLP2, FWLTHTL4.LTHSLP3, FWLTHTL5.LTHSLP4}. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: {FWLTHTL2.LTHSLP1, FWLTHTL3.LTHSLP2, FWLTHTL4.LTHSLP3, FWLTHTL5.LTHSLP4} have to less than PFL_CADF_N, if FWLTHTL1.LTHSLP0[0] == 1'b1 (Perfect filter was selected). - SW: Set 0 to the masked bit for L3/L2 stream table(FWLHTL1.LTHSLP0[0] != 1'b1).

(8) FWLTHTL5

Forwarding Engine L3 Table Learn 5

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHSLP4[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHSLP4[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	LTHSLP4	RW-D	0B	<p>L3 table Stream Learn Part 4</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in L3 table. - L3 table ID correspond to {FWLTHTL1.LTHSLP0, FWLTHTL2.LTHSLP1, FWLTHTL3.LTHSLP2, FWLTHTL4.LTHSLP3, FWLTHTL5.LTHSLP4}. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: {FWLTHTL2.LTHSLP1, FWLTHTL3.LTHSLP2, FWLTHTL4.LTHSLP3, FWLTHTL5.LTHSLP4} have to less than PFL_CADF_N, if FWLTHTL1.LTHSLP0[0] == 1'b1 (Perfect filter was selected). - SW: Set 0 to the masked bit for L3/L2 stream table(FWLTHTL1.LTHSLP0[0] != 1'b1).

(9) FWLTHTL6

Forwarding Engine L3 Table Learn 6

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHSMLP0[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHSMLP0[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	LTHSMLP0	RW-D	0B	<p>L3 table Stream Mask Learn Part 0</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in L3 table. - L3 table ID mask correspond to {FWLTHTL6.LTHSMLP0, FWLTHTL7.LTHSMLP1, FWLTHTL8.LTHSMLP2, FWLTHTL9.LTHSMLP3}. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: Set all 0 if FWLTHTL1.LTHSMLP0[0] == 1'b1 (Perfect filter was selected).

(10) FWLTHTL7

Forwarding Engine L3 Table Learn 7

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHSMLP1[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHSMLP1[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	LTHSMLP1	RW-D	0B	<p>L3 table Stream Mask Learn Part 1</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in L3 table. - L3 table ID mask correspond to {FWLTHTL6.LTHSMLP0, FWLTHTL7.LTHSMLP1, FWLTHTL8.LTHSMLP2, FWLTHTL9.LTHSMLP3}. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: Set all 0 if FWLTHTL1.LTHSLP0[0] == 1'b1 (Perfect filter was selected).

(11) FWLTHTL8

Forwarding Engine L3 Table Learn 8

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHSMLP2[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHSMLP2[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	LTHSMLP2	RW-D	0B	<p>L3 table Stream Mask Learn Part 2</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in L3 table. - L3 table ID mask correspond to {FWLTHTL6.LTHSMLP0, FWLTHTL7.LTHSMLP1, FWLTHTL8.LTHSMLP2, FWLTHTL9.LTHSMLP3}. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: Set all 0 if FWLTHTL1.LTHSLP0[0] == 1'b1 (Perfect filter was selected).

(12) FWLTHTL9

Forwarding Engine L3 Table Learn 9

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHSMLP3[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHSMLP3[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	LTHSMLP3	RW-D	0B	<p>L3 table Stream Mask Learn Part 3</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in L3 table. - L3 table ID mask correspond to {FWLTHTL6.LTHSMLP0, FWLTHTL7.LTHSMLP1, FWLTHTL8.LTHSMLP2, FWLTHTL9.LTHSMLP3}. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: Set all 0 if FWLTHTL1.LTHSLP0[0] == 1'b1 (Perfect filter was selected).

(13) FWLTHTL10

Forwarding Engine L3 Table Learn 10

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHMSD UVL	RSV												LTHMSDUNL [PSFP_MSDU_W-1:0]		
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHGA TEVL	RSV												LTHGATENL [PSFP_GATE_W-1:0]		

Bits	Bit name	RW-P	Initial value	Function description
31	LTHMSDUVL	RW-D	0B	L3 MSDU Valid Learn Functions: - Used for learning/overwriting an entry in L3 table.
30: PSFP_MSDU_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PSFP_MSDU_W+15:16	LTHMSDUNL	RW-D	0B	L3 MSDU Number Learn Functions: - SW: Used for learning/overwriting an entry in L3 table.
15	LTHGATEVL	RW-D	0B	L3 GATE Valid Learn Functions: - Used for learning/overwriting an entry in L3 table.
14: PSFP_GATE_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PSFP_GATE_W-1:0	LTHGATENL	RW-D	0B	L3 GATE Number Learn Functions: - Used for learning/overwriting an entry in L3 table.

(14) FWLTHTL11

Forwarding Engine L3 Table Learn 11

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHM TRVL	RSV									LTHMTRNL[PSFP_MTR_W-1:0]					
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHFR ERVL	RSV									LTHFRERNL[FRER_RECE_W-1:0]					

Bits	Bit name	RW-P	Initial value	Function description
31	LTHMTRVL	RW-D	0B	L3 MeTeR Valid Learn Functions: - Used for learning/overwriting an entry in L3 table.
30: PSFP_MTR_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PSFP_MTR_W+15:16	LTHMTRNL	RW-D	0B	L3 MeTeR Number Learn Functions: - Used for learning/overwriting an entry in L3 table.
15	LTHFRERVL	RW-D	0B	L3 FRER Valid Learn Functions: - Used for learning/overwriting an entry in L3 table.
14: FRER_RECE_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
FRER_RECE_W-1:0	LTHFRERNL	RW-D	0B	L3 FRER Number Learn Functions: - Used for learning/overwriting an entry in L3 table.

(15) FWLTHTL12

Forwarding Engine L3 Table Learn 12

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV / LTHSLVL[PORT_N-1:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHR VL	RSV				LTHRNL[LTH_RRULE_W-1:0]										

Bits	Bit name	RW-P	Initial value	Function description
31: PORT_N+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PORT_N+15:16	LTHSLVL	RW-D	0H	<p>L3 Source Lock Vector Learn</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in L3 table.
15	LTHRVL	RW-D	0B	<p>L3 Routing Valid Learn</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in L3 table.
14: LTH_RRULE_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
LTH_RRULE_W-1:0	LTHRNL	RW-D	0B	<p>L3 Routing Number Learn</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in L3 table.

(16) FWLTHTL13i (i=0..PORT_GWCA_N-1)

Forwarding Engine L3 Table Learn 13 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / LTHCSDLi[AXI_CHAIN_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: AXI_CHAIN_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
AXI_CHAIN_W-1:0	LTHCSDLi	RW-D	0B	L3 CPU Sub-Destination Learn i Functions: - Used for learning/overwriting an entry in L3 table.

(17) FWLTHTL14

Forwarding Engine L3 Table Learn 14

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV										LTHC MEL	LTHE MEL	LTHIP UL	LTHIPVL[2:0]		
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / LTHDVL[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
21	LTHCMEL	RW-D	0B	<p>L3 CPU Mirroring Enable Learn</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in L3 table.
20	LTHEMEL	RW-D	0B	<p>L3 Ethernet Mirroring Enable Learn</p> <p>Functions:</p> <ul style="list-style-type: none"> - SW: Used for learning/overwriting an entry in L3 table.
19	LTHIPUL	RW-D	0B	<p>L3 Internal Priority Update Learn</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in L3 table.
18:16	LTHIPVL	RW-D	0B	<p>L3 Internal Priority Value Learn</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in L3 table.
15:PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PORT_N-1:0	LTHDVL	RW-D	0B	<p>L3 Destination Vector Learn</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in L3 table.

(18) FWLTHTL15

Forwarding Engine L3 Table Learn 15

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / LTHDLVL[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PORT_N-1:0	LTHDLVL	RW-D	0B	L3 Destination Lock Vector Learn Functions: - Used for learning/overwriting an entry in L3 table.

(19) FWLHTHLR

Forwarding Engine L3 Table Learn Result

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHTL	RSV														
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV															LTHLF
F															LTHLF

Bits	Bit name	RW-P	Initial value	Function description
31	LTHTL	R-D	0B	<p>L3 Table Learn</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: Writing FWLHTHLR.LTHTL register will set this bit. <p>Clear conditions:</p> <ul style="list-style-type: none"> - HW: This bit will be de-asserted when learning is completed. <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in L3 table.
30:5	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
3	LTHLOF	R-D	0B	<p>L3 Learn Overwrite Fail</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: [Perfect filter] The entry learning didn't overwrite. [L3/L2 stream filter] The entry learning didn't fail. - 1'b1: [Perfect filter] The entry learning overwrite because of an existing entry. [L3/L2 stream filter] The entry learning failed because of an existing entry. <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLHTHLR.LTHTL clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in L3 table. <p>Notes:</p> <ul style="list-style-type: none"> - For FWLHTHLR.LTHSLP0[0] == 1'b0 (L3/L2 stream filter was selected) and if you want to update/overwrite this entry, please delete the entry before entry learn.
2	LTHLEF	R-D	0B	<p>L3 Learn ECC Fail</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Entry learning didn't fail because of an ECC error. - 1'b1: Entry learning failed because of an ECC error. <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLHTHLR.LTHTL clear event. <p>Functions:</p> <ul style="list-style-type: none"> - if FWLHTHLR.LTHSLP0[0] == 1'b1 (Perfect filter was selected), this is valid. - if FWLHTHLR.LTHSLP0[0] == 1'b0 (L3/L2 stream filter was selected), this is invalid (L3 Learn ECC Fail will no be occur). - Used for learning/overwriting an entry in L3 table. (not deleting)

1	LTHLSF	R-D	0B	<p>L3 Learn Security Fail</p> <p>Values:</p> <ul style="list-style-type: none">- 1'b0: Entry learning didn't fail because of a security error (refer to section 5.2.5.4(2)).- 1'b1: Entry learning failed because of a security error (refer to section 5.2.5.4(2)). <p>Update Conditions:</p> <ul style="list-style-type: none">- HW: FWLTHTLR.LTHTL clear event. <p>Functions:</p> <ul style="list-style-type: none">- Used for learning/overwriting an entry in L3 table.
0	LTHLF	R-D	0B	<p>L3 Learn Fail</p> <p>Values:</p> <ul style="list-style-type: none">- 1'b0: Entry learning didn't fail (refer to section 5.2.5.4(2))- 1'b1: Entry learning failed (refer to section 5.2.5.4(2)) <p>Update Conditions:</p> <ul style="list-style-type: none">- HW: FWLTHTLR.LTHTL clear event. <p>Functions:</p> <ul style="list-style-type: none">- Used for learning/overwriting an entry in L3 table.

(20) FWLHTIM

Forwarding Engine L3 Table Initialization Monitoring.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
														LTHTR	LTHTIO G

Bits	Bit name	RW-P	Initial value	Function description
31:2	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
1	LTHTR	R-RP	0H	<p>L3 Table Ready</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When FWLHTIM.LTHTIOG is getting cleared. - HW: This bit is set at "clk_period[ns]*RACE_LTH_STREAM_N" time from L3 table initialization starting. <p>Clear condition:</p> <ul style="list-style-type: none"> - SW: By writing 1 to FWLHTIM.LTHTIOG.
0	LTHTIOG	R!=W-RP	0B	<p>L3 Table Initialization Ongoing.</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - SW: By writing 1 to this register. It starts L3 Table initialization. <p>Clear condition:</p> <ul style="list-style-type: none"> - HW: This bit is cleared when L3 Table initialization is finished.

(21) FWLTHTEM0

Forwarding Engine L3 Table Entry Monitoring 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV						LTHTUPEN[PFL_CADF_W:0]									
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV						LTHTPEN[PFL_CADF_W:0]									

Bits	Bit name	RW-P	Initial value	Function description
31: PFL_TFIL_W+17	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PFL_CADF_W+16:16	LTHTUPEN	R-P	0B	<p>L3 Table Unsecure Perfect Entry Number.</p> <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: An unsecure entry is learned successfully. <p>Decrement conditions:</p> <ul style="list-style-type: none"> - HW: An unsecure entry is deleted successfully.
15: PFL_TFIL_W+1	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PFL_CADF_W:0	LTHTPEN	R-P	0B	<p>L3 Table Perfect Entry Number.</p> <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: An entry is learned successfully. <p>Decrement conditions:</p> <ul style="list-style-type: none"> - HW: An entry is deleted successfully.

(22) FWLTHTEM1

Forwarding Engine L3 Table Entry Monitoring 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV					LTHTUEN[LTH_STREAM_W:0]										
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV					LTHTEN[LTH_STREAM_W:0]										

Bits	Bit name	RW-P	Initial value	Function description
31: LTH_STREAM_W+17	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
LTH_STREAM_W+16:16	LTHTUEN	R-P	0B	<p>L3 Table Unsecure L3/L2 stream Entry Number.</p> <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: An unsecure entry is learned successfully. <p>Decrement conditions:</p> <ul style="list-style-type: none"> - HW: An unsecure entry is deleted successfully.
15:LTH_STREAM_W+1	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
LTH_STREAM_W:0	LTHTEN	R-P	0B	<p>L3 Table L3/L2 stream Entry Number.</p> <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: An entry is learned successfully. <p>Decrement conditions:</p> <ul style="list-style-type: none"> - HW: An entry is deleted successfully.

(23) FWLTHTS0

Forwarding Engine L3 Table Search 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV								LTHSSP0[7:0]							

Bits	Bit name	RW-P	Initial value	Function description
31:8	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
7:0	LTHSSP0	RW-D	0B	<p>L3 table Stream Search Part 0</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table. <p>Values:</p> <ul style="list-style-type: none"> - [0]: Invalid. (Should set to be 1'b0) Perfect table selected. - [1]: L3/L2 stream table selected and L3 stream (IPv4 Other) filter. - [2]: L3/L2 stream table selected and L3 stream (IPv4 TCP) filter. - [3]: L3/L2 stream table selected and L3 stream (IPv4 UDP) filter. - [4]: L3/L2 stream table selected and L3 stream (IPv6 Other) filter. - [5]: L3/L2 stream table selected and L3 stream (IPv6 TCP) filter. - [6]: L3/L2 stream table selected and L3 stream (IPv6 UDP) filter. - [7]: L3/L2 stream table selected and L2 stream filter. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: Not set [0] to 1'b1. If set [0] to 1'b1, search function will be failed and set FWLTHTSR0.LTHSNF to 1'b1. - SW: If set any [3:1] to 1'b1, set [0] and [7:4] to All 0. - SW: If set any [6:4] to 1'b1, set [3:0] and [7] to All 0 - SW: If set [7] to 1'b1, set [6:0] to All 0.

(24) FWLTHTS1

Forwarding Engine L3 Table Search 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHSSP1[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHSSP1[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	LTHSSP1	RW-D	0B	L3 table Stream Search Part 1 Functions: - Used for searching an entry in L3 table.

(25) FWLTHTS2

Forwarding Engine L3 Table Search 2

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHSSP2[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHSSP2[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	LTHSSP2	RW-D	0B	<p>L3 table Stream Search Part 2</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table.

(26) FWLTHTS3

Forwarding Engine L3 Table Search 3

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHSSP3[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHSSP3[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	LTHSSP3	RW-D	0B	<p>L3 table Stream Search Part 3</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table.

(27) FWLTHTS4

Forwarding Engine L3 Table Search 4

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHSSP4[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHSSP4[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	LTHSSP4	RW-D	0B	L3 table Stream Search Part 4 Functions: - Used for searching an entry in L3 table.

(28) FWLHTTS5

Forwarding Engine L3 Table Search 5

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV						LTHTSEA[LTH_STREAM_W-1:0]									
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV						LTHTSSA[LTH_STREAM_W-1:0]									

Bits	Bit name	RW-P	Initial value	Function description
31:LTH_STREAM_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
LTH_STREAM_W+15:16	LTHTSEA	RW-D	0B	<p>L3 Table Search End Address for invalid search</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table for invalid search. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: This register is only valid if FWLHTTS6.LTHTIVLS == 1'b1. - SW: This register should be set to bigger than or equal to FWLHTTS5.LTHTSSA.
15:LTH_STREAM_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
LTH_STREAM_W-1:0	LTHTSSA	RW-D	0B	<p>L3 Table Search Start Address for invalid search</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table for invalid search. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: This register is only valid if FWLHTTS6.LTHTIVLS == 1'b1. - SW: This register should be set to smaller than or equal to FWLHTTS5.LTHTSEA. - HW: Search will not be found if the Start-End constraint is violated. - HW: From unsecure APB, search only for unsecure area. (If unsecure APB access and (FWLHTTS5.LTHTSEA > FWLTHEC1.LTHTUENC-1), FWLHTTS5.LTHTSEA will be forced to FWLTHEC1.LTHTUENC-1.)

(29) FWLTHTS6

Forwarding Engine L3 Table Search 6

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV															

LTHTI
VLS

Bits	Bit name	RW-P	Initial value	Function description
31:1	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
0	LTHTIVLS	RW-D	0B	<p>L3 Table InVaLid Search</p> <p>Functions:</p> <ul style="list-style-type: none"> - 1'b0 : Used for searching an entry in L3 table for L3 stream. - 1'b1 : Used for searching an entry in L3 table for invalid entry. And invalid search done. In invalid search case, FWLTHTSR* will be cleared other than FWLTHTSR0.LTHSNF and FWLTHTSR7.LTHMCHAS.

(30) FWLHTTSR0

Forwarding Engine L3 Table Search Result 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LHTS	RSV								LTHFPS[3:0]				LTHRPS[3:0]		
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV			LTHBLS	RSV	LTHHL DS	RSV	LTHSL S	RSV							

Bits	Bit name	RW-P	Initial value	Function description
31	LHTS	R-D	0B	<p>L3 Table Search</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: Writing FWLHTTS6 register will set this bit. <p>Clear conditions:</p> <ul style="list-style-type: none"> - HW: This bit will be de-asserted when searching is completed. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table. - If FWLHTTS6.LTHTIVLS is 1, this value will not be setting.
30:24	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
23	LTHFPS[3]	R-F	0B	<p>L3 Filtering Priority Search (MSB)</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLHTTSR0.LHTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table. - If FWLHTTS6.LTHTIVLS is 1, this value is invalid (All 0).
22:20	LTHFPS[2:0]	R-D	0B	<p>L3 Filtering Priority Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLHTTSR0.LHTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table. - If FWLHTTS6.LTHTIVLS is 1, this value is invalid (All 0).
19	LTHRPS[3]	R-F	0B	<p>L3 Routing Priority Search (MSB)</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLHTTSR0.LHTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table. - If FWLHTTS6.LTHTIVLS is 1, this value is invalid (All 0).
18:16	LTHRPS[2:0]	R-D	0B	<p>L3 Routing Priority Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLHTTSR0.LHTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table. - If FWLHTTS6.LTHTIVLS is 1, this value is invalid (All 0).
15:13	RSV	R0-U	0H	Reserved area. On read, 0 will be returned

12	LTHBLS	R-D	0B	<p>L3 Block List Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTSR0.LTHTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table. - If FWLTHTS6.LTHTIVLS is 1, this value is invalid (All 0).
11	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
10	LTHHLDs	R-D	0B	<p>L3 (Source MAC) Hardware Learning Disable Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTSR0.LTHTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table. - If FWLTHTS6.LTHTIVLS is 1, this value is invalid (All 0).
9	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
8	LTHSLS	R-F	0B	<p>L3 Security Level Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTSR0.LTHTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table. - If FWLTHTS6.LTHTIVLS is 1, this value is invalid (All 0).
7:2	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
1	LTHSNF	R-D	0B	<p>L3 Search Not found</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Stream ID found in L3 Table. - 1'b1: Stream ID not found in L3 Table. <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTSR0.LTHTS clear event (or invalid search done). <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table. - The unsecure APB interface cannot find an entry with security level bit set in the L3 table.
0	LTHSEF	R-D	0B	<p>L3 Search ECC Fail</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Entry Search didn't fail because of an ECC error. - 1'b1: Entry Search failed because of an ECC error. <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTSR0.LTHTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table. - If FWLTHTS6.LTHTIVLS is 1, this value is invalid (All 0).

(31) FWLTHTSR1

Forwarding Engine L3 Table Search Result 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHMSD UVS	RSV												LTHMSDUNS [PSFP_MSDU_W-1:0]		
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHGAT EVS	RSV												LTHGATENS [PSFP_GATE_W-1:0]		

Bits	Bit name	RW-P	Initial value	Function description
31	LTHMSDUVS	R-D	0B	<p>L3 MSDU Valid Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTSR0.LTHTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table. - If FWLTHTS6.LTHTIVLS is 1, this value is invalid (All 0).
30: PSFP_MSDU_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PSFP_MSDU_W+15:16	LTHMSDUNS	R-D	0B	<p>L3 MSDU Number Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTSR0.LTHTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table. - If FWLTHTS6.LTHTIVLS is 1, this value is invalid (All 0).
15	LTHGATEVS	R-D	0B	<p>L3 GATE Valid Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTSR0.LTHTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table. - If FWLTHTS6.LTHTIVLS is 1, this value is invalid (All 0).
14: PSFP_GATE_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PSFP_GATE_W-1:0	LTHGATENS	R-D	0B	<p>L3 GATE Number Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTSR0.LTHTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table. - If FWLTHTS6.LTHTIVLS is 1, this value is invalid (All 0).

(32) FWLTHTSR2

Forwarding Engine L3 Table Search Result 2

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHM TRVS	RSV									LTHMTRNS[PSFP_MTR_W-1:0]					
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHFR ERVS	RSV									LTHFRERNS[FRER_RECE_W-1:0]					

Bits	Bit name	RW-P	Initial value	Function description
31	LTHMTRVS	R-D	0B	L3 MeTeR Valid Search Update Conditions: - HW: FWLTHTSR0.LTHTS clear event. Functions: - Used for searching an entry in L3 table. - If FWLTHTS6.LTHTIVLS is 1, this value is invalid (All 0).
30: PSFP_MTR_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PSFP_MTR_W+15:16	LTHMTRNS	R-D	0B	L3 MeTeR Number Search Update Conditions: - HW: FWLTHTSR0.LTHTS clear event. Functions: - Used for searching an entry in L3 table. - If FWLTHTS6.LTHTIVLS is 1, this value is invalid (All 0).
15	LTHFRERVS	R-D	0B	L3 FRER Valid Search Update Conditions: - HW: FWLTHTSR0.LTHTS clear event. Functions: - Used for searching an entry in L3 table. - If FWLTHTS6.LTHTIVLS is 1, this value is invalid (All 0).
14: FRER_RECE_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
FRER_RECE_W-1:0	LTHFRERNS	R-D	0B	L3 FRER Number Search Update Conditions: - HW: FWLTHTSR0.LTHTS clear event. Functions: - Used for searching an entry in L3 table. - If FWLTHTS6.LTHTIVLS is 1, this value is invalid (All 0).

(33) FWLTHTSR3

Forwarding Engine L3 Table Search Result 3

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV / LTHSLVS[PORT_N-1:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHR VS	RSV					LTHRNS[LTH_RRULE_W-1:0]									

Bits	Bit name	RW-P	Initial value	Function description
31: PORT_N+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PORT_N+15:16	LTHSLVS	R-D	0H	<p>L3 Source Lock Vector Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTSR0.LTHTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table. - If FWLTHTS6.LTHTIVLS is 1, this value is invalid (All 0).
15	LTHRVS	R-D	0B	<p>L3 Routing Valid Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTSR0.LTHTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table. - If FWLTHTS6.LTHTIVLS is 1, this value is invalid (All 0).
14: LTH_RRULE_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
LTH_RRULE_W-1:0	LTHRNS	R-D	0B	<p>L3 Routing Number Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTSR0.LTHTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table. - If FWLTHTS6.LTHTIVLS is 1, this value is invalid (All 0).

(34) FWLTHTSR4i (i=0..PORT_GWCA_N-1)

Forwarding Engine L3 Table Search Result 4 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / LTHCSDSi[AXI_CHAIN_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: AXI_CHAIN_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
AXI_CHAIN_W-1:0	LTHCSDSi	R-D	0B	<p>L3 CPU Sub-Destination Search i</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTSR0.LTHTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table. - If FWLTHTS6.LTHTIVLS is 1, this value is invalid (All 0).

(35) FWLTHTSR5

Forwarding Engine L3 Table Search Result 5

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV										LTHC MES	LTHE MES	LTHIP US	LTHIPVS[2:0]		
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / LTHDVS[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
21	LTHCMES	R-D	0B	<p>L3 CPU Mirroring Enable Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTSR0.LTHTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table. - If FWLTHTS6.LTHTIVLS is 1, this value is invalid (All 0).
20	LTHEMES	R-D	0B	<p>L3 Ethernet Mirroring Enable Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTSR0.LTHTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table. - If FWLTHTS6.LTHTIVLS is 1, this value is invalid (All 0).
19	LTHIPUS	R-D	0B	<p>L3 Internal Priority Update Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTSR0.LTHTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table. - If FWLTHTS6.LTHTIVLS is 1, this value is invalid (All 0).
18:16	LTHIPVS	R-D	0B	<p>L3 Internal Priority Value Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTSR0.LTHTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table. - If FWLTHTS6.LTHTIVLS is 1, this value is invalid (All 0).
15:PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PORT_N-1:0	LTHDVS	R-D	0B	<p>L3 Destination Vector Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTSR0.LTHTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table. - If FWLTHTS6.LTHTIVLS is 1, this value is invalid (All 0).

(36) FWLTHTSR6

Forwarding Engine L3 Table Search Result 6

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV															

Bits	Bit name	RW-P	Initial value	Function description
31:PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PORT_N-1:0	RSV	R0-U	0B	Reserved area. On read, 0 will be returned

(37) FWLTHTSR7

Forwarding Engine L3 Table Search Result 7

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV						LTHMCHAS[LTH_STREAM_W-1:0]									

Bits	Bit name	RW-P	Initial value	Function description
31:LTH_STREAM_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
LTH_STREAM_W-1:0	LTHMCHAS	R-D	0B	<p>L3 entry MatCH Address Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTSR0.LTHTS clear event (or invalid search done). <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in L3 table. - If FWLTHTS6.LTHTIVLS is 1'b0, L3 table match address. - If FWLTHTS6.LTHTIVLS is 1'b1, L3 table invalid address.

(38) FWLTHTR

Forwarding Engine L3 Table Read

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															LTHSR S
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV															LTHAR[LTH_STREAM_W -1:0]

Bits	Bit name	RW-P	Initial value	Function description
31:16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
16	LTHSRS	RW-D	0B	<p>L3 Table Read Select</p> <p>Functions:</p> <ul style="list-style-type: none"> - 1'b0: Perfect table read - 1'b1: L3/L2 stream table read
15:LTH_STREAM_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
LTH_STREAM_W-1:0	LTHAR	RW-D	0B	<p>L3 Address Read</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table. <p>Restrictions:</p> <ul style="list-style-type: none"> - If FWLTHTR.LTHSRS is 1'b0, this register should be set to smaller than PFL_CADF_N.

(39) FWLTHTRR0

Forwarding Engine L3 Table Read Result 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHTR	RSV														
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RSV														
	LTHEV R														
	LTHR EF														

Bits	Bit name	RW-P	Initial value	Function description
31	LTHTR	R-D	0B	<p>L3 Table Read</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: Writing FWLTHTR register will set this bit. <p>Clear conditions:</p> <ul style="list-style-type: none"> - HW: This bit will be de-asserted when reading is completed. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table.
30:2	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
1	LTHEVR	R-D	0B	<p>L3 Entry Valid Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table. - The unsecure APB interface cannot read an entry with security level bit set in the L3 table. - If the Invalid area is read, please ignore the information that follows because past rule information remains.
0	LTHREF	R-D	0B	<p>L3 Read ECC Fail</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Entry Read didn't fail because of an ECC error. - 1'b1: Entry Read failed because of an ECC error. <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table.

(40) FWLTHTRR1

Forwarding Engine L3 Table Read Result 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV								LTHFPR[3:0]				LTHRPR[3:0]			
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV			LTHBLR	RSV	LTHHL DR	RSV	LTHSL R	LTHSRP0[7:0]							

Bits	Bit name	RW-P	Initial value	Function description
31:24	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
23	LTHFPR[3]	R-D	0B	<p>L3 Filtering Priority Read (MSB)</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTHR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table.
22:20	LTHFPR[2:0]	R-D	0H	<p>L3 Filtering Priority Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTHR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table.
19	LTHRPR[3]	R-D	0B	<p>L3 Routing Priority Read (MSB)</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTHR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table.
18:16	LTHRPR[2:0]	R-D	0H	<p>L3 Routing Priority Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTHR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table.
15:13	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
12	LTHBLR	R-D	0B	<p>L3 Block List Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTHR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table.
11	RSV	R0-U	0H	<ul style="list-style-type: none"> - Reserved area. On read, 0 will be returned
10	LTHHLDR	R-D	0B	<p>L3 (Source MAC) Hardware Learning Disable Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTHR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table.
9	RSV	R0-U	0H	Reserved area. On read, 0 will be returned

8	LTHSLR	R-F	0B	<p>L3 Security Level Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none">- HW: FWLTHTRR0.LTHTR clear event. <p>Functions:</p> <ul style="list-style-type: none">- Used for reading an entry in L3 table.
7:0	LTHSRP0	R-D	0B	<p>L3 Stream Read Part 0</p> <p>Update Conditions:</p> <ul style="list-style-type: none">- HW: FWLTHTRR0.LTHTR clear event. <p>Functions:</p> <ul style="list-style-type: none">- Used for reading an entry in L3 table.- If FWLTHTR.LTHSRS is 1'b0, this value is invalid (All 0).

(41) FWLTHTRR2

Forwarding Engine L3 Table Read Result 2

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHSRP1[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHSRP1[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	LTHSRP1	R-D	0B	<p>L3 table Stream Read Part 1</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: 0 will be read as the masked bit for L3/L2 stream table. - If FWLTHTR.LTHSRS is 1'b0, this value is invalid (All 0).

(42) FWLTHTRR3

Forwarding Engine L3 Table Read Result 3

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHSRP2[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHSRP2[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	LTHSRP2	R-D	0B	<p>L3 table Stream Read Part 2</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: 0 will be read as the masked bit for L3/L2 stream table. - If FWLTHTR.LTHSRS is 1'b0, this value is invalid (All 0).

(43) FWLTHTRR4

Forwarding Engine L3 Table Read Result 4

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHSRP3[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHSRP3[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	LTHSRP3	R-D	0B	<p>L3 table Stream Read Part 3</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: 0 will be read as the masked bit for L3/L2 stream table. - If FWLTHTR.LTHSRS is 1'b0, this value is invalid (All 0).

(44) FWLTHTRR5

Forwarding Engine L3 Table Read Result 5

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHSRP4[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHSRP4[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	LTHSRP4	R-D	0B	<p>L3 table Stream Read Part 4</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: 0 will be read as the masked bit for L3/L2 stream table. - If FWLTHTR.LTHSRS is 1'b0, this value is invalid (All 0).

(45) FWLTHTRR6

Forwarding Engine L3 Table Read Result 6

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHSMRP0[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHSMRP0[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	LTHSMRP0	R-D	0B	<p>L3 Stream Mask Read Part 0</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTHR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table. - If FWLTHTR.LTHSRS is 1'b0, this value is invalid (All 0).

(46) FWLTHTRR7

Forwarding Engine L3 Table Read Result 7

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHSMRP1[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHSMRP1[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	LTHSMRP1	R-D	0B	<p>L3 table Stream Mask Read Part 1</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table. - If FWLTHTR.LTHSRS is 1'b0, this value is invalid (All 0).

(47) FWLTHTRR8

Forwarding Engine L3 Table Read Result 8

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHSMRP2[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHSMRP2[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	LTHSMRP2	R-D	0B	<p>L3 table Stream Mask Read Part 2</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table. - If FWLTHTR.LTHSRS is 1'b0, this value is invalid (All 0).

(48) FWLTHTRR9

Forwarding Engine L3 Table Read Result 9

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHSMRP3[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHSMRP3[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	LTHSMRP3	R-D	0B	<p>L3 table Stream Mask Read Part 3</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table. - If FWLTHTR.LTHSRS is 1'b0, this value is invalid (All 0).

(49) FWLTHTRR10

Forwarding Engine L3 Table Read Result 10

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHMSD UVR	RSV												LTHMSDUNR [PSFP_MSDU_W-1:0]		
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHGAT EVR	RSV												LTHGATENR [PSFP_GATE_W-1:0]		

Bits	Bit name	RW-P	Initial value	Function description
31	LTHMSDUVR	R-D	0B	L3 MSDU Valid Read Update Conditions: - HW: FWLTHTRR0.LTHTHR clear event. Functions: - Used for reading an entry in L3 table.
30: PSFP_MSDU_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PSFP_MSDU_W+15:16	LTHMSDUNR	R-D	0B	L3 MSDU Number Read Update Conditions: - HW: FWLTHTRR0.LTHTHR clear event. Functions: - Used for reading an entry in L3 table.
15	LTHGATEVR	R-D	0B	L3 GATE Valid Read Update Conditions: - HW: FWLTHTRR0.LTHTHR clear event. Functions: - Used for reading an entry in L3 table.
14: PSFP_GATE_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PSFP_GATE_W-1:0	LTHGATENR	R-D	0B	L3 GATE Number Read Update Conditions: - HW: FWLTHTRR0.LTHTHR clear event. Functions: - Used for reading an entry in L3 table.

(50) FWLTHTRR11

Forwarding Engine L3 Table Read Result 11

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHM TRVR	RSV									LTHMTRNR[PSFP_MTR_W-1:0]					
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHFR ERVR	RSV									LTHFRERNR[FRER_RECE_W-1:0]					

Bits	Bit name	RW-P	Initial value	Function description
31	LTHMTRVR	R-D	0B	<p>L3 MeTeR Valid Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTR clear event. - Functions: - Used for reading an entry in L3 table.
30: PSFP_MTR_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PSFP_MTR_W+15:16	LTHMTRNR	R-D	0B	<p>L3 MeTeR Number Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTR clear event. - Functions: - Used for reading an entry in L3 table.
15	LTHFRERVR	R-D	0B	<p>L3 FRER Valid Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTR clear event. - Functions: - Used for reading an entry in L3 table.
14: FRER_RECE_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
FRER_RECE_W-1:0	LTHFRERNR	R-D	0B	<p>L3 FRER Number Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTR clear event. - Functions: - Used for reading an entry in L3 table.

(51) FWLTHTRR12

Forwarding Engine L3 Table Read Result 12

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV / LTHSLVR[PORT_N-1]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHR VR	RSV				LTHRNR[LTH_RRULE_W-1:0]										

Bits	Bit name	RW-P	Initial value	Function description
31: PORT_N+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PORT_N+15:16	LTHSLVR	R-D	0H	<p>L3 Source Lock Vector Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table.
15	LTHRVR	R-D	0B	<p>L3 Routing Valid Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table.
14: LTH_RRULE_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
LTH_RRULE_W-1:0	LTHRNR	R-D	0B	<p>L3 Routing Number Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table.

(52) FWLTHTRR13i (i=0..PORT_GWCA_N-1)

Forwarding Engine L3 Table Read Result 13 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / LTHCSDRi[AXI_CHAIN_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: AXI_CHAIN_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
AXI_CHAIN_W-1:0	LTHCSDRi	R-D	0B	<p>L3 CPU Sub-Destination Read i</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTR clear event. - Used for reading an entry in L3 table. <p>Functions:</p>

(53) FWLTHTRR14

Forwarding Engine L3 Table Read Result 14

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV										LTHC MER	LTHE MER	LTHIP UR	LTHIPVR[2:0]		
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / LTHDVR[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
21	LTHCMER	R-D	0B	<p>L3 CPU Mirroring Enable Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table.
20	LTHEMER	R-D	0B	<p>L3 Ethernet Mirroring Enable Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table.
19	LTHIPUR	R-D	0B	<p>L3 Internal Priority Update Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table.
18:16	LTHIPVR	R-D	0B	<p>L3 Internal Priority Value Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table.
15:PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PORT_N-1:0	LTHDVR	R-D	0B	<p>L3 Destination Vector Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table.

(54) FWLTHTRR15

Forwarding Engine L3 Table Read Result 15

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / LTHDLVR[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PORT_N-1:0	LTHDLVR	R-D	0B	<p>L3 Destination Lock Vector Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWLTHTRR0.LTHTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in L3 table.

(55) FWLTHREUSPC

Forwarding Engine L3 REcovery US Prescaler Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV						LTHREUSP[9:0]									

Bits	Bit name	RW-P	Initial value	Function description
31:10	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
9:0	LTHREUSP	RW-F	0B	<p>L3 REcovery US Prescaler</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used to creates an internal clock for recovery at 1MHz to derive the recovery 1Hz clock. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: This register should be set to the number of clocks clk contained in 1us. Exp [R-Car/S4 clock = 320MHz] LTHREUSP = 320 clock / 1us = 140H

(56) FWLTHREC

Forwarding Engine L3 REcovery Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV		LTHR EAOG	LTHR EPOG	RSV			LTHR EAS	RSV	LTHRE PM	RSV	LTHRE E	LTHRET[19:16]			
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHRET[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:30	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
29	LTHREAOG	R-F	0B	<p>L3 REcovery Aperiodic OnGoing</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: L3 recovery aperiodic is not ongoing - 1'b1: L3 recovery aperiodic is ongoing
28	LTHREPOG	R-F	0B	<p>L3 REcovery Periodic OnGoing</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: L3 recovery periodic is not ongoing - 1'b1: L3 recovery periodic is ongoing
27:25	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
24	LTHREAS	R0W-F	0B	<p>L3 REcovery Aperiodic Start</p> <p>Functions:</p> <ul style="list-style-type: none"> - Writing 1'b1 to this register will start L3 table recovery. <p>Restrictions:</p> <ul style="list-style-type: none"> - L3/L2 stream table recover can only happen when recovering is disabled (FWLTHREC.LTHREE is not set)
23	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
22	LTHREPM	RW-F	0B	<p>L3 REcovery Polling Mode</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: L3 recovery polling mode disabled - 1'b1: L3 recovery polling mode enabled <p>Functions</p> <ul style="list-style-type: none"> - When set to 1'b1, allows software to check all L3 table recovering by recovery.
21	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
20	LTHREE	RW-F	0B	<p>L3 REcovery Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: L3 recovery is disabled - 1'b1: L3 recovery is enabled and will happen every FWLTHREC.LTHRET seconds.
19:0	LTHRET	RW-F	0B	<p>L3 REcovery Time</p> <p>Functions:</p> <ul style="list-style-type: none"> - Defines the time in seconds the L3 recovery interval.

(57) FWLTHREM

Forwarding Engine L3 REcovery Monitoring

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV						RELTHEN[LTH_STREAM_W-1:0]									

Bits	Bit name	RW-P	Initial value	Function description
31:LTH_STREAM_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
LTH_STREAM_W-1:0	RELTHEN	R-F	0B	<p>REcovered L3/L2 stream table Entry Number</p> <p>Functions:</p> <ul style="list-style-type: none"> - Shows the L3/L2 stream table entry number of the latest recovered entry.

3.3.1.7 Layer 2 forwarding function registers

(1) FWMACTEC0

Forwarding Engine MAC Table Entry Configuration 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV					MACTUENC[MAC_ENTRY_W-1:0]										

Bits	Bit name	RW-P	Initial value	Function description
31:MAC_ENTRY_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
MAC_ENTRY_W-1:0	MACTUENC	RW-F	0H	<p>MAC Table Unsecure Entry Number Configuration</p> <p>Functions:</p> <ul style="list-style-type: none"> - FWMACTEC0.MACTUENC = 0: All secure entry but none unsecure entry. - FWMACTEC0.MACTUENC = 0x8: MAC table from 0 to 7 are unsecure entry and 8 ~ MAC_ENTRY_N-1 are secure entry. - FWMACTEC0.MACTUENC = MAC_ENTRY_N-1: MAC table from 0 to MAC_ENTRY_N-2 are unsecure entry and MAC_ENTRY_N-1 is secure entry. (All entry cannot be unsecure.)

(2) FWMACTL0

Forwarding Engine MAC Table Learn 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV					MACELA[MAC_ENTRY_W:1:0]										

Bits	Bit name	RW-P	Initial value	Function description
31: MAC_ENTRY_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
MAC_ENTRY_W:1:0	MACELA	RW-D	0B	<p>MAC Entry Learn Address</p> <ul style="list-style-type: none"> - The learning address (entry number) of MAC table. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: Entry learning will be ignored if MAC table address of HW learning (from FWMACHWLC0.MACTHWLSA to FWMACHWLC0.MACTHWLEA). - SW: Entry deleting have NOT to be MAC table address of HW learning (from FWMACHWLC0.MACTHWLSA to FWMACHWLC0.MACTHWLEA). This is only for debugging.

(3) FWMACTL1

Forwarding Engine MAC Table Learn 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MACED	RSV								MACFPL[3:0]				MACRPL[3:0]		
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV	MACSB LL	MACDB LL	RSV	MACH LDL	MACD EL	RSV									

Bits	Bit name	RW-P	Initial value	Function description
31	MACED	RW-D	0B	MAC Entry Delete Values: - 1'b0: Learn the set MAC address in MAC table. - 1'b1: Delete the set MAC address in MAC table.
30:24	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
23	MACFPL[3]	RW-F	0B	MAC Filtering Priority Learn (MSB) Functions: - Used for learning/overwriting an entry in MAC table.
22:20	MACFPL[2:0]	RW-D	0B	MAC Filtering Priority Learn Functions: - Used for learning/overwriting an entry in MAC table.
19	MACRPL[3]	RW-F	0B	MAC Routing Priority Learn (MSB) Functions: - Used for learning/overwriting an entry in MAC table.
18:16	MACRPL[2:0]	RW-D	0B	MAC Routing Priority Learn Functions: - Used for learning/overwriting an entry in MAC table.
15:14	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
13	MACSBL	RW-D	0B	MAC Source MAC Block List Learn Functions: Used for learning/overwriting an entry in MAC table.
12	MACDBL	RW-D	0B	MAC Destination MAC Block List Learn Functions: Used for learning/overwriting an entry in MAC table.
11	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
10	MACHDL	RW-D	0B	MAC (Source MAC) Hardware Learning Disable Learn Functions: - Used for learning/overwriting an entry in MAC table.
9	MACDEL	RW-D	0B	MAC Dynamic Entry Learn Functions: - Used for learning/overwriting an entry in MAC table.
7:0	RSV	R0-U	0H	Reserved area. On read, 0 will be returned

(4) FWMACTL2

Forwarding Engine MAC Table Learn 2

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MACMS DUVL	RSV												MACMSDUNL [PSFP_MSDU_W-1:0]		
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACGA TEVL	RSV												MACGATENL [PSFP_GATE_W-1:0]		

Bits	Bit name	RW-P	Initial value	Function description
31	MACMSDUVL	RW-D	0B	MAC MSDU Valid Learn Functions: - Used for learning/overwriting an entry in MAC table.
30: PSFP_MSDU_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PSFP_MSDU_W+15:16	MACMSDUNL	RW-D	0B	MAC MSDU Number Learn Functions: - Used for learning/overwriting an entry in MAC table.
15	MACGATEVTL	RW-D	0B	MAC GATE Valid Learn Functions: - Used for learning/overwriting an entry in MAC table.
15:PSFP_GATE_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PSFP_GATE_W-1:0	MACGATENL	RW-D	0B	MAC GATE Number Learn Functions: - Used for learning/overwriting an entry in MAC table.

(5) FWMACTL3

Forwarding Engine MAC Table Learn 3

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MACM TRVL	RSV									MACMTRNL[PSFP_MTR_W+15:16]					
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACFR ERVL	RSV									MACFRERNL[FRER_RECE_W-1:0]					

Bits	Bit name	RW-P	Initial value	Function description
31	MACMTRVL	RW-D	0B	MAC Meter Valid Learn Functions: - Used for learning/overwriting an entry in MAC table.
30: PSFP_MTR_W+15+1	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PSFP_MTR_W+15:16	MACMTRNL	RW-D	0B	MAC Meter Number Learn Functions: - Used for learning/overwriting an entry in MAC table.
15	MACFRERVL	RW-D	0B	MAC FRER Valid Learn Functions: - Used for learning/overwriting an entry in MAC table.
14: FRER_RECE_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
FRER_RECE_W-1:0	MACFRERNL	RW-D	0B	MAC FRER Number Learn Functions: - Used for learning/overwriting an entry in MAC table.

(6) FWMACTL4

Forwarding Engine MAC Table Learn 4

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV / MACDSLVL[PORT_N-1:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / MACSSLVL[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: PORT_N+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PORT_N+15:16	MACDSLVL	RW-D	0H	MAC Destination Source Lock Vector Learn Functions: - Used for learning/overwriting an entry in MAC table.
15: PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PORT_N-1:0	MACSSLVL	RW-D	0H	MAC Source Source Lock Vector Learn Functions: - Used for learning/overwriting an entry in MAC table.

(7) FWMACTL5

Forwarding Engine MAC Table Learn 5

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACMALP0[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
15:0	MACMALP0	RW-D	0B	MAC MAC address Learn Part 0 Functions: - Used for learning/overwriting an entry in MAC table.

(8) FWMACTL6

Forwarding Engine MAC Table Learn 6

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MACMALP1[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACMALP1[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	MACMALP1	RW-D	0B	<p>MAC MAC address Learn Part 1</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in MAC table.

(9) FWMACTL7i (i=0..PORT_GWCA_N-1)

Forwarding Engine MAC Table Learn 7 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / MACCSDLi[AXI_CHAIN_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: AXI_CHAIN_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
AXI_CHAIN_W-1:0	MACCSDLi	RW-D	0B	<p>MAC CPU Sub-Destination Learn i</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in MAC table.

(10) FWMACTL8

Forwarding Engine MAC Table Learn 8

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV										MACC MEL	MACE MEL	MACIP UL	MACIPVL[2:0]		
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / MACDVL[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:22	RSV	RO-U	0H	Reserved area. On read, 0 will be returned
21	MACCMEL	RW-D	0B	MAC CPU Mirroring Enable Learn Functions: - Used for learning/overwriting an entry in MAC table.
20	MACEMEL	RW-D	0B	MAC Ethernet Mirroring Enable Learn Functions: - Used for learning/overwriting an entry in MAC table.
19	MACIPUL	RW-D	0B	MAC Internal Priority Update Learn Functions: - Used for learning/overwriting an entry in MAC table.
18:16	MACIPVL	RW-D	0B	MAC Internal Priority Value Learn Functions: - Used for learning/overwriting an entry in MAC table.
15:PORT_N	RSV	RO-U	0H	Reserved area. On read, 0 will be returned
PORT_N-1:0	MACDVL	RW-D	0B	MAC Destination Vector Learn Functions: - Used for learning/overwriting an entry in MAC table.

(11) FWMACTLR

Forwarding Engine MAC Table Learn Result

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
MACTL	RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	RSV										MACL DF	RSV	MACL OF	RSV	MACL SF	MACL F

Bits	Bit name	RW-P	Initial value	Function description
31	MACTL	R-D	0B	<p>MAC Table Learn</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: Writing FWMACTL8 register will set this bit. <p>Clear conditions:</p> <ul style="list-style-type: none"> - HW: This bit will be de-asserted when learning is completed. <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in MAC table.
30:4	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
5	MACLDF	R-D	0B	<p>MAC Learn Dynamic Fail</p> <p>Refer to Table 5-41</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Entry learning didn't fail because of a dynamic entry error. - 1'b1: Entry learning failed because of a dynamic entry error. <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTLR.MACTL clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in MAC table.
4	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
3	MACLOF	R-D	0B	<p>MAC Learn Overwrite Fail</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: The entry learning didn't fail. - 1'b1: The entry learning failed because of an existing entry. <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTLR.MACTL clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in MAC table. <p>Notes:</p> <ul style="list-style-type: none"> - If same entry (FWMACTL0.MACELA) (which has registered in the past) will be learned, FWMACTLR.MACLOF flag will be set and learning will be failed. If you want to update/overwrite this entry, please delete the entry before entry learn.
2	RSV	R0-U	0B	Reserved area. On read, 0 will be returned

1	MACSF	R-D	0B	<p>MAC Learn Security Fail</p> <p>Values:</p> <ul style="list-style-type: none">- 1'b0: Entry learning didn't fail because of a security error (refer to section 5.2.6.2(2)).- 1'b1: Entry learning failed because of a security error (refer to section 5.2.6.2(2)). <p>Update Conditions:</p> <ul style="list-style-type: none">- HW: FWMACTLR.MACTL clear event. <p>Functions:</p> <ul style="list-style-type: none">- Used for learning/overwriting an entry in MAC table.
0	MACLF	R-D	0B	<p>MAC Learn Fail</p> <p>Values:</p> <ul style="list-style-type: none">- 1'b0: Entry learning didn't fail (refer to section 5.2.6.2(2)).- 1'b1: Entry learning failed (refer to section 5.2.6.2(2)). <p>Update Conditions:</p> <ul style="list-style-type: none">- HW: FWMACTLR.MACTL clear event. <p>Functions:</p> <ul style="list-style-type: none">- Used for learning/overwriting an entry in MAC table.

(12) FWMACTIM

Forwarding Engine MAC Table Initialization Monitoring.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV															

Bits	Bit name	RW-P	Initial value	Function description
31:2	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
1	MACTR	R-RP	0H	<p>MAC Table Ready</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When FWMACTIM.MACTIOG is getting cleared. - HW: This bit is set at "clk_period[ns]* RACE_MAC_ENTRY_N" time from MAC table initialization starting. <p>Clear condition:</p> <ul style="list-style-type: none"> - SW: By writing 1 to FWMACTIM.MACTIOG.
0	MACTIOG	R!W-RP	0B	<p>MAC Table Initialization Ongoing.</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - SW: By writing 1 to this register. It starts MAC Table initialization. <p>Clear condition:</p> <ul style="list-style-type: none"> - HW: This bit is cleared when MAC Table initialization is finished.

(13) FWMACTEM

Forwarding Engine MAC Table Entry Monitoring.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV					MACTUEN[MAC_ENTRY_W:0]										
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV					MACTEN[MAC_ENTRY_W:0]										

Bits	Bit name	RW-P	Initial value	Function description
31: MAC_ENTRY_W+17	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
MAC_ENTRY_W+16:16	MACTUEN	R-P	0B	<p>MAC Table Unsecure Entry Number.</p> <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: An unsecure entry is learned successfully. <p>Decrement conditions:</p> <ul style="list-style-type: none"> - HW: An unsecure entry is deleted successfully.
15: MAC_ENTRY_W+1	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
MAC_ENTRY_W:0	MACTEN	R-P	0B	<p>MAC Table Entry Number.</p> <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: An entry is learned successfully. <p>Decrement conditions:</p> <ul style="list-style-type: none"> - HW: An entry is deleted successfully.

(14) FWMACTS0

Forwarding Engine MAC Table Search 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACMASP0[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
30:16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
15:0	MACMASP0	RW-D	0B	MAC MAC Address Search Part 0 Functions: - Used for searching an entry in MAC table.

(15) FWMACTS1

Forwarding Engine MAC Table Search 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MACMASP1[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACMASP1[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	MACMASP1	RW-D	0B	MAC MAC Address Search Part 1 Functions: - Used for searching an entry in MAC table.

(16) FWMACTS2

Forwarding Engine MAC Table Search 2

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV					MACTSEA[MAC_ENTRY_W-1:0]										
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV					MACTSSA [MAC_ENTRY_W-1:0]										

Bits	Bit name	RW-P	Initial value	Function description
31:MAC_ENTRY_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
MAC_ENTRY_W+15:16	MACTSEA	RW-D	0B	<p>MAC Table Search End Address for invalid search.</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table for invalid search. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: This register is only valid if FWMACTS3.MACTIVLS == 1'b1. - SW: This register should be set to bigger than or equal to FWMACTS2.MACTSSA.
15:MAC_ENTRY_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
MAC_ENTRY_W-1:0	MACTSSA	RW-D	0B	<p>MAC Table Search Start Address for invalid search</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table for invalid search. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: This register is only valid if FWMACTS3.MACTIVLS == 1'b1. - SW: This register should be set to smaller than or equal to FWMACTS2.MACTSEA. - HW: Search will not be found if the Start-End constraint is violated. - HW: From unsecure APB, search only for unsecure area. (If unsecure APB access and (FWMACTS2.MACTSEA > FWMACTEC0.MACTUENC-1), FWMACTS2.MACTSEA will be forced to FWMACTEC0.MACTUENC-1.)

(17) FWMACTS3

Forwarding Engine MAC Table Search 3

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV															

MACTI
VLS

Bits	Bit name	RW-P	Initial value	Function description
31:1	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
0	MACTIVLS	RW-D	0B	<p>MAC Table InVaLid Search</p> <p>Functions:</p> <ul style="list-style-type: none"> - 1'b0 : Used for searching an entry in MAC table for MAC address. - 1'b1 : Used for searching an entry in MAC table for invalid entry. And invalid search done. In invalid search case, FWMACTSR* will be cleared other than FWMACTSR0.MACSNF and FWMACTSR7.MACMCHAS.

(18) FWMACTSR0

Forwarding Engine MAC Table Search Result 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
MACT S	RSV								MACFPS[3:0]				MACRPS[3:0]			
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
RSV	MACSB LS	MACDB LS	RSV	MACH LDS	MACD ENTS	MACS LS	RSV								MACS NF	MACS EF

Bits	Bit name	RW-P	Initial value	Function description
31	MACTS	R-D	0B	<p>MAC Table Search</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: Writing FWMACTS3 register will set this bit. <p>Clear conditions:</p> <ul style="list-style-type: none"> - HW: This bit will be de-asserted when searching is completed. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. - If FWMACTS3.MACTIVLS is 1, this value will not be setting.
30:24	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
23	MACFPS[3]	R-F	0B	<p>MAC Filtering Priority Search (MSB)</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTSR0.MACTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. - If FWMACTS3.MACTIVLS is 1, this value is invalid (All 0).
22:20	MACFPS[2:0]	R-D	0B	<p>MAC Filtering Priority Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTSR0.MACTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. - If FWMACTS3.MACTIVLS is 1, this value is invalid (All 0).
19	MACRPS[3]	R-F	0B	<p>MAC Routing Priority Search (MSB)</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTSR0.MACTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. - If FWMACTS3.MACTIVLS is 1, this value is invalid (All 0).
18:16	MACRPS[2:0]	R-D	0B	<p>MAC Routing Priority Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTSR0.MACTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. - If FWMACTS3.MACTIVLS is 1, this value is invalid (All 0).
15:14	RSV	R0-U	0H	Reserved area. On read, 0 will be returned

13	MACSBL5	R-D	0B	<p>MAC Source MAC Block List Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTSR0.MACTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. - If FWMACTS3.MACTIVLS is 1, this value is invalid (All 0).
12	MACDBL5	R-D	0B	<p>MAC Destination MAC Block List Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTSR0.MACTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. - If FWMACTS3.MACTIVLS is 1, this value is invalid (All 0).
11	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
10	MACHLDS	R-D	0B	<p>MAC (Source MAC) Hardware Learning Disable Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTSR0.MACTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. - If FWMACTS3.MACTIVLS is 1, this value is invalid (All 0).
9	MACDENTS	R-D	0B	<p>MAC Dynamic ENTry Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTSR0.MACTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. - If FWMACTS3.MACTIVLS is 1, this value is invalid (All 0).
8	MACSL5	R-F	0B	<p>MAC Security Level Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTSR0.MACTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table.
7:2	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
1	MACSNF	R-D	0B	<p>MAC Search Not found</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: MAC address or invalid area found in MAC Table. - 1'b1: MAC address or invalid area not found in MAC Table. <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTSR0.MACTS clear event. (or invalid search done). <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. <p>Security restrictions:</p> <ul style="list-style-type: none"> - The unsecure APB interface cannot find an entry with security area in the MAC table.

0	MACSEF	R-D	0B	<p>MAC Search ECC Fail</p> <p>Values:</p> <ul style="list-style-type: none">- 1'b0: Entry Search didn't fail because of an ECC error.- 1'b1: Entry Search failed because of an ECC error. <p>Update Conditions:</p> <ul style="list-style-type: none">- HW: FWMACTSR0.MACTS clear event. <p>Functions:</p> <ul style="list-style-type: none">- Used for searching an entry in MAC table.- If FWMACTS3.MACTIVLS is 1, this value is invalid (All 0).
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(19) FWMACTSR1

Forwarding Engine MAC Table Search Result 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV / MACDSLVS[PORT_N-1:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / MACSSLVS[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: PORT_N+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PORT_N+15:16	MACDSLVS	R-D	0H	<p>MAC Destination Source Lock Vector Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTSR0.MACTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. - If FWMACTS3.MACTIVLS is 1, this value is invalid (All 0).
15:PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PORT_N-1:0	MACSSLVS	R-D	0H	<p>MAC Source Source Lock Vector Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTSR0.MACTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. - If FWMACTS3.MACTIVLS is 1, this value is invalid (All 0).

(20) FWMACTSR2i (i=0..PORT_GWCA_N-1)

Forwarding Engine MAC Table Search Result 2 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / MACCSDSi[AXI_CHAIN_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: AXI_CHAIN_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
AXI_CHAIN_W-1:0	MACCSDSi	R-D	0B	<p>MAC CPU Sub-Destination Search i</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTSR0.MACTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. - If FWMACTS3.MACTIVLS is 1, this value is invalid (All 0).

(21) FWMACTSR3

Forwarding Engine MAC Table Search Result 3

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV										MACCM ES	MACE MES	MACIP US	MACIPVS[2:0]		
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / MACDVS[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:22	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
21	MACCMES	R-D	0B	<p>MAC CPU Mirroring Enable Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTSR0.MACTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. - If FWMACTS3.MACTIVLS is 1, this value is invalid (All 0).
20	MACEMES	R-D	0B	<p>MAC Ethernet Mirroring Enable Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTSR0.MACTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. - If FWMACTS3.MACTIVLS is 1, this value is invalid (All 0).
19	MACIPUS	R-D	0B	<p>MAC Internal Priority Update Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTSR0.MACTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. - If FWMACTS3.MACTIVLS is 1, this value is invalid (All 0).
18:16	MACIPVS	R-D	0B	<p>MAC Internal Priority Value Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTSR0.MACTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. - If FWMACTS3.MACTIVLS is 1, this value is invalid (All 0).
15:PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PORT_N-1:0	MACDVS	R-D	0B	<p>MAC Destination Vector Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTSR0.MACTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. - If FWMACTS3.MACTIVLS is 1, this value is invalid (All 0).

(22) FWMACTSR4

Forwarding Engine MAC Table Search Result 4

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MACMS DUVS	RSV														MACMSDUNS [PSFP_MSDU_W+15:16]
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACG ATEV S	RSV														MACGATENS [PSFP_GATE_W-1:0]

Bits	Bit name	RW-P	Initial value	Function description
31	MACMSDUVS	R-D	0B	<p>MAC Table MSDU Valid Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTSR0.MACTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. - If FWMACTS3.MACTIVLS is 1, this value is invalid (All 0).
30: PSFP_MSDU_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PSFP_MSDU_W+15:16	MACMSDUNS	R-D	0B	<p>MAC Table MSDU Number Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTSR0.MACTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. - If FWMACTS3.MACTIVLS is 1, this value is invalid (All 0).
15	MACGATEVS	R-D	0B	<p>MAC Table GATE Valid Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTSR0.MACTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. - If FWMACTS3.MACTIVLS is 1, this value is invalid (All 0).
14: PSFP_GATE_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PSFP_GATE_W-1:0	MACGATENS	R-D	0B	<p>MAC Table GATE Number Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTSR0.MACTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. - If FWMACTS3.MACTIVLS is 1, this value is invalid (All 0).

(23) FWMACTSR5

Forwarding Engine MAC Table Search Result 5

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MACM TRVS	RSV									MACMTRNS[PSFP_MTR_W+15:16]					
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACFR ERVS	RSV									MACFRERNNS[FRER_RECE_W-1:0]					

Bits	Bit name	RW-P	Initial value	Function description
31	MACMTRVS	R-D	0B	<p>MAC Table Meter Valid Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTSR0.MACTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. - If FWMACTS3.MACTIVLS is 1, this value is invalid (All 0).
30: PSFP_MTR_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PSFP_MTR_W+15:16	MACMTRNS	R-D	0B	<p>MAC Table Meter Number Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTSR0.MACTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. - If FWMACTS3.MACTIVLS is 1, this value is invalid (All 0).
15	MACFRERVS	R-D	0B	<p>MAC FRER Valid Search</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. - If FWMACTS3.MACTIVLS is 1, this value is invalid (All 0).
14: FRER_RECE_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
FRER_RECE_W-1:0	MACFRERNNS	R-D	0B	<p>MAC FRER Number Search</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. - If FWMACTS3.MACTIVLS is 1, this value is invalid (All 0).

(24) FWMACTSR6

Forwarding Engine MAC Table Search Result 6

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV					MACMCHAS[MAC_ENTRY_W-1:0]										

Bits	Bit name	RW-P	Initial value	Function description
31: MAC_ENTRY_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
MAC_ENTRY_W-1:0	MACMCHAS	R-D	0B	<p>MAC entry MatCH Address Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTSR0.MACTS clear event. (or invalid search done). <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in MAC table. - If FWMACTS3.MACTIVLS is 1'b0, MAC table match address with MAC address. - If FWMACTS3.MACTIVLS is 1'b1, MAC table invalid address.

(25) FWMACTR

Forwarding Engine MAC Table Read

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV					MACAR[MAC_ENTRY_W-1:0]										

Bits	Bit name	RW-P	Initial value	Function description
31: MAC_ENTRY_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
MAC_ENTRY_W-1:0	MACAR	RW-D	0B	MAC table Address Read Functions: - Used for reading an entry in MAC table.

(26) FWMACTRR0

Forwarding Engine MAC Table Read Result 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MACT R	RSV														
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV														MACR EF	MACE VR

Bits	Bit name	RW-P	Initial value	Function description
31	MACTR	R-D	0B	<p>MAC Table Read</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: Writing FWMACTR register will set this bit. <p>Clear conditions:</p> <ul style="list-style-type: none"> - HW: This bit will be de-asserted when reading is completed. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in MAC table.
30:3	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
1	MACREF	R-D	0B	<p>MAC Read ECC Fail</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Entry Read didn't fail because of an ECC error. - 1'b1: Entry Read failed because of an ECC error. <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTRR0.MACTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in MAC table.
0	MACEVR	R-D	0B	<p>MAC Entry Valid Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTRR0.MACTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in MAC table. - The unsecure APB interface cannot find a valid entry with security level bit set in the MAC table. - If the Invalid area is read, please ignore the information that follows because past rule information remains.

(27) FWMACTRR1

Forwarding Engine MAC Table Read Result 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV								MACFPR[3:0]				MACRPR[3:0]			
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV	MACA BR	MACSB LR	MACDB LR	RSV	MACH LDR	MACD ER	MACS LR	RSV							

Bits	Bit name	RW-P	Initial value	Function description
31:24	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
23	MACFPR[3]	R-F	0B	<p>MAC Filtering Priority Read (MSB)</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTRR0.MACTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in MAC table.
22:20	MACFPR[2:0]	R-D	0B	<p>MAC Filtering Priority Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTRR0.MACTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in MAC table.
19	MACRPR[3]	R-F	0B	<p>MAC Routing Priority Read (MSB)</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTRR0.MACTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in MAC table.
18:16	MACRPR[2:0]	R-D	0B	<p>MAC Routing Priority Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTRR0.MACTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in MAC table.
15	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
14	MACABR	R-D	0B	<p>MAC Aging Bit Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTRR0.MACTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in MAC table.
13	MACSBLR	R-D	0B	<p>MAC Source MAC Block List Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTRR0.MACTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in MAC table.

12	MACDBLR	R-D	0B	<p>MAC Destination MAC Block List Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTRR0.MACTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in MAC table.
11	RSV	R0-U	0H	- Reserved area. On read, 0 will be returned
10	MACHLDR	R-D	0B	<p>MAC (Source MAC) Hardware Learn Disable Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTRR0.MACTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in MAC table.
9	MACDER	R-D	0B	<p>MAC Dynamic Entry Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTRR0.MACTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in MAC table.
8	MACSLR	R-F	0B	<p>MAC Security Level Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTRR0.MACTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in MAC table.
7:0	RSV	R0-U	0H	Reserved area. On read, 0 will be returned

(28) FWMACTRR2

Forwarding Engine MAC Table Read Result 2

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MACMS DUVR	RSV												MACMSDUNR [PSFP_MSDU_W+15:16]		
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACGA TEVR	RSV												MACGATENR [PSFP_GATE_W-1:0]		

Bits	Bit name	RW-P	Initial value	Function description
31	MACMSDUVR	R-D	0B	MAC Table MSDU Valid Read Update Conditions: - HW: FWMACTRR0.MACTR clear event. Functions: - Used for reading an entry in MAC table.
30: PSFP_MSDU_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PSFP_MSDU_W+15:16	MACMSDUNR	R-D	0B	MAC Table MSDU Number Read Update Conditions: - HW: FWMACTRR0.MACTR clear event. Functions: - Used for reading an entry in MAC table.
15	MACGATEVR	R-D	0B	MAC Table GATE Valid Read Update Conditions: - HW: FWMACTRR0.MACTR clear event. Functions: - Used for reading an entry in MAC table.
14: PSFP_GATE_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PSFP_GATE_W-1:0	MACGATENR	R-D	0B	MAC Table GATE Number Read Update Conditions: - HW: FWMACTRR0.MACTR clear event. Functions: - Used for reading an entry in MAC table.

(29) FWMACTRR3

Forwarding Engine MAC Table Read Result 3

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MACM TRVR	RSV									MACMTRNR[PSFP_MTR_W+15:16]					
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACFR ERVR	RSV									MACFRERNR[FRER_RECE_W-1:0]					

Bits	Bit name	RW-P	Initial value	Function description
31	MACMTRVR	R-D	0B	MAC Table Meter Valid Read Update Conditions: - HW: FWMACTRR0.MACTR clear event. Functions: - Used for reading an entry in MAC table.
30:PSFP_MTR_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PSFP_MTR_W+15:16	MACMTRNR	R-D	0B	MAC Table Meter Number Read Update Conditions: - HW: FWMACTRR0.MACTR clear event. Functions: - Used for reading an entry in MAC table.
15	MACFRERVR	R-D	0B	MAC FRER Valid Read Update Conditions: - HW: FWMACTRR0.MACTR clear event. Functions: - Used for reading an entry in MAC table.
14:FRER_RECE_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
FRER_RECE_W-1:0	MACFRERNR	R-D	0B	MAC FRER Number Read Update Conditions: - HW: FWMACTRR0.MACTR clear event. Functions: - Used for reading an entry in MAC table.

(30) FWMACTRR4

Forwarding Engine MAC Table Read Result 4

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV / MACDSLVR[PORT_N-1]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / MACSSLVR[PORT_N-1]															

Bits	Bit name	RW-P	Initial value	Function description
31: PORT_N+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PORT_N+15:16	MACDSLVR	R-D	0H	<p>MAC Destination Source Lock Vector Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTRR0.MACTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in MAC table.
15: PORT_N-1	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PORT_N-1:0	MACSSLVR	R-D	0H	<p>MAC Source Source Lock Vector Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTRR0.MACTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in MAC table.

(31) FWMACTRR5

Forwarding Engine MAC Table Read Result 5

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACMAR0[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
15:0	MACMAR0	R-D	0B	<p>MAC MAC address Read Part 0</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTRR0.MACTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in MAC table.

(32) FWMACTRR6

Forwarding Engine MAC Table Read Result 6

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MACMARP1[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACMARP1[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	MACMARP1	R-D	0B	<p>MAC MAC Address Read Part 1</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTRR0.MACTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in MAC table.

(33) FWMACTRR7i (i=0..PORT_GWCA_N-1)

Forwarding Engine MAC Table Read Result 7 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / MACCSDRi[AXI_CHAIN_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: AXI_CHAIN_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
AXI_CHAIN_W-1:0	MACCSDRi	R-D	0B	<p>MAC CPU Sub-Destination Read i</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTRR0.MACTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in MAC table.

(34) FWMACTRR8

Forwarding Engine MAC Table Read Result 8

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV										MACCM ER	MACEM ER	MACIP UR	MACIPVR[2:0]		
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / MACDVR[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:22	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
21	MACCMER	R-D	0B	<p>MAC CPU Mirroring Enable Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTRR0.MACTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in MAC table.
20	MACEMER	R-D	0B	<p>MAC Ethernet Mirroring Enable Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTRR0.MACTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in MAC table.
19	MACIPUR	R-D	0B	<p>MAC Internal Priority Update Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTRR0.MACTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in MAC table.
18:16	MACIPVR	R-D	0B	<p>MAC Internal Priority Value Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTRR0.MACTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in MAC table.
15:PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PORT_N-1:0	MACDVR	R-D	0B	<p>MAC Destination Vector Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWMACTRR0.MACTR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for reading an entry in MAC table.

(35) FWMACHWLC0

Forwarding Engine MAC table HW Learning Configuration 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MACTH WLFC3	MACTH WLFC2	RSV			MACTHWLEA[MAC_ENTRY_W-1:0]										
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACTH WLFC1	MACTH WLFC0	RSV			MACTHWLSA[MAC_ENTRY_W-1:0]										

Bits	Bit name	RW-P	Initial value	Function description
31	MACTHWLFC3	RW-P	1H	MAC Table HardWare Learning Filtering Configuration 3 Functions: - 1'b0: No functions - 1'b1: MAC hardware learning/Migration will not be occurred with follow filtering. "Acceptance list (Ingress/Egress) filtering rejecting" (Secure and Unsecure) "Block list filtering rejecting" (Secure and Unsecure)
30	MACTHWLFC2	RW-P	1H	MAC Table HardWare Learning Filtering Configuration 2 Functions: - 1'b0: No functions - 1'b1: MAC hardware learning/Migration will not be occurred with follow filtering. "Layer two VLAN source port filtering rejecting" (Secure and Unsecure) "Layer two VLAN unknown filtering rejecting" (Secure and Unsecure)
29: MAC_ENTRY_W+17	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
MAC_ENTRY_W+16:16	MACTHWLEA	RW-P	0B	MAC Table HardWare Learning End Address Functions: - MAC table address of HW learning end point configuration. Restrictions: - SW: This register should be set to bigger than or equal to FWMACHWLC0.MACTHWLSA . - SW: This register should be set to smaller than FWMACTEC0.MACTUENC . - HW: If FWMACHWLC0.MACTHWLSA > FWMACHWLC0.MACTHWLEA , no hardware learning area. - HW: If FWMACTEC0.MACTUENC is 0x0, this value is invalid (no HW learning).
15	MACTHWLFC1	RW-P	0H	MAC Table HardWare Learning Filtering Configuration 1 Functions: - 1'b0: No functions - 1'b1: MAC hardware learning/Migration will not be occurred with follow filtering. "Layer 3 source port filtering rejecting" (Secure and Unsecure) "Layer 3 unknown filtering rejecting" (Secure and Unsecure)
14	MACTHWLFC0	RW-P	0H	MAC Table HardWare Learning Filtering Configuration 0 Functions: - 1'b0: No functions - 1'b1: MAC hardware learning/Migration will not be occurred with follow filtering. "Layer two destination source port filtering rejecting" (Secure and Unsecure) "Layer two destination unknown filtering rejecting" (Secure and Unsecure)
13: MAC_ENTRY_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned

MAC_ENTRY_W-1:0	MACTHWLSA	RW-P	0B	<p>MAC Table HardWare Learning Start Address</p> <p>Functions:</p> <ul style="list-style-type: none">- MAC table address of HW learning start point configuration. <p>Restrictions:</p> <ul style="list-style-type: none">- SW: This register should be set to smaller than or equal to FWMACHWLCO.MACTHWLEA.- HW: If FWMACHWLCO.MACTHWLSA > FWMACHWLCO.MACTHWLEA, no hardware learning area.- HW: If FWMACTEC0.MACTUENC is 0x0, this value is invalid (no HW learning).
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(36) FWMACHWLC1

Forwarding Engine MAC table HW Learning Configuration 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV				MACDEN[MAC_ENTRY_W:0]											
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV															

Bits	Bit name	RW-P	Initial value	Function description
31: MAC_ENTRY_W+17	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
MAC_ENTRY_W+17:16	MACDEN	R-P	0B	<p>MAC Dynamic Entry Number</p> <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: A entry is learned successfully on MAC table address of HW learning. (MAC table address of learned entry was from FWMACHWLC0.MACTHWLSA to FWMACHWLC0.MACTHWLEA). <p>Decrement conditions:</p> <ul style="list-style-type: none"> - HW: A dynamic entry is deleted successfully (MAC table address of deleted entry was from FWMACHWLC0.MACTHWLSA to FWMACHWLC0.MACTHWLEA). <p>Restrictions:</p> <ul style="list-style-type: none"> - This counter cannot operate normally for an entry with an ECC (2bit) error in RAM. (Because the information about whether it is a Dynamic entry is broken.)
15:0	RSV	R0-U	0H	- Reserved area. On read, 0 will be returned

(37) FWMACHWLC2i (i=0..PORT_N-1)

Forwarding Engine MAC table HW Learning Configuration 2 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV				MACDENPPi[MAC_ENTRY_W:0]											
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV				MACDELNPPi[MAC_ENTRY_W:0]											

Bits	Bit name	RW-P	Initial value	Function description
31: MAC_ENTRY_W+17	RSV	RO-U	0H	Reserved area. On read, 0 will be returned
MAC_ENTRY_W+17:16	MACDENPPi	R-P	0B	<p>MAC Dynamic Entry Number Per Port i</p> <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: A dynamic entry is learned/migrated successfully for source port i. (Entries learnt with MAC table address of HW learning and MAC.DV[i] set with MAC table address of learned entry was from FWMACHWLCO.MACTHWLSA to FWMACHWLCO.MACTHWLEA). <p>Decrement conditions:</p> <ul style="list-style-type: none"> - HW: A dynamic entry is deleted (and overwritten by migration) successfully for source port i. (Entries delete with MAC table address of HW learning and MAC.DV[i] set with MAC table address of learned entry was from FWMACHWLCO.MACTHWLSA to FWMACHWLCO.MACTHWLEA) <p>Restrictions:</p> <ul style="list-style-type: none"> - This counter cannot operate normally for an entry with an ECC (2bit) error in RAM. (Because the information about whether it is a Dynamic entry is broken.) - If the same Source MAC is received from multiple ports, this counter will not work properly due to HW migration.
15: MAC_ENTRY_W	RSV	RO-U	0H	Reserved area. On read, 0 will be returned
MAC_ENTRY_W:0	MACDELNPPi	RW-P	MAC_ENTRY_N	<p>MAC Dynamic Entry Limit Number Per Port i</p> <p>Functions:</p> <ul style="list-style-type: none"> - Set the maximum number of dynamic entries that can be learnt for port i in MAC table (Entries learnt with MAC table address of HW learning set and MAC.DV[i] set with MAC table address of learned entry was from FWMACHWLCO.MACTHWLSA to FWMACHWLCO.MACTHWLEA). If dynamic entry number reached limit of this setting (FWMACHWL2i.MACDENPPi >= FWMACHWL2i.MACDELNPPi), HW learning will be failed. - This function will be disabled by setting all 0. <p>Restrictions:</p> <ul style="list-style-type: none"> - This register should be set to smaller than or equal to MAC_ENTRY_N.

(38) FWMACAGUSPC

Forwarding Engine MAC AGing US Prescaler Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV						MACAGUSP[9:0]									

Bits	Bit name	RW-P	Initial value	Function description
31:10	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
9:0	MACAGUSP	RW-F	0B	<p>MAC AGing US prescaler</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used to creates an internal clock for aging at 1MHz to derive the aging 1Hz clock. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: This register should be set to the number of clocks clk contained in 1us. Exp [R-Car/S4 clock = 320MHz] MACAGUSP = 320 clock / 1us = 140H

(39) FWMACAGC

Forwarding Engine MAC AGing Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV		MACDE SOG	MACAG OG	RSV			MACD ES	RSV	MACAGP M	MACAG SL	MACAG E	MACAGT[19:16]			
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACAGT[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:30	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
29	MACDESOG	R-P	0B	<p>MAC Dynamic Entry Suppression OnGoing</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: MAC Dynamic Entry Suppression is not ongoing - 1'b1: MAC Dynamic Entry Suppression is ongoing
28	MACAGOG	R-P	0B	<p>MAC AGing OnGoing</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: MAC aging is not ongoing - 1'b1: MAC aging is ongoing
27:25	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
24	MACDES	R0W-P	0B	<p>MAC Dynamic Entry Suppression</p> <p>Functions:</p> <ul style="list-style-type: none"> - Writing 1'b1 to this register will start dynamic entry suppression. - Dynamic entry suppression will delete all dynamic entries from MAC table (including hardware learning entries). <p>Restrictions:</p> <ul style="list-style-type: none"> - Dynamic Entry Suppression can only happen when aging is disabled (FWMACAGC.MACAGE is not set)
23	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
22	MACAGPM	RW-P	0B	<p>MAC AGing Polling Mode</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: MAC aging polling mode disabled - 1'b1: MAC aging polling mode enabled <p>Functions</p> <ul style="list-style-type: none"> - When set, allows software to check all MAC addresses suppresses by aging or dynamic entry suppressed.
21	MACAGSL	RW-RP	0B	<p>MAC AGing Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Only unsecure entries (MAC.SL == 1'b0) will be aged or suppressed - 1'b1: All entries will be aged or suppressed.
20	MACAGE	RW-P	0B	<p>MAC AGing Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: MAC aging is disabled - 1'b1: MAC aging is enabled and will happen every FWMACAGC.MACAGT seconds.

19:0	MACAGT	RW-P	0B	MAC AGing Time Functions: - Defines the time in seconds the MAC aging interval. - This value recommended setting to 10~300 sec.
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(40) FWMACAGM0

Forwarding Engine MAC AGing Monitoring 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AGMACAP0[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
15:0	AGMACAP0	R-P	0B	Aged MAC Address Part 0 Functions: - Shows the MAC address part 0 of the latest aged entry or dynamic entry suppressed.

(41) FWMACAGM1

Forwarding Engine MAC AGing Monitoring 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AGMACAP1[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AGMACAP1[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	AGMACAP1	R-P	0B	Aged MAC Address Part 1 Functions: - Shows the MAC address part 1 of the latest aged entry or dynamic entry suppressed.

(42) FWMACREUSPC

Forwarding Engine MAC REcovery US Prescaler Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV						MACREUSP[9:0]									

Bits	Bit name	RW-P	Initial value	Function description
31:10	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
9:0	MACREUSP	RW-F	0B	<p>MAC REcovery US Prescaler</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used to creates an internal clock for recovery at 1MHz to derive the recovery 1Hz clock. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: This register should be set to the number of clocks clk contained in 1us. Exp [R-Car/S4 clock = 320MHz] MACREUSP = 320 clock / 1us = 140H

(43) FWMACREC

Forwarding Engine MAC REcovery Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV		MACR EAOG	MACR EPOG	RSV			MACR EAS	RSV	MACR EPM	RSV	MACRE E	MACRET[19:16]			
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACRET[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:30	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
29	MACREAOG	R-F	0B	<p>MAC REcovery Aperiodic OnGoing</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: MAC recovery aperiodic is not ongoing - 1'b1: MAC recovery aperiodic is ongoing
28	MACREPOG	R-F	0B	<p>MAC REcovery Periodic OnGoing</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: MAC recovery periodic is not ongoing - 1'b1: MAC recovery periodic is ongoing
27:25	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
24	MACREAS	R0W-F	0B	<p>MAC REcovery Aperiodic Start</p> <p>Functions:</p> <ul style="list-style-type: none"> - Writing 1'b1 to this register will start MAC table recovery. <p>Restrictions:</p> <ul style="list-style-type: none"> - MAC table recover can only happen when recovering is disabled (FWMACREC.MACREE is not set)
23	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
22	MACREPM	RW-F	0B	<p>MAC REcovery Polling Mode</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: MAC recovery polling mode disabled - 1'b1: MAC recovery polling mode enabled <p>Functions</p> <ul style="list-style-type: none"> - When set to 1'b1, allows software to check all MAC table recovering by recovery.
21	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
20	MACREE	RW-F	0B	<p>MAC REcovery Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: MAC recovery is disabled - 1'b1: MAC recovery is enabled and will happen every FWMACREC.MACRET seconds.
19:0	MACRET	RW-F	0B	<p>MAC REcovery Time</p> <p>Functions:</p> <ul style="list-style-type: none"> - Defines the time in seconds the MAC recovery interval.

(44) FWMACREM

Forwarding Engine MAC REcovery Monitoring

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV					REMACEN[MAC_ENTRY_W-1:0]										

Bits	Bit name	RW-P	Initial value	Function description
31: MAC_ENTRY_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
MAC_ENTRY_W-1:0	REMACEN	R-F	0B	<p>REcovered MAC table Entry Number</p> <p>Functions:</p> <ul style="list-style-type: none"> - Shows the MAC table entry number of the latest recovered entry.

(45) FWVLANTEC

Forwarding Engine VLAN Table Entry Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV		VLANTMUE[12:0]													
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV															

Bits	Bit name	RW-P	Initial value	Function description
31:29	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
28:16	VLANTMUE	RW-F	0B	VLAN Table Maximum Unsecure Entry Functions: - SW: Maximum unsecure entry number that can be set in table
15:0	RSV	R0-U	0H	Reserved area. On read, 0 will be returned

(46) FWVLANTL0

Forwarding Engine VLAN Table Learn 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VLANE D	RSV								VLANFPL[3:0]			VLANRPL[3:0]			
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV			VLANBL L	RSV	VLAN HDL	RSV	VLANS LL	RSV							

Bits	Bit name	RW-P	Initial value	Function description
31	VLANED	RW-D	0B	VLAN Entry Delete Values: - 1'b0: Learn/overwrite the set VLAN in VLAN table. - 1'b1: Delete the set VLAN in VLAN table.
31:24	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
23	VLANFPL[3]	RW-F	0B	VLAN Filtering Priority Learn (MSB) Functions: - Used for learning/overwriting an entry in VLAN table.
22:20	VLANFPL[2:0]	RW-D	0B	VLAN Filtering Priority Learn Functions: - Used for learning/overwriting an entry in VLAN table.
19	VLANRPL[3]	RW-F	0B	VLAN Routing Priority Learn (MSB) Functions: - Used for learning/overwriting an entry in VLAN table.
18:16	VLANRPL[2:0]	RW-D	0B	VLAN Routing Priority Learn Functions: - Used for learning/overwriting an entry in VLAN table.
15:13	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
12	VLANBLL	RW-D	0B	VLAN Block List Learn Functions: Used for learning/overwriting an entry in VLAN table.
11	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
10	VLANHDL	RW-D	0B	VLAN (Source MAC) Hardware Learning Disable Learn Functions: - Used for learning/overwriting an entry in VLAN table.
9	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
8	VLANSLL	RW-F	0B	VLAN Security Level Learn Functions: - Used for learning/overwriting an entry in VLAN table.
7:0	RSV	R0-U	0H	Reserved area. On read, 0 will be returned

(47) FWVLANTL1

Forwarding Engine VLAN Table Learn 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV				VLANVIDL[11:0]											

Bits	Bit name	RW-P	Initial value	Function description
31:12	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
11:0	VLANVIDL	RW-D	0B	VLAN VID Learn Functions: - Used for learning/overwriting an entry in VLAN table.

(48) FWVLANTL2

Forwarding Engine VLAN Table Learn 2

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VLANMSDUVL	RSV														VLANMSDUNL [PSFP_MSDU_W-1:0]
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VLANGATEVL	RSV														VLANGATENL [PSFP_GATE_W-1:0]

Bits	Bit name	RW-P	Initial value	Function description
31	VLANMSDUVL	RW-D	0B	VLAN MSDU Valid Learn Functions: - Used for learning/overwriting an entry in VLAN table.
30: PSFP_MSDU_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PSFP_MSDU_W+15:16	VLANMSDUNL	RW-D	0B	VLAN MSDU Number Learn Functions: - Used for learning/overwriting an entry in VLAN table.
15	VLANGATEVL	RW-D	0B	VLAN GATE Valid Learn Functions: - Used for learning/overwriting an entry in VLAN table.
15:PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PSFP_GATE_W-1:0	VLANGATENL	RW-D	0B	VLAN GATE Number Learn Functions: - Used for learning/overwriting an entry in VLAN table.

(49) FWVLANTL3

Forwarding Engine VLAN Table Learn 3

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VLANM TRVL	RSV									VLANMTRNL[PSFP_MTR_W+15:16]					
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VLANFR ERVL	RSV									VLANFRERNL[FRER_RECE_W-1:0]					

Bits	Bit name	RW-P	Initial value	Function description
31	VLANMTRVL	RW-D	0B	VLAN Meter Valid Learn Functions: - Used for learning/overwriting an entry in VLAN table.
30: PSFP_MTR_W+15+1	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PSFP_MTR_W+15:16	VLANMTRNL	RW-D	0B	VLAN Meter Number Learn Functions: - Used for learning/overwriting an entry in VLAN table.
15	VLANFRERVL	RW-D	0B	VLAN FRER Valid Learn Functions: - Used for learning/overwriting an entry in VLAN table.
14: FRER_RECE_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
FRER_RECE_W-1:0	VLANFRERNL	RW-D	0B	VLAN FRER Number Learn Functions: - Used for learning/overwriting an entry in VLAN table.

(50) FWVLANTL4

Forwarding Engine VLAN Table Learn 4

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV / VLANSLVL[PORT_N:1:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VLANR VL	RSV				VLANRNL[LTH_RRULE_W:1:0]										

Bits	Bit name	RW-P	Initial value	Function description
31: PORT_N+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PORT_N+15:16	VLANSLVL	RW-D	0H	VLAN Source Lock Vector Learn Functions: - Used for learning/overwriting an entry in VLAN table.
15	VLANRVL	RW-D	0B	VLAN Routing Valid Learn Functions: - Used for learning/overwriting an entry in VLAN table.
14: LTH_RRULE_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
LTH_RRULE_W:1:0	VLANRNL	RW-D	0B	VLAN Routing Number Learn Functions: - Used for learning/overwriting an entry in VLAN table.

(51) FWVLANTL5

Forwarding Engine VLAN Table Learn 5

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / VLANFMVL[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PORT_N-1:0	VLANFMVL	RW-D	0H	<p>VLAN Forwarding Mask Vector Learn</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in VLAN table. <p>Details:</p> <ul style="list-style-type: none"> - Bit i set to 1'b1: Frames forwarded by Layer 3 or Layer 2 forwarding cannot be forwarded to port i. (same as forwarding mask)

(52) FWVLANTL6i (i=0..PORT_GWCA_N-1)

Forwarding Engine VLAN Table Learn 6 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / VLANCSDLi[AXI_CHAIN_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: AXI_CHAIN_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
AXI_CHAIN_W-1:0	VLANCSDLi	RW-D	0B	VLAN CPU Sub-Destination Learn i Functions: - Used for learning/overwriting an entry in VLAN table.

(53) FWVLANTL7

Forwarding Engine VLAN Table Learn 7

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV											VLAN CMEL	VLAN EMEL	VLANIPVL[2:0]		
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / VLANDVL[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:16	RSV	RO-U	0H	Reserved area. On read, 0 will be returned
21	VLANCMEL	RW-D	0B	VLAN CPU Mirroring Enable Learn Functions: - Used for learning/overwriting an entry in VLAN table.
20	VLANEMEL	RW-D	0B	VLAN Ethernet Mirroring Enable Learn Functions: - Used for learning/overwriting an entry in VLAN table.
19	VLANIPUL	RW-D	0B	VLAN Internal Priority Update Learn Functions: - Used for learning/overwriting an entry in VLAN table.
18:16	VLANIPVL	RW-D	0B	VLAN Internal Priority Value Learn Functions: - Used for learning/overwriting an entry in VLAN table.
15:PORT_N	RSV	RO-U	0H	Reserved area. On read, 0 will be returned
PORT_N-1:0	VLANDVL	RW-D	0B	VLAN Destination Vector Learn Functions: - Used for learning/overwriting an entry in VLAN table.

(54) FWVLANTLR

Forwarding Engine VLAN Table Learn Result

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VLANT L	RSV														
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RSV														
												VLANL O	VLANL EF	VLANL SF	VLANL F

Bits	Bit name	RW-P	Initial value	Function description
31	VLANTL	R-D	0B	<p>VLAN Table Learn</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: Writing FWVLANTL7 register will set this bit. <p>Clear conditions:</p> <ul style="list-style-type: none"> - HW: This bit will be de-asserted when learning is completed. <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in VLAN table.
30:4	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
3	VLANLO	R-D	0B	<p>VLAN Learn Overwrite</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: The entry learning didn't overwrite an existing entry. - 1'b1: The entry learning overwrote an existing entry. <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWVLANTLR.VLANTL clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in VLAN table.
2	VLANLEF	R-D	0B	<p>VLAN Learn ECC Fail</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Entry learning didn't fail because of an ECC error. - 1'b1: Entry learning failed because of an ECC error. <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWVLANTLR.VLANTL clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in VLAN table.
1	VLANLSF	R-D	0B	<p>VLAN Learn Security Fail</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Entry learning didn't fail because of a security error (refer to section 5.2.6.3(2)). - 1'b1: Entry learning failed because of a security error (refer to section 5.2.6.3(2)). <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWVLANTLR.VLANTL clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for learning/overwriting an entry in VLAN table.

0	VLANLF	R-D	0B	<p>VLAN Learn Fail</p> <p>Values:</p> <ul style="list-style-type: none">- 1'b0: Entry learning didn't fail (refer to section 5.2.6.3(2)).- 1'b1: Entry learning failed (refer to section 5.2.6.3(2)). <p>Update Conditions:</p> <ul style="list-style-type: none">- HW: FWVLANTLR.VLANTL clear event. <p>Functions:</p> <ul style="list-style-type: none">- Used for learning/overwriting an entry in VLAN table.
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(55) FWVLANTIM

Forwarding Engine VLAN Table Initialization Monitoring.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV															

Bits	Bit name	RW-P	Initial value	Function description
31:2	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
1	VLANTR	R-RP	0H	<p>VLAN Table Ready</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When FWVLANTIM.VLANTIOG is getting cleared. - HW: This bit is set at "clk_period[ns]*4096" time from VLAN table initialization starting. <p>Clear condition:</p> <ul style="list-style-type: none"> - SW: By writing 1 to FWVLANTIM.VLANTIOG.
0	VLANTIOG	R!=W-RP	0B	<p>VLAN Table Initialization Ongoing.</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - SW: By writing 1 to this register. It starts VLAN Table initialization. <p>Clear condition:</p> <ul style="list-style-type: none"> - HW: This bit is cleared when VLAN Table initialization is finished.

(56) FWVLANTEM

Forwarding Engine VLAN Table Entry Monitoring

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV			VLANTUEN[12:0]												
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV			VLANTEN[12:0]												

Bits	Bit name	RW-P	Initial value	Function description
31:29	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
28:16	VLANTUEN	R-RP	0B	VLAN Table Unsecure Entry Number. Increment conditions: - HW: An unsecure entry is learned successfully. Decrement conditions: - HW: An unsecure entry is deleted successfully.
15:13	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
12:0	VLANTEN	R-RP	0B	VLAN Table Entry Number. Increment conditions: - HW: An entry is learned successfully. Decrement conditions: - HW: An entry is deleted successfully.

(57) FWVLANTS

Forwarding Engine VLAN Table Search

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV				VLANVIDS[11:0]											

Bits	Bit name	RW-P	Initial value	Function description
31:12	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
11:0	VLANVIDS	RW-D	0B	VLAN VID Search Functions: - Used for searching an entry in VLAN table.

(58) FWVLANTSRO

Forwarding Engine VLAN Table Search Result 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VLANT S	RSV								VLANFPS[3:0]				VLANRPS[3:0]		
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV			VLANBL S	RSV	VLAN HLDS	RSV	VLAN SLS	RSV							

Bits	Bit name	RW-P	Initial value	Function description
31	VLANTS	R-D	0B	VLAN Table Search Set conditions: - HW: Writing FWVLANTS register will set this bit. Clear conditions: - HW: This bit will be de-asserted when searching is completed. Functions: - Used for searching an entry in VLAN table.
30:24	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
23	VLANFPS[3]	R-F	0B	VLAN Filtering Priority Search (MSB) Update Conditions: - HW: FWVLANTSRO.VLANTS clear event. Functions: - Used for searching an entry in VLAN table.
22:20	VLANFPS[2:0]	R-D	0B	VLAN Filtering Priority Search Update Conditions: - HW: FWVLANTSRO.VLANTS clear event. Functions: Used for searching an entry in VLAN table.
19	VLANRPS[3]	R-F	0B	VLAN Routing Priority Search (MSB) Update Conditions: - HW: FWVLANTSRO.VLANTS clear event. Functions: Used for searching an entry in VLAN table.
18:16	VLANRPS[2:0]	R-D	0B	VLAN Routing Priority Search Update Conditions: - HW: FWVLANTSRO.VLANTS clear event. Functions: Used for searching an entry in VLAN table.
15:13	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
12	VLANBLS	R-D	0B	VLAN Block List Search Update Conditions: - HW: FWVLANTSRO.VLANTS clear event. Functions: - Used for searching an entry in VLAN table.
11	RSV	R0-U	0H	- Reserved area. On read, 0 will be returned

10	VLANHLD\$	R-D	0B	<p>VLAN (Source MAC) Hardware Learning Disable Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWVLANTS\$R0.VLANTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in VLAN table.
9	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
8	VLANSLS	R-F	0B	<p>VLAN Security Level Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWVLANTS\$R0.VLANTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in VLAN table.
7:2	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
1	VLANSNF	R-D	0B	<p>VLAN Search Not found</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: VLAN found in VLAN Table. - 1'b1: VLAN not found in VLAN Table. <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWVLANTS\$R0.VLANTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in VLAN table. <p>Security restrictions:</p> <ul style="list-style-type: none"> - The unsecure APB interface cannot find an entry with security level bit set in the VLAN table.
0	VLANSEF	R-D	0B	<p>VLAN Search ECC Fail</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Entry Search didn't fail because of an ECC error. - 1'b1: Entry Search failed because of an ECC error. <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWVLANTS\$R0.VLANTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in VLAN table.

(59) FWVLANTS1

Forwarding Engine VLAN Table Search Result 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VLANMSDUNS	RSV												VLANMSDUNS [PSFP_MSDU_W-1:0]		
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VLANGATEVS	RSV												VLANGATEVS [PSFP_GATE_W-1:0]		

Bits	Bit name	RW-P	Initial value	Function description
31	VLANMSDUVS	R-D	0B	VLAN MSDU Valid Search Update Conditions: - HW: FWVLANTS1.VLANTS clear event. Functions: - Used for searching an entry in VLAN table.
30: PSFP_MSDU_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PSFP_MSDU_W+15:16	VLANMSDUNS	R-D	0B	VLAN MSDU Number Search Functions: Update Conditions: - HW: FWVLANTS1.VLANTS clear event. Functions: - Used for searching an entry in VLAN table.
15	VLANGATEVS	R-D	0B	VLAN GATE Valid Search Update Conditions: - HW: FWVLANTS1.VLANTS clear event. Functions: - Used for searching an entry in VLAN table.
15:PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PSFP_GATE_W-1:0	VLANGATENS	R-D	0B	VLAN GATE Number Search Functions: Update Conditions: - HW: FWVLANTS1.VLANTS clear event. Functions: - Used for searching an entry in VLAN table.

(60) FWVLANTS2

Forwarding Engine VLAN Table Search Result 2

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VLANM TRVS	RSV									VLANMTRNS[PSFP_MTR_W+15:16]					
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VLANFR ERVS	RSV									VLANFRERNS[FRER_RECE_W-1:0]					

Bits	Bit name	RW-P	Initial value	Function description
31	VLANMTRVS	R-D	0B	VLAN Meter Valid Search Update Conditions: - HW: FWVLANTS2.VLANTS clear event. Functions: - Used for searching an entry in VLAN table.
30: PSFP_MTR_W+15+1	RSV	RO-U	0H	Reserved area. On read, 0 will be returned
PSFP_MTR_W+15:16	VLANMTRNS	R-D	0B	VLAN Meter Number Search Update Conditions: - HW: FWVLANTS2.VLANTS clear event. Functions: - Used for searching an entry in VLAN table.
15	VLANFRERVS	R-D	0B	VLAN FRER Valid Search Update Conditions: - HW: FWVLANTS2.VLANTS clear event. Functions: - Used for searching an entry in VLAN table.
14: FRER_RECE_W+16	RSV	RO-U	0H	Reserved area. On read, 0 will be returned
FRER_RECE_W-1:0	VLANFRERNS	R-D	0B	VLAN FRER Number Search Update Conditions: - HW: FWVLANTS2.VLANTS clear event. Functions: - Used for searching an entry in VLAN table.

(61) FWVLANTSRS3

Forwarding Engine VLAN Table Search Result 3

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV / VLANSLVS[PORT_N:1:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VLANR VS	RSV				VLANRNS[LTH_RRULE_W:1:0]										

Bits	Bit name	RW-P	Initial value	Function description
31: PORT_N+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PORT_N+15:16	VLANSLVS	R-D	0H	<p>VLAN Source Lock Vector Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWVLANTSRS0.VLANTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in VLAN table.
15	VLANRVS	R-D	0B	<p>VLAN Routing Valid Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWVLANTSRS0.VLANTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in VLAN table.
14: LTH_RRULE_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
LTH_RRULE_W:1:0	VLANRNS	R-D	0B	<p>VLAN Routing Number Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWVLANTSRS0.VLANTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in VLAN table.

(62) FWVLANTS4

Forwarding Engine VLAN Table Search Result 4

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / VLANFMVS[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PORT_N-1:0	VLANFMVS	R-D	0H	<p>VLAN Forwarding Mask Vector Search</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWVLANTS4.VLANTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in VLAN table.

(63) FWVLANTSRSR5i (i=0..PORT_GWCA_N-1)

Forwarding Engine VLAN Table Search Result 5 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / VLANCSDSi[AXI_CHAIN_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: AXI_CHAIN_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
AXI_CHAIN_W-1:0	VLANCSDSi	R-D	0B	<p>VLAN CPU Sub-Destination Search i</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWVLANTSRSR0.VLANTS clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used for searching an entry in VLAN table.

(64) FWVLANTS6

Forwarding Engine VLAN Table Search Result 6

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV										VLANC MES	VLAN EMES	VLANI PUS	VLANIPVS[2:0]		
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / VLANDVS[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description			
31:22	RSV	R0-U	0H	Reserved area. On read, 0 will be returned			
21	VLANCMES	R-D	0B	VLAN CPU Mirroring Enable Search Update Conditions: - HW: FWVLANTS6.VLANTS clear event. Functions: - Used for searching an entry in VLAN table.			
20	VLANEMES	R-D	0B	VLAN Ethernet Mirroring Enable Search Update Conditions: - HW: FWVLANTS6.VLANTS clear event. Functions: - Used for searching an entry in VLAN table.			
19	VLANIPUS	R-D	0B	VLAN Internal Priority Update Search Update Conditions: - HW: FWVLANTS6.VLANTS clear event. Functions: - Used for searching an entry in VLAN table.			
18:16	VLANIPVS	R-D	0B	VLAN Internal Priority Value Search Update Conditions: - HW: FWVLANTS6.VLANTS clear event. Functions: - Used for searching an entry in VLAN table.			
15:PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned			
PORT_N-1:0	VLANDVS	R-D	0B	VLAN Destination Vector Search Update Conditions: - HW: FWVLANTS6.VLANTS clear event. Functions: - Used for searching an entry in VLAN table.			

3.3.1.8 Port based forwarding function registers

(1) FWPBFC0i (i=0..PORT_N-1)

Forwarding Engine Port Based Forwarding Configuration 0 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV					FAIFPi	IP6PDEi	IP4PDMi	IP4PDEi	PBSLi	PBCMEi	PBEMEi	PBIPUi	PBIPVi[2:0]		
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / PBDVi[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:27	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
26	FAIFPi	RW-P	0H	<p>Force All Input Frame Priority i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: For port i, Input frame priority is given by frame decoding. - 1'b1: For port i, Input frame priority is forced to FWPBFC0i.PBIPVi
25	IP6PDEi	RW-P	0H	<p>IPv6 Priority Decode Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: For port i, Input frame priority is taken from VLAN TAGs. - 1'b1: For port i , If an IPv6 frame is detected, input frame priority is decoded from DSCP field in ToS. Else Input frame priority is taken from VLAN TAGs.
24	IP4PDMi	RW-P	0H	<p>IPv4 Priority Decode Mode i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: For port i, Input frame priority is taken from precedent field in ToS. - 1'b1: For port i, Input frame priority is decoded from DSCP field in ToS.
23	IP4PDEi	RW-P	0H	<p>IPv4 Priority Decode Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: For port i, Input frame priority is taken from VLAN TAGs for port i. - 1'b1: For port i, If an IPv4 frame is detected, input frame priority is taken from precedence ToS. Else Input frame priority is taken from VLAN TAGs.
22	PBSLi	RW-RP	0H	<p>Port Based Security Level i.</p> <p>Functions:</p> <ul style="list-style-type: none"> - Set descriptor security level for port i.
21	PBCMEi	RW-P	0H	<p>Port Based CPU Mirroring Enabled i.</p> <p>Functions:</p> <ul style="list-style-type: none"> - Enables CPU mirroring for port i.
20	PBEMEi	RW-P	0H	<p>Port Based Ethernet Mirroring Enabled i.</p> <p>Functions:</p> <ul style="list-style-type: none"> - Enables ethernet mirroring for port i.
19	PBIPUi	RW-P	0H	<p>Port Based Internal Priority Update i</p> <p>Functions:</p> <ul style="list-style-type: none"> - Enables frame priority update to internal priority value (FWPBFC0i.PBIPVi) for port i.
18:16	PBIPVi	RW-P	0H	<p>Port Based Internal Priority Value i.</p> <p>Functions:</p> <ul style="list-style-type: none"> - Internal priority value for port i port-based forwarding.

15:PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
POR T_N-1:0	PBDVi	RW-P	0H	<p>Port Based Destination Vector i.</p> <p>Functions:</p> <ul style="list-style-type: none">- Destination vector for port i port-based forwarding.- Setting this register to 0 disables port-based forwarding for port i.

(2) FWPBFC1i (i=0..PORT_N-1)

Forwarding Engine Port Based Forwarding Configuration 1 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV												PBRPi[3:0]			
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV					PBHLDi	RSV									

Bits	Bit name	RW-P	Initial value	Function description
31:20	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
19	PBRPi[3]	RW-RP	0B	Port Based forwarding Routing Priority (MSB) i Functions: - Routing priority value for port based forwarding.
18:16	PBRPi[2:0]	RW-P	0B	Port Based forwarding Routing Priority i Functions: - Routing priority value for port based forwarding.
15:11	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
10	PBHLDi	RW-P	0B	Port based forwarding (Source MAC) Hardware Learning Disable i Functions: - This function disables Source MAC address hardware learning with Port based forwarding.
9:0	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.

(3) FWPBFCSDC_{ji} (j=0..PORT_GWCA_N-1)(i=0..PORT_N-1)

Forwarding Engine Port Based Forwarding CSD Configuration j i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / PBCSD _{ji} [AXI_CHAIN_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:AXI_CHAIN_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
AXI_CHAIN_W-1:0	PBCSD _{ji}	RW-P	0H	Port Based CPU Sub Destination j i. Functions: - CPU Sub Destination for GWCA _j [GWCA] for port i port-based forwarding.

3.3.1.9 Layer2/Layer 3 update function registers

(1) FWL23URL0

Forwarding Engine Layer2/Layer3 Update Rule Learn 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV / L23URPVL[PORT_N-1:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV					L23URNL[LTH_RRULE_W-1:0]										

Bits	Bit name	RW-P	Initial value	Function description
31: PORT_N+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PORT_N+15:16	L23URPVL	RW-D	0B	Layer2/Layer3 Update Routing destination Port Valid Learn Functions: - Used to learn a Layer2/Layer3 update rule
15: LTH_RRULE_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
LTH_RRULE_W-1:0	L23URNL	RW-D	0B	Layer2/Layer3 Update Routing rule Number Learn Functions: - Used to learn a Layer2/Layer3 update rule

(2) FWL23URL1

Forwarding Engine Layer2/Layer3 Update Rule Learn 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV	L23UTCL[2:0]				L23URTUL [1:0]	L23USDE IUL	L23USPC PUL	L23USVI DUL	L23UCDE IUL	L23UCPC PUL	L23UCVI DUL	L23UMSA UL	L23UMD AUL	L23UTTL UL	
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L23UMDALP0[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:30	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
29:27	L23UTCL	RW-D	0B	Layer2/Layer3 Update TAG Configuration for tagging/un-tagging Learn Functions: - Used to learn a Layer2/Layer3 update rule
26:25	L23URTUL	RW-D	0B	Layer2/Layer3 Update R-TAG Update Learn Functions: - Used to learn a Layer2/Layer3 update rule
24	L23USDEIUL	RW-D	0B	Layer2/Layer3 Update S-TAG DEI Update Learn Functions: - Used to learn a Layer2/Layer3 update rule
23	L23USPCPUL	RW-D	0B	Layer2/Layer3 Update S-TAG PCP Update Learn Functions: - Used to learn a Layer2/Layer3 update rule
22	L23USVIDUL	RW-D	0B	Layer2/Layer3 Update S-TAG VID Update Learn Functions: - Used to learn a Layer2/Layer3 update rule
21	L23UCDEIUL	RW-D	0B	Layer2/Layer3 Update C-TAG DEI Update Learn Functions: - Used to learn a Layer2/Layer3 update rule
20	L23UCPCPUL	RW-D	0B	Layer2/Layer3 Update C-TAG PCP Update Learn Functions: - Used to learn a Layer2/Layer3 update rule
19	L23UCVIDUL	RW-D	0B	Layer2/Layer3 Update C-TAG VID Update Learn Functions: - Used to learn a Layer2/Layer3 update rule
18	L23UMSAUL	RW-D	0B	Layer2/Layer3 Update MAC Source Address Update Learn Functions: - Used to learn a Layer2/Layer3 update rule
17	L23UMDAUL	RW-D	0B	Layer2/Layer3 Update MAC Destination Address Update Learn Functions: - Used to learn a Layer2/Layer3 update rule
16	L23UTTLUL	RW-D	0B	Layer2/Layer3 Update Time To Live Update Learn Functions: - Used to learn a Layer2/Layer3 update rule

15:0	L23UMDALP0	RW-D	0B	Layer2/Layer3 Update MAC Destination Address Learn Part 0 Functions: - Used to learn a Layer2/Layer3 update rule
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(3) FWL23URL2

Forwarding Engine Layer2/Layer3 Update Rule Learn 2

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
L23UMDALP1[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L23UMDALP1[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	L23UMDALP1	RW-D	0B	Layer2/Layer3 Update MAC Destination Address Learn Part 1 Functions: - Used to learn a Layer2/Layer3 update rule

(4) FWL23URL3

Forwarding Engine Layer2/Layer3 Update Rule Learn 3

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
L23USD EIL	L23USPCPL[2:0]		L23USVIDL[11:0]													
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
L23UC DEIL	L23UCPCPL[2:0]		L23UCVIDL[11:0]													

Bits	Bit name	RW-P	Initial value	Function description
31	L23USDEIL	RW-D	0B	Layer2/Layer3 Update S-TAG DEI Learn Functions: - Used to learn a Layer2/Layer3 update rule
30:28	L23USPCPL	RW-D	0B	Layer2/Layer3 Update S-TAG PCP Learn Functions: - Used to learn a Layer2/Layer3 update rule
27:16	L23USVIDL	RW-D	0B	Layer2/Layer3 Update S-TAG VID Learn Functions: - Used to learn a Layer2/Layer3 update rule
15	L23UCDEIL	RW-D	0B	Layer2/Layer3 Update C-TAG DEI Learn Functions: - Used to learn a Layer2/Layer3 update rule
14:12	L23UCPCPL	RW-D	0B	Layer2/Layer3 Update C-TAG PCP Learn Functions: - Used to learn a Layer2/Layer3 update rule
11:0	L23UCVIDL	RW-D	0B	Layer2/Layer3 Update C-TAG VID Learn Functions: - Used to learn a Layer2/Layer3 update rule

(5) FWL23URLR

Forwarding Engine Layer2/Layer3 Update Rule Learn Result

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
L23UR L	RSV														
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RSV														

Bits	Bit name	RW-P	Initial value	Function description
31	L23URL	R-D	0B	<p>Layer2/Layer3 Update Rule Learn</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: Writing FWL23URL3 register will set this bit. <p>Clear conditions:</p> <ul style="list-style-type: none"> - HW: This bit will be de-asserted when learning is completed.
30:2	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
1	L23ULSF	R-D	0B	<p>Layer2/Layer3 Update Learn Security Fail</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Entry learning didn't fail because of a security error (refer to section 5.2.8.2). - 1'b1: Entry learning failed because of a security error (refer to section 5.2.8.2). <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWL23URLR.L23URL clear event. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: This register never gets set for the secure APB interface.
0	L23ULF	R-D	0B	<p>Layer2/Layer3 Update Learn Fail</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Entry learning didn't fail because the layer2/Layer3 table is ready. - 1'b1: Entry learning failed because the layer2/Layer3 table is not ready. <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWL23URLR.L23URL clear event.

(6) FWL23UTIM

Forwarding Engine Layer2/Layer3 Update Table Initialization Monitoring.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV															

Bits	Bit name	RW-P	Initial value	Function description
31:2	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
1	L23UTR	R-RP	0H	<p>Layer2/Layer3 Update Table Ready</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When FWL23UTIM.L23UTIOG is getting cleared. - HW: This bit is set at "clk_period[ns]* LTH_RRULE_N" time from L23 update table initialization starting. <p>Clear condition:</p> <ul style="list-style-type: none"> - SW: By writing 1 to FWL23UTIM.L23UTIOG.
0	L23UTIOG	R!=W-RP	0B	<p>Layer2/Layer3 Update Table Initialization Ongoing.</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - SW: By writing 1 to this register. It starts Layer2/Layer3 Update Table initialization. <p>Clear condition:</p> <ul style="list-style-type: none"> - HW: This bit is cleared when Layer2/Layer3 Update Table initialization is finished.

(7) FWL23URR

Forwarding Engine Layer2/Layer3 Update Rule Read

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV					L23RNR[LTH_RRULE_W-1:0]										

Bits	Bit name	RW-P	Initial value	Function description
31: LTH_RRULE_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
LTH_RRULE_W-1:0	L23RNR	RW-D	0B	<p>Layer2/Layer3 Routing Number Read</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used to read a Layer2/Layer3 update rule

(8) FWL23URRR0

Forwarding Engine Layer2/Layer3 Update Rule Read Result 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
L23UR R	RSV														L23UR EF
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / L23URPVR[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31	L23URR	R-D	0B	Layer2/Layer3 Update Rule Read Set conditions: - HW: Writing FWL23URR register will set this bit. Clear conditions: - HW: This bit will be de-asserted when reading is completed.
30:17	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
16	L23UREF	R-D	0B	Layer2/Layer3 Update Read ECC Fail Values: - 1'b0: Entry reading didn't fail because of an ECC error. - 1'b1: Entry reading failed because of an ECC error. Update Conditions: - HW: FWL23URRR0.L23URR clear event.
15:PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PORT_N-1:0	L23URPVR	R-D	0B	Layer2/Layer3 Update Routing destination Port Valid Read Update Conditions: - HW: FWL23RRR0.L23URR clear event. Functions: - Used to read a Layer2/Layer3 update rule

(9) FWL23URRR1

Forwarding Engine Layer2/Layer3 Update Rule Read Result 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV		L23UTCR[2:0]			L23URTUR [1:0]		L23USDE	L23USPC	L23USVI	L23UCDE	L23UCPC	L23UCVI	L23UMSA	L23UMD	L23UTTL
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L23UMDARP0[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:30	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
29:27	L23UTCR	R-D	0B	Layer2/Layer3 Update TAG Configuration for tagging/un-tagging Read Update Conditions: - HW: FWL23RRR0.L23URR clear event. Functions: - Used to read a Layer2/Layer3 update rule
26:25	L23URTUR	R-D	0B	Layer2/Layer3 R-TAG Update Read Update Conditions: - HW: FWL23RRR0.L23URR clear event. Functions: - Used to read a Layer2/Layer3 update rule
24	L23USDEIUR	R-D	0B	Layer2/Layer3 S-TAG DEI Update Read Update Conditions: - HW: FWL23RRR0.L23URR clear event. Functions: - Used to read a Layer2/Layer3 update rule
23	L23USPCPUR	R-D	0B	Layer2/Layer3 S-TAG PCP Update Read Update Conditions: - HW: FWL23RRR0.L23URR clear event. Functions: - Used to read a Layer2/Layer3 update rule
22	L23USVIDUR	R-D	0B	Layer2/Layer3 S-TAG VID Update Read Update Conditions: - HW: FWL23RRR0.L23URR clear event. Functions: - Used to read a Layer2/Layer3 update rule
21	L23UCDEIUR	R-D	0B	Layer2/Layer3 C-TAG DEI Update Read Update Conditions: - HW: FWL23RRR0.L23URR clear event. Functions: - Used to read a Layer2/Layer3 update rule
20	L23UCPCPUR	R-D	0B	Layer2/Layer3 C-TAG PCP Update Read Update Conditions: - HW: FWL23RRR0.L23URR clear event. Functions: - Used to read a Layer2/Layer3 update rule

19	L23UCVIDUR	R-D	0B	<p>Layer2/Layer3 C-TAG VID Update Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWL23RRR0.L23URR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used to read a Layer2/Layer3 update rule
18	L23UMSAUR	R-D	0B	<p>Layer2/Layer3 MAC Source Address Update Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWL23RRR0.L23URR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used to read a Layer2/Layer3 update rule
17	L23UMDAUR	R-D	0B	<p>Layer2/Layer3 MAC Destination Address Update Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWL23RRR0.L23URR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used to read a Layer2/Layer3 update rule
16	L23UTTLUR	R-D	0B	<p>Layer2/Layer3 Time To Live Update Read</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWL23RRR0.L23URR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used to read a Layer2/Layer3 update rule
15:0	L23UMDARPO	R-D	0B	<p>Layer2/Layer3 MAC Destination Address Read Part 0</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWL23RRR0.L23URR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used to read a Layer2/Layer3 update rule

(10) FWL23URRR2

Forwarding Engine Layer2/Layer3 Update Rule Read Result 2

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
L23UMDARP1[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L23UMDARP1[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	L23UMDARP1	R-D	0B	<p>Layer2/Layer3 Update MAC Destination Address Read Part 1</p> <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWL23RRR0.L23URR clear event. <p>Functions:</p> <ul style="list-style-type: none"> - Used to read a Layer2/Layer3 update rule

(11) FWL23URRR3

Forwarding Engine Layer2/Layer3 Update Rule Read Result 3

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
L23USD EIR	L23USPCPR[2:0]			L23USVIDR[11:0]											
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L23UC DEIR	L23UCPCPR[2:0]			L23UCVIDR[11:0]											

Bits	Bit name	RW-P	Initial value	Function description
31	L23USDEIR	R-D	0B	Layer2/Layer3 Update MAC S-TAG DEI Read Update Conditions: - HW: FWL23RRR0.L23URR clear event. Functions: - Used to read a Layer2/Layer3 update rule
30:28	L23USPCPR	R-D	0B	Layer2/Layer3 Update MAC S-TAG PCP Read Update Conditions: - HW: FWL23RRR0.L23URR clear event. Functions: - Used to read a Layer2/Layer3 update rule
27:16	L23USVIDR	R-D	0B	Layer2/Layer3 Update MAC S-TAG VID Read Update Conditions: - HW: FWL23RRR0.L23URR clear event. Functions: - Used to read a Layer2/Layer3 update rule
15	L23UCDEIR	R-D	0B	Layer2/Layer3 Update MAC C-TAG DEI Read Update Conditions: - HW: FWL23RRR0.L23URR clear event. Functions: - Used to read a Layer2/Layer3 update rule
14:12	L23UCPCPR	R-D	0B	Layer2/Layer3 Update MAC C-TAG PCP Read Update Conditions: - HW: FWL23RRR0.L23URR clear event. Functions: - Used to read a Layer2/Layer3 update rule
11:0	L23UCVIDR	R-D	0B	Layer2/Layer3 Update MAC C-TAG VID Read Update Conditions: - HW: FWL23RRR0.L23URR clear event. Functions: - Used to read a Layer2/Layer3 update rule

(12) FWL23URMCi (i=0..LTH_REMAP_N-1)

Forwarding Engine Layer2/Layer3 Update ReMapping Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV		RMEi	RSV	RMNRNi[LTH_RRULE_W-1:0]											
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / RMSPNi[PORT_W-1:0]				RSV	RMRNi[LTH_RRULE_W-1:0]										

Bits	Bit name	RW-P	Initial value	Function description
31:29	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
28	RMEi	R!=W-P	0B	<p>ReMapping Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Remapping rule i disabled - 1'b1: Remapping rule i enabled <p>Set conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1'b1 to this register will set it.
27:LTH_RRULE_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
LTH_RRULE_W+15:16	RMNRNi	RW-P	0B	<p>ReMapping New routing Rule Number i</p> <p>Functions:</p> <ul style="list-style-type: none"> - Set the rule number to which routing should be remapped for remapping rule i
15: PORT_W+12	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PORT_W+11:12	RMSPNi	RW-P	0B	<p>ReMapping Source Port Number i</p> <p>Functions:</p> <ul style="list-style-type: none"> - Set the port number for which rule number should be remapped for remapping rule i
11: LTH_RRULE_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
LTH_RRULE_W-1:0	RMRNi	RW-P	0B	<p>ReMapping routing Rule Number i</p> <p>Functions:</p> <ul style="list-style-type: none"> - Set the rule number that should be remapped for remapping rule i

3.3.1.10 PSFP (Per Stream Filtering and Policing) [802.1Qci]

(1) FWPMFGCi (i=0..PSFP_MSDU_N-1)

Forwarding Engine PSFP MSDU Filter Global Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MFMi	RSV														
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSDUVi[FRM_TPL_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31	MFMi	RW-P	0B	<p>MSDU Filter Mode i Values:</p> <ul style="list-style-type: none"> - 1'b0: Normal mode: Any frame linked to MSDU filter i thanks to L3 table received with LDESCR.TPL [GWCA] bigger than FWPMFGCi.MSDUVi will be filtered. - 1'b1: Throttle mode: Any frame linked to MSDU filter i thanks to L3 table received with LDESCR.TPL [GWCA] bigger than FWPMFGCi.MSDUVi will be filtered. Any frame linked to MSDU filter i thanks to L3 table received when FWEIS2.PMFS[i] is set will be filtered.
30: FRM_TPL_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
FRM_TPL_W-1:0	MSDUVi	RW-P	0B	<p>MSDU Value i Functions:</p> <ul style="list-style-type: none"> - HW: Maximum frame size for stream linked to MSDU filter i thanks to L3 table.

(2) FWPGFCi (i=0..PSFP_GATE_N-1)

Forwarding Engine PSFP Gate Filter Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV								GFCAi[GATE_RAM_AW-1:0]							
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV								GFTSi				RSV			

Bits	Bit name	RW-P	Initial value	Function description
31: GATE_RAM_AW+16	RSV	RO-U	0H	Reserved area. On read, 0 will be returned
GATE_RAM_AW+15:16	GFCAi	R-S	PSFP_GENTR Y_N*i	Gate filter Configuration Address i Functions: - Shows the address from which entry learning should happen in Gate RAM for the next configuration for gate number i.
15: PTP_TN_W+8	RSV	RO-U	0H	Reserved area. On read, 0 will be returned
PTP_TN_W+7:8	GFTSi	RW-S	0H	Gate Filter Timer Select i Functions: - Selects the gPTP that will be used for Gate filter module for gate number i.
7:3	RSV	RO-U	0H	Reserved area. On read, 0 will be returned
2	GFCl	R-S	0H	Gate Filter Config Impossible i Values: - 1'b0: Gate Filter configuration possible for gate number i - 1'b1: Gate Filter configuration is not possible for gate number i Functions: - This bit helps the SW to know when Gate filter configuration is possible for gate number i, it is equal to (FWPGFCi.GFEi & ~FWPGFSMi.GFSOi) FWPGFCi.GFCCi.
1	GFCCi	R!=W-S	0H	Gate Filter Config Change i Values: - 1'b0: Gate number i is not changing configuration - 1'b1: Gate number i is changing configuration Set conditions: - SW: Writing 1 to this bit will set it Clear conditions: - HW: This bit will be cleared when Gate Filter configuration change is done for gate number i. Refer to section 5.3.1.2(1)
0	GFEi	RW-S	0H	Gate Filter enable i Values: - 1'b0: Gate Filter disabled for gate number i - 1'b1: Gate Filter enabled for gate number i Functions: - Enables the Gate Filter schedule for gate number i

(3) FWPGFIGSci (i=0..PSFP_GATE_N-1)

Forwarding Engine PSFP Gate Filter Initial Gate State Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV												GFIGSi[3:0]			

Bits	Bit name	RW-P	Initial value	Function description
31: 4	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
3:0	GFIGSi	RW-S	0H	<p>Gate Filter Initial Gate State i</p> <p>Functions:</p> <ul style="list-style-type: none"> - Bit 0 represents the gate status. If equal to 1'b0, the gate state is closed and if equal to 1'b1 the gate is opened. - Bit [3:1] represents the IPV value of the associated gate.

(4) FWPGFENCi (i=0..PSFP_GATE_N-1)

Forwarding Engine PSFP Gate Filter Entry Number Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV												GFAENi[PSFP_GENTRY_W1:0]			

Bits	Bit name	RW-P	Initial value	Function description
31: PSFP_GENTRY_W1	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PSFP_GENTRY_W1:0	GFAENi	RW-S	0H	<p>Gate Filtering Entry Number for gate i</p> <p>Functions:</p> <ul style="list-style-type: none"> - This register is only used to configure Gate filter i and is not directly used by Gate filtering module. - Sets the number of entries used by gate i schedule in gate RAM. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: This register maximum value is PSFP_GENTRY_N-1. - SW: If Gate filter is used in dynamic (Gate i setting flow is used when FWPGFCi.GFEi is already set), the sum of FWPGFENCi.GFAENi should be smaller or equal to PSFP_GENTRY_N/2 - 1. - SW: If Gate filter is used in static (Gate i setting flow is never used when FWPGFCi.GFEi is already set), the sum of FWPGFENCi.GFAENi should be smaller or equal to PSFP_GENTRY_N - 1.

(5) FWPGFENMi (i=0..PSFP_GATE_N-1)

Forwarding Engine PSFP Gate Filter Entry Number Monitoring i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV										GFOENi[PSFP_GENTRY_W1:1:0]					

Bits	Bit name	RW-P	Initial value	Function description
31: PSFP_GENTRY_W1	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
PSFP_GENTRY_W1-1:0	GFOENi	R-S	0H	<p>Gate Filter Oper Entry Number for gate i</p> <p>Update conditions:</p> <ul style="list-style-type: none"> - HW: This register is updated to FWPGFENCi.GFAENi when configuration change occurs or when schedule start occurs. Refer to section 5.3.1.2(1)

(6) FWPGFCSTC0i (i=0..PSFP_GATE_N-1)

Forwarding Engine PSFP Gate Filter Cycle Start Time Configuration 0 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GFACSTP0i[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GFACSTP0i[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	GFACSTP0i	RW-S	0H	<p>Gate Filter Admin Cycle Start Time Part 0 i</p> <p>Functions:</p> <ul style="list-style-type: none"> - Time at which Gate Filter scheduler i should start/change configuration - This register is in ns.

(7) FWPGFCSTC1i (i=0..PSFP_GATE_N-1)

Forwarding Engine PSFP Gate Filter Cycle Start Time Configuration 1 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GFACSTP1i[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GFACSTP1i[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	GFACSTP1i	RW-S	0H	<p>Gate Filter Admin Cycle Start Time Part 1</p> <p>Functions:</p> <ul style="list-style-type: none"> - Time at which Gate Filter scheduler i should start/change configuration - This register is in $2^{32} \times ns$.

(8) FWPGFCSTM0i (i=0..PSFP_GATE_N-1)

Forwarding Engine PSFP Gate Filter Cycle Start Time Monitoring 0 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GFOCSTP0i[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GFOCSTP0i[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	GFOCSTP0i	R-S	0H	<p>Gate Filter Oper Cycle Start Time Part 0 i</p> <p>Update conditions:</p> <ul style="list-style-type: none"> - HW: {FWPGFCSTM1i,FWPGFCSTM0i} is updated to {FWPGFCSTC1i,FWPGFCSTC0i} + FWPGFCTCi This register is updated to FWPGFCSTC0i.GFACSTP0i when (before 1 clock cycle) configuration change occurs or when (before 1 clock cycle) schedule start occurs for gate filter i. Refer to section 5.3.1.2(1) - HW: This register is updated to the next cycle start time every time a new cycle starts.

(9) FWPGFCSTM1i (i=0..PSFP_GATE_N-1)

Forwarding Engine PSFP Gate Filter Cycle Start Time Monitoring 1 i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GFOCSTP1i[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GFOCSTP1i[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	GFOCSTP1i	R-S	0H	<p>Gate Filter Oper Cycle Start Time Part 1 i</p> <p>Update conditions:</p> <ul style="list-style-type: none"> - HW: This register is updated to FWPGFCSTC1i.GFACSTP1i when configuration change occurs or when schedule start occurs for gate filter i. Refer to section 5.3.1.2(1) - HW: This register is updated to the next cycle start time every time a new cycle starts.

(10) FWPGFCTCi (i=0..PSFP_GATE_N-1)

Forwarding Engine PSFP Gate Filter Cycle Time Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GFACTi[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GFACTi[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	GFACTi	RW-S	0H	<p>Gate Filter Admin Cycle Time i</p> <p>Functions:</p> <ul style="list-style-type: none"> - Configure the cycle time for Gate filter i

(11) FWPGFCTMi (i=0..PSFP_GATE_N-1)

Forwarding Engine PSFP Gate Filter Cycle Time Monitoring i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GFOCTi[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GFOCTi[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	GFOCTi	R-S	0H	<p>Gate Filter Oper Cycle Time i</p> <p>Update conditions:</p> <ul style="list-style-type: none"> - HW: This register is updated to FWPGFCTCi.GFACTi when (before 1 clock cycle) configuration change occurs or when (before 1 clock cycle) schedule start occurs. <p>Refer to section 5.3.1.2(1)</p>

(12) FWPGFHCC_i (i=0..PSFP_GATE_N-1)

Forwarding Engine PSFP Gate Filter Hardware Calibration Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GFJ _i [15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
15:0	GFJ _i	RW-S	0H	<p>Gate Filter Jitter i</p> <p>Functions:</p> <ul style="list-style-type: none"> - Configure the jitter between the data reception on the RMAC PHY interface [RMAC] and the GF module. - Refer to section 5.3.1.2(2)

(13) FWPGFSMi (i=0..PSFP_GATE_N-1)

Forwarding Engine PSFP Gate Filter Status Monitoring i.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															GFSOi
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV															GFGSi[3:0]

Bits	Bit name	RW-P	Initial value	Function description
31:17	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
16	GFSOi	R-S	0H	<p>Gate Filter Scheduler Ongoing i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Gate Filter Scheduler is not ongoing for gate filter i - 1'b1: Gate Filter Scheduler is ongoing for gate filter i
15:4	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
3:0	GFGSi	R-S	All1	<p>Gate Filter Gate State i</p> <p>Functions:</p> <ul style="list-style-type: none"> - Bit 0 represents the gate status. If equal to 1'b0, the gate state is closed and if equal to 1'b1 the gate is opened. - Bit [3:1] represents the IPV value of the associated gate.

(14) FWPGFGCi (i=0..PSFP_GATE_N-1)

Forwarding Engine PSFP Gate Filter Global Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV															

Bits	Bit name	RW-P	Initial value	Function description
31:2	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
1	GIPVUEi	RW-P	0B	<p>Gate IPV Update Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: IPV update disabled. - 1'b1: IPV update enabled. Any frame linked to Gate filter i thanks to L3 table received will have its IPV updated to the value given by the PSFP Gate Scheduler.
0	GFMi	RW-P	0B	<p>Gate Filter Mode i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Normal mode: Any frame linked to Gate filter i thanks to L3 table received with at least a beat of data during a closed gate will be filtered. - 1'b1: Throttle mode: Any frame linked to Gate filter i thanks to L3 table received with at least beat of data during a closed gate will be filtered. Any frame linked to Gate filter i thanks to L3 table received when FWEIS3.PGFS is set will be filtered.

(15) FWPGFGL0

Forwarding Engine PSFP Gate Filter Gate Learn 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV								GFGAL[GATE_RAM_AW:1:0]							

Bits	Bit name	RW-P	Initial value	Function description
31: GATE_RAM_AW	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
GATE_RAM_AW:1: 0	GFGAL	RW-D	0H	Gate Filter Gate Address Learn Functions: - Configures the address in which the Gate entry will be learnt

(16) FWPGFGL1

Forwarding Engine PSFP Gate Filter Learn 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GFGSL[3:0]				GFGTL[27:16]											
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GFGTL[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:28	GFGSL	RW-D	0H	<p>Gate Filter Gate State Learn</p> <p>Functions:</p> <ul style="list-style-type: none"> - Configures gate state - Bit 0 represents the gate status. If equal to 1'b0, the gate state is closed and if equal to 1'b1 the gate is opened. - Bit [3:1] represents the IPV value of the associated gate.
27:0	GFGTL	RW-D	0H	<p>Gate Filter Gate Time Learn</p> <p>Functions:</p> <ul style="list-style-type: none"> - Configures gate time

(17) FWPGFGLR

Forwarding Engine PSFP Gate Filter Learn Result

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GL	RSV														
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RSV														

Bits	Bit name	RW-P	Initial value	Function description
31	GL	R-D	0B	<p>Gate Learn</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: Writing FWPGFGL1 register will set this bit. <p>Clear conditions:</p> <ul style="list-style-type: none"> - HW: This bit will be de-asserted when learning is completed.
30:1	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
0	GLSF	R-D	0H	<p>Gate Learning Security Fail</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Entry learning didn't fail because of a security error. - 1'b1: Entry learning failed because of a security error. <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWPGFGLR.GL clear event clear event.

(18) FWPGFGR

Forwarding Engine PSFP Gate Filter Gate Read

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV								GFGAR[GATE_RAM_AW-1:0]							

Bits	Bit name	RW-P	Initial value	Function description
31:GATE_RAM_AW	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
GATE_RAM_AW-1: 0	GFGAR	RW-D	0H	<p>Gate Filter Gate Address Read</p> <p>Functions:</p> <ul style="list-style-type: none"> - Configures the address in which the Gate entry will be read

(19) FWPGFGR0

Forwarding Engine PSFP Gate Filter Read Result 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GR	RSV														
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RSV														

Bits	Bit name	RW-P	Initial value	Function description
31	GR	R-D	0B	<p>Gate Read</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: Writing FWPGFGR register will set this bit. <p>Clear conditions:</p> <ul style="list-style-type: none"> - HW: This bit will be de-asserted when reading is completed.
30:1	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
0	GFREF	R-D	0H	<p>Gate Filter Read ECC Fail</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Entry read didn't fail because of an ECC error. - 1'b1: Entry read failed because of an ECC error. <p>Update conditions:</p> <ul style="list-style-type: none"> - FWPGFGR0.GR clear event

(20) FWPGFGR1

Forwarding Engine PSFP Gate Filter Read Result 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GFGSR[3:0]				GFGTR[27:16]											
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GFGTR[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:28	GFGSR	R-D	0H	<p>Gate Filter Gate State Read</p> <p>Update conditions:</p> <ul style="list-style-type: none"> - FWPGFGR0.GR clear event <p>Functions:</p> <ul style="list-style-type: none"> - Displays gate state read value. - Bit 0 represents the gate status. If equal to 1'b0, the gate state is closed and if equal to 1'b1 the gate is opened. - Bit [3:1] represents the IPV value of the associated gate.
27:0	GFGTR	R-D	0H	<p>Gate Filter Gate Time Read</p> <p>Update conditions:</p> <ul style="list-style-type: none"> - FWPGFGR0.GR clear event <p>Functions:</p> <ul style="list-style-type: none"> - Displays gate time read value.

(21) FWPGFRIM

Forwarding Engine PSFP Gate Filter RAM Initialization Monitoring.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV															
														GFRR	GFRIOG

Bits	Bit name	RW-P	Initial value	Function description
31:2	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
1	GFRR	R-RP	0H	<p>Gate Filter RAM Ready</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When FWPGFRIM.GFRIOG is getting cleared. - HW: This bit is set at "clk_period[ns]* GATE_RAM_DP" time from gate filter RAM initialization starting. <p>Clear condition:</p> <ul style="list-style-type: none"> - SW: By writing 1 to FWPGFRIM.GFRIOG.
0	GFRIOG	R!=W-RP	0B	<p>Gate Filter RAM Initialization Ongoing.</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - SW: By writing 1 to this register. It starts Gate Filter RAM initialization. <p>Clear condition:</p> <ul style="list-style-type: none"> - HW: This bit is cleared when Gate Filter RAM initialization is finished. <p>Notes:</p> <ul style="list-style-type: none"> - This process is required only once during initialization. This process cannot complete with Gate Filter already enabled (FWPGFCi.GFEi == 1'b1).

(22) FWPMTRFCi (i=0..PSFP_MTR_N-1)

Forwarding Engine PSFP MeTeR Filter Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MTRCMi[15:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV												MTRC Fi	MTRF RFDi	MTRFMi[1:0]	MTRF Ei

Bits	Bit name	RW-P	Initial value	Function description
31:16	MTRCMi	RW-P	0H	<p>MeTeR Color Mode i</p> <ul style="list-style-type: none"> - If bit j is set to 0: Incoming frame with {PCP,DEI} == j is coming as green (Green or yellow bucket can be used by the frame). - If bit j is set to 1: Incoming frame with {PCP,DEI} == j is coming as Yellow (Only yellow bucket can be used by the frame). <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: This register exists only in i=0..PSFP_DMTR_N-1 - SW: in ATS mode (FWPMTRFCi.MTRFMi set to 2'b10) or in ATS throttle mode (FWPMTRFCi.MTRFMi set to 2'b11) Color mode is not available so this register should be set to All0.
15:5	RSV	R0-	0H	Reserved area. On read, 0 will be returned
4	MTRCFi	RW-P	0B	<p>MeTeR Coupling Flag</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: When green bucket is full, CIR tokens are lost. - 1'b1: When green bucket is full, CIR tokens are added to the yellow bucket. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: This register exists only in i=0..PSFP_DMTR_N-1
3	MTRFRFDi	RW-P	0B	<p>MeTeR Filter Red Frame Drop</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Red frames are not dropped by meter i - 1'b1: Red frames are dropped by meter i
2:1	MTRFMi	RW-P	0B	<p>MeTeR Filter Mode i</p> <p>Values:</p> <ul style="list-style-type: none"> - 2'b00: Normal mode: Any frame linked to Meter filter i thanks to L3 table received when not enough token is available will be red. - 2'b01: Throttle mode: Any frame linked to Meter filter i thanks to L3 table received when not enough token is available or when FWEIS50/51/52/53.PMRFS[i] is set will be red. - 2'b10: ATS mode: Any frame linked to Meter filter i thanks to L3 table received when not enough token is available will be stored in ATS RAM until enough tokens are available. When enough tokens are available, frame will be forwarded as yellow or green. - 2'b11: ATS throttle mode: Any frame linked to Meter filter i thanks to L3 table received when not enough token is available will be stored in ATS RAM until enough tokens are available. When enough tokens are available, frame will be forwarded as yellow or green if FWEIS50/51/52/53.PMRFS[i] is not set and will be red if FWEIS50/51/52/53.PMRFS[i] is set.

0	MTRFEi	RW-P	0B	MeTeR Filter Enable i Values: - 1'b0: Meter i disabled (Pass through all frames.) - 1'b1: Meter i enabled (Reject target stream frames by meter filter.)
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(23) FWPMTRCBSci (i=0..PSFP_MTR_N-1)

Forwarding Engine PSFP MeTeR CBS Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															CBSi [FRM_TPL_W+1:16]
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CBSi[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: FRM_TPL_W+2	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
FRM_TPL_W+1:0	CBSi	RW-P	0B	CBSi Functions: - Maximum number of tokens (in bytes) contained in meter i green bucket.

(24) FWPMTRCIRCi (i=0..PSFP_MTR_N-1)

Forwarding Engine PSFP MeTeR CIR Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV														CIRi[19:16]	
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CIRi[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: 20	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
19:0	CIRi	RW-P	0B	<p>CIRi</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used to increment green token tokens when meter i green bucket is not full. - CIRi[19:16] is the credit increment in byte per clock and CIRi[15:0] is the credit increment in sub-byte per clock. <p>Cautions:</p> <ul style="list-style-type: none"> - SW: In ATS mode, setting this register to 0 or a value close to 0 would set corresponding queue to a very low throughput or could stuck the corresponding queue and lead to a queue overflow.

(25) FWPMTREBSCi (i=0..PSFP_DMTR_N-1)

Forwarding Engine PSFP MeTeR EBS Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															EBSi [FRM_TPL_W+1:16]
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EBSi[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: FRM_TPL_W+2	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
FRM_TPL_W+1:0	EBSi	RW-P	0B	EBSi Functions: - Maximum number of tokens (in bytes) contained in meter i yellow bucket.

(26) FWPMTREIRCi (i=0..PSFP_DMTR_N-1)

Forwarding Engine PSFP MeTeR EIR Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV														EIRi[19:16]	
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EIRi[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: 20	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
19:0	EIRi	RW-P	0B	<p>EIRi</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used to increment green token tokens when meter i yellow bucket is not full. - EIRi[19:16] is the credit increment in byte per clock and EIRi[15:0] is the credit increment in sub-byte per clock. <p>Cautions:</p> <ul style="list-style-type: none"> - SW: In ATS mode, setting this register to 0 or a value close to 0 would set corresponding queue to a very low throughput or could stuck the corresponding queue and lead to a queue overflow.

(27) FWPMTRFMi (i=0..PSFP_MTR_N-1)

Forwarding Engine PSFP MeTeR Filter Monitoring i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV												MTRARDNMNi[ATS_DESCR_W1:1:0]			
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV												MTRARDNi[ATS_DESCR_W1:1:0]			

Bits	Bit name	RW-P	Initial value	Function description
31: ATS_DESCR_W1+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
ATS_DESCR_W1+15:16	MTRARDNM Ni	RC-P	0H	<p>MeTeR ATS RAM Descriptor Number Maximum Number i</p> <p>Update conditions:</p> <ul style="list-style-type: none"> - SW: Reading this register update it to FWPMTRFMi.MTRARDNi value. - HW: When FWPMTRFMi.MTRARDNMNi < FWPMTRFMi.MTRARDNi, this register is updated to FWPMTRFMi.MTRARDNi value.
15: ATS_DESCR_W1	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
ATS_DESCR_W1:1:0	MTRARDNi	R-P	0H	<p>MeTeR ATS RAM Descriptor Number i</p> <p>Functions:</p> <ul style="list-style-type: none"> - Shown the number of descriptors in the ATS RAM for meter number i. <p>Increment conditions:</p> <ul style="list-style-type: none"> - A descriptor is received for meter i but there is already a descriptor in the ATS RAM for meter i or there is not even token available for the frame.

3.3.1.11 FRER (Frame Replication and Elimination for Reliability) [802.1CB]

(1) FWFTL0

Forwarding Engine FRER Table Learn 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV									FSRPL[FRER_RECE_W-1:0]						
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV									FEAL[FRER_RECE_W-1:0]						

Bits	Bit name	RW-P	Initial value	Function description
31:FRER_RECE_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
FRER_RECE_W+15:16	FSRPL	RW-D	0H	FRER Sequence Recovery Pointer Learn Functions: - Used to set an FRER entry in FRER RAM.
15: FRER_RECE_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
FRER_RECE_W-1:0	FEAL	RW-D	0H	FRER Entry Address Learn Functions: - Used to set an FRER entry in FRER RAM.

(2) FWFTL1

Forwarding Engine FRER Table Learn 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV						FSRRTL[9:0]									
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV						FSRP VL	FTNSL	RSV				FSHLL [FRER_HIST_LEN_W -1:0]			

Bits	Bit name	RW-P	Initial value	Function description
31:26	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
25:16	FSRRTL	RW-D	0H	FRER Sequence Recovery Remaining Ticks Learn Functions: - Used to set an FRER entry in FRER RAM.
15:10	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
9	FSRPVL	RW-D	0H	FRER Sequence Recovery Pointer Valid Learn Functions: - Used to set an FRER entry in FRER RAM.
8	FTNSL	RW-D	0H	FRER Take No Sequence Learn Functions: - Used to set an FRER entry in FRER RAM.
7: FRER_HIST_LEN_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
FRER_HIST_LEN_W-1:0	FSHLL	RW-D	0H	FRER Sequence History Length Learn Functions: - Used to set an FRER entry in FRER RAM. Restrictions: - SW: This register should never be set to a value bigger than FRER_HIST_LEN

(3) FWFTLR

Forwarding Engine FRER Table Learn Result

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FTL	RSV														
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RSV														

Bits	Bit name	RW-P	Initial value	Function description
31	FTL	R-D	0B	<p>FRER Table Learn</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: Writing FWFTL1 register will set this bit. <p>Clear conditions:</p> <ul style="list-style-type: none"> - HW: This bit will be de-asserted when learning is completed.
30:2	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
1	FLSF	R-D	0B	<p>FRER Learn Security Fail</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Entry learning didn't fail because of a security error (refer to section 5.3.2.3(2)(b)). - 1'b1: Entry learning failed because of a security error (refer to section 5.3.2.3(2)(b)). <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWFTLR.FTL clear event. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: This register never gets set for the secure APB interface.
0	FLF	R-D	0B	<p>FRER Learn Fail</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Entry learning didn't fail because the FRER RAM is ready. - 1'b1: Entry learning failed because the FRER RAM is not ready. <p>Update Conditions:</p> <ul style="list-style-type: none"> - HW: FWFTLR.FTL clear event.

(4) FWFTOC

Forwarding Engine FRER TimeOut Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV														TOOG	TOCE
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOT[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:18	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
17	TOOG	R-P	0H	<p>TimeOut OnGoing</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: TimeOut check is not ongoing - 1'b1: TimeOut check is ongoing
16	TOCE	RW-P	0H	<p>TimeOut Check Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: TimeOut check is disabled. - 1'b1: TimeOut check is enabled.
15:0	TOT	RW-P	0H	<p>TimeOut Time (ms)</p> <p>Functions:</p> <ul style="list-style-type: none"> - When timeout check is enabled (FWFTOC.TOCE set to 1'b1), timeout check will happen every FWFTOC.TOT milliseconds.

(5) FWFTOPC

Forwarding Engine FRER TimeOut Prescaler Configuration 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV						USP[9:0]									

Bits	Bit name	RW-P	Initial value	Function description
31:10	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
9:0	USP	RW-F	0H	<p>MicroSecond Prescaler</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used to creates an internal clock for aging at 1MHz to derive the Timeout 1kHz clock. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: This register should be set to the number of clocks clk contained in 1us.

(6) FWFTIM

Forwarding Engine FRER Table Initialization Monitoring.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV															
														FTR	FTIOP

Bits	Bit name	RW-P	Initial value	Function description
31:2	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
1	FTR	R-RP	0H	<p>FRER Table Ready</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When FWFTIM.FTIOP is getting cleared. - HW: This bit is set at "clk_period[ns]* FRER_RECE_N" time from buffer pool initialization starting. <p>Clear condition:</p> <ul style="list-style-type: none"> - SW: By writing 1 to FWFTIM.FTIOP.
0	FTIOP	R!=W-RP	0B	<p>FRER Table Initialization OnGoing.</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - SW: By writing 1 to this register. It starts FRER Table initialization. <p>Clear condition:</p> <ul style="list-style-type: none"> - HW: This bit is cleared when FRER Table initialization is finished.

(7) FWFTR

Forwarding Engine FRER Table Read

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV										FEAR[FRER_RECE_W-1:0]					

Bits	Bit name	RW-P	Initial value	Function description
31: FRER_RECE_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
FRER_RECE_W-1:0	FEAR	RW-D	0H	FRER Entry Address Read Functions: - Used to read an FRER entry in FRER RAM.

(8) FWFTRR0

Forwarding Engine FRER Table Read Result 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FTR	FTREF	RSV				FSRRTR[9:0]									
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV						FSRP	FTNS	RSV				FSHLR [FRER_HIST_LEN_W -1:0]			

Bits	Bit name	RW-P	Initial value	Function description
31	FTR	R-D	0B	FRER Table Read Set conditions: - HW: Writing FWFTR register will set this bit. Clear conditions: - HW: This bit will be de-asserted when reading is completed.
30	FTREF	R-D	0H	FRER Table Read ECC Fail Values: - 1'b0: Entry read didn't fail because of an ECC error. - 1'b1: Entry read failed because of an ECC error. Update conditions: - HW: FWFTLRR0.FTR clear event.
29:26	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
25:16	FSRRTR	R-D	0H	FRER Set Recovery Remaining Ticks Read Update conditions: - HW: FWFTLRR0.FTR clear event.
15:10	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
9	FSRPVR	R-D	0H	FRER Sequence Recovery Pointer Valid Read Update conditions: - HW: FWFTLRR0.FTR clear event.
8	FTNSR	R-D	0H	FRER Take No Sequence Read Update conditions: - HW: FWFTLRR0.FTR clear event.
7: FRER_HIST_LEN_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
FRER_HIST_LEN_W-1:0	FSHLR	R-D	0H	FRER Sequence History Length Read Update conditions: - HW: FWFTLRR0.FTR clear event.

(9) FWFTRR1

Forwarding Engine FRER Table Read Result 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV									FSRPR[FRER_RECE_W-1:0]						
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV	FSHR[FRER_HIST_LEN1-1:0]														

Bits	Bit name	RW-P	Initial value	Function description
31:FRER_RECE_W+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
FRER_RECE_W+15:16	FSRPR	R-D	0H	FRER Sequence Recovery Pointer Read Update conditions: - HW: FWFTLRR0.FTR clear event.
15:FRER_HIST_LEN1	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
FRER_HIST_LEN1-1:0	FSHR	R-D	0H	FRER Sequence History Read Update conditions: - HW: FWFTLRR0.FTR clear event.

(10) FWFTRR2

Forwarding Engine FRER Table Read Result 2

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV						FRRTR[9:0]									
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRSNR[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:26	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
25:16	FRRTR	R-D	0H	<p>FRER Recovery Remaining Ticks Read</p> <p>Update conditions:</p> <ul style="list-style-type: none"> - HW: FWFTLRR0.FTR clear event.
15:0	FRSNR	R-D	0H	<p>FRER Recovery Sequence Number Read</p> <p>Update conditions:</p> <ul style="list-style-type: none"> - HW: FWFTLRR0.FTR clear event.

(11) FWSEQNGCi (i=0.. LTH_SEQGN_N-1)

Forwarding Engine SEQuence Number Generation Configuration i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															SEQN GEi
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV					SEQNCRNi[LTH_RRULE_W-1:0]										

Bits	Bit name	RW-P	Initial value	Function description
31:17	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
16	SEQNCEi	RW-P	0H	<p>SEQuence Number Generation Emable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Sequence number generation disabled for routing number FWSEQNGCi.SEQNCRNi - 1'b1: Sequence number generation enabled for routing number FWSEQNGCi.SEQNCRNi
15: LTH_RRULE_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
LTH_RRULE_W-1:0	SEQNCRNi	RW-P	0H	<p>SEQuence Number Generation Routing Number i</p> <p>Functions:</p> <ul style="list-style-type: none"> - Specifies the routing number for which sequence number will be generated

(12) FWSEQNGMi (i=0.. LTH_SEQGN_N-1)

Forwarding Engine SEQuence Number Generation Monitoring i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEQNi[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
15:0	SEQNi	R-P	0H	<p>SEQuence Number i</p> <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: When FWSEQNGCi.SEQNGEi is set and a descriptor is forwarded with FDESCR.RV set and FDESCR.RN set to FWSEQNGCi.SEQNGRNi. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1'b1 to FWSEQNRC.SEQNR[i] will clear this register. <p>Functions:</p> <ul style="list-style-type: none"> - Displays the next sequence number to be appended to a descriptor for sequence number generation rule i

(13) FWSEQNRC

Forwarding Engine SEQuence Number Reset Configuration

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEQNR[LTH_SEQGN_N-1:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEQNR[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
LTH_SEQGN_N-1:0	SEQNR	R0W-P	0H	<p>SEQuence Number Generation Reset</p> <p>Functions:</p> <ul style="list-style-type: none"> - Writing 1'b1 to bit i of this register will reset to 0 the sequence generator number i counter

3.3.2 Forwarding Engine Counter registers

This section describes Forwarding Engine counter registers.

(1) FWCTFDCNi (i=0..PORT_TIME_N-1)

Forwarding Engine Cut-Through Forwarded Descriptor CouNter i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CTFDNi[COUNT_MED_W-1:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTFDNi[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
COUNT_MED_W-1:0	CTFDNi	RC-P	0H	<p>Cut-Through Forwarded Descriptor Number i</p> <p>Functions:</p> <ul style="list-style-type: none"> - This register counts the number of descriptors forwarded by Cut-Through forwarding from port i. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Reading this register clears it. <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: Incremented by 1 when a frame coming from port i is forwarded by Cut-Through Forwarding in store and forward mode and if this register has a value different than {{COUNT_MED_W}{1'b1}}. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: This register does not take in account the cut-through path of cut-through forwarding but only the store and forward path so, any frame forwarded in store and forward with cut-through (for at least one value of j, if FWCTTC0i.CTDVi[j] is set, FWCTTC0i.CTFMi[j] is also set) will be counted here.

(2) FWDDFDCNi (i=0..PORT_SLOW_N-1)

Forwarding Engine Direct Descriptor Forwarded Descriptor Counter

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DDFDNi[COUNT_MED_W-1:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDFDNi[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
COUNT_MED_W:0	DDFDNi	RC-P	0H	<p>Direct Descriptor Forwarded Descriptor Number i</p> <p>Functions:</p> <ul style="list-style-type: none"> - This register counts the number of descriptors forwarded by Direct Descriptor forwarding from port i+PORT_TIME_N. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Reading this register clears it. <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: Incremented by 1 when a frame coming from port i+PORT_TIME_N is forwarded by Direct Descriptor Forwarding and if this register has a value different than {{COUNT_MED_W}{1'b1}}.

(3) FWLTHFDCNi (i=0..PORT_N-1)

Forwarding Engine Layer 3 Forwarded Descriptor CouNter i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTHFDNi[COUNT_MED_W-1:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHFDNi[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
COUNT_MED_W:0	LTHFDNi	RC-P	0H	<p>Layer 3 Forwarded Descriptor Number i</p> <p>Functions:</p> <ul style="list-style-type: none"> - This register counts the number of descriptors forwarded by Layer 3 forwarding from port i. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Reading this register clears it. <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: Incremented by 1 when a frame coming from port i is forwarded by Layer 3 Forwarding and if this register has a value different than {{COUNT_MED_W}{1'b1}}. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: This register counts the frame selected by Layer 3 forwarding mechanism before PSFP/ATS and FRER filtering functions. Frame rejected by these filtering functions are still taken in account here.

(4) FWLTWFDCNi (i=0..PORT_N-1)

Forwarding Engine Layer 2 Forwarded Descriptor CouNter i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTWFDNi[COUNT_MED_W-1:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTWFDNi[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
COUNT_MED_W-1:0	LTWFDNi	RC-P	0H	<p>Layer 2 Forwarded Descriptor Number i</p> <p>Functions:</p> <ul style="list-style-type: none"> - This register counts the number of descriptors forwarded by Layer 2 forwarding from port i. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Reading this register clears it. <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: Incremented by 1 when a frame coming from port i is forwarded by Layer 2 Forwarding and if this register has a value different than {{COUNT_MED_W}{1'b1}}. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: This register counts the frame selected by Layer 2 forwarding mechanism before PSFP/ATS and FRER filtering functions. Frame rejected by these filtering functions are still taken in account here.

(5) FWFBFDNI (i=0..PORT_N-1)

Forwarding Engine Port Based Forwarded Descriptor Counter i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PBFDNI[i][COUNT_MED_W-1:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PBFDNI[i][15:0]															

Bits	Bit name	RW-P	Initial value	Function description
COUNT_MED_W:0	PBFDNI	RC-P	0H	<p>Port Based Forwarded Descriptor Number i</p> <p>Functions:</p> <ul style="list-style-type: none"> - This register counts the number of descriptors forwarded by Port Based forwarding from port i. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Reading this register clears it. <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: Incremented by 1 when a frame coming from port i is forwarded by Port Based Forwarding and if this register has a value different than {{COUNT_MED_W}{1'b1}}. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: This register counts the frame selected by Port based forwarding mechanism before PSFP/ATS and FRER filtering functions. Frame rejected by these filtering functions are still taken in account here.

(6) FWMHLCNi (i=0..PORT_N-1)

Forwarding Engine MAC Hardware Learn Counter i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MHLNi[COUNT_MED_W-1:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MHLNi[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
COUNT_MED_W-1:0	MHLNi	RC-P	0H	<p>MAC Hardware Learn Number i</p> <p>Functions:</p> <ul style="list-style-type: none"> - This register counts the number of MAC source addresses that has been learnt or migrated from port i. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Reading this register clears it. <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: Incremented by 1 when a frame is selected for source MAC address HW learning or HW migrated (section 5.1.5.2) and learning rate is not too high and if this register has a value different than {{COUNT_MED_W}{1'b1}}. <p>This counter is incremented regardless of the MAC learn result Table 5-41. (It counts even if it fails)</p> <p>This counter is incremented only learning or migrated HW request. So, the counter increments twice even for consecutive requests with the same content. Since the processing is the same, it looks like one time.</p>

(7) FWICRDCNi (i=0..PORT_N-1)

Forwarding Engine Integrity Check Rejected Descriptor Counter i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICRDNi[COUNT_LOW_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: COUNT_LOW_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
COUNT_LOW_W-1:0	ICRDNi	RC-P	0H	<p>Integrity Check rejected Descriptor Number i</p> <p>Functions:</p> <ul style="list-style-type: none"> - This register counts the number of descriptors rejected by Integrity Check from port i. Detail of factor is 5.2.3.1 <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Reading this register clears it. <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: Incremented by 1 when a frame coming from port i is rejected by Integrity Check and if this register has a value different than {{COUNT_LOW_W}{1'b1}}.

(8) FWWMRDCNi (i=0..PORT_N-1)

Forwarding Engine WaterMark Rejected Descriptor CouNter i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WMRDNi[COUNT_LOW_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: COUNT_LOW_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
COUNT_LOW_W-1:0	WMRDNi	RC-P	0H	<p>WaterMark rejected Descriptor Number i</p> <p>Functions:</p> <ul style="list-style-type: none"> - This register counts the number of descriptors rejected by WaterMark from port i. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Reading this register clears it. <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: Incremented by 1 when a frame coming from port i is rejected by WaterMark and if this register has a value different than {{COUNT_LOW_W}{1'b1}}.

(9) FWCTRDCNi (i=0..PORT_TIME_N-1)

Forwarding Engine Cut-Through Rejected Descriptor Counter i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTRDCNi[COUNT_LOW_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: COUNT_LOW_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
COUNT_LOW_W-1:0	CTRDCNi	RC-P	0H	<p>Cut-through rejected Descriptor Number i</p> <p>Functions:</p> <ul style="list-style-type: none"> - This register counts the number of descriptors rejected by Cut-through forwarding from port i. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Reading this register clears it. <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: Incremented by 1 when a frame coming from port i is forwarded by Cut-Through Forwarding but not in store and forward mode and if this register has a value different than {{COUNT_MED_W}{1'b1}}. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: This register does not take in account the cut-through path of cut-through forwarding but only the store and forward path so, any frame not forwarded in store and forward with cut-through (for any j, if FWCTTC0i.CTDVi[j] is set, FWCTTC0i.CTFMi[j] is not set) will be counted here.

(10) FWDDRDCNi (i=0..PORT_SLOW_N-1)

Forwarding Engine Direct Descriptor Rejected Descriptor Counter i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDRDNI[i:COUNT_LOW_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: COUNT_LOW_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
COUNT_LOW_W-1:0	DDRDNI	RC-P	0H	<p>Direct Descriptor rejected Descriptor Number i</p> <p>Functions:</p> <ul style="list-style-type: none"> - This register counts the number of descriptors rejected by Direct Descriptor forwarding from port i. Detail of factor is 5.2.4.1 <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Reading this register clears it. <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: Incremented by 1 when a frame coming from port i is rejected by Direct Descriptor forwarding and if this register has a value different than {{COUNT_LOW_W}{1'b1}}.

(11) FWLTHRDCNi (i=0..PORT_N-1)

Forwarding Engine Layer 3 Rejected Descriptor Counter i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHRDNi[COUNT_LOW_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: COUNT_LOW_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
COUNT_LOW_W-1:0	LTHRDNi	RC-P	0H	<p>Layer 3 rejected Descriptor Number i</p> <p>Functions:</p> <ul style="list-style-type: none"> - This register counts the number of descriptors rejected by Layer 3 forwarding from port i. Detail of factor is 5.2.5.5(1) <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Reading this register clears it. <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: Incremented by 1 when a frame coming from port i is rejected by Layer 3 forwarding and if this register has a value different than {{COUNT_LOW_W}{1'b1}}.

(12) FWLTWRDCNi (i=0..PORT_N-1)

Forwarding Engine Layer 2 Rejected Descriptor Counter i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTWRDNi[COUNT_LOW_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: COUNT_LOW_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
COUNT_LOW_W-1:0	LTWRDNi	RC-P	0H	<p>Layer 2 rejected Descriptor Number i</p> <p>Functions:</p> <ul style="list-style-type: none"> - This register counts the number of descriptors rejected by Layer 2 forwarding from port i. Detail of factor is 5.2.6.4(1) <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Reading this register clears it. <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: Incremented by 1 when a frame coming from port i is rejected by Layer 2 forwarding and if this register has a value different than {{COUNT_LOW_W}{1'b1}}.

(13) FWPBRDCNi (i=0..PORT_N-1)

Forwarding Engine Port Based Rejected Descriptor CouNter i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PBRDNI[COUNT_LOW_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: COUNT_LOW_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
COUNT_LOW_W-1:0	PBRDNI	RC-P	0H	<p>Port Based rejected Descriptor Number i</p> <p>Functions:</p> <ul style="list-style-type: none"> - This register counts the number of descriptors rejected by Port Based forwarding from port i. Detail of factor is 5.2.7.1 <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Reading this register clears it. <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: Incremented by 1 when a frame coming from port i is rejected by Port Based forwarding and if this register has a value different than {{COUNT_LOW_W}{1'b1}}.

(14) FWPMFDCNi (i=0..PSFP_MSDU_N-1)

Forwarding Engine PSFP MSDU Filtered Descriptor Counter i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMFDNi[COUNT_LOW_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: COUNT_LOW_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
COUNT_LOW_W-1:0	PMFDNi	RC-P	0H	<p>PSFP MSDU Filtered Descriptor Number i</p> <p>Functions:</p> <ul style="list-style-type: none"> - This register counts the number of descriptors rejected by PSFP MSDU Filter i. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Reading this register clears it. <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: Incremented by 1 when a frame is rejected by rejected by PSFP MSDU Filter i and if this register has a value different than {{COUNT_LOW_W}{1'b1}}.

(15) FWPGFDCNi (i=0..PSFP_GATE_N-1)

Forwarding Engine PSFP Gate Filtered Descriptor Counter i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PGFDNi[COUNT_LOW_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: COUNT_LOW_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
COUNT_LOW_W-1:0	PGFDNi	RC-P	0H	<p>PSFP Gate Filtered Descriptor Number i</p> <p>Functions:</p> <ul style="list-style-type: none"> - This register counts the number of descriptors rejected by PSFP Gate Filter i. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Reading this register clears it. <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: Incremented by 1 when a frame is rejected by rejected by PSFP Gate Filter i and if this register has a value different than {{COUNT_LOW_W}{1'b1}}.

(16) FWPMGDCNi (i=0..PSFP_MTR_N-1)

Forwarding Engine PSFP Meter Green Descriptor CouNter i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMGDNi[COUNT_LOW_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: COUNT_LOW_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
COUNT_LOW_W-1:0	PMGDNi	RC-P	0H	<p>PSFP Meter Green Descriptor Number i</p> <p>Functions:</p> <ul style="list-style-type: none"> - This register counts the number of descriptors with the color green given by PSFP meter Filter i. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Reading this register clears it. <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: Incremented by 1 when a frame has green color associated by PSFP meter Filter i and if this register has a value different than {{COUNT_LOW_W}{1'b1}}.

(17) FWPMYDCNi (i=0..PSFP_DMTR_N-1)

Forwarding Engine PSFP Meter Yellow Descriptor Counter i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMYDNI[COUNT_LOW_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: COUNT_LOW_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
COUNT_LOW_W-1:0	PMYDNI	RC-P	0H	<p>PSFP Meter Yellow Descriptor Number i</p> <p>Functions:</p> <ul style="list-style-type: none"> - This register counts the number of descriptors with the color Yellow given by PSFP meter Filter i. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Reading this register clears it. <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: Incremented by 1 when a frame has yellow color associated by PSFP meter Filter i and if this register has a value different than {{COUNT_LOW_W}{1'b1}}.

(18) FWPMRDCNi (i=0..PSFP_MTR_N-1)

Forwarding Engine PSFP Meter Red Descriptor Counter i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMRDNI[COUNT_LOW_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: COUNT_LOW_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
COUNT_LOW_W-1:0	PMRDN	RC-P	0H	<p>PSFP Meter Red Descriptor Number i</p> <p>Functions:</p> <ul style="list-style-type: none"> - This register counts the number of descriptors with the color Red given by PSFP meter Filter i. (All and only frames rejected by meter filter are accounted) <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Reading this register clears it. <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: Incremented by 1 when a frame has Red color associated and is rejected by PSFP meter Filter i and if this register has a value different than {{COUNT_LOW_W}{1'b1}}. - HW: Incremented by 1 when a frame is rejected by PSFP meter Filter i because ATS RAM corresponding queue is full and if this register has a value different than {{COUNT_LOW_W}{1'b1}}. - HW: Incremented by 1 when a frame is rejected by PSFP meter Filter i because corresponding meter is disabled and if this register has a value different than {{COUNT_LOW_W}{1'b1}}.

(19) FWFRPPCNI (i=0..FRER_RECE_N-1)

Forwarding Engine FRER Passed Packet Counter i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPCi[COUNT_LOW_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: COUNT_LOW_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
COUNT_LOW_W-1:0	PPCi	RC-P	0H	<p>Passed Packet Count i</p> <p>Functions:</p> <ul style="list-style-type: none"> - This register counts the number of packets that passed FRER recovery rule number i. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Reading this register clears it. <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: Incremented by 1 when a frame passed FRER recovery rule number i and if this register has a value different than {{COUNT_LOW_W}{1'b1}}.

(20) FWFRDPCNi (i=0..FRER_RECE_N-1)

Forwarding Engine FRER Discarded Packet Counter i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DPCI[COUNT_LOW_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: COUNT_LOW_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
COUNT_LOW_W-1:0	DPCI	RC-P	0H	<p>Discarded Packet Count i</p> <p>Functions:</p> <ul style="list-style-type: none"> - This register counts the number of packets that has been discarded by FRER recovery rule number i. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Reading this register clears it. <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: Incremented by 1 when a frame has been discarded by FRER recovery rule number i and if this register has a value different than {{COUNT_LOW_W}{1'b1}}.

(21) FWBLFCNi (i=0..PORT_N -1)

Forwarding Engine Block List Filtering descriptor CouNter i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BLFCi[COUNT_LOW_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: COUNT_LOW_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
COUNT_LOW_W-1:0	BLFCi	RC-P	0H	<p>Block List Filtering Count i</p> <p>Functions:</p> <ul style="list-style-type: none"> - This register counts the number of (Port based, Layer 2 or Layer 3)descriptors filtered by block list control from port i. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Reading this register clears it. <p>Increment conditions:</p> <ul style="list-style-type: none"> - HW: Incremented by 1 when a frame has been discarded (or forwarded to exceptional path) by block list control from port i and if this register has a value different than {{COUNT_LOW_W}{1'b1}}.

(22) FWALFCNi (i=0..PORT_N -1)

Forwarding Engine Acceptance List Filtering descriptor Counter i

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALFCi[COUNT_LOW_W-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: COUNT_LOW_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned
COUNT_LOW_W-1:0	ALFCi	RC-P	0H	<p>Acceptance List Filtering Count i</p> <p>Functions:</p> <ul style="list-style-type: none"> This register counts the number of (Port based, Layer 2 or Layer 3) descriptors filtered by acceptance list control from port i. <p>Clear conditions:</p> <ul style="list-style-type: none"> SW: Reading this register clears it. <p>Increment conditions:</p> <ul style="list-style-type: none"> HW: Incremented by 1 when a frame has been discarded (or forwarded to exceptional path) by acceptance list control from port i and if this register has a value different than {{COUNT_LOW_W}{1'b1}}.

3.3.3 Forwarding Engine Interrupt registers

This section describes Forwarding Engine interrupt registers.

(1) FWEIS0i (i=0..PORT_N-1)

Forwarding Engine Error Interrupt Status 0 i.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV	ICFSi	DDNTFSi	DDSESi	DDFESi	DDESi	WMIUFSi	WMISFSi	WMFFSi	WMCFSi	PBFSFSi	LTWFSF Si	SMHMF Si	SMHLFSi	PBNNTFSi	LTWVUF Si
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTWD UFSi	LTWS UFSi	LTWN TFSi	LTWV SPFSi	LTWS SPFSi	LTWD SPFSi	PBBLF Si	LTWB LFSi	LTHBL FSi	PBAFL Si	LTWA LFSi	LTHAL FSi	LTHUF Si	LTHNT FSi	LTHFS FSi	LTHSP FSi

Bits	Bit name	RW-P	Initial value	Function description
31	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
30	ICFSi	R!=W-P	0H	<p>Integrity Check Filtering Status i</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When a frame is filtered by integrity check. For more details refer to FWICETC1i, FWICETC2i, FWICETC3ij, FWICIP4Ci, FWICIP6Ci, FWIP4SFCij, FWIP6SFCij, FWIP6SFCij, FWIP4TLCCi, FWIP6PLCCi, FWICL4Ci and FWICL4THLCi register explanations. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.
29	DDNTFSi	R!=W-P	0H	<p>Direct Descriptor No Target Filtering Status i</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When a directed descriptor (LDESCR.FMT [GWCA] set to 1'b1) is received from port PORT_TIME_N+i and LDESCR.DV [GWCA] is set to All0. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: This bit exists only in i=PORT_TIME_N..PORT_N-1.
28	DDSESi	R!=W-F	0H	<p>Direct Descriptor Security Error Status i</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When a secure direct descriptor (LDESCR.FMT [GWCA] and LDESCR.SEC [GWCA] are both set to 1'b1) is received from port PORT_TIME_N+i, FWPC1i.DDEi is set and FWPC1i.DDSLi is not set. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: This bit exists only in i=PORT_TIME_N..PORT_N-1.

				Direct Descriptor Format Error Status i Set conditions: - HW: When an unsecure direct descriptor (LDESCR.FMT [GWCA] and LDESCR.SEC [GWCA] respectively set to 1'b1 and 1'b0) is received from port PORT_TIME_N+i, FWPC1i.DDEi is set, LDESCR.RV [GWCA] bit is set in the local descriptor and LDESCR.RN [GWCA] correspond to a secure routing number (when FWSCR27/28/29/30/31/32/33/34.L23URSL[LDESCR.RN] [GWCA] is not set). Clear conditions: - SW: Writing 1 to one of these bits will clear it. Error recovery: - HW: Descriptor corresponding frame is rejected. Restrictions: - HW: This bit exists only in i=PORT_TIME_N..PORT_N-1.
26	DDESi	R!=W-P	0H	Direct Descriptor Error Status i Set conditions: - HW: When a direct descriptor (LDESCR.FMT [GWCA] set to 1'b1) is received from port PORT_TIME_N+i and FWPC1i.DDEi is not set. Clear conditions: - SW: Writing 1 to one of these bits will clear it. Error recovery: - HW: Descriptor corresponding frame is rejected. Restrictions: - HW: This bit exists only in i=PORT_TIME_N..PORT_N-1.
25	WMIUFSi	R!=W-P	0H	WaterMark IPV Unsecure Filtering Status i Set conditions: - HW: A frame coming from port i is forwarded with a Layer 3/Layer 2/Port based normal descriptor and SEC is not set and corresponding IPV is rejected by IPV based unsecure watermark [COMA] (where SEC and IPV are respectively Frame corresponding normal descriptor, selected by the forwarding flow, FDESCR.SEC and FDESCR.IPV values before filtering). Clear conditions: - SW: Writing 1 to one of these bits will clear it. Error recovery: - HW: Descriptor corresponding frame is rejected.
24	WMISFSi	R!=W-F	0H	WaterMark IPV Secure Filtering Status i Set conditions: - HW: A frame coming from port i is forwarded with a Layer 3/Layer 2/Port based normal descriptor and corresponding IPV is rejected by IPV based secure watermark [COMA] (where IPV is Frame corresponding normal descriptor, selected by the forwarding flow, FDESCR.IPV value before filtering). Clear conditions: - SW: Writing 1 to one of these bits will clear it. Error recovery: - HW: Descriptor corresponding frame is rejected.

				WaterMark Flush Filtering Status i
23	WMFFSi	R!=W-P	0H	<p>Set conditions:</p> <ul style="list-style-type: none"> - HW: A frame coming from port i is forwarded with a Layer 3/IP/Layer 2/Port based normal descriptor and FWLBWMCi.WMFLPRI bit {DEI,IPV} is set and coa_watermark_flush[i] pin is set (where DEI is set to input frame C-TAG DEI if FWGC.SVM is set to 2'b01, input frame S-TAG DEI if FWGC.SVM is set to 2'b10 and set to 1'b0 if FWGC.SVM is set to 2'b00 and IPV is the Frame corresponding normal descriptor, selected by the forwarding flow, FDESCR.IPV value). <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.
22	WMCFSi	R!=W-P	0H	<p>WaterMark Critical Filtering Status i</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: A frame coming from port i is forwarded with a Layer 3/IP/Layer 2/Port based normal descriptor and FWLBWMCi.WMCLPRI bit {DEI,IPV} is set and coa_watermark_critical[i] pin is set (where DEI is set to input frame C-TAG DEI if FWGC.SVM is set to 2'b01, input frame S-TAG DEI if FWGC.SVM is set to 2'b10 and set to 1'b0 if FWGC.SVM is set to 2'b00 and IPV is the Frame corresponding normal descriptor, selected by the forwarding flow, FDESCR.IPV value). <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.
21	PBFSFSi	R!=W-F	0H	<p>Port Based Format Security Filtering Status i</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When forwarding flow for a frame coming from port i goes until "Port based forwarding error" block in Fig 5.56 and, PB.MSDUV bit is set in the local descriptor and PB.MSDUN correspond to a secure MSDU filter number (when FWSCR38.PMSDURSL[PB.MSDUN] is not set). - HW: When forwarding flow for a frame coming from port i goes until "Port based forwarding error" block in Fig 5.56 and, PB.GATEV bit is set in the local descriptor and PB.GATEN correspond to a secure Gate filter number (when FWSCR39.PGATERSL[PB.GATEN] is not set). - HW: When forwarding flow for a frame coming from port i goes until "Port based forwarding error" block in Fig 5.56 and, PB.MTRV bit is set in the local descriptor and PB.MTRN correspond to a secure Meter filter number (when FWSCR40/41/42/43.PMTRRSRSL[PB.MTRN] is not set). <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.

				Layer TWo Format Security Filtering Status i
20	LTWFSFSi	R!=W-F	0H	<p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding error" block in Fig 5.52 and, L2.RV bit is set in the local descriptor and L2.RN correspond to a secure routing number (when FWSCR27/28/29/30/31/32/33/34.L23URSL[L2.RN] is not set). - HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding error" block in Fig 5.52 and, L2.MSDUV bit is set in the local descriptor and L2.MSDUN correspond to a secure MSDU filter number (when FWSCR38.PMSDURSL[L2.MSDUN] is not set). - HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding error" block in Fig 5.52 and, L2.GATEV bit is set in the local descriptor and L2.GATEN correspond to a secure Gate filter number (when FWSCR39.PGATERSL[L2.GATEN] is not set). - HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding error" block in Fig 5.52 and, L2.MTRV bit is set in the local descriptor and L2.MTRN correspond to a secure Meter filter number (when FWSCR40/41/42/43.PMTRRSI[L2.MTRN] is not set). - HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding error" block in Fig 5.52 and, L2.FRERV bit is set in the local descriptor and L2.FRERN correspond to a secure recovery entry number (when FWSCR44/45/46/47.FRERRSL[L2.FRERN] is not set). <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.
19	SMHMFSi	R!=W-P	0H	<p>Source MAC Hardware Migration Fail Status i</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When a frame is selected for source MAC address HW migration (section 5.1.5.2) and it couldn't be learnt because follow any conditions. <ul style="list-style-type: none"> - The learning rate is too high For detail, "If Hardware learning descriptor are issued continuously from the same port (Due to extremely small frames etc.) while HW learning descriptor is stagnant, the second descriptor will be treated as "learning rate is too high". <ul style="list-style-type: none"> - Reached limit of HW learning (FWMACHWLC1.MACDEN >= (FWMACHWLC0.MACTHWLEA - FWMACHWLC0.MACTHWLSA + 1)) - Reached limit of HW learning (FWMACHWLC2i.MACDENPPI >= FWMACHWLC2i.MACDELNPPI) for source port i. - HW: When a frame is selected for source MAC address HW migration and its source MAC address contained in the table in static (MAC.DE is not set). - HW: When a frame is selected for source MAC address HW migration and its source MAC address contained in the table is secure (MAC.SL is set). - HW: When a frame is selected for source MAC address HW migration and its source MAC address contained in the table has one of its destination port which does not allow migration (for at least one i, MAC.DV[i] is set and FWPC0i.MACHMAi is not set). <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.

				Source MAC Hardware Learning Fail Status i
18	SMHLFSi	R!=W-P	0H	<p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When a frame is selected for source MAC address HW learning (section 5.1.5.2) and it couldn't be learnt because follow any conditions. - The learning rate is too high. <p>For detail, "If Hardware learning descriptor are issued continuously from the same port (Due to extremely small frames etc.) while HW learning descriptor is stagnant, the second descriptor will be treated as "learning rate is too high".</p> <ul style="list-style-type: none"> - Reached limit of HW learning (FWMACHWLC1.MACDEN >= (FWMACHWLC0.MACTHWLEA - FWMACHWLC0.MACTHWLSA + 1)) - Reached limit of HW learning (FWMACHWLC2i.MACDENPPI >= FWMACHWLC2i.MACDELNPPI) for source port i. <p>This error has nothing to do with fail of Table 5-41.</p> <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.
17	PBNTFSi	R!=W-P	0H	<p>Port Based No Target Filtering Status i</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When forwarding flow for a frame coming from port i goes until "Port based forwarding secure error" block in Fig 5.55 and FWPBFC0i.PBDVi is null. - HW: When forwarding flow for a frame coming from port i goes until "Port based forwarding unsecure error" block in Fig 5.56 and FWPBFC0i.PBDVi is null. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.
16	LTWVUFSi	R!=W-P	0H	<p>Layer Two VLAN Unknown Filtering Status i</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding secure error" block in Fig 5.51 and, {FWPC0i.VLANSAi is not set or VLAN is not valid or VLAN ID is not set in the VLAN table or VLAN.SL is not set for VLAN ID} and FWPC0i.VLANRUSi is set. - HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding error" block in Fig 5.52 and, {FWPC0i.VLANSAi is not set or VLAN is not valid or VLAN ID is not set in the VLAN table} and FWPC0i.VLANRUi is set. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.

				Layer TWo Destination Unknown Filtering Status i
15	LTWDUFSi	R!=W-P	0H	<p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding secure error" block in Fig 5.51 and, {FWPC0i.MACDSA_i is not set or Destination MAC is not set in the MAC table or MAC.SL is not set for destination MAC} and FWPC0i.MACRUDSA_i is set. - HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding error" block in Fig 5.52 and, {FWPC0i.MACDSA_i is not set or Destination MAC is not set in the MAC table} and FWPC0i.MACRUDSA_i is set. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.
14	LTWSUFSi	R!=W-P	0H	<p>Layer TWo Source Unknown Filtering Status i</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding secure error" block in Fig 5.51 and, {FWPC0i.MACSSA_i is not set or Source MAC is not set in the MAC table or MAC.SL is not set for Source MAC} and FWPC0i.MACRUSSA_i is set. - HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding error" block in Fig 5.52 and, {FWPC0i.MACSSA_i is not set or Source MAC is not set in the MAC table} and FWPC0i.MACRUSSA_i is set. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.

				Layer TWo No Target Filtering Status i Set conditions: <ul style="list-style-type: none">- HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding secure error" block in Fig 5.51 and, FWPC0i.MACDSA_i is set, Destination MAC is set in the MAC table, MAC.SL is set, FWPC0i.VLANS_{Ai} is set, VLAN ID is valid, VLAN ID is set in the VLAN table, VLAN.SL is set and MAC.DV & VLAN.DV & !FWPC2i.LTWFMi & !VLAN.FMi is null.- HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding secure error" block in Fig 5.51 and, FWPC0i.MACDSA_i is set, Destination MAC is set in the MAC table, MAC.SL is set, {FWPC0i.VLANS_{Ai} is not set or VLAN ID is not valid or VLAN ID is not set in the VLAN table or VLAN.SL is not set} and MAC.DV & !FWPC2i.LTWFMi & !VLAN.FMi is null.- HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding secure error" block in Fig 5.51 and, {FWPC0i.MACDSA_i is not set or Destination MAC is not set in the MAC table or MAC.SL is not set}, VLAN ID is valid, VLAN ID is set in the VLAN table, VLAN.SL is set and VLAN.DV & !FWPC2i.LTWFMi & !VLAN.FMi is null.- HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding error" block in Fig 5.52 and, FWPC0i.MACDSA_i is set, Destination MAC is set in the MAC table, FWPC0i.VLANS_{Ai} is set, VLAN ID is valid, VLAN ID is set in the VLAN table and MAC.DV & VLAN.DV & !FWPC2i.LTWFMi & !VLAN.FMi is null.- HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding error" block in Fig 5.52 and, {FWPC0i.MACDSA_i is not set or Destination MAC is not set in the MAC table, FWPC0i.VLANS_{Ai} is not set or VLAN ID is not valid or VLAN ID is not set in the VLAN table } and MAC.DV & !FWPC2i.LTWFMi & !VLAN.FMi is null.- HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding error" block in Fig 5.52 and, {FWPC0i.MACDSA_i is not set or Destination MAC is not set in the MAC table}, VLAN ID is valid, VLAN ID is set in the VLAN table and VLAN.DV & !FWPC2i.LTWFMi & !VLAN.FMi is null. Clear conditions: <ul style="list-style-type: none">- SW: Writing 1 to one of these bits will clear it. Error recovery: <ul style="list-style-type: none">- HW: Descriptor corresponding frame is rejected.
12	LTWVSPFSi	R!=W-P	0H	Layer TWo VLAN Source Port Filtering Status i Set conditions: <ul style="list-style-type: none">- HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding secure error" block in Fig 5.51 and, FWPC0i.VLANS_{Ai} is set, VLAN ID is valid, VLAN ID is set in the VLAN table, VLAN.SL is set and VLAN.SLV is not set for VLAN ID.- HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding error" block in Fig 5.52 and, FWPC0i.VLANS_{Ai} is set, VLAN ID is valid, VLAN ID is set in the VLAN table and VLAN.SLV is not set for VLAN ID. Clear conditions: <ul style="list-style-type: none">- SW: Writing 1 to one of these bits will clear it. Error recovery: <ul style="list-style-type: none">- HW: Descriptor corresponding frame is rejected.

				Layer TWo Source Source Port Filtering Status i
11	LTWSSPFSi	R!=W-P	0H	<p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding secure error" block in Fig 5.51 and, FWPC0i.MACSSAi is set, Source MAC is set in the MAC table, MAC.SL is set and MAC.SSLV is not set for source MAC. - HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding error" block in Fig 5.52 and, FWPC0i.MACSSAi is set, Source MAC is set in the MAC table and MAC.SSLV is not set for source MAC. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.
10	LTWDSPFSi	R!=W-P	0H	<p>Layer TWo Destination Source Port Filtering Status i</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding secure error" block in Fig 5.51 and, FWPC0i.MACDSAi is set, Destination MAC is set in the MAC table, MAC.SL is set and MAC.DSLV is not set for destination MAC. - HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding error" block in Fig 5.52 and, FWPC0i.MACDSAi is set, Destination MAC is set in the MAC table and MAC.DSLV is not set for destination MAC. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.
9	PBBLFSi	R!=W-P	0H	<p>Port Based Block List Filtering Status i</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When forwarding flow for a frame coming from port i goes until "Port based forwarding secure error" block in Fig 5.55 and frame is filtered by block list. - HW: When forwarding flow for a frame coming from port i goes until "Port based forwarding unsecure error" block in Fig 5.56 and frame is filtered by block list. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.
8	LTWBLFSi	R!=W-P	0H	<p>Layer TWo Block List Filtering Status i</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding secure error" block in Fig 5.51 and frame is filtered by block list. - HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding error" block in Fig 5.52 and frame is filtered by block list. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.

				Layer THree Block List Filtering Status i
7	LTHBLFSi	R!=W-P	0H	<p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When forwarding flow for a frame coming from port i goes until "Layer 3 routing secure error" block in Fig 5.42 and frame is filtered by block list. - HW: When forwarding flow for a frame coming from port i goes until "Layer 3 routing error" block in Fig 5.43 and frame is filtered by block list. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.
6	PBALFSi	R!=W-P	0H	<p>Port Based Acceptance List Filtering Status i</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When forwarding flow for a frame coming from port i goes until "Port based forwarding secure error" block in Fig 5.55 and frame is filtered by acceptance list. - HW: When forwarding flow for a frame coming from port i goes until "Port based forwarding unsecure error" block in Fig 5.56 and frame is filtered by acceptance list. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.
5	LTWALFSi	R!=W-P	0H	<p>Layer TWo Acceptance List Filtering Status i</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding secure error" block in Fig 5.51 and frame is filtered by acceptance list. - HW: When forwarding flow for a frame coming from port i goes until "L2 forwarding error" block in Fig 5.52 and frame is filtered by acceptance list. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.
4	LTHALFSi	R!=W-P	0H	<p>Layer THree Acceptance List Filtering Status i</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When forwarding flow for a frame coming from port i goes until "Layer 3 routing secure error" block in Fig 5.42 and frame is filtered by acceptance list. - HW: When forwarding flow for a frame coming from port i goes until "Layer 3 routing error" block in Fig 5.43 and frame is filtered by acceptance list. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.

				Layer THree Unknown Filtering Status i Set conditions: <ul style="list-style-type: none">- HW: When forwarding flow for a frame coming from port i goes until "Layer 3 routing unknown secure stream error" block in Fig 5.42 and FWPC0i.LTHRUSi is set.- HW: When forwarding flow for a frame coming from port i goes until "Layer 3 routing error" block in Fig 5.43 and FWPC0i.LTHRUSi is set. Clear conditions: <ul style="list-style-type: none">- SW: Writing 1 to one of these bits will clear it. Error recovery: <ul style="list-style-type: none">- HW: Descriptor corresponding frame is rejected.
3	LTHUFSi	R!=W-P	0H	Layer THree No Target Filtering Status i Set conditions: <ul style="list-style-type: none">- HW: When forwarding flow for a frame coming from port i goes until "Layer 3 routing secure error" block in Fig 5.42 and L3.DV & !FWPC1i.LTHFMi & !VLAN.FMi is null.- HW: When forwarding flow for a frame coming from port i goes until "Layer 3 routing error" block in Fig 5.43 and L3.DV & !FWPC1i.LTHFMi & !VLAN.FMi is null. Clear conditions: <ul style="list-style-type: none">- SW: Writing 1 to one of these bits will clear it. Error recovery: <ul style="list-style-type: none">- HW: Descriptor corresponding frame is rejected.
2	LTHNTFSi	R!=W-P	0H	Layer THree Format Security Filtering Status i Set conditions: <ul style="list-style-type: none">- HW: When forwarding flow for a frame coming from port i goes until "Layer 3 routing error" block in Fig 5.43 and, L3.RV bit is set in the local descriptor and L3.RN correspond to a secure routing number (when FWSCR27/28/29/30/31/32/33/34.L23URSL[L3.RN] is not set)- HW: When forwarding flow for a frame coming from port i goes until "Layer 3 routing error" block in Fig 5.43 and, L3.MSDUV bit is set in the local descriptor and L3.MSDUN correspond to a secure MSDU filter number (when FWSCR38.PMSDURSL[L3.MSDUN] is not set)- HW: When forwarding flow for a frame coming from port i goes until "Layer 3 routing error" block in Fig 5.43 and, L3.GATEV bit is set in the local descriptor and L3.GATEN correspond to a secure Gate filter number (when FWSCR39.PGATERSL[L3.GATEN] is not set)- HW: When forwarding flow for a frame coming from port i goes until "Layer 3 routing error" block in Fig 5.43 and, L3.MTRV bit is set in the local descriptor and L3.MTRN correspond to a secure Meter filter number (when FWSCR40/41/42/43.PMTRRSL[L3.MTRN] is not set)- HW: When forwarding flow for a frame coming from port i goes until "Layer 3 routing error" block in Fig 5.43 and, L3.FRREV bit is set in the local descriptor and L3.FRERN correspond to a secure Recovery filter number (when FWSCR44/45/46/47.FRERRSRL[L3.FRERN] is not set) Clear conditions: <ul style="list-style-type: none">- SW: Writing 1 to one of these bits will clear it. Error recovery: <ul style="list-style-type: none">- HW: Descriptor corresponding frame is rejected.
1	LTHFSFSi	R!=W-F	0H	Layer THree Format Security Filtering Status i Set conditions: <ul style="list-style-type: none">- HW: When forwarding flow for a frame coming from port i goes until "Layer 3 routing error" block in Fig 5.43 and, L3.RV bit is set in the local descriptor and L3.RN correspond to a secure routing number (when FWSCR27/28/29/30/31/32/33/34.L23URSL[L3.RN] is not set)- HW: When forwarding flow for a frame coming from port i goes until "Layer 3 routing error" block in Fig 5.43 and, L3.MSDUV bit is set in the local descriptor and L3.MSDUN correspond to a secure MSDU filter number (when FWSCR38.PMSDURSL[L3.MSDUN] is not set)- HW: When forwarding flow for a frame coming from port i goes until "Layer 3 routing error" block in Fig 5.43 and, L3.GATEV bit is set in the local descriptor and L3.GATEN correspond to a secure Gate filter number (when FWSCR39.PGATERSL[L3.GATEN] is not set)- HW: When forwarding flow for a frame coming from port i goes until "Layer 3 routing error" block in Fig 5.43 and, L3.MTRV bit is set in the local descriptor and L3.MTRN correspond to a secure Meter filter number (when FWSCR40/41/42/43.PMTRRSL[L3.MTRN] is not set)- HW: When forwarding flow for a frame coming from port i goes until "Layer 3 routing error" block in Fig 5.43 and, L3.FRREV bit is set in the local descriptor and L3.FRERN correspond to a secure Recovery filter number (when FWSCR44/45/46/47.FRERRSRL[L3.FRERN] is not set) Clear conditions: <ul style="list-style-type: none">- SW: Writing 1 to one of these bits will clear it. Error recovery: <ul style="list-style-type: none">- HW: Descriptor corresponding frame is rejected.

0	LTHSPFSi	R!=W-P	0H	<p>Layer THree Source Port Filtering Status i</p> <p>Set conditions:</p> <ul style="list-style-type: none">- HW: When forwarding flow for a frame coming from port i goes until "Layer 3 routing secure error" block in Fig 5.42 and L3.SLV[i] is not set.- HW: When forwarding flow for a frame coming from port i goes until "Layer 3 routing error" block in Fig 5.43 and L3.SLV[i] is not set. <p>Clear conditions:</p> <ul style="list-style-type: none">- SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none">- HW: Descriptor corresponding frame is rejected.
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(2) FWEIE0i (i=0..PORT_N-1)

Forwarding Engine Error Interrupt Enable 0 i.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV	ICFEi	DDNTFEi	DDSEEi	DDFEEi	DDEEi	WMIUFEi	WMISFEi	WMFFEi	WMCFEi	PBFSFEi	LTWFSF <i>Ei</i>	SMHMF <i>Ei</i>	SMHLFEi	PBNTE <i>Ei</i>	LTWVUF <i>Ei</i>
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTWD	LTWS	LTWN	LTWV	LTWS	LTWD	PBBLF	LTWB	LTHBL	PBAFL	LTWA	LTHAL	LTHUF	LTHNT	LTHFS	LTHSP
UFEi	UFEi	TFEi	SPFEi	SPFEi	SPFEi	Ei	LFEi	FEi	Ei	LFEi	FEi	Ei	FEi	FEi	FEi

Bits	Bit name	RW-P	Initial value	Function description
31	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
30	ICFEi	R!=W-P	0H	<p>Integrity Check Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.ICFDi register will clear this bit.
29	DDNTFEi	R!=W-P	0H	<p>Direct Descriptor No Target Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.DDNTFDi register will clear this bit.
28	DDSEEi	R!=W-F	0H	<p>Direct Descriptor Security Error Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.DDSEDi register will clear this bit.
27	DDFEEi	R!=W-F	0H	<p>Direct Descriptor Format Error Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.DDFEDI register will clear this bit.

26	DDEEi	R!=W-P	0H	<p>Direct Descriptor Error Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.DDEDi register will clear this bit.
25	WMIUFEi	R!=W-P	0H	<p>WaterMark IPV Unsecure Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.WMIUFDi register will clear this bit.
24	WMISFEi	R!=W-F	0H	<p>WaterMark IPV Secure Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.WMISFDi register will clear this bit.
23	WMFFEi	R!=W-P	0H	<p>WaterMark Flush Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.WMFFEi register will clear this bit.
22	WMCFEi	R!=W-P	0H	<p>WaterMark Critical Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.WMFFDi register will clear this bit.
21	PBFSFEi	R!=W-F	0H	<p>Port Based Format Security Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.PBFSFDi register will clear this bit.

20	LTWFSFEi	R!=W-F	0H	<p>Layer TWo Format Security Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.LTWFSFDi register will clear this bit.
19	SMHMFEi	R!=W-P	0H	<p>Source MAC Hardware Migration Fail Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.SMHMFDi register will clear this bit.
18	SMHLFEi	R!=W-P	0H	<p>Source MAC Hardware Learning Fail Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.SMHLFDi register will clear this bit.
17	PBNTFEi	R!=W-P	0H	<p>Port Based No Target Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.PBNTFDi register will clear this bit.
16	LTWVUFEi	R!=W-P	0H	<p>Layer TWo VLAN Unknown Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.LTWVUFDi register will clear this bit.
15	LTWDUFEi	R!=W-P	0H	<p>Layer TWo Destination Unknown Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.LTWDUFDi register will clear this bit.

14	LTWSUFEi	R!=W-P	0H	<p>Layer TWo Source Unknown Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.LTWSUFDi register will clear this bit.
13	LTWNTEFi	R!=W-P	0H	<p>Layer TWo No Target Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.LTWNTFDi register will clear this bit.
12	LTWVSPFEi	R!=W-P	0H	<p>Layer TWo VLAN Source Port Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.LTWVSPFDi register will clear this bit.
11	LTWSSPFEi	R!=W-P	0H	<p>Layer TWo Source Source Port Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.LTWSSPFDi register will clear this bit.
10	LTWDSPFEi	R!=W-P	0H	<p>Layer TWo Destination Source Port Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.LTWDSPFDi register will clear this bit.
9	PBBLFEi	R!=W-P	0H	<p>Port Based Block List Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.PBBLFDi register will clear this bit.

8	LTWBLFEi	R!=W-P	0H	<p>Layer TWo Block List Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.LTWBLFDi register will clear this bit.
7	LTHBLFEi	R!=W-P	0H	<p>Layer THree Block List Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.LTHBLFDi register will clear this bit.
6	PBALFEi	R!=W-P	0H	<p>Port Based Acceptance List Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.PBALFDi register will clear this bit.
5	LTWALFEi	R!=W-P	0H	<p>Layer TWo Acceptance List Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.LTWALFDi register will clear this bit.
4	LTHALFEi	R!=W-P	0H	<p>Layer THree Acceptance List Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.LTHALFDi register will clear this bit.
3	LTHUFEi	R!=W-P	0H	<p>Layer THree Unknown Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.LTHUFDi register will clear this bit.

2	LTHNTFEi	R!=W-P	0H	<p>Layer THree No Target Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.LTHNTFDi register will clear this bit.
1	LTHFSFEi	R!=W-F	0H	<p>Layer THree Format Security Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.LTHFSFDi register will clear this bit.
0	LTHSPFEi	R!=W-P	0H	<p>Layer THree Source Port Filtering Enable i</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt i disabled. - 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID0i.LTHSPFDi register will clear this bit.

(3) FWEID0i (i=0..PORT_N-1)

Forwarding Engine Error Interrupt Disable 0 i.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV	ICFDi	DDNTFDi	DDSEDi	DDFEDI	DDEDi	WMIUFDi	WMISFDi	WMFFDI	WMCFDI	PBFSFDi	LTWFSSFDi	SMHMFDi	SMHLFDi	PBNTFDi	LTWVUFDi
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTWD	LTWS	LTWN	LTWVS	LTWSS	LTWDS	PBBLF	LTWB	LTHBL	PBALF	LTWA	LTHAL	LTHUF	LTHNT	LTHFS	LTHSP
UFDi	UFDi	TFDi	PFDi	PFDi	PFDi	Di	LFDi	FDi	Di	LFDi	FDi	Di	FDi	FDi	FDi

Bits	Bit name	RW-P	Initial value	Function description
31	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
30	ICFDi	R0W-P	0H	Integrity Check Filtering Disable i Functions: - Writing 1 to this register will clear FWEIE0.ICFEi register.
29	DDNTFDi	R0W-P	0H	Direct Descriptor No Target Filtering Disable i Functions: - Writing 1 to this register will clear FWEIE0.DDNTFEi register.
28	DDSEDi	R0W-F	0H	Direct Descriptor Security Error Disable i Functions: - Writing 1 to this register will clear FWEIE0.DDSEEi register.
27	DDFEDI	R0W-F	0H	Direct Descriptor Format Error Disable i Functions: - Writing 1 to this register will clear FWEIE0.DDFEEi register.
26	DDEDI	R0W-P	0H	Direct Descriptor Error Disable i Functions: - Writing 1 to this register will clear FWEIE0.DDEEi register.
25	WMIUFDi	R0W-P	0H	WaterMark IPV Unsecure Filtering Disable i Functions: - Writing 1 to this register will clear FWEIE0.WMIUFEi register.
24	WMISFDi	R0W-F	0H	WaterMark IPV Secure Filtering Disable i Functions: - Writing 1 to this register will clear FWEIE0.WMISFEi register.
23	WMFFDI	R0W-P	0H	WaterMark Flush Filtering Disable i Functions: - Writing 1 to this register will clear FWEIE0.WMFFEi register.
22	WMCFDI	R0W-P	0H	WaterMark Critical Filtering Disable i Functions: - Writing 1 to this register will clear FWEIE0.WMCFEi register.
21	PBFSFDi	R0W-F	0H	Port Based Format Security Filtering Disable i Functions: Writing 1 to this register will clear FWEIE0.PBFSFEi register.
20	LTWFSSFDi	R0W-F	0H	Layer TWo Format Security Filtering Disable i Functions: - Writing 1 to this register will clear FWEIE0.LTWFSFEi register.

19	SMHMFDi	R0W-P	0H	Source MAC Hardware Migration Fail Disable i Functions: - Writing 1 to this register will clear FWEIE0.SMHMFEi register.
18	SMHLFDi	R0W-P	0H	Source MAC Hardware Learning Fail Disable i Functions: - Writing 1 to this register will clear FWEIE0.SMHLFEi register.
17	PBNTFDi	R0W-P	0H	Port Based No Target Filtering Disable i Functions: - Writing 1 to this register will clear FWEIE0.PBNTFEi register.
16	LTWVUFDi	R0W-P	0H	Layer TWo VLAN Unknown Filtering Disable i Functions: - Writing 1 to this register will clear FWEIE0.LTWVUFEi register.
15	LTWDUFDi	R0W-P	0H	Layer TWo Destination Unknown Filtering Disable i Functions: - Writing 1 to this register will clear FWEIE0.LTWDUFEi register.
14	LTWSUFDi	R0W-P	0H	Layer TWo Source Unknown Filtering Disable i Functions: - Writing 1 to this register will clear FWEIE0.LTWSUFEi register.
13	LTWNNTFDi	R0W-P	0H	Layer TWo No Target Filtering Disable i Functions: - Writing 1 to this register will clear FWEIE0.LTWNTFEi register.
12	LTWVSPFDi	R0W-P	0H	Layer TWo VLAN Source Port Filtering Disable i Functions: - Writing 1 to this register will clear FWEIE0.LTWVSPFEi register.
11	LTWSSPFDi	R0W-P	0H	Layer TWo Source Source Port Filtering Disable i Functions: - Writing 1 to this register will clear FWEIE0.LTWSSPFEi register.
10	LTWDSPFDi	R0W-P	0H	Layer TWo Destination Source Port Filtering Disable i Functions: - Writing 1 to this register will clear FWEIE0.LTWDSPFEi register.
9	PBBLFDi	R0W-F	0H	Port Based Block List Filtering Disable i Functions: Writing 1 to this register will clear FWEIE0.PBBLFEi register.
8	LTWBLFDi	R0W-F	0H	Layer TWo Block List Filtering Disable i Functions: - Writing 1 to this register will clear FWEIE0.LTWBLFEi register.
7	LTHBLFDi	R0W-F	0H	Layer THree Block List Filtering Disable i Functions: - Writing 1 to this register will clear FWEIE0.LTHBLFEi register.
6	PBALFDi	R0W-P	0H	Port Based Acceptance List Filtering Disable i Functions: - Writing 1 to this register will clear FWEIE0.PBALFEi register.
5	LTWALFDi	R0W-P	0H	Layer TWo Acceptance List Filtering Disable i Functions: - Writing 1 to this register will clear FWEIE0.LTWALFEi register.
4	LTHALFDi	R0W-P	0H	Layer THree Acceptance List Filtering Disable i Functions: - Writing 1 to this register will clear FWEIE0.LTHALFEi register.

3	LTHUFDi	R0W-P	0H	Layer THree Unknown Filtering Disable i Functions: - Writing 1 to this register will clear FWEIE0.LTHUFEi register.
2	LTHNTFDi	R0W-P	0H	Layer THree No Target Filtering Disable i Functions: - Writing 1 to this register will clear FWEIE0.LTHNTFEi register.
1	LTHFSFDi	R0W-F	0H	Layer THree Format Security Filtering Disable i Functions: - Writing 1 to this register will clear FWEIE0.LTHFSFEi register.
0	LTHSPFDi	R0W-P	0H	Layer THree Source Port Filtering Disable i Functions: - Writing 1 to this register will clear FWEIE0.LTHSPFEi register.

(4) FWEIS1

Forwarding Engine Error Interrupt Status 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															FTEES AREES
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV						L23US ES	L23UE ES	VLANT SES	VLANT EES	MACT SES	MACT EES	RSV		LTHTS ES	LTHTE ES

Bits	Bit name	RW-P	Initial value	Function description
31:18	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
17	FTEES	R!=W-P	0H	<p>FRER Table ECC Error Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When an ECC error has been detected while reading an entry from the FRER RAM. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to this bit will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: The corresponding descriptor is forwarded. - SW: The corresponding entry should be learned again
16	AREES	R!=W-P	0H	<p>ATS RAM ECC Error Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When an ECC error has been detected while reading a descriptor from the ATS RAM. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to this bit will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Loss of the descriptor. One or several pointers will be lost so the switch will continue operating but with a reduced Local RAM. - SW: Nothing if it is acceptable to operate with a reduced Local RAM else Switch reset.
15:10	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
9	L23USES	R!=W-RP	0H	<p>Layer2/Layer3 Update Security Error Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: Unsecure CPU tried to overwrite a secure entry. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Unsecure entry won't be learned - SW: System dependent, cannot be defined here. <p>Security restrictions:</p> <ul style="list-style-type: none"> - HW: This register cannot be accessed by the unsecure APB interface.

8	L23UEES	R!=W-P	0H	<p>Layer2/Layer3 Update ECC Error Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: An ECC error is detected in VLAN Table <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: The rule number is not given by Forwarding Engine for error recovery, this value should be read from the Layer2/Layer3 Update RAM ECC module. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: The table will be used normally for entries not affected by the ECC error. - SW: Re-learn ECC error corresponding entry.
7	VLANTSES	R!=W-RP	0H	<p>VLAN Table Security Error Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: Unsecure CPU tried to overwrite a secure entry. - HW: A CPU tried to learn an unsecure entry, but the unsecure entry maximum number is already reached. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Unsecure entry won't be learned - SW: System dependent, cannot be defined here. <p>Security restrictions:</p> <ul style="list-style-type: none"> - HW: This register cannot be accessed by the unsecure APB interface.
6	VLANTEES	R!=W-P	0H	<p>VLAN Table ECC Error Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: An ECC error is detected in VLAN Table <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: The table will be used normally for entries not affected by the ECC error. - SW: Switch or table reset.
5	MACTSES	R!=W-RP	0H	<p>MAC Table Security Error Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: Unsecure CPU tried to overwrite a secure entry. - HW: A CPU tried to learn an unsecure entry, but the unsecure entry maximum number is already reached. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Unsecure entry won't be learned - SW: System dependent, cannot be defined here. <p>Security restrictions:</p> <ul style="list-style-type: none"> - HW: This register cannot be accessed by the unsecure APB interface.

				MAC Table ECC Error Status Set conditions: - HW: An ECC error is detected in MAC Table Clear conditions: - SW: Writing 1 to one of these bits will clear it. Error recovery: - HW: The table will be used normally for entries not affected by the ECC error. - SW: Switch or table reset. Notes: - This flag will set by follow cases. TCAM : 1) SW read entry from APB. RAM : 1) HW read (after TCAM HW search) entry for forwarding. 2) SW read entry from APB. 3) SW search (after TCAM SW search) entry from APB. The following actions do not set this bit. TCAM : 1) Search. RAM : 1) Aging read. 2) Self-Recovery read.
4	MACTEES	R!=W-P	0H	
3:2	RSV	R0-U	0H	- Reserved area. On read, 0 will be returned.
1	LTHSES	R!=W-RP	0H	L3 Table Security Error Status Set conditions: - HW: Unsecure CPU tried to overwrite a secure entry. Clear conditions: - SW: Writing 1 to one of these bits will clear it. Error recovery: - HW: Unsecure entry won't be learned - SW: System dependent, cannot be defined here. Security restrictions: - HW: This register cannot be accessed by the unsecure APB interface.
0	LTHTEES	R!=W-P	0H	L3 Table ECC Error Status Set conditions: - HW: An ECC error is detected in L3 Table Clear conditions: - SW: Writing 1 to one of these bits will clear it. Error recovery: - HW: The table will be used normally for entries not affected by the ECC error. - SW: Switch or table reset. Notes: - Since ECC error of TCAM reads do not occur during normal operation (forwarding), this flag is set only on RAM reads.

(5) FWEIE1

Forwarding Engine Error Interrupt Enable 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV														FTEEE	AREEE
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV						L23US EE	L23UE EE	VLANT SEE	VLANT EEE	MACT SEE	MACT EEE	RSV		LTHTS EE	LTHTE EE

Bits	Bit name	RW-P	Initial value	Function description
31:18	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
17	FTEEE	R!=W-P	0H	<p>FRER Table ECC Error Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt disabled. - 1'b1: Interrupt Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID1.FTEED register will clear this bit.
16	AREEE	R!=W-P	0H	<p>ATS RAM ECC Error Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt disabled. - 1'b1: Interrupt Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID1.AREED register will clear this bit.
15:10	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
9	L23USEE	R!=W-RP	0H	<p>Layer2/Layer3 Update Security Error Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt disabled. - 1'b1: Interrupt Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID1.L23USED register will clear this bit.
8	L23UEEE	R!=W-P	0H	<p>Layer2/Layer3 Update ECC Error Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt disabled. - 1'b1: Interrupt Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID1.L23UEED register will clear this bit.

7	VLANTSEE	R!=W-RP	0H	VLAN Table Security Error Enable Values: - 1'b0: Interrupt disabled. - 1'b1: Interrupt Enabled. Set conditions: - Writing 1 to this bit will set it. Clear conditions: - Writing 1 to FWEID1.VLANTSED register will clear this bit.
6	VLANTEE	R!=W-P	0H	VLAN Table ECC Error Enable Values: - 1'b0: Interrupt disabled. - 1'b1: Interrupt Enabled. Set conditions: - Writing 1 to this bit will set it. Clear conditions: - Writing 1 to FWEID1.VLANTEED register will clear this bit.
5	MACTSEE	R!=W-RP	0H	MAC Table Security Error Enable Values: - 1'b0: Interrupt disabled. - 1'b1: Interrupt Enabled. Set conditions: - Writing 1 to this bit will set it. Clear conditions: - Writing 1 to FWEID1.MACTSED register will clear this bit.
4	MACTEEE	R!=W-P	0H	MAC Table ECC Error Enable Values: - 1'b0: Interrupt disabled. - 1'b1: Interrupt Enabled. Set conditions: - Writing 1 to this bit will set it. Clear conditions: - Writing 1 to FWEID1.MACTEED register will clear this bit.
3:2	RSV	R0-U	0H	- Reserved area. On read, 0 will be returned.
1	LTHTSEE	R!=W-RP	0H	L3 Table Security Error Enable Values: - 1'b0: Interrupt disabled. - 1'b1: Interrupt Enabled. Set conditions: - Writing 1 to this bit will set it. Clear conditions: - Writing 1 to FWEID1.LTHTSED register will clear this bit.
0	LTHTEEE	R!=W-P	0H	L3 Table ECC Error Enable Values: - 1'b0: Interrupt disabled. - 1'b1: Interrupt Enabled. Set conditions: - Writing 1 to this bit will set it. Clear conditions: - Writing 1 to FWEID1.LTHTEED register will clear this bit.

(6) FWEID1

Forwarding Engine Error Interrupt Disable 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV														FTEED	AREED
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV						L23US ED	L23UE ED	VLANT SED	VLANT EED	MACT SED	MACT EED	RSV		LTHTS ED	LTHTE ED

Bits	Bit name	RW-P	Initial value	Function description
31:18	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
17	FTEED	R0W-P	0H	FRER Table ECC Error Disable Functions: - Writing 1 to this bit will clear FWEIE1.FTEEE
16	AREED	R0W-P	0H	ATS RAM ECC Error Disable Functions: - Writing 1 to this bit will clear FWEIE1.AREEE .
15:10	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
9	L23USED	R0W-F	0H	Layer2/Layer3 Update Security Error Disable Functions: - Writing 1 to this bit will clear FWEIE1.L23USEE .
8	L23UEED	R0W-P	0H	Layer2/Layer3 Update Error Disable Functions: - Writing 1 to this bit will clear FWEIE1.L23UEEE .
7	VLANTSED	R0W-F	0H	VLAN Table Security Error Disable Functions: - Writing 1 to this bit will clear FWEIE1.VLANTSEE
6	VLANTEED	R0W-P	0H	VLAN Table ECC Error Disable Functions: - Writing 1 to this bit will clear FWEIE1.VLANTEE .
5	MACTSED	R0W-F	0H	MAC Table Security Error Disable Functions: - Writing 1 to this bit will clear FWEIE1.MACTSEE .
4	MACTEED	R0W-P	0H	MAC Table ECC Error Disable Functions: - Writing 1 to this bit will clear FWEIE1.MACTEEE .
3:2	RSV	R0-U	0H	- Reserved area. On read, 0 will be returned.
1	LTHTSED	R0W-F	0H	L3 Table Security Error Disable Functions: - Writing 1 to this bit will clear FWEIE1.LTHTSEE .
0	LTHTEED	R0W-P	0H	L3 Table ECC Error Disable Functions: - Writing 1 to this bit will clear FWEIE1.LTHTEEE .

(7) FWEIS2

Forwarding Engine Error Interrupt Status 2.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMFS[PSFP_MSDU_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: PSFP_MSDU_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PSFP_MSDU_N- 1:0	PMFS	R!=W-P	0H	<p>PSFP MSDU Filtering Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: Bit i is set when a descriptor is rejected by MSDU filter number i (refer to section 5.3.1.1). <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.

(8) FWEIE2

Forwarding Engine Error Enable Status 2.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMFE[PSFP_MSDU_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: PSFP_MSDU_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PSFP_MSDU_N- 1:0	PMFE	R!=W-P	0H	<p>PSFP MSDU Filtering Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt disabled. - 1'b1: Interrupt Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to one of these bits will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID2.PMFD register bit i will clear this register bit i.

(9) FWEID2

Forwarding Engine Error Disable Status 2.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMFD[PSFP_MSDU_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: PSFP_MSDU_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PSFP_MSDU_N- 1:0	PMFD	R0W-P	0H	PSFP MSDU Filtering Disable Functions: - Writing 1 to this register bit i will clear FWEIE2.PMFE register bit i.

(10) FWEIS3

Forwarding Engine Error Interrupt Status 3.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															GBPES
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV								PGFS[PSFP_GATE_N-1:0]							

Bits	Bit name	RW-P	Initial value	Function description
31:17	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
16	GBPES	R!=W-F	0H	<p>Gate Back Pressure Error Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: Back pressure happened at the input path of forwarding engine and it could have impacted PSFP gate filtering. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Some frames could be lost because of PSFP gate filtering. - SW: Forwarding engine back pressure is due to a too high throughput on the agents.
15: PSFP_GATE_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PSFP_GATE_N-1:0	PGFS	R!=W-P	0H	<p>PSFP Gate Filtering Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: Bit i is set when a descriptor is rejected by GATE filter number i (refer to section 5.3.1.2(3)). <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.

(11) FWEIE3

Forwarding Engine Error Enable Status 3

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															GBPEE
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV								PGFE[PSFP_GATE_N-1:0]							

Bits	Bit name	RW-P	Initial value	Function description
31:17	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
16	GBPEE	R!=W-F	0H	<p>Gate Back Pressure Error Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt disabled. - 1'b1: Interrupt Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID3.GBPED register will clear this bit.
15: PSFP_GATE_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PSFP_GATE_N-1:0	PGFE	R!=W-P	0H	<p>PSFP Gate Filtering Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Interrupt i disabled. - Bit i set to 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to one of these bits will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID3.PGFD register bit i will clear this register bit i.

(12) FWEID3

Forwarding Engine Error Disable Status 3.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															GBPED
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV								PGFD[PSFP_GATE_N-1:0]							

Bits	Bit name	RW-P	Initial value	Function description
31:17	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
16	GBPED	R0W-F	0H	Gate Back Pressure Error Disable Functions: - Writing 1 to this bit will clear FWEIE3.GBPEE register.
15: PSFP_GATE_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PSFP_GATE_N-1:0	PGFD	R0W-P	0H	PSFP Gate Filtering Disable Functions: - Writing 1 to this register bit i will clear FWEIE3.PGFE register bit i.

(13) FWEIS4

Forwarding Engine Error Interrupt Status 4.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV								GFGees[PSFP_GATE_N:0]							
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV								GFGes[PSFP_GATE_N:0]							

Bits	Bit name	RW-P	Initial value	Function description
31: PSFP_GATE_N+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PSFP_GATE_N+15: 16	GFGees	R!=W-P	0H	<p>Gate Filter Gate ECC Error Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: Bit i of this register is set when an ECC error is detected while reading the Gate RAM to control gate for Gate Filter i (This flag is not set when SW reads the gate RAM and an ECC error happens. In this case, ECC error detection should happen using FWPGFGR0.GFREF register). <p>This flag cannot be set a second time before Gate Filter i disable or switch reset.</p> <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Gate i will go back to initial gate state. - SW: Nothing if it is acceptable to operate with corresponding gate in initial gate state else Gate Filter i disable -> gate filter i setting or Gate Filter i disable or switch reset.
15: PSFP_GATE_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PSFP_GATE_N-1:0	GFGes	R!=W-P	0H	<p>Gate Filter Gate Error Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: Bit i of this register is set when Gate Filter i corresponding gate had no time to fetch the next gate state value until it starts. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Gate with restart during next cycle. - SW: If this error happens regularly, Gate filter i should be reconfigured with a different schedule (software issue because the minimum gate time is not respected). <p>Cautions:</p> <ul style="list-style-type: none"> - This error can happen for the following reasons: Gate Filter start time FWPGFCSTC0i/1i is set in the past, gPTP timer had an offset correction [gPTP] or the minimum gate time is not respected.

(14) FWEIE4

Forwarding Engine Error Enable Status 4

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV								GFGEEE[PSFP_GATE_N-1:0]							
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV								GFGEE[PSFP_GATE_N-1:0]							

Bits	Bit name	RW-P	Initial value	Function description
31: PSFP_GATE_N+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PSFP_GATE_N+15: 16	GFGEEE	R!=W-P	0H	<p>Gate Filter Gate ECC Error Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Interrupt i disabled. - Bit i set to 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to one of these bits will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID4.GFGEED register bit i will clear this register bit i.
15: PSFP_GATE_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PSFP_GATE_N-1:0	GFGEE	R!=W-P	0H	<p>Gate Filter Gate Error Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Interrupt i disabled. - Bit i set to 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to one of these bits will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID4.GFGED register bit i will clear this register bit i.

(15) FWEID4

Forwarding Engine Error Disable Status 4.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV								GFGEED[PSFP_GATE_N-1:0]							
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV								GFGED[PSFP_GATE_N-1:0]							

Bits	Bit name	RW-P	Initial value	Function description
31: PSFP_GATE_N+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PSFP_GATE_N+15: 16	GFGEED	R0W-P	0H	Gate Filter Gate ECC Error Disable Functions: - Writing 1 to this register bit i will clear FWEIE4.GFGEEE register bit i.
15: PSFP_GATE_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PSFP_GATE_N-1:0	GFGED	R0W-P	0H	Gate Filter Gate Error Disable Functions: - Writing 1 to this register bit i will clear FWEIE4.GFGEE register bit i.

(16) FWEIS50

Forwarding Engine Error Interrupt Status 5 0.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMRFS[PSFP_MTR_N-1:96]															

Bits	Bit name	RW-P	Initial value	Function description
PSFP_MTR_N-97:0	PMRFS	R!=W-P	0H	<p>PSFP Meter Filtering Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: Bit i is set when a descriptor is filtered by PSFP Meter filter number i (refer to section 5.3.1.3). <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.

(17) FWEIE50

Forwarding Engine Error Enable Status 5 0.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMRFE[PSFP_MTR_N-1:96]															

Bits	Bit name	RW-P	Initial value	Function description
PSFP_MTR_N-97:0	PMRFE	R!=W-P	0H	<p>PSFP Meter Filtering Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit I set to 1'b0: Interrupt I disabled. - Bit I set to 1'b1: Interrupt I Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to one of these bits will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID50.PMRFID register bit I will clear this register bit i.

(18) FWEID50

Forwarding Engine Error Disable Status 5 0.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMRFD[PSFP_MTR_N-1:96]															

Bits	Bit name	RW-P	Initial value	Function description
PSFP_MTR_N-97:0	PMRFD	R0W-P	0H	PSFP MeteR Filtering Disable Functions: - Writing 1 to this register bit i will clear FWEIE50.PMRFD register bit i.

(19) FWEIS51

Forwarding Engine Error Interrupt Status 5 1.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMRFS[95:64]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	PMRFS	R!=W-P	0H	<p>PSFP Meter Filtering Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: Bit i is set when a descriptor is filtered by PSFP Meter filter number i (refer to section 5.3.1.3). <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.

(20) FWEIE51

Forwarding Engine Error Enable Status 5 1.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMRFE[95:64]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	PMRFE	R!=W-P	0H	<p>PSFP MeteR Filtering Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Interrupt i disabled. - Bit i set to 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to one of these bits will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID51.PMRFID register bit i will clear this register bit i.

(21) FWEID51

Forwarding Engine Error Disable Status 5 1.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMRFD[95:64]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	PMRFD	R0W-P	0H	PSFP MeteR Filtering Disable Functions: - Writing 1 to this register bit i will clear FWEIE51.PMRFD register bit i.

(22) FWEIS52

Forwarding Engine Error Interrupt Status 5 2.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMRFS[63:32]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	PMRFS	R!=W-P	0H	<p>PSFP Meter Filtering Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: Bit i is set when a descriptor is filtered by PSFP Meter filter number i (refer to section 5.3.1.3). <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.

(23) FWEIE52

Forwarding Engine Error Enable Status 5 2.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMRFE[63:32]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	PMRFE	R!=W-P	0H	<p>PSFP Meter Filtering Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit I set to 1'b0: Interrupt I disabled. - Bit I set to 1'b1: Interrupt I Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to one of these bits will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID50.PMRFID register bit I will clear this register bit i.

(24) FWEID52

Forwarding Engine Error Disable Status 5 2.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMRFD[63:32]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	PMRFD	R0W-P	0H	PSFP MeteR Filtering Disable Functions: - Writing 1 to this register bit i will clear FWEIE50.PMRFD register bit i.

(25) FWEIS53

Forwarding Engine Error Interrupt Status 5 3.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMRFS[31:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	PMRFS	R!=W-P	0H	<p>PSFP Meter Filtering Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: Bit i is set when a descriptor is filtered by PSFP Meter filter number i (refer to section 5.3.1.3). <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.

(26) FWEIE53

Forwarding Engine Error Enable Status 5 3.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMRFE[31:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	PMRFE	R!=W-P	0H	<p>PSFP Meter Filtering Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Interrupt i disabled. - Bit i set to 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to one of these bits will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID51.PMRFID register bit i will clear this register bit i.

(27) FWEID53

Forwarding Engine Error Disable Status 5 3.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMRFD[31:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	PMRFD	R0W-P	0H	PSFP MeteR Filtering Disable Functions: - Writing 1 to this register bit i will clear FWEIE51.PMRFD register bit i.

(28) FWEIS60

Forwarding Engine Error Interrupt Status 6 0.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FFS[FRER_RECE_N-1:112]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FFS [111:96]															

Bits	Bit name	RW-P	Initial value	Function description
FRER_RECE_N-97:0	FFS	R!=W-P	0H	<p>FRER Filtering Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: If FRER rule $i+96$ is used for individual recovery, bit i is set when a descriptor is filtered by FRER rule number $i+96$ because of no sequence error or struck error (refer to section 5.3.2.3(2)(e)). - HW: If FRER rule $i+96$ is used for sequence recovery, bit i is set when a descriptor is filtered by FRER rule number $i+96$ because of no sequence error (refer to section 5.3.2.3(2)(f)). <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.

(29) FWEIE60

Forwarding Engine Error Interrupt Enable 6 0.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FFE[FRER_RECE_N-1:112]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FFE[111:96]															

Bits	Bit name	RW-P	Initial value	Function description
FRER_RECE_N-97:0	FFE	R!=W-P	0H	<p>FRER Filtering Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Interrupt i disabled. - Bit i set to 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to one of these bits will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID60.FFD[i+96] register bit i will clear this register bit i.

(30) FWEID60

Forwarding Engine Error Interrupt Disable 6 0.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FFD[FRER_RECE_N-1:112]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FFD[111:96]															

Bits	Bit name	RW-P	Initial value	Function description
FRER_RECE_N-97:0	FFD	R0W-P	0H	FRER Filtering Disable Functions: - Writing 1 to this register bit will clear FWEIE60.FFE[i+96] register bit i.

(31) FWEIS61

Forwarding Engine Error Interrupt Status 6 1.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FFS[95:80]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FFS [79:64]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	FFS	R!=W-P	0H	<p>FRER Filtering Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: If FRER rule $i+64$ is used for individual recovery, bit i is set when a descriptor is filtered by FRER rule number $i+64$ because of no sequence error or struck error (refer to section 5.3.2.3(2)(e)). - HW: If FRER rule $i+64$ is used for sequence recovery, bit i is set when a descriptor is filtered by FRER rule number $i+64$ because of no sequence error (refer to section 5.3.2.3(2)(f)). <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.

(32) FWEIE61

Forwarding Engine Error Interrupt Enable 6 1.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FFE[95:80]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FFE[79:64]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	FFE	R!=W-P	0H	<p>FRER Filtering Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Interrupt i disabled. - Bit i set to 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to one of these bits will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID61.FFD[i+64] register bit i will clear this register bit i.

(33) FWEID61

Forwarding Engine Error Interrupt Disable 6 1.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FFD[95:80]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FFD[79:64]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	FFD	R0W-P	0H	FRER Filtering Disable Functions: - Writing 1 to this register bit will clear FWEIE61.FFE[i+64] register bit i.

(34) FWEIS62

Forwarding Engine Error Interrupt Status 6 2.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FFS[63:48]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FFS [47:32]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	FFS	R!=W-P	0H	<p>FRER Filtering Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: If FRER rule $i+32$ is used for individual recovery, bit i is set when a descriptor is filtered by FRER rule number $i+32$ because of no sequence error or struck error (refer to section 5.3.2.3(2)(e)). - HW: If FRER rule $i+32$ is used for sequence recovery, bit i is set when a descriptor is filtered by FRER rule number $i+32$ because of no sequence error (refer to section 5.3.2.3(2)(f)). <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.

(35) FWEIE62

Forwarding Engine Error Interrupt Enable 6 2.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FFE[63:48]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FFE[47:32]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	FFE	R!=W-P	0H	<p>FRER Filtering Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Interrupt i disabled. - Bit i set to 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to one of these bits will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID62.FFD[i+32] register bit i will clear this register bit i.

(36) FWEID62

Forwarding Engine Error Interrupt Disable 6 2.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FFD[63:48]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FFD[47:32]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	FFD	R0W-P	0H	FRER Filtering Disable Functions: - Writing 1 to this register bit will clear FWEIE62.FFE[i+32] register bit i.

(37) FWEIS63

Forwarding Engine Error Interrupt Status 6 3.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FFS[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FFS [15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	FFS	R!=W-P	0H	<p>FRER Filtering Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: If FRER rule i is used for individual recovery, bit i is set when a descriptor is filtered by FRER rule number i because of no sequence error or struck error (refer to section 5.3.2.3(2)(e)). - HW: If FRER rule i is used for sequence recovery, bit i is set when a descriptor is filtered by FRER rule number i because of no sequence error (refer to section 5.3.2.3(2)(f)). <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.

(38) FWEIE63

Forwarding Engine Error Interrupt Enable 6 3.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FFE[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FFE[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	FFE	R!=W-P	0H	<p>FRER Filtering Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Interrupt i disabled. - Bit i set to 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to one of these bits will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID63.FFD[i] register bit i will clear this register bit i.

(39) FWEID63

Forwarding Engine Error Interrupt Disable 6 3.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FFD[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FFD[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	FFD	R0W-P	0H	FRER Filtering Disable Functions: - Writing 1 to this register bit will clear FWEIE63.FFE[i] register bit i.

(40) FWEIS70

Forwarding Engine Error Interrupt Status 7 0.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FOORS[FRER_RECE_N-1:112]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOORS [111:96]															

Bits	Bit name	RW-P	Initial value	Function description
FRER_RECE_N-97:0	FOORS	R=W-P	0H	<p>FRER Out Of Range Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: If FRER rule $i+96$ is used with match algorithm, bit i is set when a descriptor an out of order error happens (refer to section 5.3.2.3(2)(e) and 5.3.2.3(2)(f)). - HW: If FRER rule $i+96$ is used with vector algorithm, bit i is set when a descriptor is filtered by FRER rule number $i+96$ because of an out of range error (refer to section 5.3.2.3(2)(e) and 5.3.2.3(2)(f)). <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.

(41) FWEIE70

Forwarding Engine Error Interrupt Enable 7 0.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FOORE[FRER_RECE_N-1:112]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOORE[111:96]															

Bits	Bit name	RW-P	Initial value	Function description
FRER_RECE_N-97:0	FOORE	R!=W-P	0H	<p>FRER Out Of Range Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Interrupt i disabled. - Bit i set to 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to one of these bits will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID70.FOORD[i+96] register bit i will clear this register bit i.

(42) FWEID70

Forwarding Engine Error Interrupt Disable 7 0.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FOORD[FRER_RECE_N-1:112]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOORD[111:96]															

Bits	Bit name	RW-P	Initial value	Function description
FRER_RECE_N-97:0	FOORD	R0W-P	0H	FRER Out Of Range Disable Functions: - Writing 1 to this register bit i will clear FWEIE70.FOORE[i+96] register bit i.

(43) FWEIS71

Forwarding Engine Error Interrupt Status 7 1.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FOORS[95:80]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOORS [79:64]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	FOORS	R=W-P	0H	<p>FRER Out Of Range Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: If FRER rule i+64 is used with match algorithm, bit i is set when a descriptor an out of order error happens (refer to section 5.3.2.3(2)(e) and 5.3.2.3(2)(f)). - HW: : If FRER rule i+64 is used with vector algorithm, bit i is set when a descriptor is filtered by FRER rule number i+64 because of an out of range error(refer to section 5.3.2.3(2)(e) and 5.3.2.3(2)(f)). <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.

(44) FWEIE71

Forwarding Engine Error Interrupt Enable 7 1.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FOORE[95:80]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOORE[79:64]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	FOORE	R!=W-P	0H	<p>FRER Out Of Range Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Interrupt i disabled. - Bit i set to 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to one of these bits will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID71.FOORD[i+64] register bit i will clear this register bit i.

(45) FWEID71

Forwarding Engine Error Interrupt Disable 7 1.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FOORD[95:80]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOORD[79:64]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	FOORD	R0W-P	0H	FRER Out Of Range Disable Functions: - Writing 1 to this register bit i will clear FWEIE71.FOORE[i+64] register bit i.

(46) FWEIS72

Forwarding Engine Error Interrupt Status 7 2.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FOORS[63:48]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOORS [47:32]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	FOORS	R=W-P	0H	<p>FRER Out Of Range Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: If FRER rule i+32 is used with match algorithm, bit i is set when a descriptor an out of order error happens (refer to section 5.3.2.3(2)(e) and 5.3.2.3(2)(f)). - HW: : If FRER rule i+32 is used with vector algorithm, bit i is set when a descriptor is filtered by FRER rule number i+32 because of an out of range error(refer to section 5.3.2.3(2)(e) and 5.3.2.3(2)(f)). <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.

(47) FWEIE72

Forwarding Engine Error Interrupt Enable 7 2.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FOORE[63:48]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOORE[47:32]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	FOORE	R!=W-P	0H	<p>FRER Out Of Range Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Interrupt i disabled. - Bit i set to 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to one of these bits will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID72.FOORD[i+32] register bit i will clear this register bit i.

(48) FWEID72

Forwarding Engine Error Interrupt Disable 7 2.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FOORD[63:48]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOORD[47:32]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	FOORD	R0W-P	0H	FRER Out Of Range Disable Functions: - Writing 1 to this register bit i will clear FWEIE72.FOORE[i+32] register bit i.

(49) FWEIS73

Forwarding Engine Error Interrupt Status 7 3.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FOORS[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOORS [15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	FOORS	R!=W-P	0H	<p>FRER Out Of Range Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: If FRER rule i is used with match algorithm, bit i is set when a descriptor an out of order error happens (refer to section 5.3.2.3(2)(e) and 5.3.2.3(2)(f)). - HW: : If FRER rule i is used with vector algorithm, bit i is set when a descriptor is filtered by FRER rule number i because of an out of range error(refer to section 5.3.2.3(2)(e) and 5.3.2.3(2)(f)). <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.

(50) FWEIE73

Forwarding Engine Error Interrupt Enable 7 3.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FOORE[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOORE[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	FOORE	R!=W-P	0H	<p>FRER Out Of Range Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Interrupt i disabled. - Bit i set to 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to one of these bits will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID73.FOORD[i] register bit i will clear this register bit i.

(51) FWEID73

Forwarding Engine Error Interrupt Disable 7 3.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FOORD[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOORD[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	FOORD	R0W-P	0H	FRER Out Of Range Disable Functions: - Writing 1 to this register bit i will clear FWEIE73.FOORE[i] register bit i.

(52) FWEIS80

Forwarding Engine Error Interrupt Status 8 0.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TOS[FRER_RECE_N-1:112]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOS[111:96]															

Bits	Bit name	RW-P	Initial value	Function description
FRER_RECE_N-97:0	TOS	R!=W-P	0H	<p>TimeOut Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When timeout happens for FRER rule i+96 (refer to section 5.3.2.3(3)). <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.

(53) FWEIE80

Forwarding Engine Error Interrupt Enable 8 0.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TOE[FRER_RECE_N-1:112]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOE[111:96]															

Bits	Bit name	RW-P	Initial value	Function description
FRER_RECE_N-97:0	TOE	R!=W-P	0H	<p>TimeOut Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Interrupt i disabled. - Bit i set to 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to one of these bits will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID80.TOD[i+96] register bit i will clear this register bit i.

(54) FWEID80

Forwarding Engine Error Interrupt Disable 8 0.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TOD[FRER_RECE_N-1:112]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOD[111:96]															

Bits	Bit name	RW-P	Initial value	Function description
FRER_RECE_N-97:0	TOD	R0W-P	0H	<p>TimeOut Disable</p> <p>Functions:</p> <ul style="list-style-type: none"> - Writing 1 to this register bit i will clear FWEIE80.TOE[i+96] register bit i.

(55) FWEIS81

Forwarding Engine Error Interrupt Status 8 1.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TOS[95:80]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOS [79:64]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	TOS	R!=W-P	0H	<p>TimeOut Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When timeout happens for FRER rule i+64 (refer to section 5.3.2.3(3)). <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.

(56) FWEIE81

Forwarding Engine Error Interrupt Enable 8 1.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TOE[95:80]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOE[79:64]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	TOE	R!=W-P	0H	<p>TimeOut Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Interrupt i disabled. - Bit i set to 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to one of these bits will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID81.TOD[i+64] register bit i will clear this register bit i.

(57) FWEID81

Forwarding Engine Error Interrupt Disable 8 1.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TOD[95:80]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOD[79:64]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	TOD	R0W-P	0H	<p>TimeOut Disable</p> <p>Functions:</p> <ul style="list-style-type: none"> - Writing 1 to this register bit i will clear FWEIE81.TOE[i+64] register bit i.

(58) FWEIS82

Forwarding Engine Error Interrupt Status 8 2.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TOS[63:48]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOS [47:32]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	TOS	R!=W-P	0H	<p>TimeOut Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When timeout happens for FRER rule i+32 (refer to section 5.3.2.3(3)). <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.

(59) FWEIE82

Forwarding Engine Error Interrupt Enable 8 2.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TOE[63:48]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOE[47:32]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	TOE	R!=W-P	0H	<p>TimeOut Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Interrupt i disabled. - Bit i set to 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to one of these bits will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID82.TOD[i+32] register bit i will clear this register bit i.

(60) FWEID82

Forwarding Engine Error Interrupt Disable 8 2.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TOD[63:48]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOD[47:32]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	TOD	R0W-P	0H	<p>TimeOut Disable</p> <p>Functions:</p> <ul style="list-style-type: none"> - Writing 1 to this register bit i will clear FWEIE82.TOE[i+32] register bit i.

(61) FWEIS83

Forwarding Engine Error Interrupt Status 8 3.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TOS[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOS [15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	TOS	R!=W-P	0H	<p>TimeOut Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: When timeout happens for FRER rule i (refer to section 5.3.2.3(3)). <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it. <p>Error recovery:</p> <ul style="list-style-type: none"> - HW: Descriptor corresponding frame is rejected.

(62) FWEIE83

Forwarding Engine Error Interrupt Enable 8 3.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TOE[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOE[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	TOE	R!=W-P	0H	<p>TimeOut Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Interrupt i disabled. - Bit i set to 1'b1: Interrupt i Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to one of these bits will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWEID83.TOD[i] register bit i will clear this register bit i.

(63) FWEID83

Forwarding Engine Error Interrupt Disable 8 3.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TOD[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOD[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	TOD	R0W-P	0H	<p>TimeOut Disable</p> <p>Functions:</p> <ul style="list-style-type: none"> - Writing 1 to this register bit i will clear FWEIE83.TOE[i] register bit i.

(64) FWMIS0

Forwarding Engine Monitoring Interrupt Status 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
RSV												LTHEDR S	MACED RS	MACADA S	RSV		
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
RSV												VLANTF S	MACUT FS	MACS TFS	LTHUT FS	LTHST FS	PFTFS

Bits	Bit name	RW-P	Initial value	Function description
31:20	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
19	LTHEDRS	R!=W-P	0H	<p>L3/L2 stream Entry Deleted Recovery Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: A L3/L2 stream entry has been deleted by self-recovery. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it.
18	MACEDRS	R!=W-P	0H	<p>MAC Entry Deleted Recovery Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: A MAC entry has been deleted by self-recovery. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it.
17	MACADAS	R!=W-P	0H	<p>MAC Address Deleted Aging Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: A MAC address has been suppressed by aging or dynamic entry delete. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it.
16:6	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
5	VLANTFS	R!=W-P	0H	<p>VLAN Table Full Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: VLAN table becomes full. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it.
4	MACUTFS	R!=W-P	0H	<p>MAC Unsecure Table Full Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: MAC unsecure table becomes full. (Excluding hardware learning area.) <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it.
3	MACSTFS	R!=W-P	0H	<p>MAC Secure Table Full Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: MAC secure table becomes full. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it.

2	LTHUTFS	R!=W-P	0H	<p>L3/L2 Unsecure Table Full Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: L3/L2 unsecure table becomes full. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it.
1	LTHSTFS	R!=W-P	0H	<p>L3/L2 Secure Table Full Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: L3/L2 secure table becomes full. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it.
0	PFTFS	R!=W-P	0H	<p>PerFect Table Full Status</p> <p>Set conditions:</p> <ul style="list-style-type: none"> - HW: Perfect table becomes full. <p>Clear conditions:</p> <ul style="list-style-type: none"> - SW: Writing 1 to one of these bits will clear it.

(65) FWMIE0

Forwarding Engine Monitoring Interrupt Enable 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
RSV												LTHEDR E	MACED RE	MACADA E	RSV		
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
RSV												VLANTF E	MACUT FE	MACS TFE	LTHUT FE	LTHST FE	PFTFE

Bits	Bit name	RW-P	Initial value	Function description
31:20	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
19	LTHEDRE	R!=W-P	0H	<p>L3/L2 stream Entry Deleted Recovery Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt disabled. - 1'b1: Interrupt Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWMID0.LTHEDRD register will clear this bit.
18	MACEDRE	R!=W-P	0H	<p>MAC Entry Deleted Recovery Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt disabled. - 1'b1: Interrupt Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWMID0.MACEDRD register will clear this bit.
17	MACADAE	R!=W-P	0H	<p>MAC Address Deleted Aging Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt disabled. - 1'b1: Interrupt Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWMID0.MACADAD register will clear this bit.
16:6	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
5	VLANTFE	R!=W-P	0H	<p>VLAN Table Full Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt disabled. - 1'b1: Interrupt Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWMID0.VLANTFD register will clear this bit.

4	MACUTFE	R!=W-P	0H	<p>MAC Unsecure Table Full Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt disabled. - 1'b1: Interrupt Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWMID0.MACUTFD register will clear this bit.
3	MACSTFE	R!=W-P	0H	<p>MAC Secure Table Full Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt disabled. - 1'b1: Interrupt Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWMID0.MACSTFD register will clear this bit.
2	LTHUTFE	R!=W-P	0H	<p>L3/L2 Unsecure Table Full Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt disabled. - 1'b1: Interrupt Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWMID0.LTHUTFD register will clear this bit.
1	LTHSTFE	R!=W-P	0H	<p>L3/L2 Secure Table Full Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt disabled. - 1'b1: Interrupt Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWMID0.LTHSTFD register will clear this bit.
0	PFTFE	R!=W-P	0H	<p>PerFect Table Full Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Interrupt disabled. - 1'b1: Interrupt Enabled. <p>Set conditions:</p> <ul style="list-style-type: none"> - Writing 1 to this bit will set it. <p>Clear conditions:</p> <ul style="list-style-type: none"> - Writing 1 to FWMID0.PFTFD register will clear this bit.

(66) FWMID0

Forwarding Engine Monitoring Interrupt Disable 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
RSV												LTHEDR D	MACED RD	MACADA D	RSV		
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
RSV												VLANTF D	MACUT FD	MACS TFD	LTHUT FD	LTHST FD	PFTFD

Bits	Bit name	RW-P	Initial value	Function description
31:20	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
19	LTHEDRD	ROW-P	0H	L3/L2 stream Entry Deleted Recovery Disable Functions: - Writing 1 to this bit will clear FWMIE0.LTHEDRE .
18	MACEDRD	ROW-P	0H	MAC Entry Deleted Recovery Disable Functions: - Writing 1 to this bit will clear FWMIE0.MACEDRE .
17	MACADAD	ROW-P	0H	MAC Address Deleted Aging Disable Functions: - Writing 1 to this bit will clear FWMIE0.MACADAD
16:6	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
5	VLANTFD	ROW-P	0H	VLAN Table Full Disable Functions: - Writing 1 to this bit will clear FWMIE0.VLANTFE .
4	MACUTFD	ROW-P	0H	MAC Unsecure Table Full Disable Functions: - Writing 1 to this bit will clear FWMIE0.MACUTFE .
3	MACSTFD	ROW-P	0H	MAC Secure Table Full Disable Functions: - Writing 1 to this bit will clear FWMIE0.MACSTFE .
2	LTHUTFD	ROW-P	0H	L3/L2 Unsecure Table Full Disable Functions: - Writing 1 to this bit will clear FWMIE0.LTHUTFE .
1	LTHSTFD	ROW-P	0H	L3/L2 Secure Table Full Disable Functions: - Writing 1 to this bit will clear FWMIE0.LTHSTFE .
0	PFTFD	ROW-P	0H	PerFect Table Full Disable Functions: - Writing 1 to this bit will clear FWMIE0.PFTFE .

3.3.4 Forwarding Engine Security registers

(1) FWSCR0

Forwarding Engine Security Configuration Register 0.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV / FMRSLi[PORT_N-1:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV					CRSL	MIRSL	EIRSL	WMRSL	SDMPRS L	EMPRSL	CMPRSL	CLPRSL	CEPRSL	TTRSL	MRSRL

Bits	Bit name	RW-P	Initial value	Function description
31:PORT_N+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_N+15:16	FMRSLi	RW-F	0H	<p>Forwarding Mask Register Security Level i.</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Forwarding Mask registers can only be accessed by the APB secure interface - 1'b1: Forwarding Mask registers can be accessed by both APBs <p>Forwarding Mask registers include the following registers:</p> <ul style="list-style-type: none"> - FWPC1i.LTHFMI - FWPC2i.LTWFMi
15:11	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.

				Counter Register Security Level. Values: <ul style="list-style-type: none">- 1'b0: Counter registers can only be accessed by the APB secure interface- 1'b1: Counter registers can be accessed by both APBs Counter registers include the following registers: <ul style="list-style-type: none">- FWCTFDCNi- FWDDFDCNi- FWLTHFDCNi- FWLTWFDCNi- FWPBFDCCNi- FWMHLCNi- FWICRDCNi- FWWMRDCNi- FWCTRDCNi- FWDDRDCNi- FWLTHRDCNi- FWLTWRDCNi- FWPBRDCNi- FWPMFDCNi- FWPGFDCNi- FWPMGDCNi- FWPMYDCNi- FWPMRDCNi- FWFRPPCNI- FWFRDPCNI- FWBLFCNi- FWALFCNi
10	CRSL	RW-F	0H	Monitoring Interrupt Register Security Level Values: <ul style="list-style-type: none">- 1'b0: Monitoring Interrupt registers can only be accessed by the APB secure interface- 1'b1: Monitoring Interrupt registers can be accessed by both APBs Error Interrupt registers include the following registers: <ul style="list-style-type: none">- FWMIS0- FWMIE0- FWMID0
9	MIRSL	RW-F	0H	Error Interrupt Register Security Level Values: <ul style="list-style-type: none">- 1'b0: Error Interrupt registers can only be accessed by the APB secure interface- 1'b1: Error Interrupt registers can be accessed by both APBs Error Interrupt registers include the following registers: <ul style="list-style-type: none">- FWEIS1- FWEIE1- FWEID1
8	EIRSL	RW-F	0H	Error Interrupt Register Security Level Values: <ul style="list-style-type: none">- 1'b0: Error Interrupt registers can only be accessed by the APB secure interface- 1'b1: Error Interrupt registers can be accessed by both APBs Error Interrupt registers include the following registers: <ul style="list-style-type: none">- FWEIS1- FWEIE1- FWEID1

				WaterMark Register Security Level Values: <ul style="list-style-type: none">- 1'b0: WaterMark registers can only be accessed by the APB secure interface- 1'b1: WaterMark registers can be accessed by both APBs WaterMark registers include the following registers: <ul style="list-style-type: none">- FWIBWMC- FWLBWMCi (for all i)- FWEIS0i.WMCFSi (for all i)- FWEIS0i.WMFFSi (for all i)- FWEIS0i.WMIUFSi (for all i)- FWEIE0i.WMCFEi (for all i)- FWEIE0i.WMFFEi (for all i)- FWEIE0i.WMIUFEi (for all i)- FWEID0i.WMCFDi (for all i)- FWEID0i.WMFFDi (for all i)- FWEID0i.WMIUFDi (for all i)
7	WMRSL	RW-F	0H	Source-Destination and Source Mirroring Path Register Security Level Values: <ul style="list-style-type: none">- 1'b0: Source-Destination and Source Mirroring Path registers can only be accessed by the APB secure interface- 1'b1: Source-Destination and Source Mirroring Path registers can be accessed by both APBs Source-Destination Mirroring Path registers include the following registers: <ul style="list-style-type: none">- FWSDMPTC- FWSDMPVC- FWSDMPL23URC- FWSMPTC- FWSMPVC- FWSMPL23URC
6	SDMPRL	RW-F	0H	Ethernet Mirroring Path Register Security Level Values: <ul style="list-style-type: none">- 1'b0: Ethernet Mirroring Path registers can only be accessed by the APB secure interface- 1'b1: Ethernet Mirroring Path registers can be accessed by both APBs Ethernet Mirroring Path registers include the following registers: <ul style="list-style-type: none">- FWEMPTC- FWEMPL23URC
5	EMPRSL	RW-F	0H	CPU Mirroring Path Register Security Level Values: <ul style="list-style-type: none">- 1'b0: CPU Mirroring Path registers can only be accessed by the APB secure interface- 1'b1: CPU Mirroring Path registers can be accessed by both APBs CPU Mirroring Path registers include the following registers: <ul style="list-style-type: none">- FWCMPTC- FWCMPL23URC
4	CMPRSL	RW-F	0H	CPU Learning Path Register Security Level Values: <ul style="list-style-type: none">- 1'b0: CPU Learning Path registers can only be accessed by the APB secure interface- 1'b1: CPU Learning Path registers can be accessed by both APBs CPU Learning Path registers include the following registers: <ul style="list-style-type: none">- FWCLPTC- FWCLPRC
3	CLPRSL	RW-F	0H	

2	CEPRSL	RW-F	0H	<p>CPU Exceptional Path Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: CPU Exceptional Path registers can only be accessed by the APB secure interface - 1'b1: CPU Exceptional Path registers can be accessed by both APBs <p>CPU Exceptional Path registers include the following registers:</p> <ul style="list-style-type: none"> - FWCEPTC - FWCEPRC0 - FWCEPRC1 - FWCEPRC2
1	TTRSL	RW-F	0H	<p>TAG TPID Register Security Level.</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: TAG TPID registers can only be accessed by the APB secure interface - 1'b1: TAG TPID registers can be accessed by both APBs <p>TAG TPID registers include the following registers:</p> <ul style="list-style-type: none"> - FWTTC0 - FWTTC1
0	MRSL	RW-F	0H	<p>Mode Register Security Level.</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Mode registers can only be accessed by the APB secure interface - 1'b1: Mode registers can be accessed by both APBs <p>Mode registers include the following registers:</p> <ul style="list-style-type: none"> - FWGC

(2) FWSCR1

Forwarding Engine Security Configuration Register 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV / DDRSL[PORT_SLOW_N -1:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV															

Bits	Bit name	RW-P	Initial value	Function description
31:PORT_SLOW_N+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
POR T_SLOW_N+15:16	DDRSL	RW-F	0H	<p>Direct Descriptor Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Port i Direct Descriptor registers can only be accessed by the APB secure interface - Bit i set to 1'b1: Port i Direct Descriptor registers can be accessed by both APBs <p>Port i Direct Descriptor registers include the following registers:</p> <ul style="list-style-type: none"> - FWPC1i.DDEi - FWEIS0{i+PORT_TIME_N}.DDES{i+PORT_TIME_N} - FWEIS0{i+PORT_TIME_N}.DDNTFS{i+PORT_TIME_N} - FWEIE0{i+PORT_TIME_N}.DDEE{i+PORT_TIME_N} - FWEIE0{i+PORT_TIME_N}.DDNTFE{i+PORT_TIME_N} - FWEID0{i+PORT_TIME_N}.DDED{i+PORT_TIME_N} - FWEID0{i+PORT_TIME_N}.DDNTFD{i+PORT_TIME_N}
15:0	RSV	R0-U	0H	- Reserved area. On read, 0 will be returned.

(3) FWSCR2

Forwarding Engine Security Configuration Register 2

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV / BLRSL[PORT_N-1:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / PFALRSL[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:PORT_N+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_N+15:16	BLRSL	RW-F	0H	<p>Block List Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Port i Block list registers can only be accessed by the APB secure interface - Bit i set to 1'b1: Port i Block list registers can be accessed by both APBs <p>Block list registers include the following registers:</p> <ul style="list-style-type: none"> - FWPC1i.BLSLDi - FWPC1i.BLEi <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: Setting this register to 1 is not recommended as it causes security issues.
15:PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_N-1:0	PFALRSL	RW-F	0H	<p>Perfect Filter Acceptance List Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Port i Acceptance list registers can only be accessed by the APB secure interface - Bit i set to 1'b1: Port i Acceptance list registers can be accessed by both APBs <p>Acceptance list registers include the following registers:</p> <ul style="list-style-type: none"> - FWPC1i.PFALSLDi - FWPC1i.PFALEi[1:0] <p>Restrictions:</p> <ul style="list-style-type: none"> - SW: Setting this register to 1 is not recommended as it causes security issues.

(4) FWSCR3

Forwarding Engine Security Configuration Register 3

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / PCL23URSL[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_N-1:0	PCL23URSL	RW-F	0H	<p>Port Configuration Layer2/Layer3 Update Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Port i follow registers can only be accessed by the APB secure interface - Bit i set to 1'b1: Port i follow registers can be accessed by both APBs <p>Acceptance list registers include the following registers:</p> <ul style="list-style-type: none"> - FWPC3i.LTHFMDi[PORT_N-1:0] - FWPC3i.L23UOEi

(5) FWSCR4

Forwarding Engine Security Configuration Register 4

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / PIFRSL[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_N-1:0	PIFRSL	RW-F	0H	<p>Port and IPV Filtering Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Port i follow registers can only be accessed by the APB secure interface - Bit i set to 1'b1: Port i follow registers can be accessed by both APBs <p>Acceptance list registers include the following registers:</p> <ul style="list-style-type: none"> - FWPIFPLij (j = all)

(6) FWSCRTOi

Forwarding Engine Security Configuration Register Two byte filter i. (i=0..PFL_TWBF_N/32-1)

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TWBFRSL[i*32+31:i*32+16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TWBFRSL[i*32+15:i*32]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	TWBFRSL	RW-F	0H	<p>TWo Byte Filter Register Security Level</p> <p>Values: (j=0..PFL_TWBF_N-1)</p> <ul style="list-style-type: none"> - Bit j set to 1'b0: Two Byte Filter registers for filter number j can only be accessed by the APB secure interface - Bit j set to 1'b1: Two Byte Filter registers for filter number j can be accessed by both APBs <p>Two Byte Filter registers for filter number j include the following registers:</p> <ul style="list-style-type: none"> - FWTWBFCj - FWTWBVFVCj

(7) FWSCRTHi

Forwarding Engine Security Configuration Register THree byte filter i. (i=0..PFL_THBF_N/32-1)

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
THBFRSL[*32+31:i*32+16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
THBFRSL[i*32+15:i*32]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	THBFRSL	RW-F	0H	<p>THree Byte Filter Register Security Level</p> <p>Values: (j=0..PFL_THBF_N-1)</p> <ul style="list-style-type: none"> - Bit j set to 1'b0: Three Byte Filter registers for filter number j can only be accessed by the APB secure interface - Bit j set to 1'b1: Three Byte Filter registers for filter number j can be accessed by both APBs <p>Three Byte Filter registers for filter number j include the following registers:</p> <ul style="list-style-type: none"> - FWTHBFCj - FWTHBFV0Cj - FWTHBFV1Cj

(8) FWSCRFOi

Forwarding Engine Security Configuration Register FOur byte filter i. (i=0..PFL_FOBF_N/32-1)

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FOBFRSL[*32+31:i*32+16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOBFRSL[i*32+15:i*32]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	FOBFRSL	RW-F	0H	<p>FOur Byte Filter Register Security Level</p> <p>Values: (j=0..PFL_FOBF_N-1)</p> <ul style="list-style-type: none"> - Bit j set to 1'b0: Four Byte Filter registers for filter number j can only be accessed by the APB secure interface - Bit j set to 1'b1: Four Byte Filter registers for filter number j can be accessed by both APBs <p>Four Byte Filter registers for filter number j include the following registers:</p> <ul style="list-style-type: none"> - FWFOBFCj - FWFOBFV0Cj - FWFOBFV1Cj

(9) FWSCRRAi

Forwarding Engine Security Configuration Register RAnge byte filter i. (i=0..PFL_RAGF_N/32-1)

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RFRSL[i*32+31:i*32+16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFRSL[i*32+15:i*32]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	RFRSL	RW-F	0H	<p>Range Filter Register Security Level</p> <p>Values: (j=0..PFL_RAGF_N-1)</p> <ul style="list-style-type: none"> - Bit j set to 1'b0: Range Filter registers for filter number j can only be accessed by the APB secure interface - Bit j set to 1'b1: Range Filter registers for filter number j can be accessed by both APBs <p>Range Filter registers for filter number j include the following registers:</p> <ul style="list-style-type: none"> - FWRFCj - FWRFSVCj - FWRFEVCj

(10) FWSCRCAi

Forwarding Engine Security Configuration Register CAscade filter i. (i=0..PFL_CADF_N/32-1)

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CFRSL[i*32+31:i*32+16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFRSL[i*32+15:i*32]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	CFRSL	RW-F	0H	<p>Cascade Filter Register Security Level</p> <p>Values: (j=0..PFL_CADF_N-1)</p> <ul style="list-style-type: none"> - Bit j set to 1'b0: Cascade Filter registers for filter number j + 32 can only be accessed by the APB secure interface - Bit j set to 1'b1: Cascade Filter registers for filter number j + 32 can be accessed by both APBs <p>Cascade Filter registers for filter number j + 32 include the following registers:</p> <ul style="list-style-type: none"> - FWCFCj - FWCFMCj* <p>Recommendations:</p> <ul style="list-style-type: none"> - It is recommended to reserve cascade filter access to secure APB for higher cascade filter number.

(11) FWSCR21

Forwarding Engine Security Configuration Register 21

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV / IP4RSL[PORT_N-1:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / IP6RSL[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:PORT_N+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_N+15:16	IP4RSL	RW-F	0H	<p>IPv4 Register Security Level Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Port i IPv4 registers can only be accessed by the APB secure interface - Bit i set to 1'b1: Port i IPv4 registers can be accessed by both APBs <p>Port i IPv4 registers include the following registers:</p> <ul style="list-style-type: none"> - FWPC0i.IP4UEi - FWPC0i.IP4TEi - FWPC0i.IP4OEi
15:PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_N-1:0	IP6RSL	RW-F	0H	<p>IPv6 Register Security Level Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Port i IPv6 registers can only be accessed by the APB secure interface - Bit i set to 1'b1: Port i IPv6 registers can be accessed by both APBs <p>Port i IPv6 registers include the following registers:</p> <ul style="list-style-type: none"> - FWPC0i.IP6UEi - FWPC0i.IP6TEi - FWPC0i.IP6OEi

(12) FWSCR22

Forwarding Engine Security Configuration Register 22

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
RSV														L2SCRS L	IP6CRSL	IP4CRSL
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
RSV / L2SRSL[PORT_N-1:0]																

Bits	Bit name	RW-P	Initial value	Function description
31:19	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
18	L2SCRSL	RW-F	0H	<p>Layer 2 Stream Configuration Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Layer 2 Configuration registers can only be accessed by the APB secure interface - 1'b1: Layer 2 Configuration registers can be accessed by both APBs <p>IPv6 Configuration registers include the following registers:</p> <ul style="list-style-type: none"> - FWL2SC
17	IP6CRSL	RW-F	0H	<p>IPv6 Configuration Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: IPv6 Configuration registers can only be accessed by the APB secure interface - 1'b1: IPv6 Configuration registers can be accessed by both APBs <p>IPv6 Configuration registers include the following registers:</p> <ul style="list-style-type: none"> - FWIP6SC - FWIP6OC
16	IP4CRSL	RW-F	0H	<p>IPv4 Configuration Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: IPv4 Configuration registers can only be accessed by the APB secure interface - 1'b1: IPv4 Configuration registers can be accessed by both APBs <p>IPv4 Configuration registers include the following registers:</p> <ul style="list-style-type: none"> - FWIP4SC
15:PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_N-1:0	L2SRSL	RW-F	0H	<p>Layer 2 Stream Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Port i Layer 2 Stream registers can only be accessed by the APB secure interface - Bit i set to 1'b1: Port i Layer 2 Stream registers can be accessed by both APBs <p>Port i Layer 2 Stream registers include the following registers:</p> <ul style="list-style-type: none"> - FWPC0i.L2SEi

(13) FWSCR23

Forwarding Engine Security Configuration Register 23

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															LTHTMR SL
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / LTHTRSL[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:17	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
16	LTHTMRSL	RW-F	0H	<p>Layer 3 Table Monitoring Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Layer 3 Table Monitoring registers can only be accessed by the APB secure interface - 1'b1: Layer 3 Table Monitoring registers can be accessed by both APBs <p>Layer 3 Table Monitoring registers include the following registers:</p> <ul style="list-style-type: none"> - FWLTHTIM - FWLTHTEM0 - FWLTHTEM1
15:PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_N-1:0	LTHTRSL	RW-F	0H	<p>Layer 3 Table Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Port i Layer 3 Table registers can only be accessed by the APB secure interface - Bit i set to 1'b1: Port i Layer 3 Table registers can be accessed by both APBs <p>Port i Layer 3 Table registers include the following registers:</p> <ul style="list-style-type: none"> - FWPC0i.LTHTAI - FWPC0i.LTHRUSi - FWPC0i.LTHTDDMi - FWEIS0i.LTHUFSi - FWEIS0i.LTHNTFSi - FWEIS0i.LTHSPFSi - FWEIS0.i.LTHALFSi - FWEIS0.i.LTHBLFSi - FWEIE0i.LTHUFEi - FWEIE0i.LTHNTFEi - FWEIE0i.LTHSPFEi - FWEIE0.i.LTHALFEi - FWEIE0.i.LTHBLFEi - FWEID0i.LTHUFDi - FWEID0i.LTHNTFDi - FWEID0i.LTHSPFDi - FWEID0.i.LTHALFDi - FWEID0.i.LTHBLFDi

(14) FWSCR24

Forwarding Engine Security Configuration Register 24

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															LTWHLRL SL
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / LTWHLPPRSL[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:17	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
16	LTWHLRLSL	RW-F	0H	<p>Layer 2 Hardware Learning Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Layer 2 hardware learning registers can only be accessed by the APB secure interface - 1'b1: Layer 2 hardware learning registers can be accessed by both APBs <p>Layer 2 Hardware learning registers include the following registers:</p> <ul style="list-style-type: none"> - FWMACHWLC0/1
15:PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_N-1:0	LTWHLPPRSL	RW-F	0H	<p>Layer 2 Hardware Learning Per Port Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Layer 2 hardware learning per port register i can only be accessed by the APB secure interface - Bit i set to 1'b1: Layer 2 hardware learning per port register i can be accessed by both APBs <p>Layer 2 Hardware learning registers include the following register i:</p> <ul style="list-style-type: none"> - FWMACHWLC2i

(15) FWSCR25

Forwarding Engine Security Configuration Register 25

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV														LTWARS	LTWTMR
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / LTWTRSL[PORT_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:18	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
17	LTWARSL	RW-F	0H	<p>Layer 2 Aging Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Layer 2 Aging registers can only be accessed by the APB secure interface - 1'b1: Layer 2 Aging registers can be accessed by both APBs <p>Layer 2 Aging registers include the following registers:</p> <ul style="list-style-type: none"> - FWMACAGC - FWMACAGM0/1
16	LTWTMRSL	RW-F	0H	<p>Layer 2 Table Monitoring Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Layer 2 Table Monitoring registers can only be accessed by the APB secure interface - 1'b1: Layer 2 Table Monitoring registers can be accessed by both APBs <p>Layer 2 Table Monitoring registers include the following registers:</p> <ul style="list-style-type: none"> - FWMACTIM - FWMACTEM - FWVLANTIM - FWVLANTEM
15:PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.

				Layer 2 Table Register Security Level Values: - Bit i set to 1'b0: Port i Layer 2 Table registers can only be accessed by the APB secure interface - Bit i set to 1'b1: Port i Layer 2 Table registers can be accessed by both APBs Port i Layer 2 Table registers include the following registers: - FWPC0i.MACSSAi - FWPC0i.MACDSAi - FWPC0i.VLANSAi - FWPC0i.MACRUDAi - FWPC0i.MACRUSAi - FWPC0i.VLANSLVFEi - FWPC0i.VLANRUI - FWPC0i.MACHLAI - FWPC0i.MACHMAi - FWEIS0i.LTWDSPFSi - FWEIS0i.LTWSSPFSi - FWEIS0i.LTWNTFSi - FWEIS0i.LTWSUFSi - FWEIS0i.LTWDUFSi - FWEIS0i.LTWVUFSi - FWEIS0i.SMHLFSi - FWEIS0i.SMHMFSi - FWEIS0i.LTWALFSi - FWEIS0i.LTWBLFSi - FWEIE0i.LTWDSPFEi - FWEIE0i.LTWSSPFEi - FWEIE0i.LTWVSPFEi - FWEIE0i.LTWNTFEi - FWEIE0i.LTWSUFEi - FWEIE0i.LTWDUFEi - FWEIE0i.LTWVUFEi - FWEIE0i.SMHLFEi - FWEIE0i.SMHMFEi - FWEIE0i.LTWALFEi - FWEIE0i.LTWBLFEi - FWEID0i.LTWDSPFDi - FWEID0i.LTWSSPFDi - FWEID0i.LTWNTFDi - FWEID0i.LTWSUFDi - FWEID0i.LTWDUFDi - FWEID0i.LTWALFDi - FWEID0i.LTWBLFDi - FWEIS0i.LTWVUFDi - FWEIS0i.SMHLFDi - FWEIS0i.SMHMFDi
PORT_N-1:0	LTWTRSL	RW-F	0H	

(16) FWSCR26

Forwarding Engine Security Configuration Register 26

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV / ICRSL[PORT_N:1:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / PBRSL[PORT_N:1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:PORT_N+16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PORT_N+15:16	ICRSL	RW-F	0H	<p>Integrity Check Register Security Level Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Port i Integrity Check registers can only be accessed by the APB secure interface - Bit i set to 1'b1: Port i Integrity Check registers can be accessed by both APBs <p>Port i Integrity Check registers include the following registers:</p> <ul style="list-style-type: none"> - FWEIS0i.ICFSi - FWEIE0i.ICFEi - FWEID0i.ICFDi - FWICETC1i - FWICIP4Ci - FWIP4ACi - FWICIP6Ci - FWIP6AC0i - FWIP6AC1i - FWIP6AC2i - FWIP6AC3i - FWIP4APCi - FWIP6APCi - FWICETC2i - FWICETC3ij - FWIP4FACij - FWIP4SFCij - FWIP6FAC0ij - FWIP6FAC1ij - FWIP6FAC2ij - FWIP6FAC3ij - FWIP6SFCij - FWIP4TLCCI - FWIP6PLCCI - FWICL4Ci - FWICL4THLCi
15:PORT_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.

PORT_N-1:0	PBRSL	RW-F	0H	<p>Port Based Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none">- Bit i set to 1'b0: Port i Port Based registers can only be accessed by the APB secure interface- Bit i set to 1'b1: Port i Port Based registers can be accessed by both APBs <p>Port i Port Based registers include the following registers:</p> <ul style="list-style-type: none">- FWPBFC0i- FWPBFC1i- FWPBFCSDCji- FWEIS0i.PBNTFSi- FWEIS0i.PBALFSi- FWEIS0i.PBBLFSi- FWEIE0i.PBNTFEi- FWEIE0i.PBALFEi- FWEIE0i.PBBLFEi- FWEID0i.PBNTFDi- FWEID0i.PBALFDi- FWEID0i.PBBLFDi
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(17) FWSCR27

Forwarding Engine Security Configuration Register 27.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
L23URSL[255:240]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L23URSL[239:224]															

Bits	Bit name	RW-P	Initial value	Function description
LTH_RRULE_N-224:0	L23URSL	RW-F	0H	Layer2/Layer3 Update Register Security Level - Refer to FWSCR34

(18) FWSCR28

Forwarding Engine Security Configuration Register 28.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
L23URSL[223:208]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L23URSL[207:192]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	L23URSL	RW-F	0H	Layer2/Layer3 Update Register Security Level - Refer to FWSCR34

(19) FWSCR29

Forwarding Engine Security Configuration Register 29.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
L23URSL[191:176]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L23URSL[175:160]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	L23URSL	RW-F	0H	Layer2/Layer3 Update Register Security Level - Refer to FWSCR34

(20) FWSCR30

Forwarding Engine Security Configuration Register 30.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
L23URSL[159:144]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L23URSL[143:128]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	L23URSL	RW-F	0H	Layer2/Layer3 Update Register Security Level - Refer to FWSCR34

(21) FWSCR31

Forwarding Engine Security Configuration Register 31.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
L23URSL[127:112]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L23URSL[111:96]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	L23URSL	RW-F	0H	Layer2/Layer3 Update Register Security Level - Refer to FWSCR34

(22) FWSCR32

Forwarding Engine Security Configuration Register 32.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
L23URSL[95:80]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L23URSL[79:64]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	L23URSL	RW-F	0H	Layer2/Layer3 Update Register Security Level - Refer to FWSCR34

(23) FWSCR33

Forwarding Engine Security Configuration Register 33.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
L23URSL[63:48]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L23URSL[47:32]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	L23URSL	RW-F	0H	Layer2/Layer3 Update Register Security Level - Refer to FWSCR34

(24) FWSCR34

Forwarding Engine Security Configuration Register 34.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
L23URSL[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L23URSL[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	L23URSL	RW-F	0H	<p>Layer2/Layer3 Update Register Security Level</p> <p>x = from (((LTH_RRULE_N/256) * (i+1)) - 1) to ((LTH_RRULE_N/256) * (i))</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Layer2/Layer3 Update rule number x can only be accessed by the APB secure interface - Bit i set to 1'b1: Layer2/Layer3 Update rule number x can be accessed by both APBs <p>Functions:</p> <ul style="list-style-type: none"> - If bit i is set to 1'b0, any learning done by unsecure APB interface through FWI23URL0/1/2/3/R registers with FWI23URL0.L23RNL set to x with fail with security error. - If bit i is set to 1'b0, any reading done by unsecure APB interface through FWI23URR/R0/R1/R2/R3 registers with FWI23URR.L23RNR set to x with give back an empty entry. - If bit i is set to 1'b0, for any j FWSEQNGCj is protected in writing for unsecure APB interface while trying to write x to FWSEQNGCj.SEQNGRNj. - If bit i is set to 1'b0, for any j FWL23URMCj is protected in writing for unsecure APB interface while trying to write x to FWL23URMCi.RMRNi or FWL23URMCi.RMNRNi.

(25) FWSCR35

Forwarding Engine Security Configuration Register 35.

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV															

Bits	Bit name	RW-P	Initial value	Function description
31:0	RSV	R0-U	0H	Reserved area. On read, 0 will be returned. Reserved to extend FWSCR36

(26) FWSCR36

Forwarding Engine Security Configuration Register 36

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
L23URRSI[LTH_REMAP_N-1:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L23URRSI[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
LTH_REMAP_N-1:0	L23URRSI	RW-F	0H	<p>Layer2/Layer3 Update Remapping Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Layer2/Layer3 Update Remapping register i can only be accessed by the APB secure interface - Bit i set to 1'b1: Layer2/Layer3 Update Remapping rule number i can be accessed by both APBs <p>Layer2/Layer3 Update Remapping register i include the following registers:</p> <ul style="list-style-type: none"> - FWL23URMCi

(27) FWSCR37

Forwarding Engine Security Configuration Register 37

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV															

L23UTM
RSL

Bits	Bit name	RW-P	Initial value	Function description
31:1	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
0	L23UTMRS	RW-F	0H	<p>Layer2/Layer3 Update Table Monitoring Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Layer2/Layer3 Update Table Monitoring registers can only be accessed by the APB secure interface - 1'b1: Layer2/Layer3 Update Table Monitoring registers can be accessed by both APBs <p>Layer2/Layer3 Update Table Monitoring registers include the following registers:</p> <ul style="list-style-type: none"> - FWL23UTIM

(28) FWSCR38

Forwarding Engine Security Configuration Register 38

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMSDURSL[PSFP_MSDU_N -1:0]															

Bits	Bit name	RW-P	Initial value	Function description
31: PSFP_MSDU_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
PSFP_MSDU_N-1:0	PMSDURSL	RW-F	0H	<p>PSFP MSDU Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: MSDU filter number i registers can only be accessed by the APB secure interface - Bit i set to 1'b1: MSDU filter number i registers can be accessed by both APBs <p>MSDU filter number i registers include the following registers:</p> <ul style="list-style-type: none"> - FWPMFGCi - FWEIS2.PMFS[i] - FWEIE2.PMFE[i] - FWEID2.PMFD[i]

(29) FWSCR39

Forwarding Engine Security Configuration Register 39

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															PGRMR SL
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV								PGATERSL[PSFP_GATE_N -1:0]							

Bits	Bit name	RW-P	Initial value	Function description
31:17	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
16	PGRMRSL	RW-F	0H	<p>PSFP Gate RAM Monitoring Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Gate RAM Monitoring registers can only be accessed by the APB secure interface - 1'b1: Gate RAM Monitoring registers can be accessed by both APBs <p>PSFP Gate RAM Monitoring registers include the following registers:</p> <ul style="list-style-type: none"> - FWPGFRIM
15: PSFP_GATE_N	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.

				PSFP GATE Register Security Level Values: - Bit i set to 1'b0: PSFP GATE filter number i registers can only be accessed by the APB secure interface - Bit i set to 1'b1: PSFP GATE filter number i registers can be accessed by both APBs or can only be accessed by the APB unsecure interface PSFP GATE filter number i registers include the following registers: - FWPGFCi - FWPGFCi - FWPGFIGSCI - FWPGFENCI - FWPGFENMi - FWPGFCSTC0i - FWPGFCSTC1i - FWPGFCSTM0i - FWPGFCSTM1i - FWPGFCTCi - FWPGFCTMi - FWPGFHCCI - FWPGFSMi - FWPGFGCi - FWEIS3.PGFS[i] - FWEIE3.PGFE[i] - FWEID3.PGFD[i] - FWEIS4.GFGES[i] - FWEIS4.GFGEES[i] - FWEIE4.GFGEE[i] - FWEIE4.GFGEEE[i] - FWEID4.GFGED[i] - FWEID4.GFGEED[i]
PSFP_GATE_N-1:0	PGATERSL	RW-F	0H	

(30) FWSCR40

Forwarding Engine Security Configuration Register 40

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMTRRS[PSFP_MTR_N-1:96]															

Bits	Bit name	RW-P	Initial value	Function description
PSFP_MTR_N-97:0	PMTRRS	RW-F	0H	<p>PSFP MeTeR Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: PSFP MeTeR number i registers can only be accessed by the APB secure interface - Bit i set to 1'b1: PSFP MeTeR number i registers can be accessed by both APBs <p>PSFP MeTeR number i registers include the following registers:</p> <ul style="list-style-type: none"> - FWPMTRFCi - FWPMTRCBSci - FWPMTRCIRCi - FWPMTREBSci - FWPMTREIRCi - FWPMTRFMi - FWEIS50/51/52/53.PMRFS[i] - FWEIE50/51/52/53.PMRFE[i] - FWEID50/51/52/53.PMRFD[i]

(31) FWSCR41

Forwarding Engine Security Configuration Register 41

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMTRRSL[95:64]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	PMTRRSL	RW-F	0H	<p>PSFP MeTeR Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: PSFP MeTeR number i registers can only be accessed by the APB secure interface - Bit i set to 1'b1: PSFP MeTeR number i registers can be accessed by both APBs <p>PSFP MeTeR number i registers include the following registers:</p> <ul style="list-style-type: none"> - FWPMTRFC<i>i</i> - FWPMTRCB<i>S</i>C<i>i</i> - FWPMTRCIRC<i>i</i> - FWPMTREB<i>S</i>C<i>i</i> - FWPMTREIRC<i>i</i> - FWPMTRF<i>M</i><i>i</i> - FWEIS50/51/52/53.PMRFS[i] - FWEIE50/51/52/53.PMRFE[i] - FWEID50/51/52/53.PMRFD[i]

(32) FWSCR42

Forwarding Engine Security Configuration Register 42

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMTRRSL[63:32]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	PMTRRSL	RW-F	0H	<p>PSFP MeTeR Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: PSFP MeTeR number i registers can only be accessed by the APB secure interface - Bit i set to 1'b1: PSFP MeTeR number i registers can be accessed by both APBs <p>PSFP MeTeR number i registers include the following registers:</p> <ul style="list-style-type: none"> - FWPMTRFCi - FWPMTRCBSci - FWPMTRCIRCi - FWPMTREBSci - FWPMTREIRCi - FWPMTRFMi - FWEIS50/51/52/53.PMRFS[i] - FWEIE50/51/52/53.PMRFE[i] - FWEID50/51/52/53.PMRFD[i]

(33) FWSCR43

Forwarding Engine Security Configuration Register 43

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMTRRSL[31:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	PMTRRSL	RW-F	0H	<p>PSFP MeTeR Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: PSFP MeTeR number i registers can only be accessed by the APB secure interface - Bit i set to 1'b1: PSFP MeTeR number i registers can be accessed by both APBs <p>PSFP MeTeR number i registers include the following registers:</p> <ul style="list-style-type: none"> - FWPMTRFC<i>i</i> - FWPMTRCB<i>S</i>C<i>i</i> - FWPMTRCIRC<i>i</i> - FWPMTREB<i>S</i>C<i>i</i> - FWPMTREIRC<i>i</i> - FWPMTRF<i>M</i><i>i</i> - FWEIS50/51/52/53.PMRFS[i] - FWEIE50/51/52/53.PMRFE[i] - FWEID50/51/52/53.PMRFD[i]

(34) FWSCR44

Forwarding Engine Security Configuration Register 44

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FRERRSL[FRER_RECE_N-1:112]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRERRSL[111:96]															

Bits	Bit name	RW-P	Initial value	Function description
FRER_RECE_N-97:0	FRERRSL	RW-F	0H	<p>FRER Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: FRER registers for recovery entry i + 96 can only be accessed by the APB secure interface - Bit i set to 1'b1: FRER registers for recovery entry i + 96 can be accessed by both APBs <p>FRER registers for recovery entry i + 96 include the following registers:</p> <ul style="list-style-type: none"> - FWEIS60.FFS[i] - FWEIE60.FFE[i] - FWEID60.FFD[i] - FWEIS70.FOORS[i] - FWEIE70.FOORE[i] - FWEID70.FOORD[i] - FWEIS80.TOS[i] - FWEIE80.TOS[i] - FWEID80.TOS[i]

(35) FWSCR45

Forwarding Engine Security Configuration Register 45

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FRERRSL[95:80]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRERRSL[79:64]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	FRERRSL	RW-F	0H	<p>FRER Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: FRER registers for recovery entry i + 64 can only be accessed by the APB secure interface - Bit i set to 1'b1: FRER registers for recovery entry i + 64 can be accessed by both APBs <p>FRER registers for recovery entry i + 64 include the following registers:</p> <ul style="list-style-type: none"> - FWEIS61.FFS[i] - FWEIE61.FFE[i] - FWEID61.FFD[i] - FWEIS71.FOORS[i] - FWEIE71.FOORE[i] - FWEID71.FOORD[i] - FWEIS81.TOS[i] - FWEIE81.TOS[i] - FWEID81.TOS[i]

(36) FWSCR46

Forwarding Engine Security Configuration Register 46

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FRERRSL[63:48]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRERRSL[47:32]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	FRERRSL	RW-F	0H	<p>FRER Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: FRER registers for recovery entry i + 32 can only be accessed by the APB secure interface - Bit i set to 1'b1: FRER registers for recovery entry i + 32 can be accessed by both APBs <p>FRER registers for recovery entry i + 32 include the following registers:</p> <ul style="list-style-type: none"> - FWEIS62.FFS[i] - FWEIE62.FFE[i] - FWEID62.FFD[i] - FWEIS72.FOORS[i] - FWEIE72.FOORE[i] - FWEID72.FOORD[i] - FWEIS82.TOS[i] - FWEIE82.TOS[i] - FWEID82.TOS[i]

(37) FWSCR47

Forwarding Engine Security Configuration Register 47

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FRERRSL[31:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRERRSL[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
31:0	FRERRSL	RW-F	0H	<p>FRER Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: FRER registers for recovery entry i can only be accessed by the APB secure interface - Bit i set to 1'b1: FRER registers for recovery entry i can be accessed by both APBs <p>FRER registers for recovery entry i include the following registers:</p> <ul style="list-style-type: none"> - FWEIS63.FFS[i] - FWEIE63.FFE[i] - FWEID63.FFD[i] - FWEIS73.FOORS[i] - FWEIE73.FOORE[i] - FWEID73.FOORD[i] - FWEIS83.TOS[i] - FWEIE83.TOS[i] - FWEID83.TOS[i]

(38) FWSCR48

Forwarding Engine Security Configuration Register 48

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV															

Bits	Bit name	RW-P	Initial value	Function description
31:2	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
1	FTORSL	RW-F	0H	<p>FRER TimeOut Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: FRER TimeOut registers can only be accessed by the APB secure interface - 1'b1: FRER TimeOut registers can be accessed by both APBs <p>FRER TimeOut registers include the following registers:</p> <ul style="list-style-type: none"> - FWFTOC
0	FTMRSRL	RW-F	0H	<p>FRER Table Monitoring Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: FRER Table Monitoring registers can only be accessed by the APB secure interface - 1'b1: FRER Table Monitoring registers can be accessed by both APBs <p>FRER Table Monitoring registers include the following registers:</p> <ul style="list-style-type: none"> - FWFTIM

(39) FWSCR49

Forwarding Engine Security Configuration Register 49

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEQNGRSL[LTH_SEQGN_N-1:16]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEQNGRSL[15:0]															

Bits	Bit name	RW-P	Initial value	Function description
LTH_SEQGN_N-1:0	SEQNGRSL	RW-F	0H	<p>SEQuence Number Generation Register Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: SEQuence Number Generation registers for recovery entry i can only be accessed by the APB secure interface - Bit i set to 1'b1: SEQuence Number Generation registers for recovery entry i can be accessed by both APBs <p>SEQuence Number Generation registers for recovery entry i include the following registers:</p> <ul style="list-style-type: none"> - FWSEQNGCi - FWSEQNGMi - FWSEQNRC.SEQNR[i]

4. Register utilization

4.1 Software flows

Restrictions:

SW: Please follow to the flow in this section.

4.1.1 Software flow legend

Software flow legend is described in Fig 4.1.

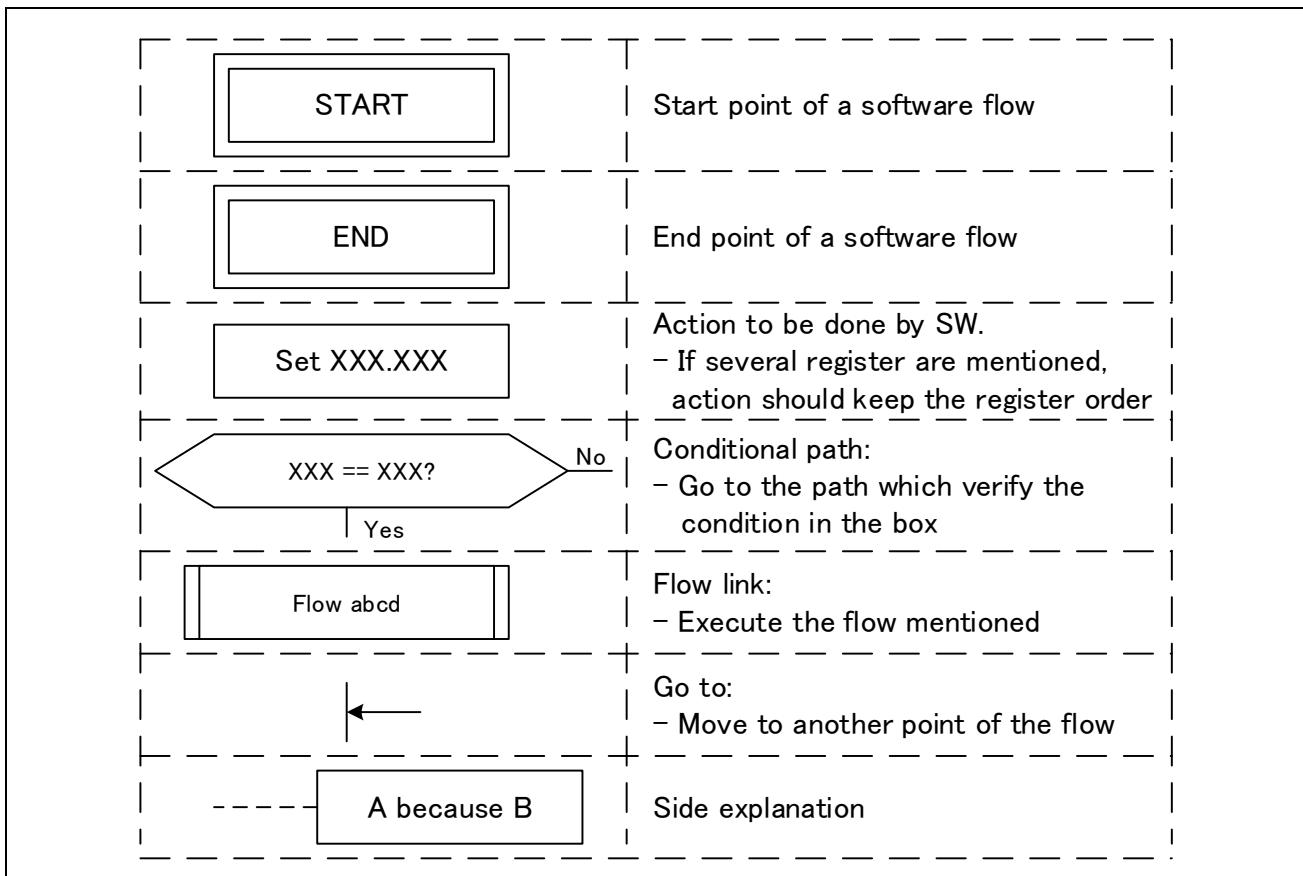


Fig 4.1: Software flow legend

4.1.2 Interrupt handling flow

Interrupt handling flow can be used in any mode except RESET mode.

The interrupt handling flow is described in Fig 4.2.

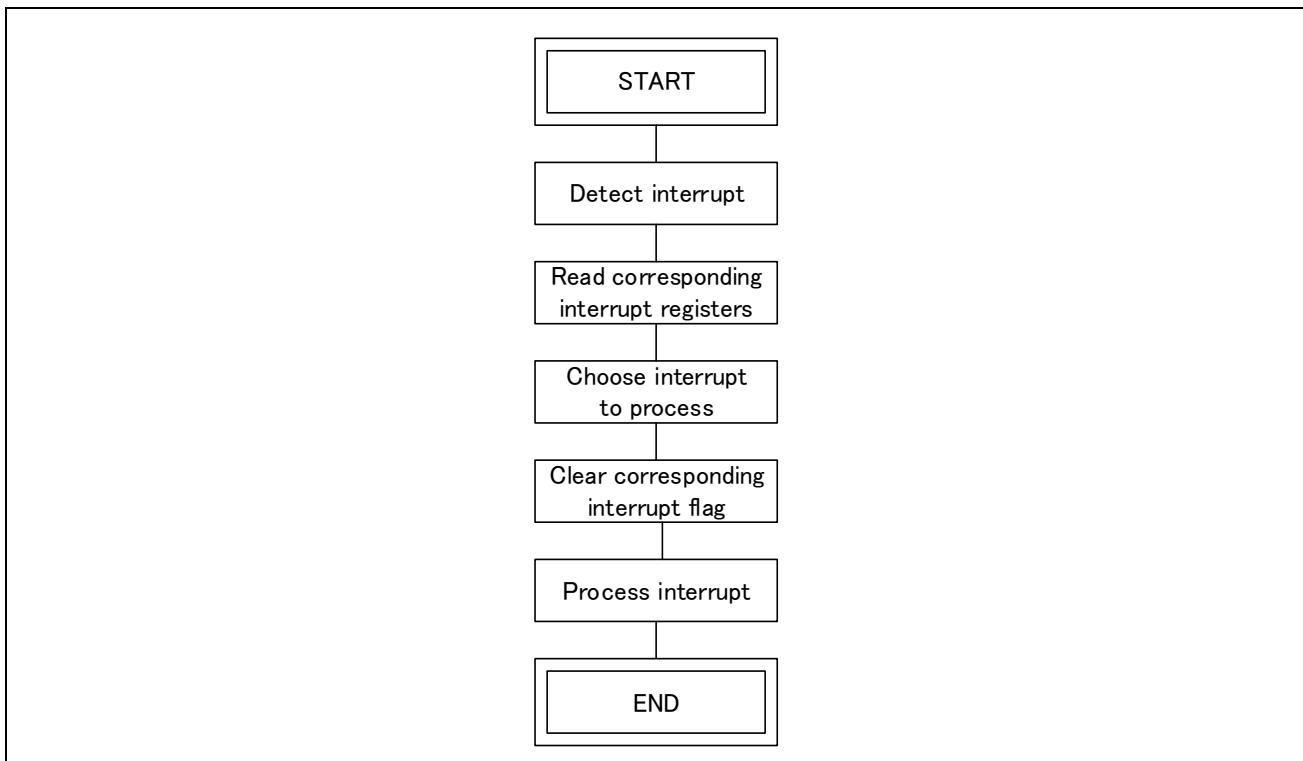


Fig 4.2: Interrupt handling flow

4.1.3 Port i and IPV j setting flow

Port i and IPV j setting flow is described in Fig 4.3.

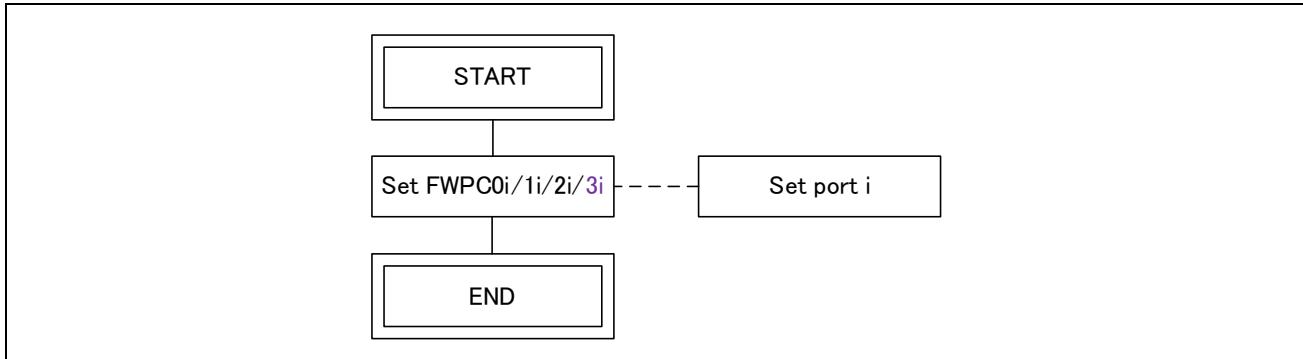


Fig 4.3: Port i and IPV j setting flow

4.1.4 Cut-through forwarding flows

4.1.4.1 Cut-through rule i setting flow

Cut-through rule i setting flow is described in Fig 4.4.

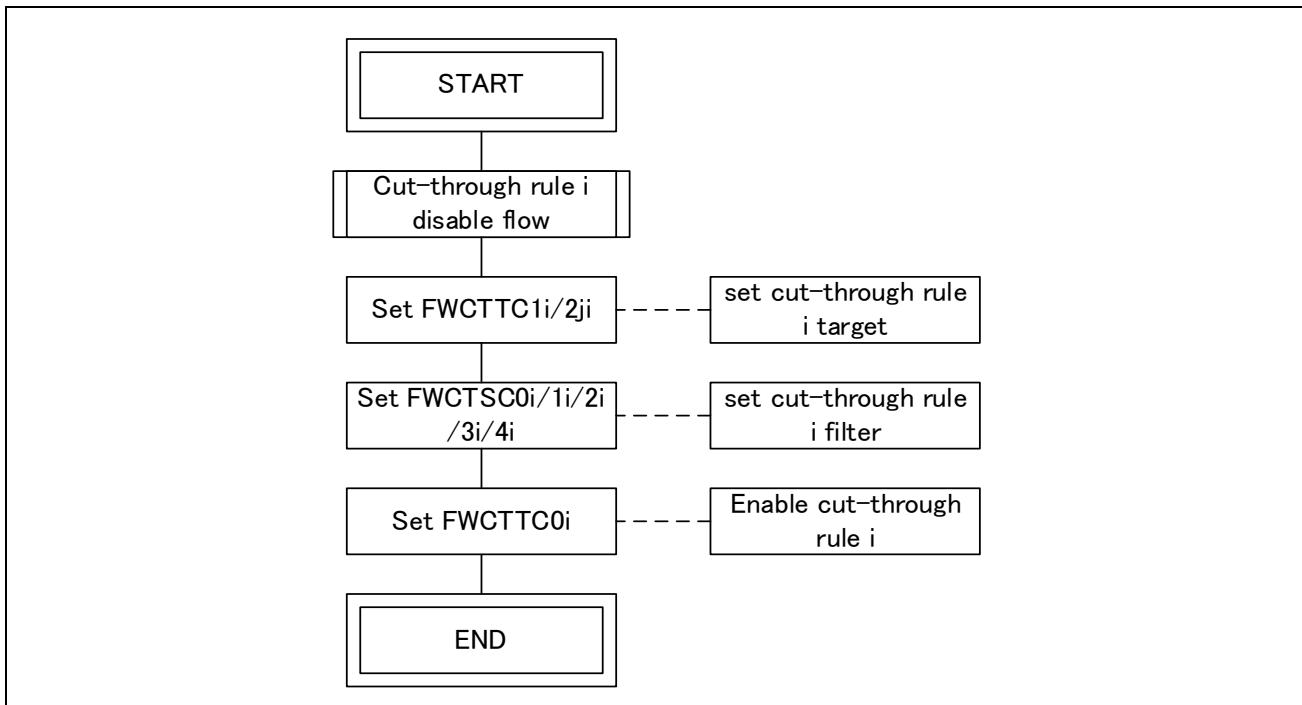


Fig 4.4: Cut-through rule i setting flow

4.1.4.2 Cut-through rule i disable flow

Cut-through rule i disable flow is described in Fig 4.5.

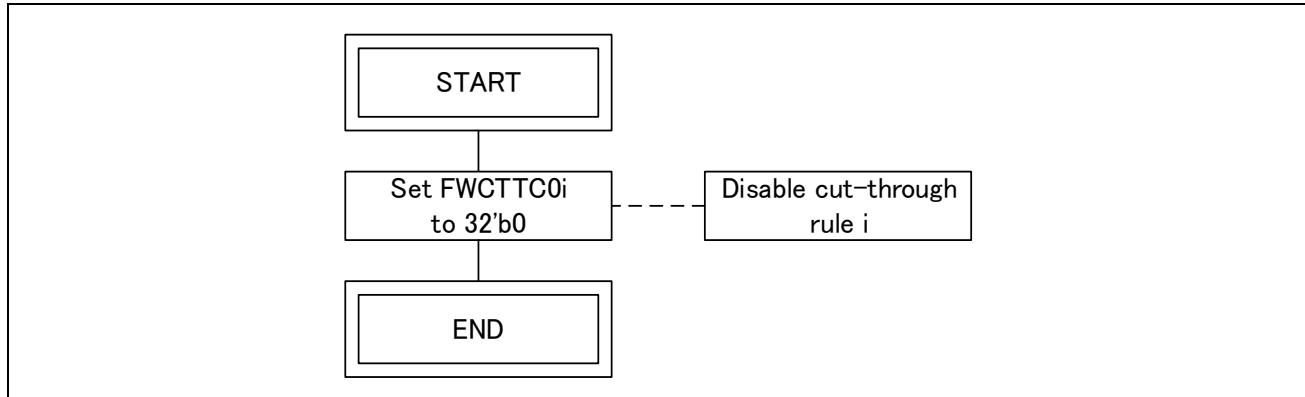


Fig 4.5: Cut-through rule i disable flow

4.1.5 Integrity check port i setting flow

Integrity check port i setting flow is described in Fig 4.6.

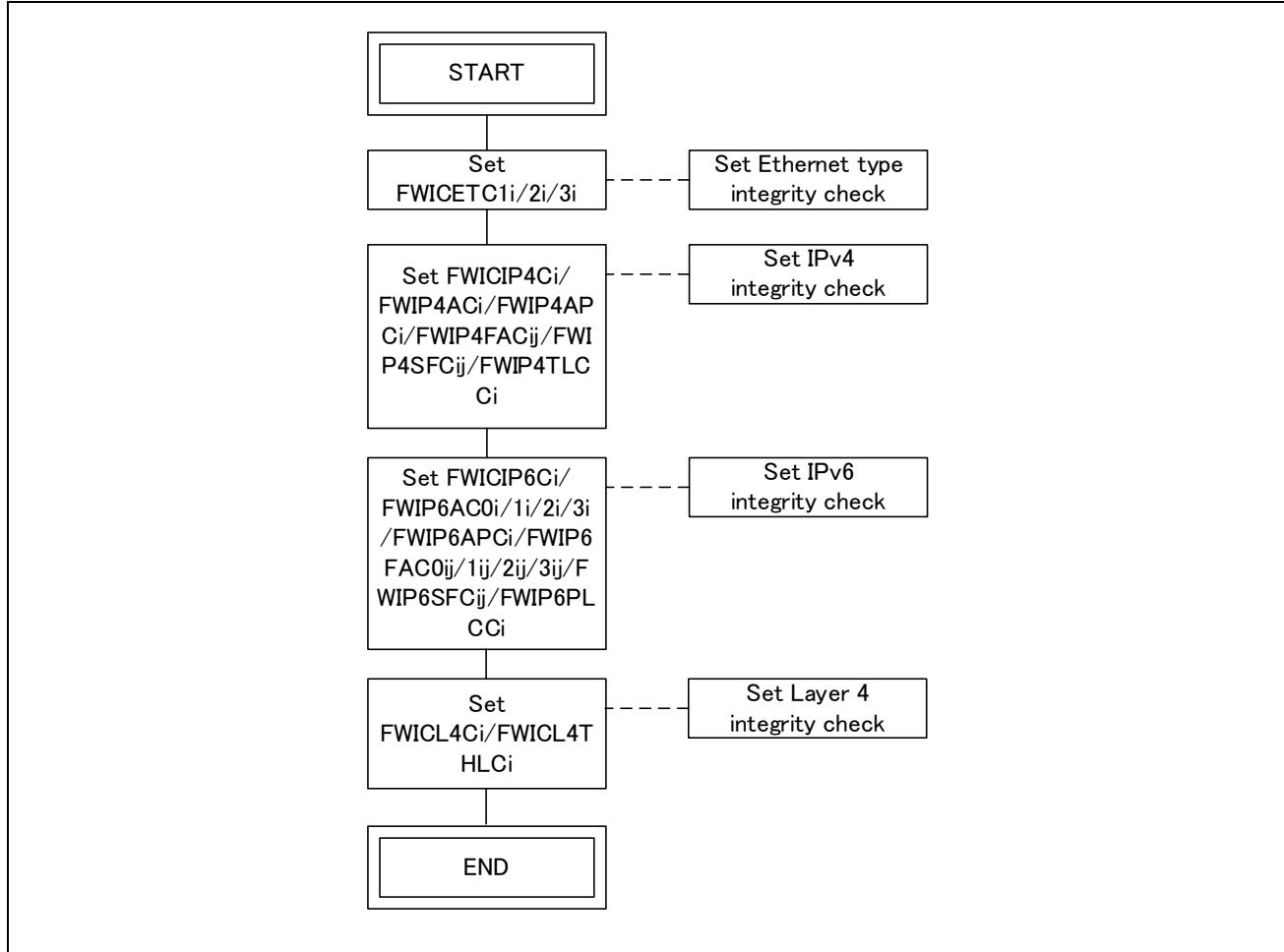


Fig 4.6: Integrity check port i setting flow

4.1.6 Layer 3 forwarding/routing/filtering flows

4.1.6.1 Perfect filter i setting flow

Perfect filter i setting flow is described in Fig 4.7.

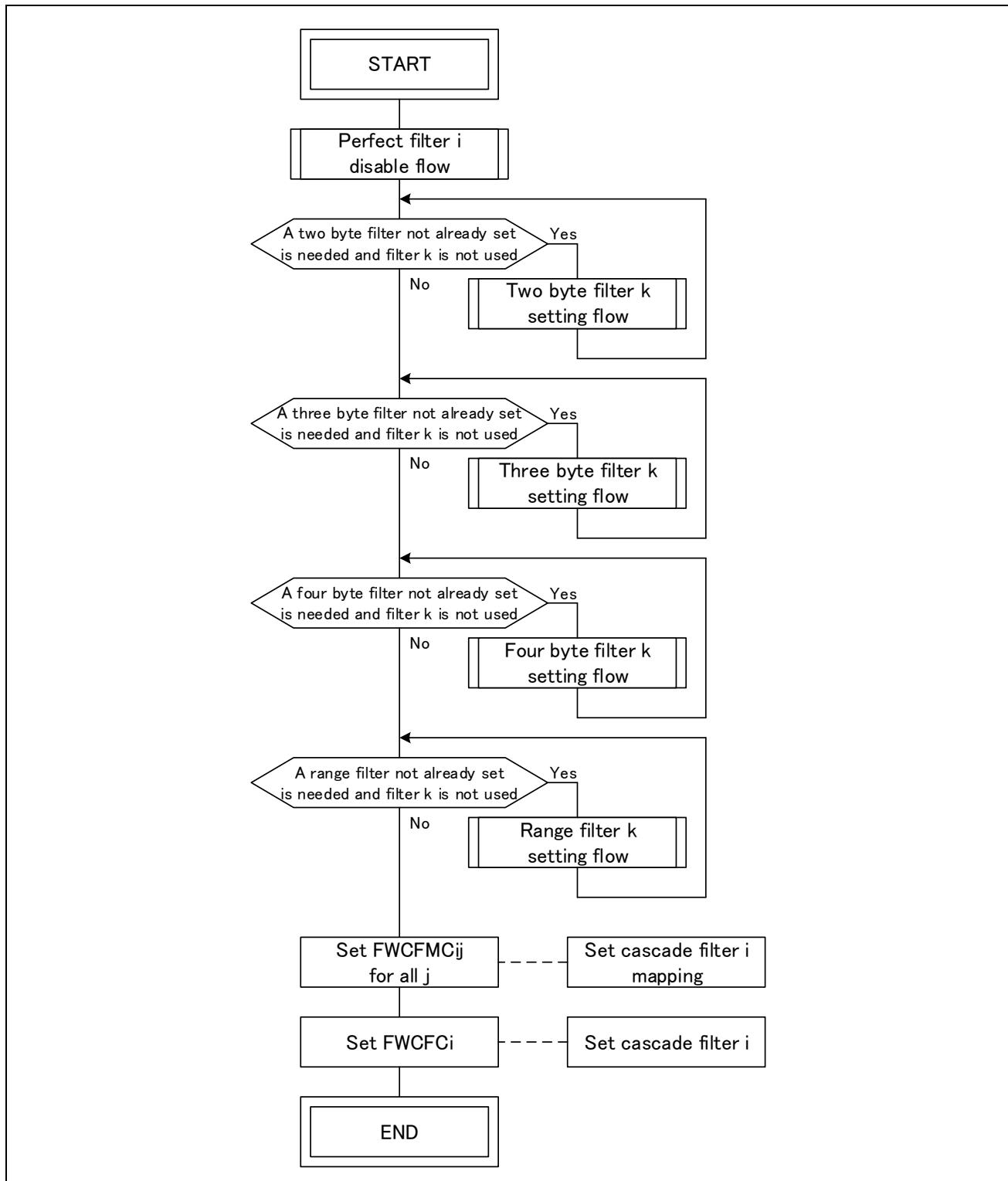


Fig 4.7: Perfect filter i setting flow

4.1.6.2 Perfect filter i disable flow

Perfect filter i disable flow is described in Fig 4.8.

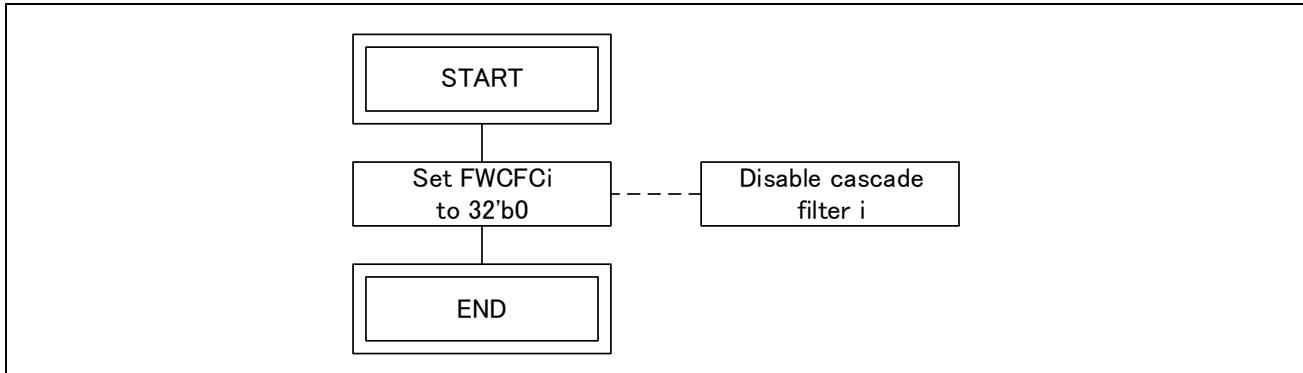


Fig 4.8: Perfect filter i disable flow

4.1.6.3 Perfect filter priority change flow

Perfect filter priority change flow is described in Fig 4.9.

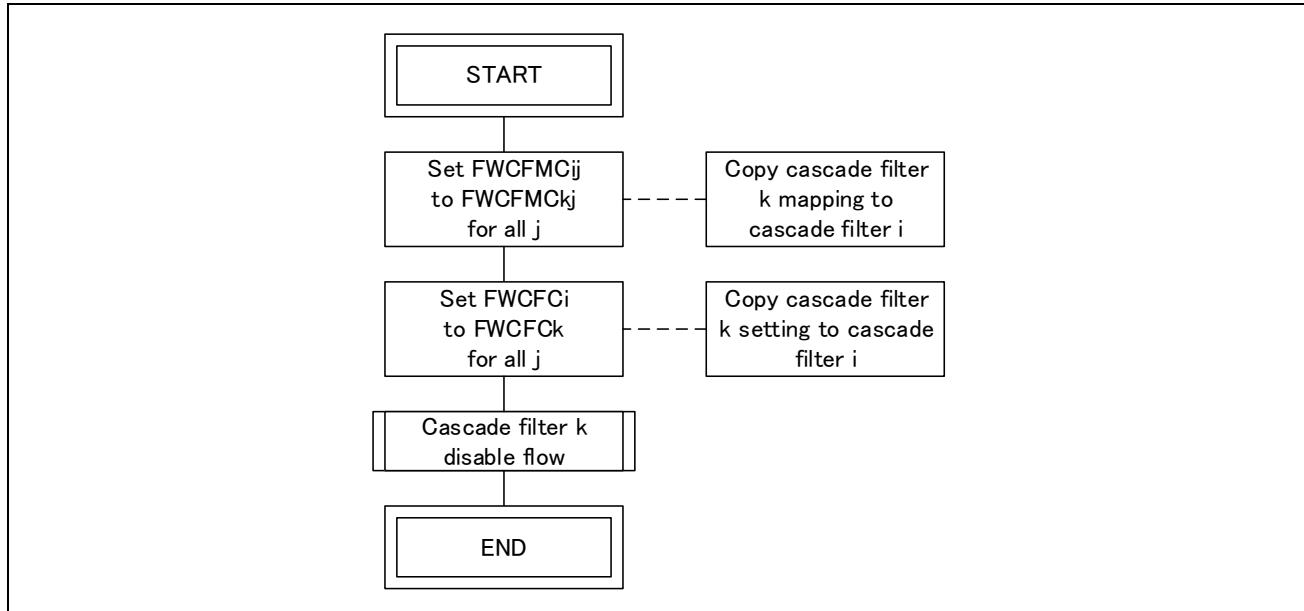


Fig 4.9: Perfect filter priority change flow (from k to i)

4.1.6.4 Software Hash hardware calculation flow (for L3 stream creation)

Software Hash calculation by hardware flow is described in Fig 4.10

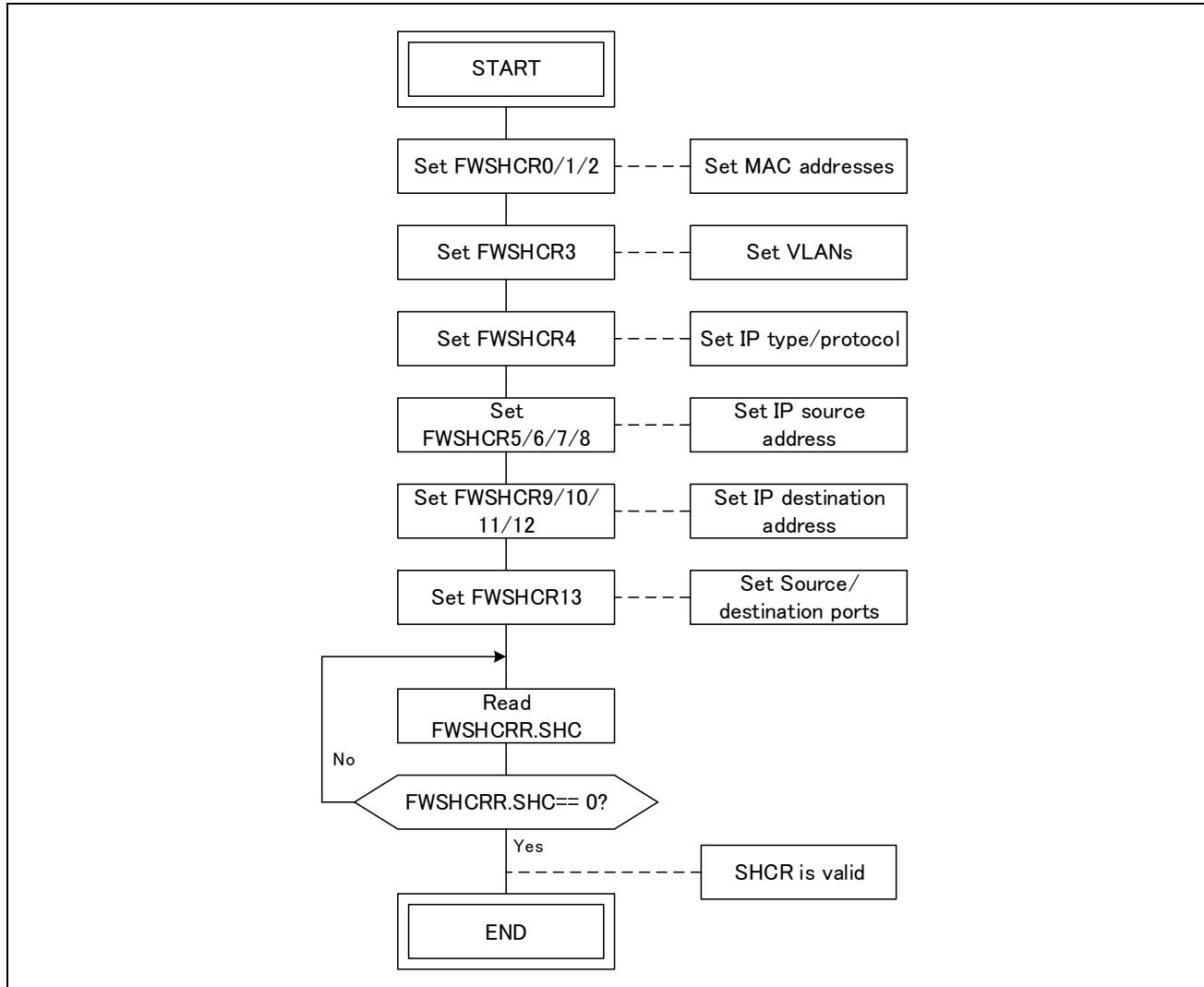


Fig 4.10: Hash hardware calculation flow

4.1.6.5 Layer 3 table reset flow

Layer 3 table reset flow is described in Fig 4.11.

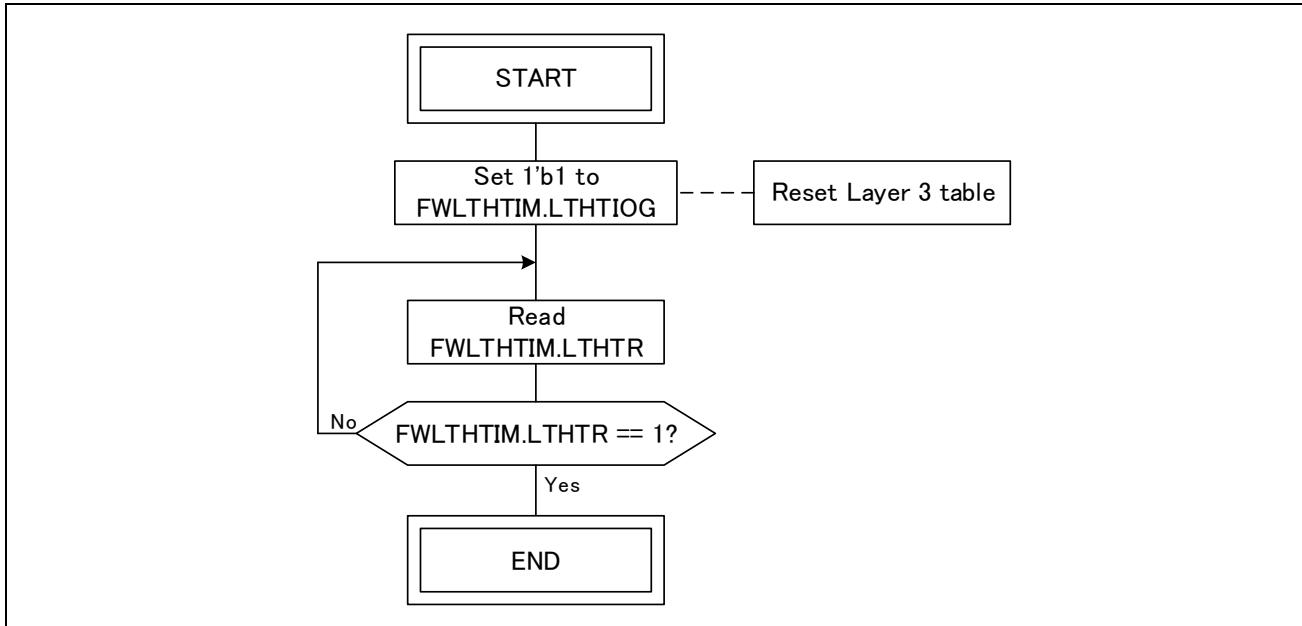


Fig 4.11: Layer 3 table reset flow

4.1.6.6 Layer 3 entry learn flow

Layer 3 entry learn flow is described in Fig 4.12.

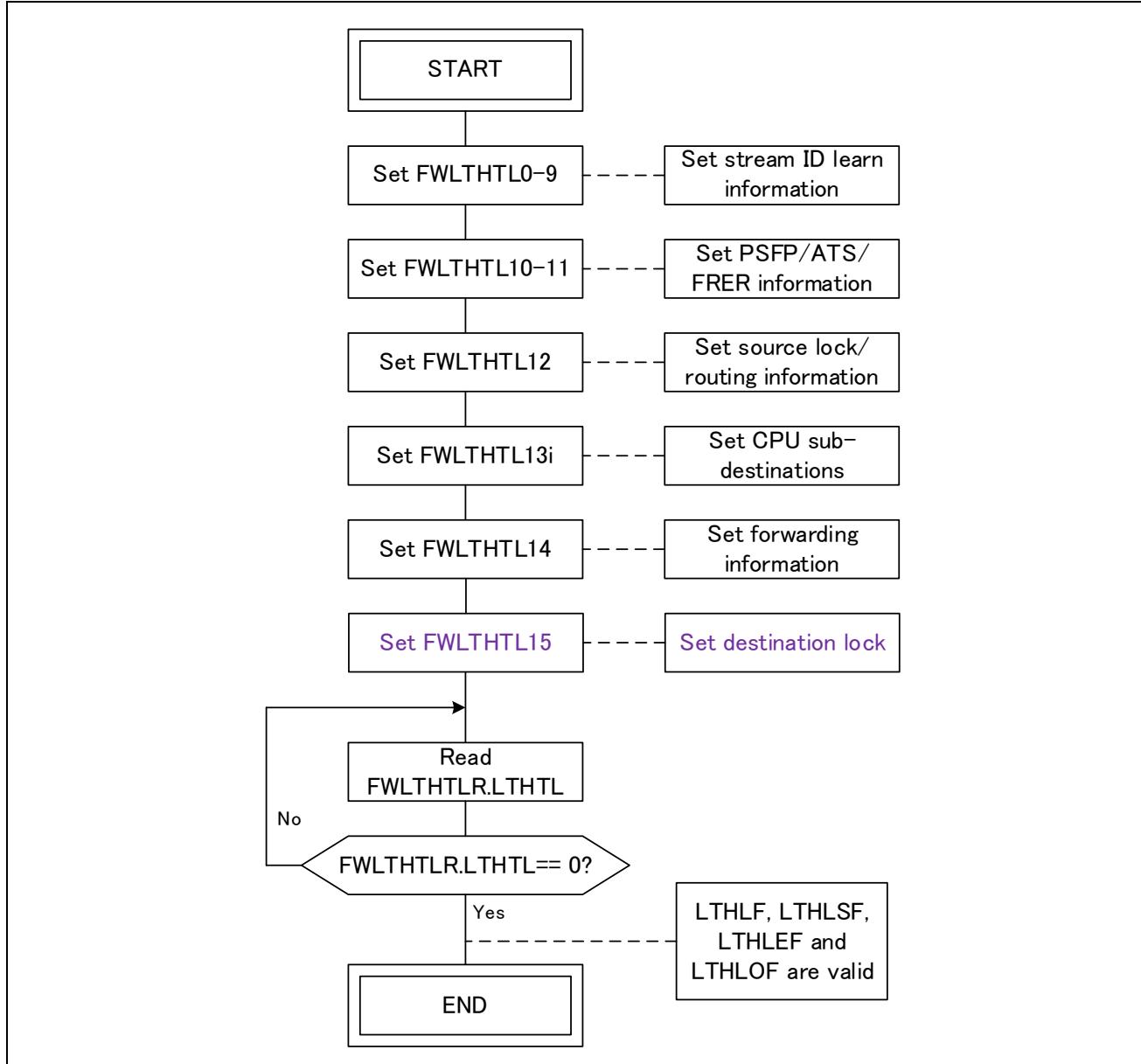


Fig 4.12: Layer 3 entry learn flow

4.1.6.7 Layer 3 entry search flow

Layer 3 entry search flow is described in Fig 4.13.

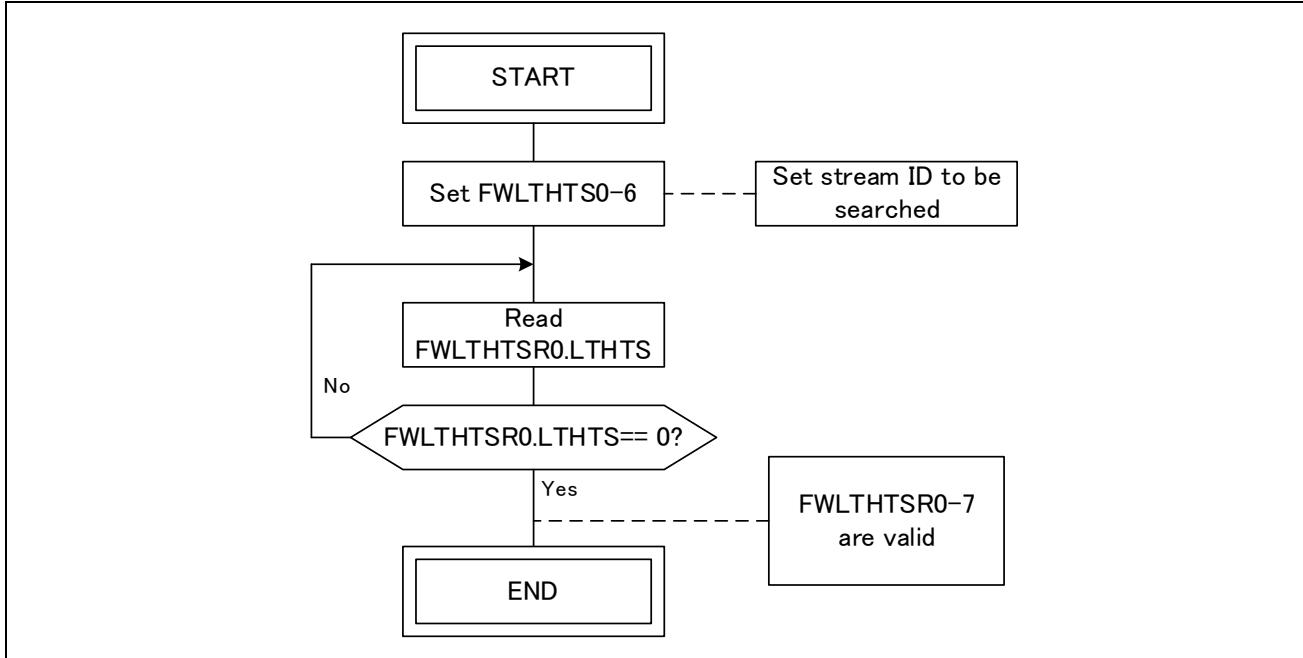


Fig 4.13: Layer 3 entry search flow

4.1.6.8 Layer 3 entry read flow

Layer 3 entry read flow is described in Fig 4.14.

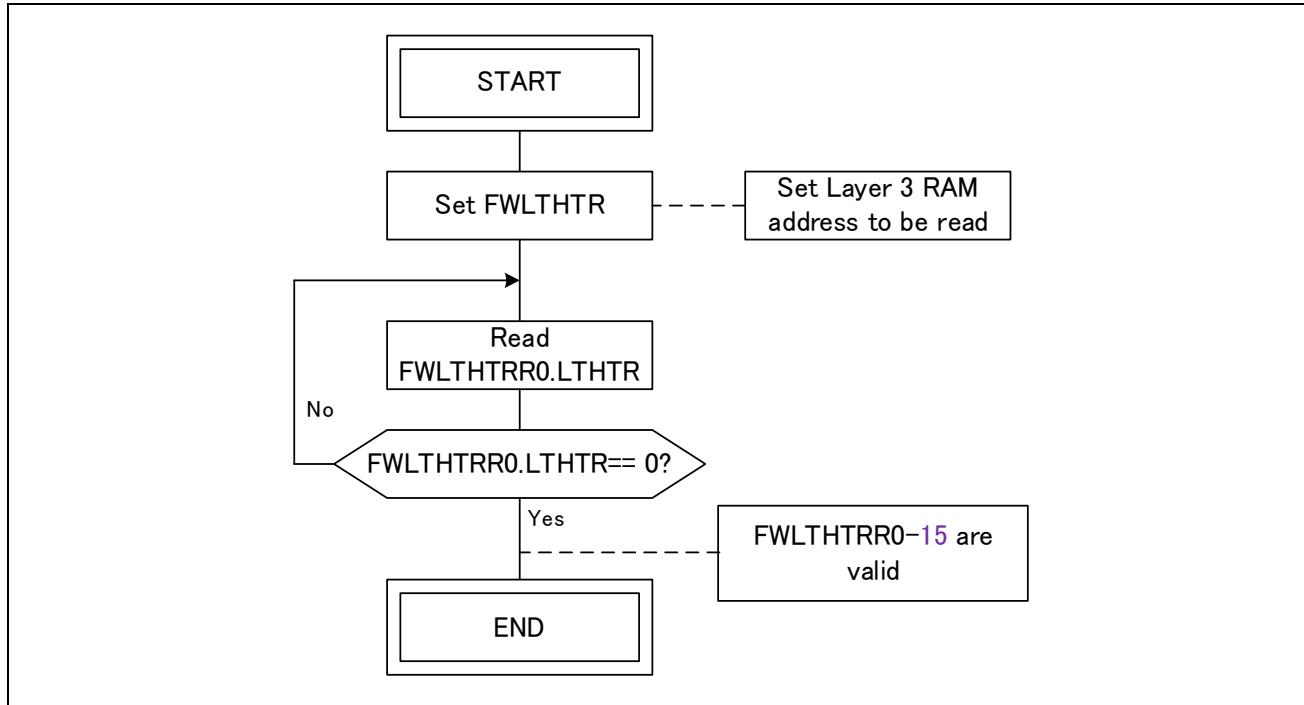


Fig 4.14: Layer 3 entry read flow

4.1.7 Layer 2 forwarding flows

4.1.7.1 MAC table reset flow

MAC table reset flow is described in Fig 4.15.

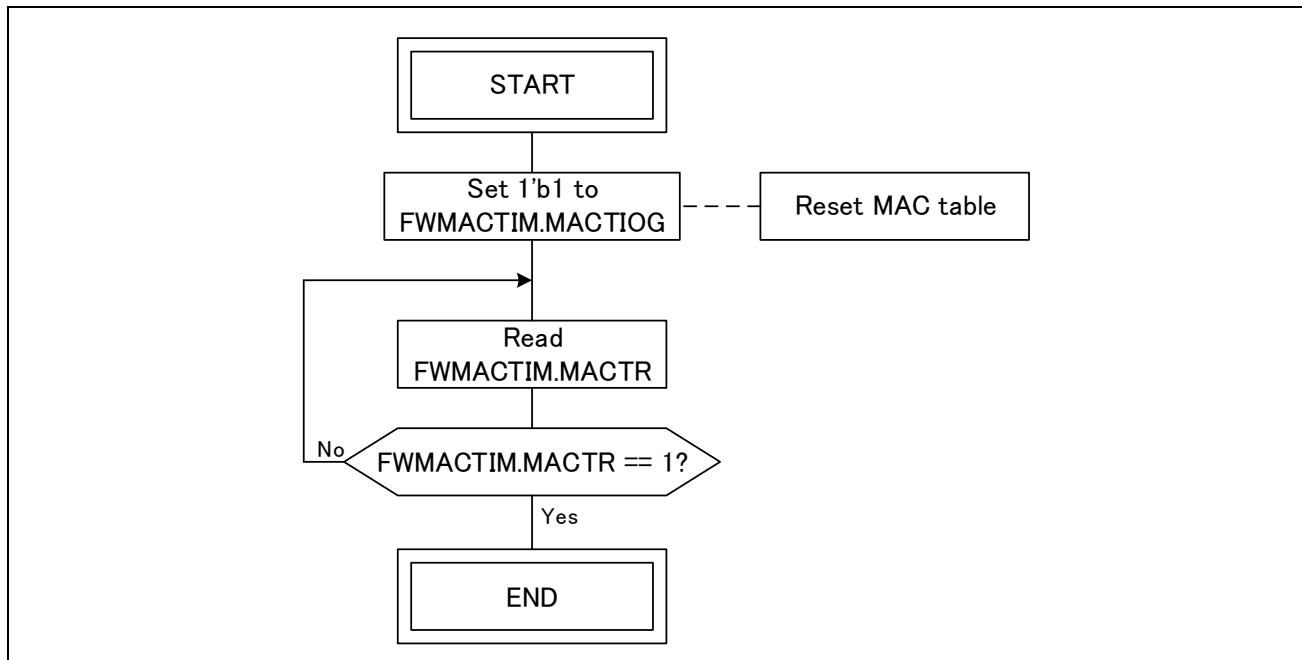


Fig 4.15: MAC table reset flow

4.1.7.2 VLAN table reset flow

VLAN table reset flow is described in Fig 4.16.

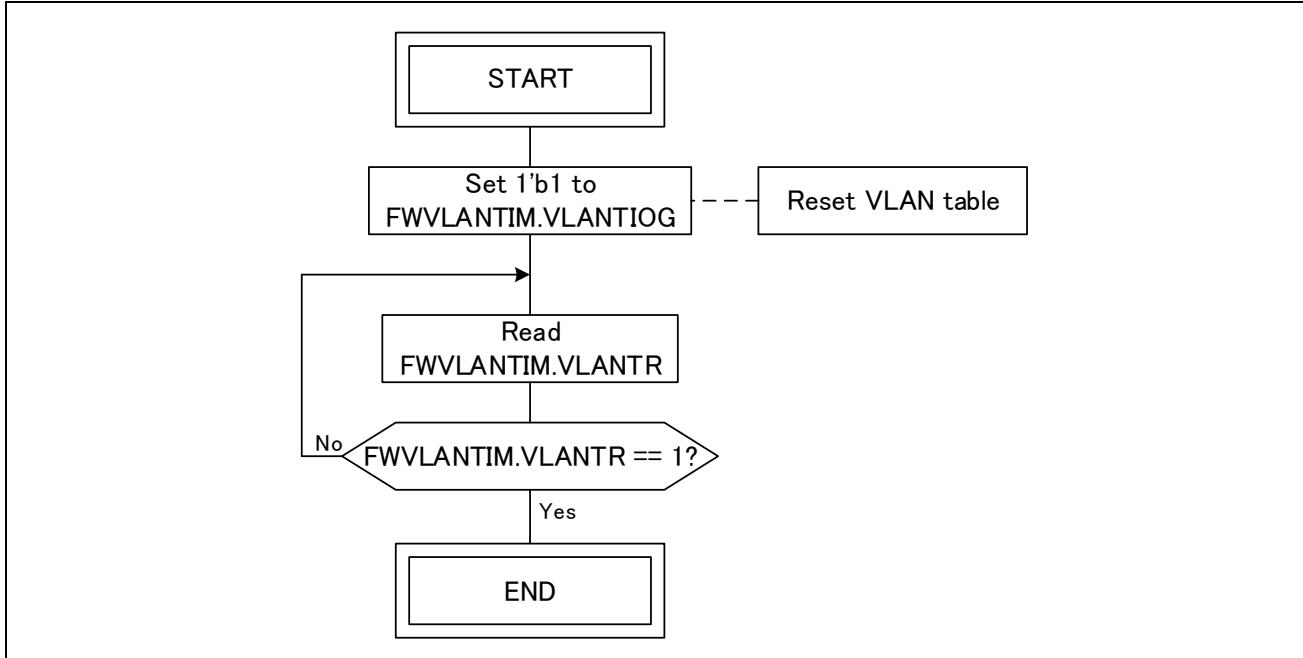


Fig 4.16: VLAN table reset flow

4.1.7.3 MAC entry learn flow

MAC entry learn flow is described in Fig 4.17.

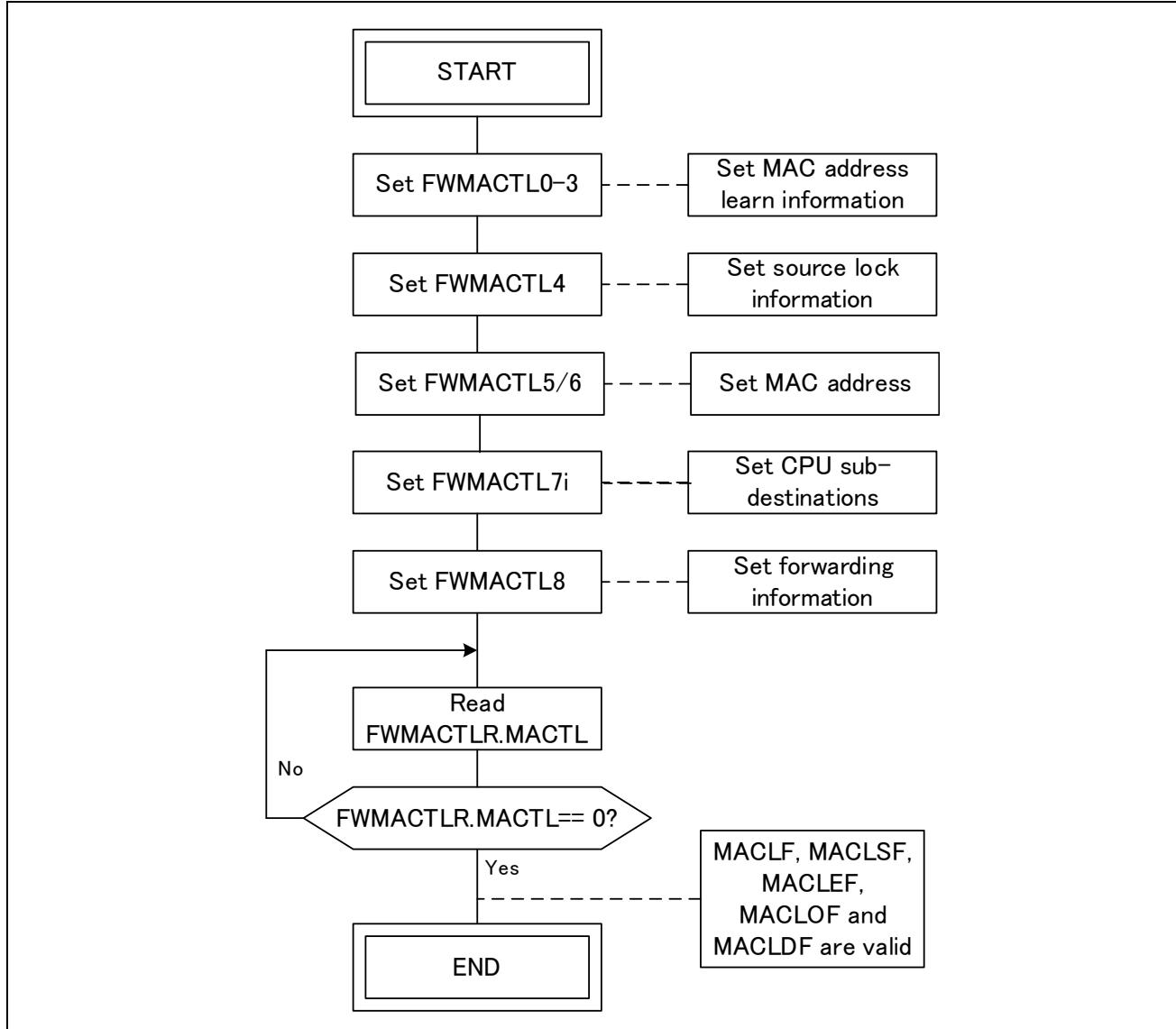


Fig 4.17: MAC entry learn flow

4.1.7.4 VLAN entry learn flow

VLAN entry learn flow is described in Fig 4.18.

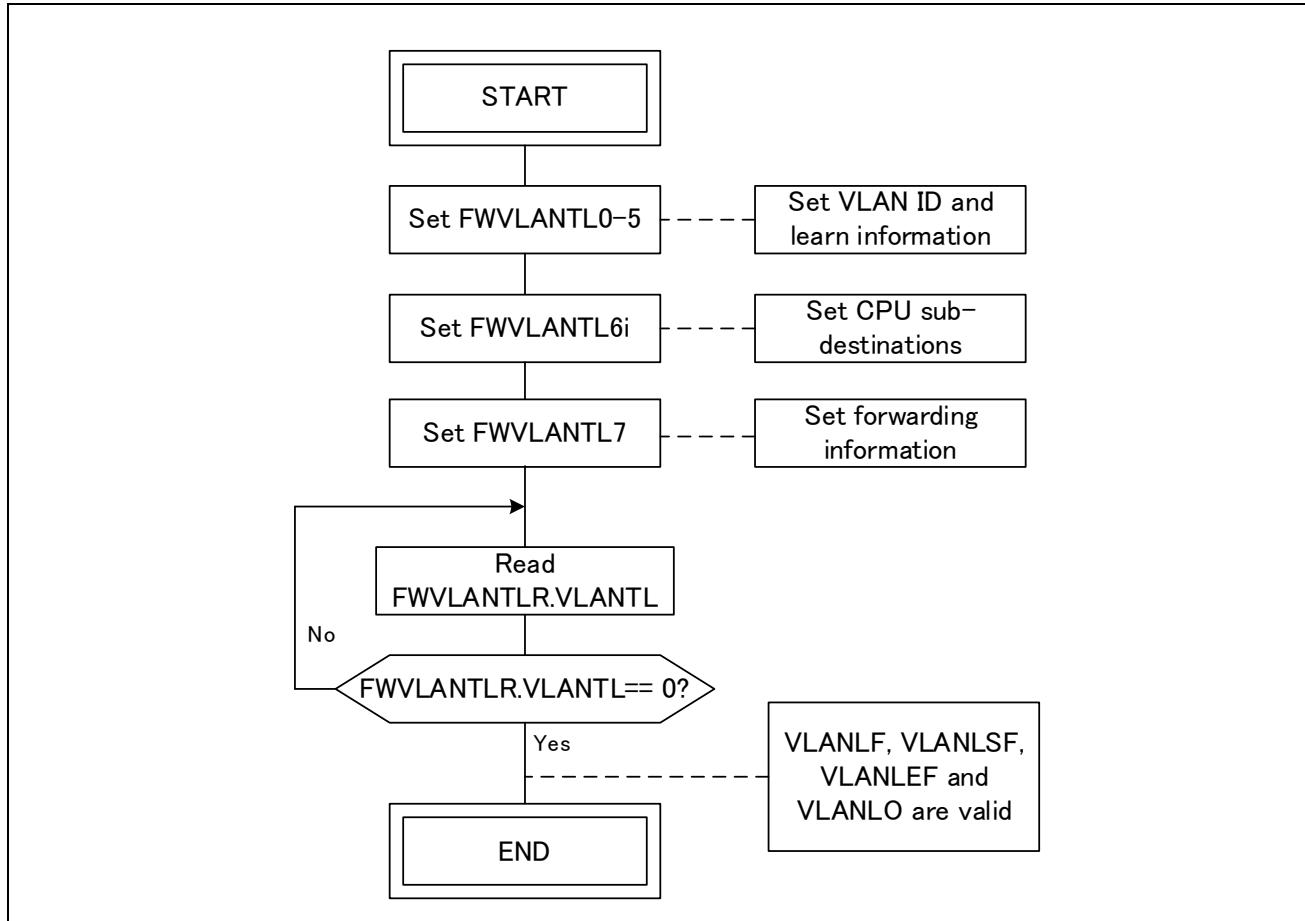


Fig 4.18: VLAN entry learn flow

4.1.7.5 MAC entry search flow

MAC entry search flow is described in Fig 4.19.

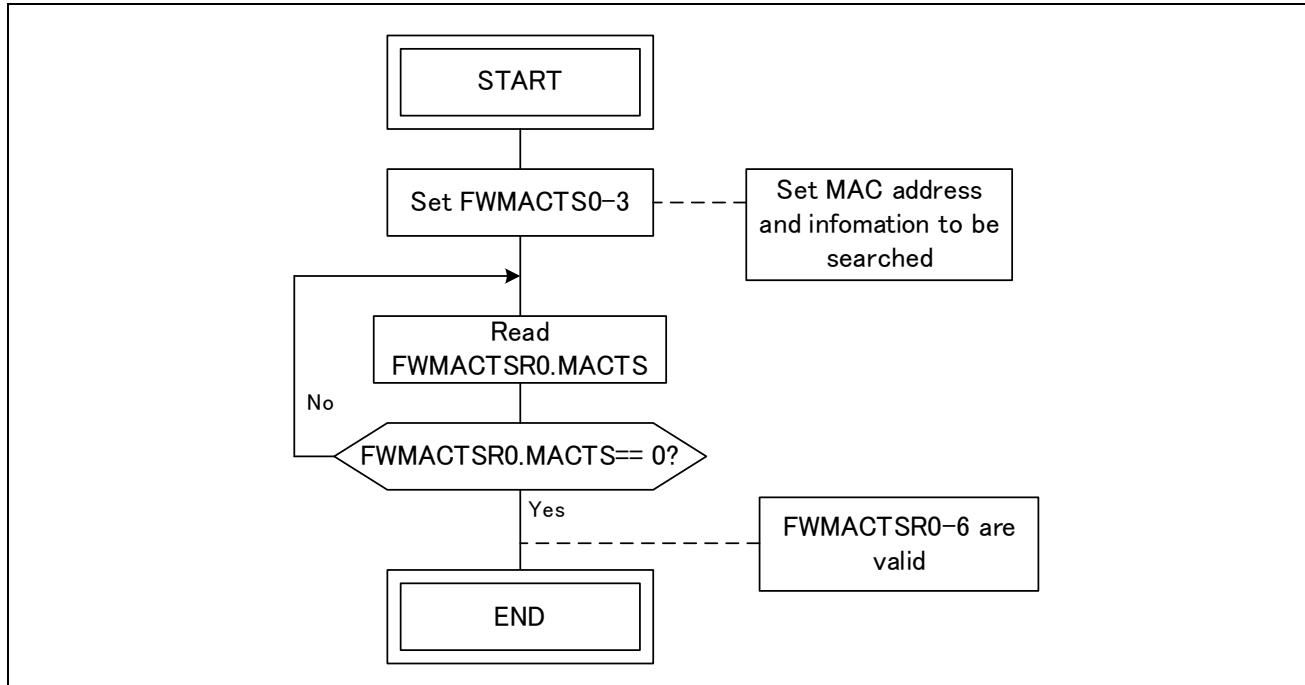


Fig 4.19: MAC entry search flow

4.1.7.6 VLAN entry search flow

VLAN entry search flow is described in Fig 4.20.

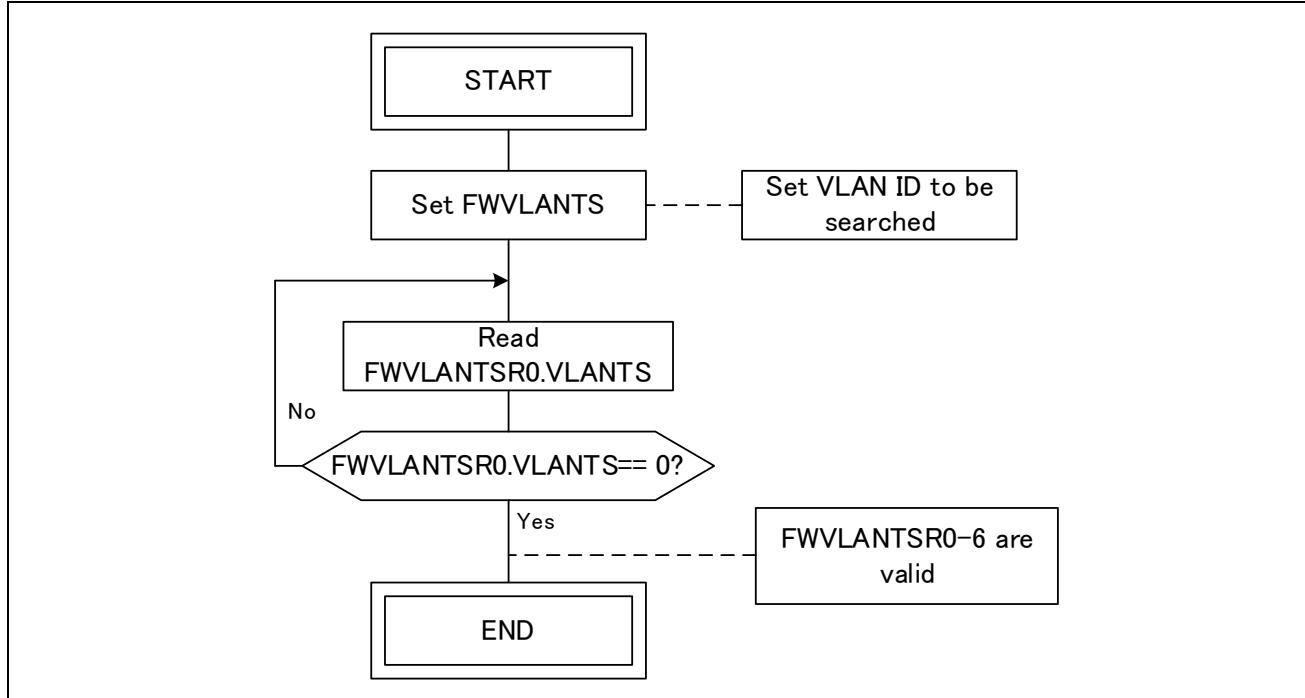


Fig 4.20: VLAN entry search flow

4.1.7.7 MAC entry read flow

MAC entry read flow is described in Fig 4.21.

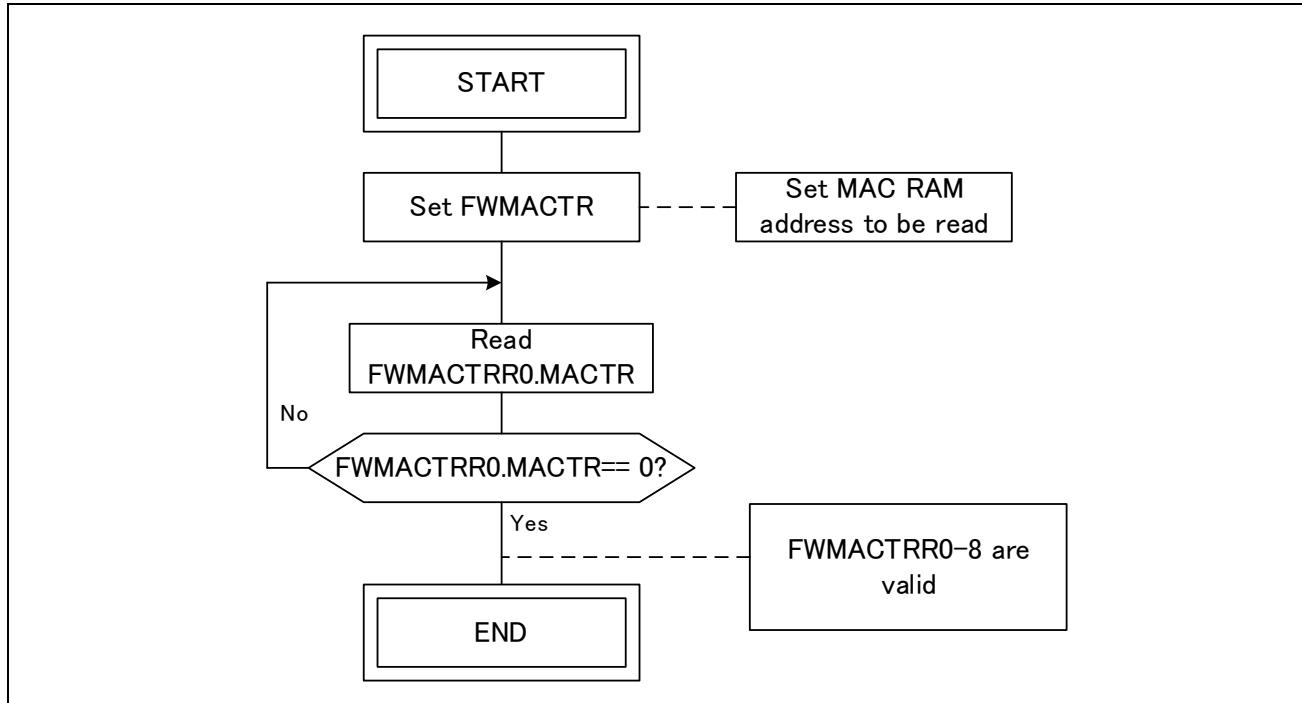


Fig 4.21: MAC entry read flow

4.1.8 Port based forwarding flows

4.1.8.1 Port i port-based setting flow

Port i port-based setting flow is described in Fig 4.22.

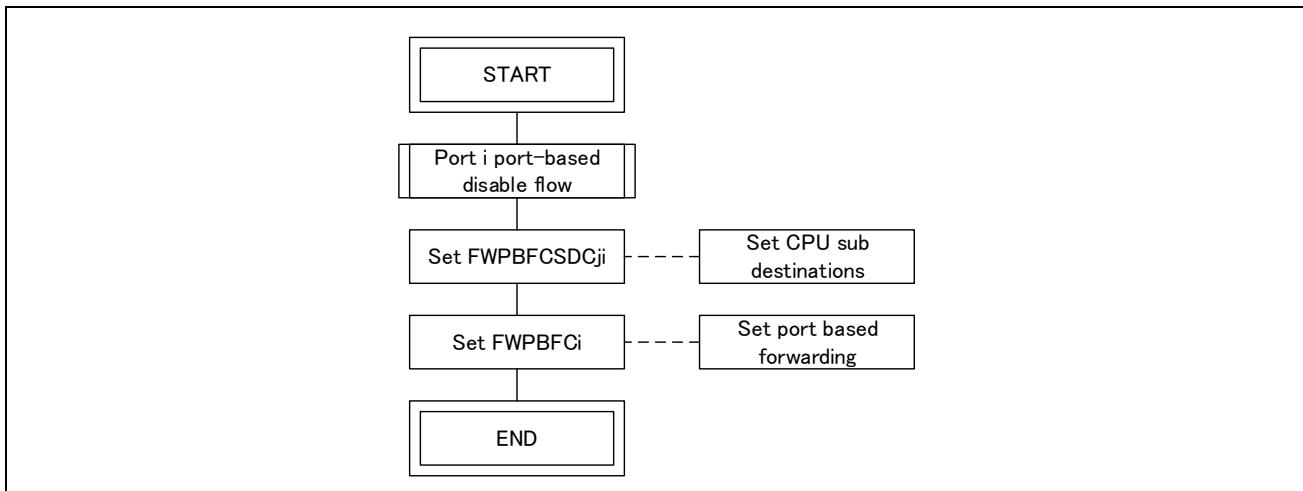


Fig 4.22: Port i port-based setting flow

4.1.8.2 Port i port-based disable flow

Port i port-based disable flow is described in Fig 4.23.

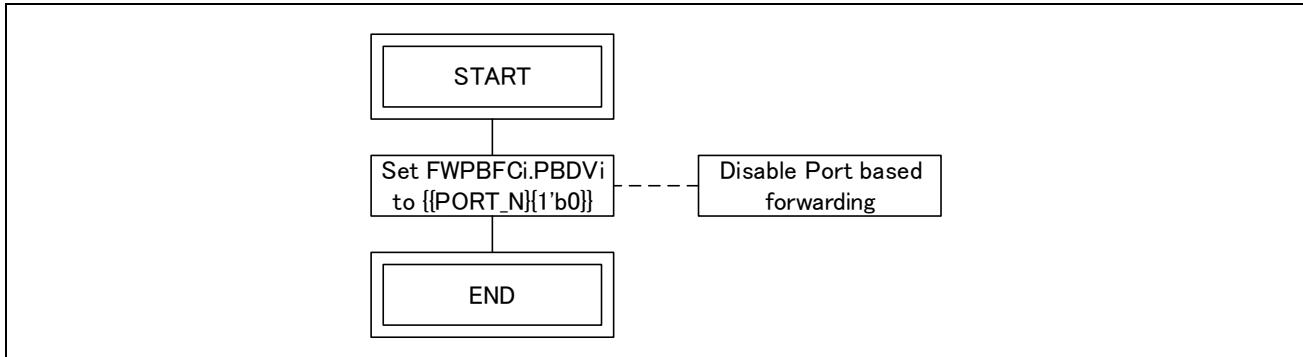


Fig 4.23: Port i port-based disable flow

4.1.9 Layer2/Layer3 update flows

4.1.9.1 Layer2/Layer3 Update table reset flow

Layer2/Layer3 Update table reset flow is described in Fig 4.24.

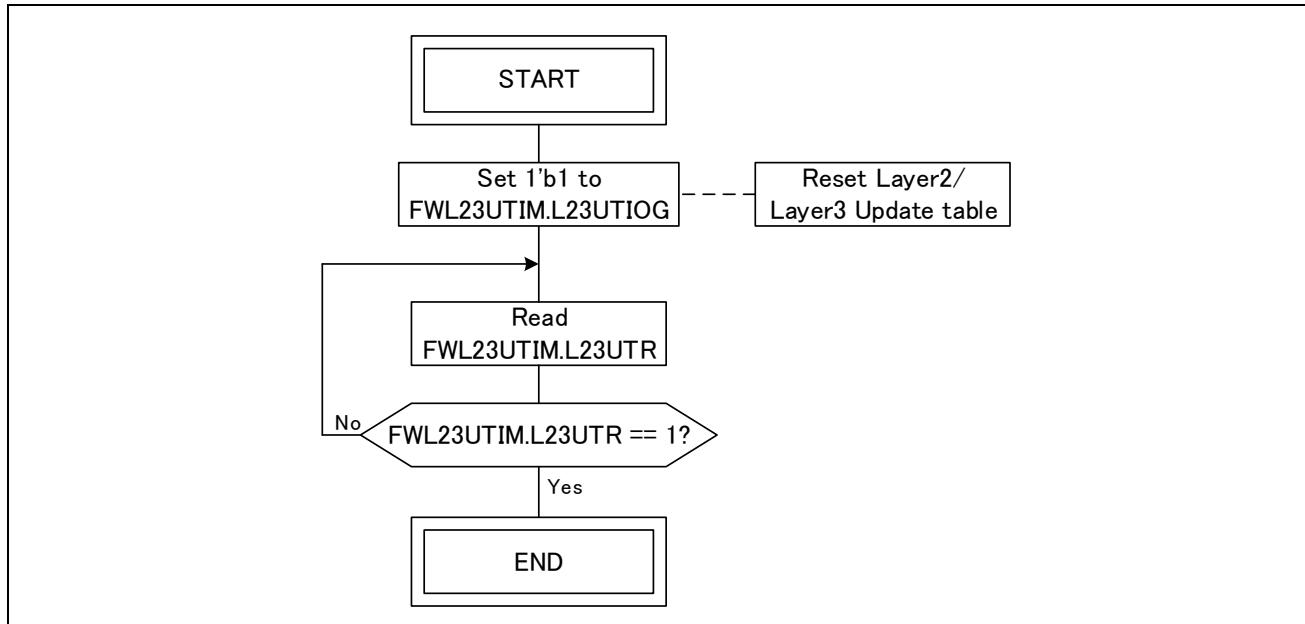


Fig 4.24: Layer2/Layer3 Update table reset flow

4.1.9.2 Layer2/Layer3 Update rule learn flow

Layer2/Layer3 Update rule learn flow is described in Fig 4.25.

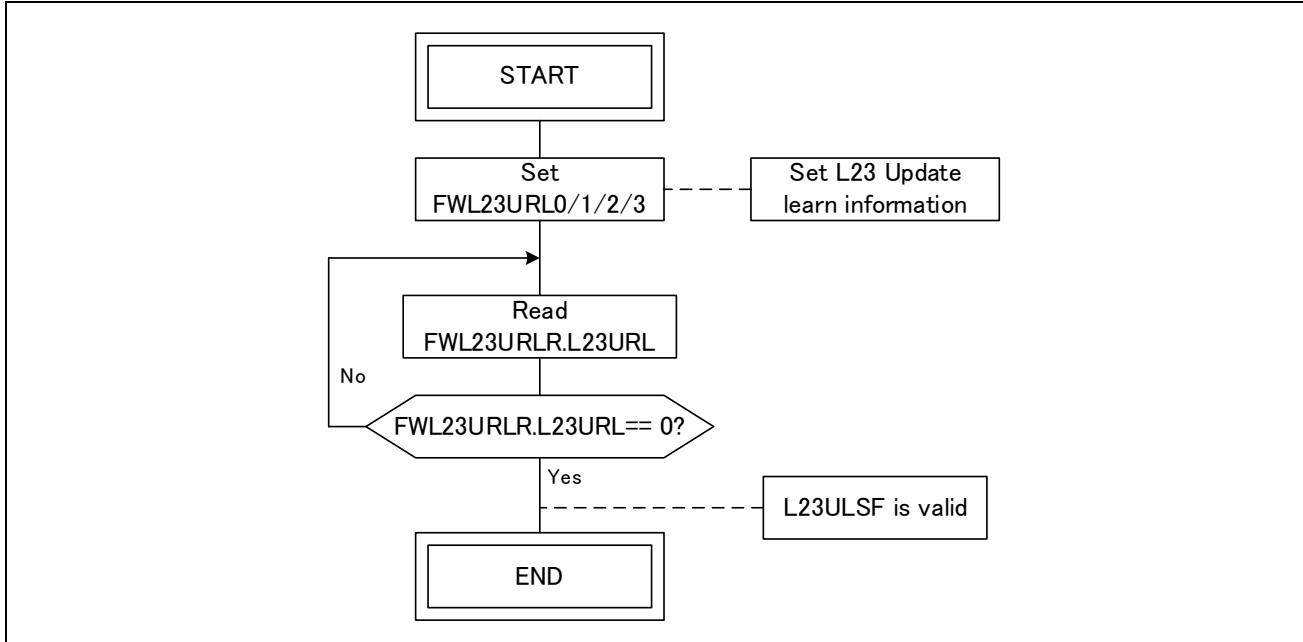


Fig 4.25: Layer2/Layer3 Update rule learn flow

4.1.9.3 Layer2/Layer3 Update rule read flow

Layer2/Layer3 Update rule read flow is described in Fig 4.26.

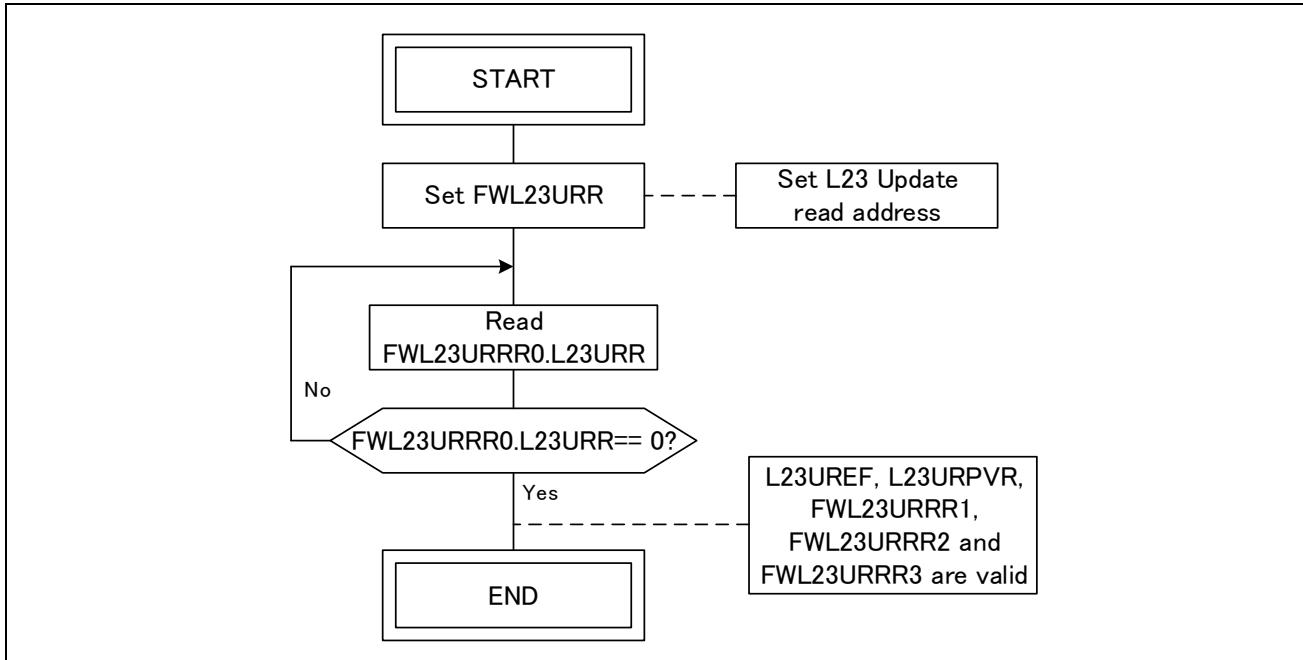


Fig 4.26: Layer2/Layer3 Update rule read flow

4.1.10 PSFP flows

4.1.10.1 MSDU filter i setting flow

MSDU filter i setting flow is described in Fig 4.27.

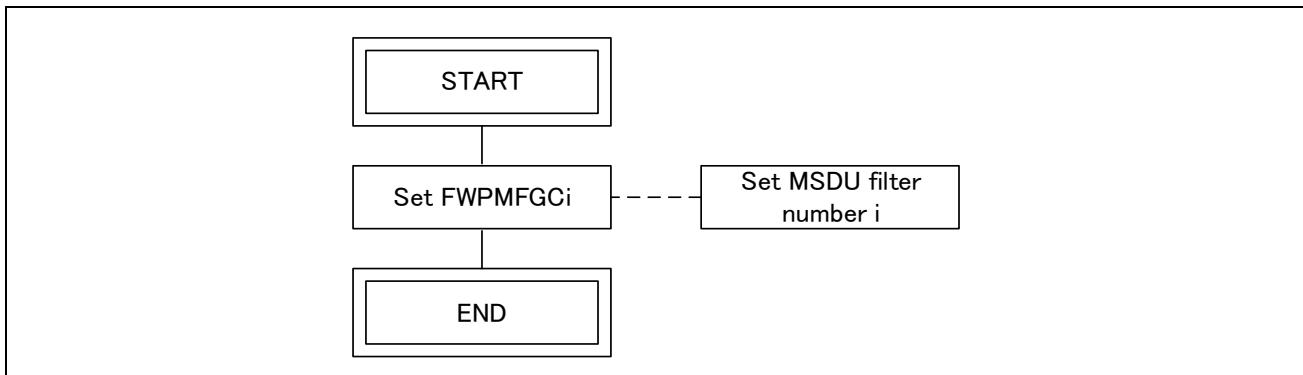


Fig 4.27: MSDU filter i setting flow

4.1.10.2 Gate RAM reset flow

Gate RAM reset flow is described in Fig 4.28.

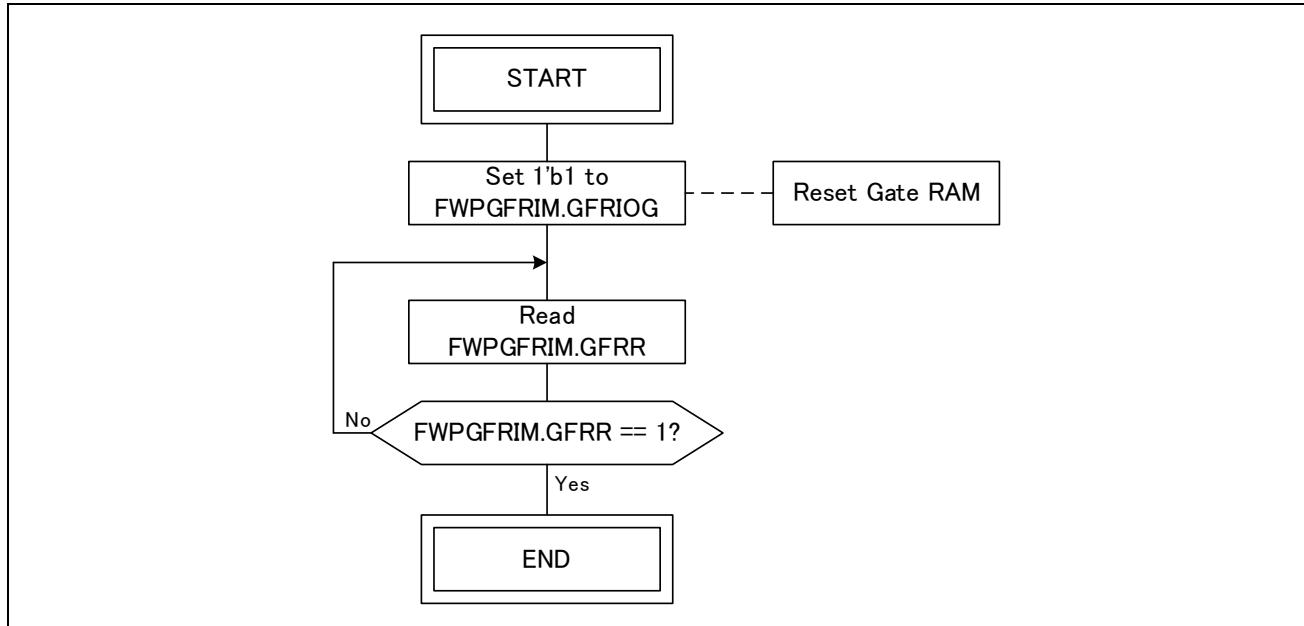


Fig 4.28: Gate RAM reset flow

4.1.10.3 Gate i setting flow

Gate i setting (and re-config) flow is described in Fig 4.29.

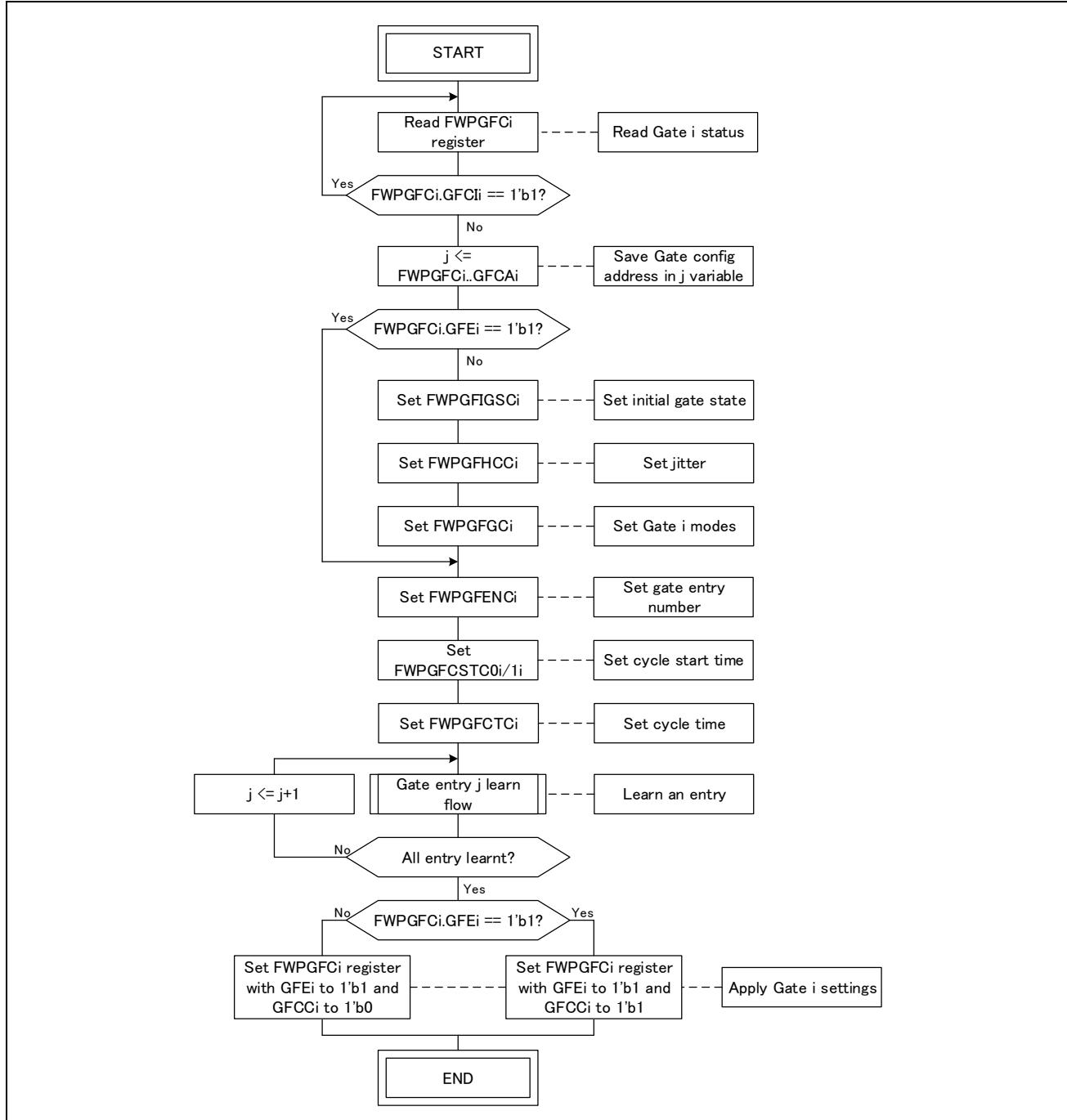


Fig 4.29: Gate i setting flow

4.1.10.4 Gate i disabling flow

Gate i disabling flow is described in Fig 4.30.

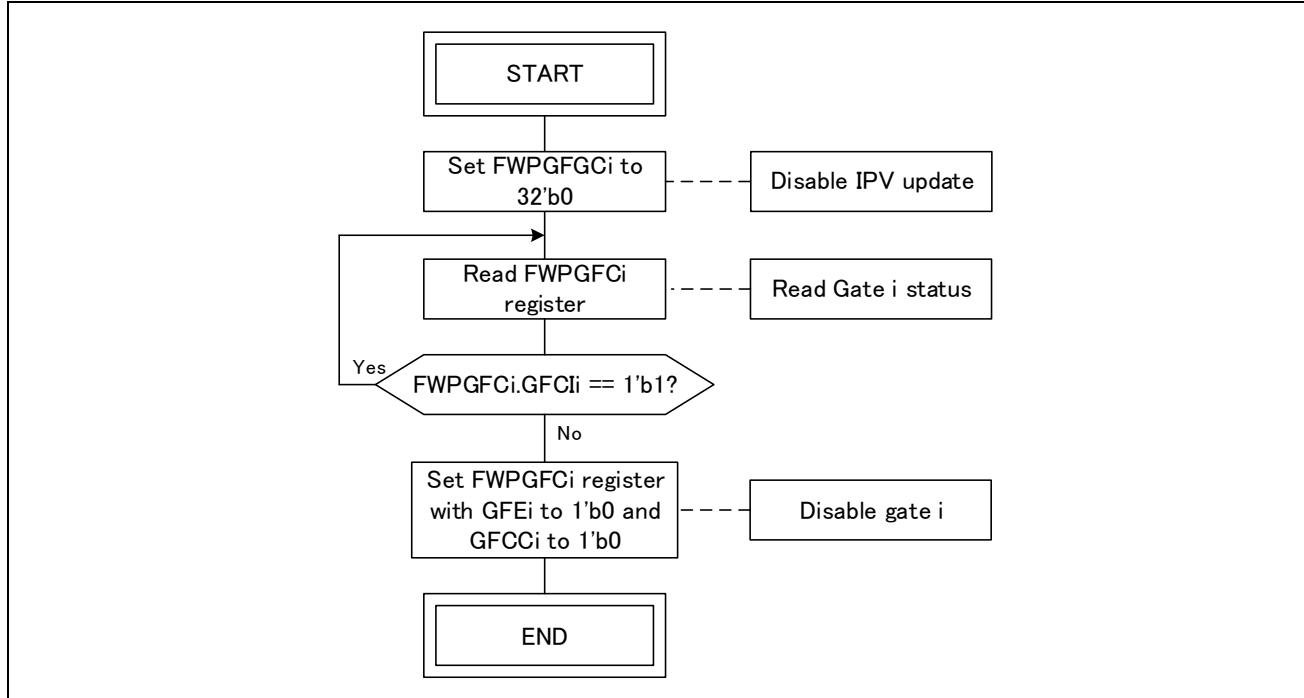


Fig 4.30: Gate i disabling flow

4.1.10.5 Gate i enabling flow

Gate i enabling flow is described in Fig 4.31.

Restrictions:

- Gate i enabling flow can only be applied after Gate i setting flow has been done at least one. By using Gate i enabling flow, Gate i will start will the schedule previously set with Gate i setting flow.

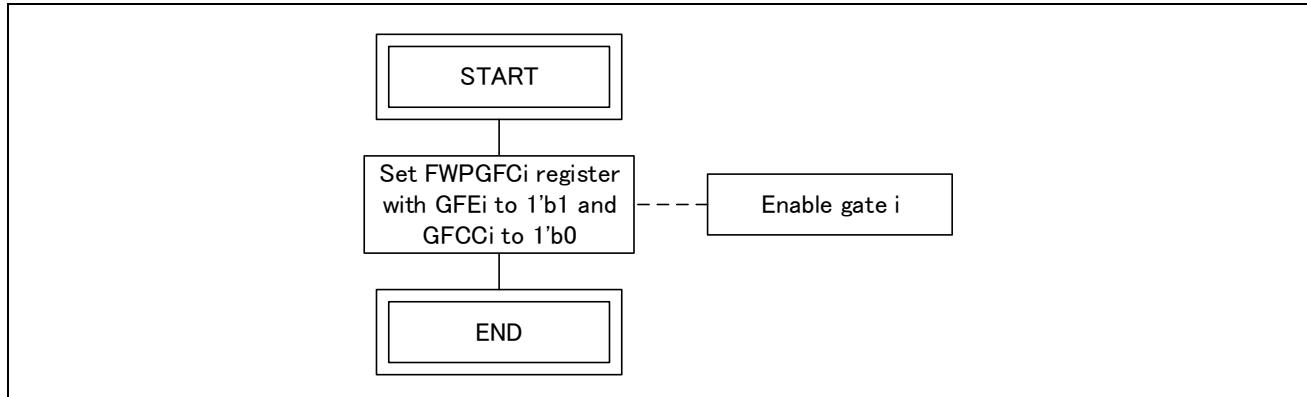


Fig 4.31: Gate i enabling flow

4.1.10.6 Gate entry i learn flow

Gate entry i learn is described in Fig 4.32.

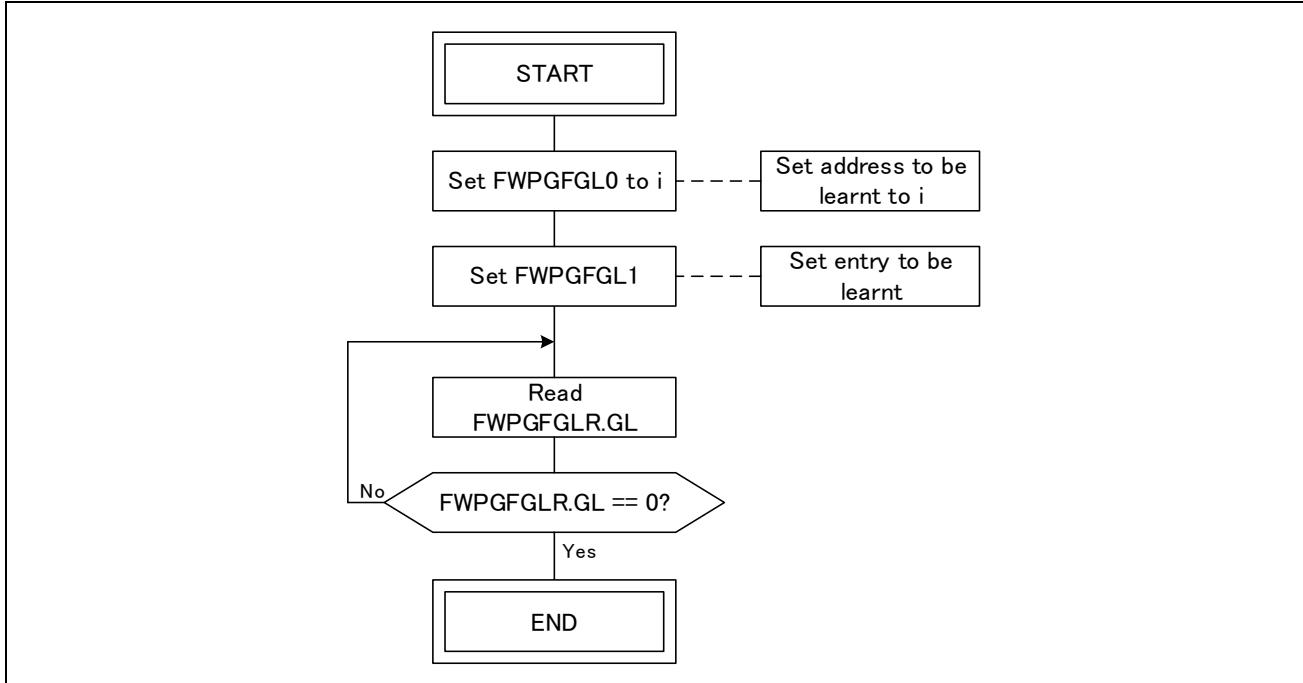


Fig 4.32: Gate entry i learn flow

4.1.10.7 Gate entry i read flow

Gate entry i read flow is described in Fig 4.33.

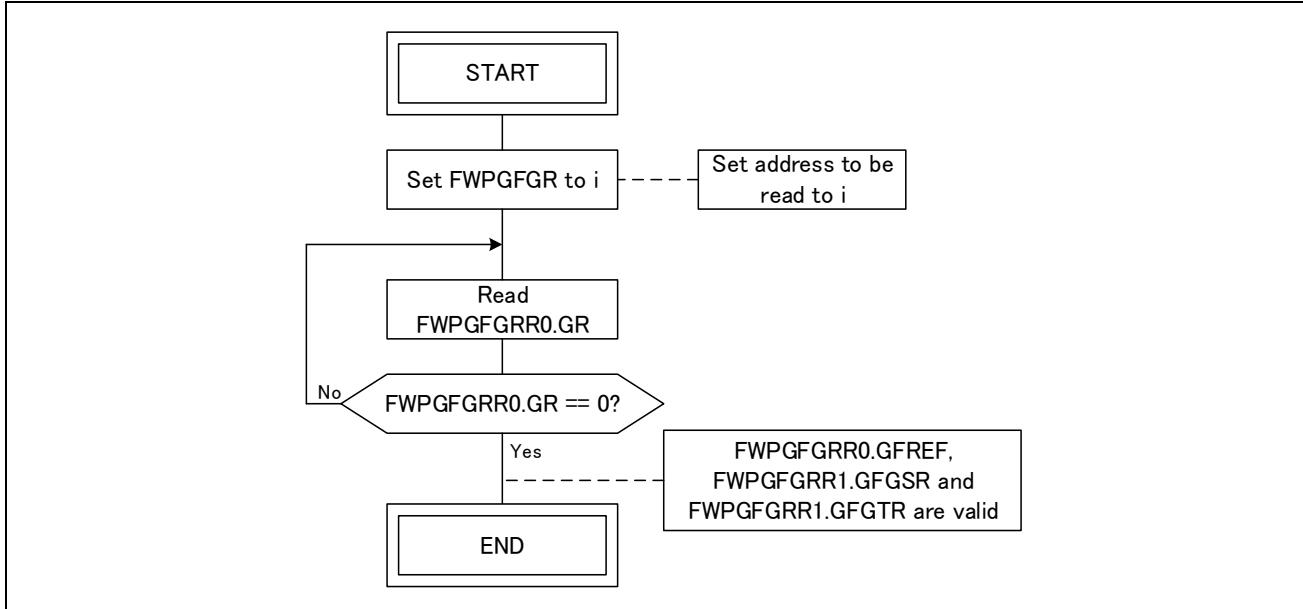


Fig 4.33: Gate entry i read flow

4.1.10.8 Meter i setting flow

Meter i setting flow is described in Fig 4.34.

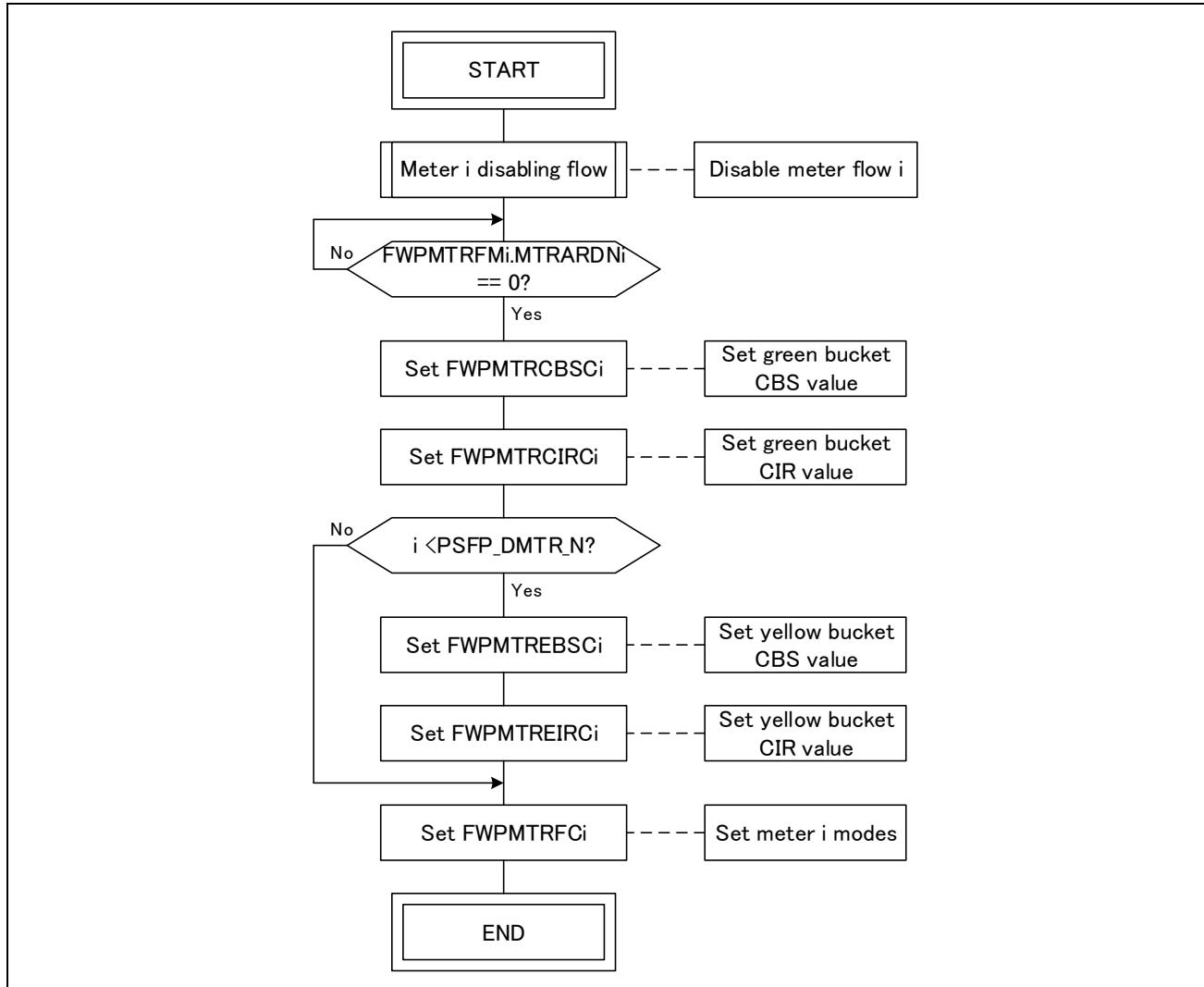


Fig 4.34: Meter i setting flow

4.1.10.9 Meter i disabling flow

Meter i disabling flow is described in Fig 4.35.

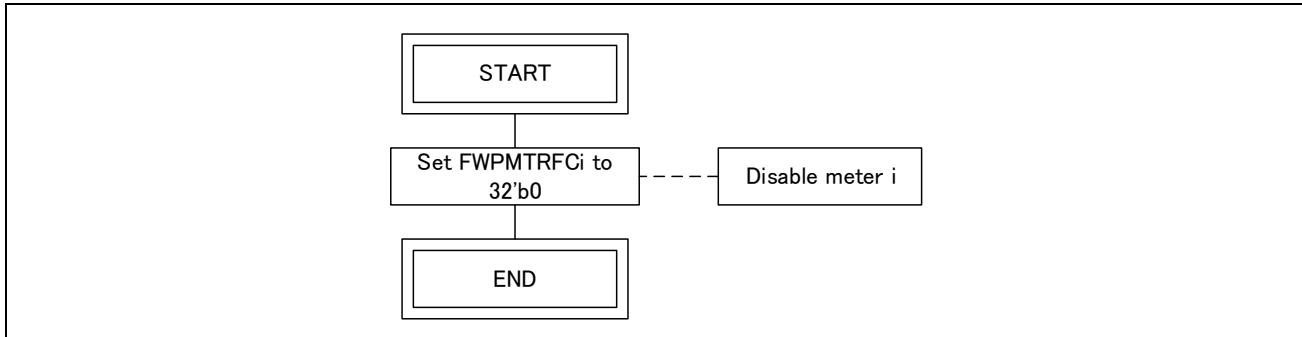


Fig 4.35: Meter i disabling flow

4.1.10.10 Per port i and IPV j filtering setting flow

Per port i and IPV j filtering setting flow is described in Fig 4.36.

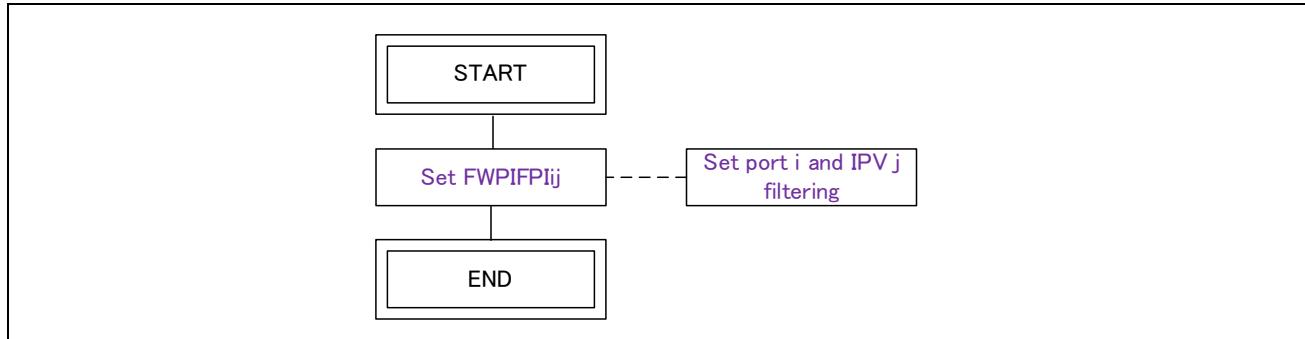


Fig 4.36: Per port i and IPV j filtering setting flow

4.1.11 FRER flows

4.1.11.1 FRER table reset flow

FRER table reset flow is described in Fig 4.37.

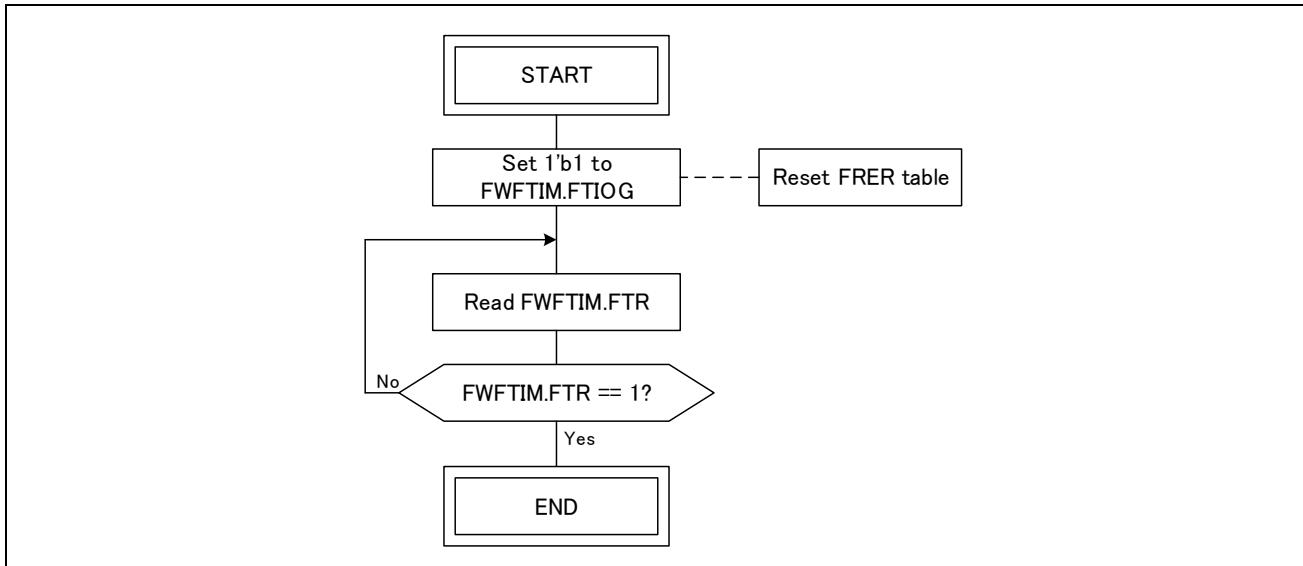


Fig 4.37: FRER table reset flow

4.1.11.2 FRER entry i learn flow

FRER entry i learn flow is described in Fig 4.38.

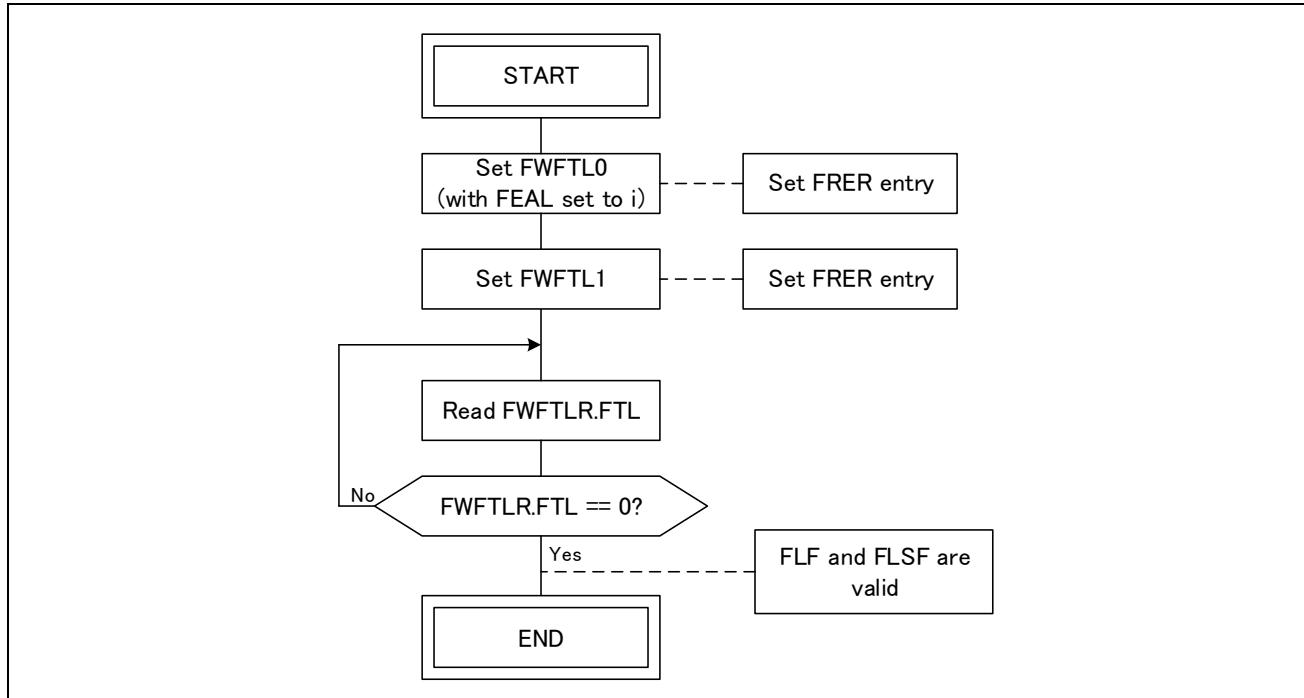


Fig 4.38: FRER entry i learn flow

4.1.11.3 FRER entry i read flow

FRER entry i read flow is described in Fig 4.39.

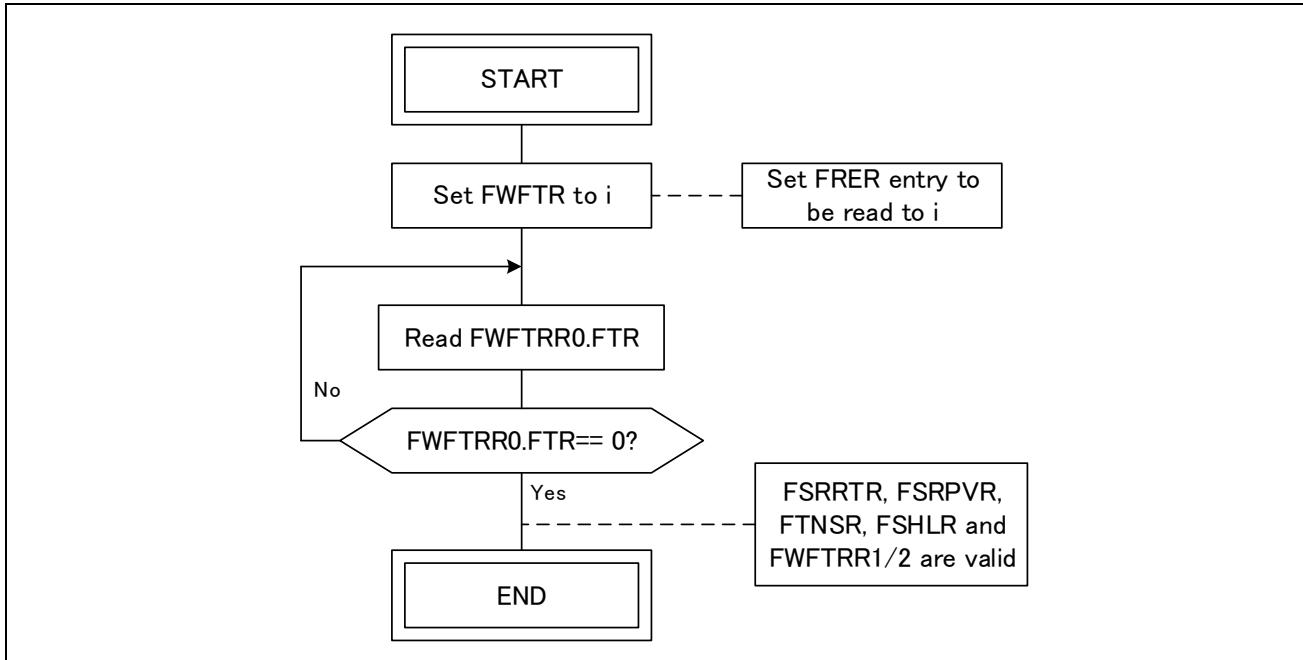


Fig 4.39: FRER entry i read flow

4.1.12 Called software flows

The flows described in this section can only be called from other flows thanks to a “flow link” box (Fig 4.1) and cannot be used alone.

4.1.12.1 Full setting flow

Full setting flow is described in Fig 4.40.

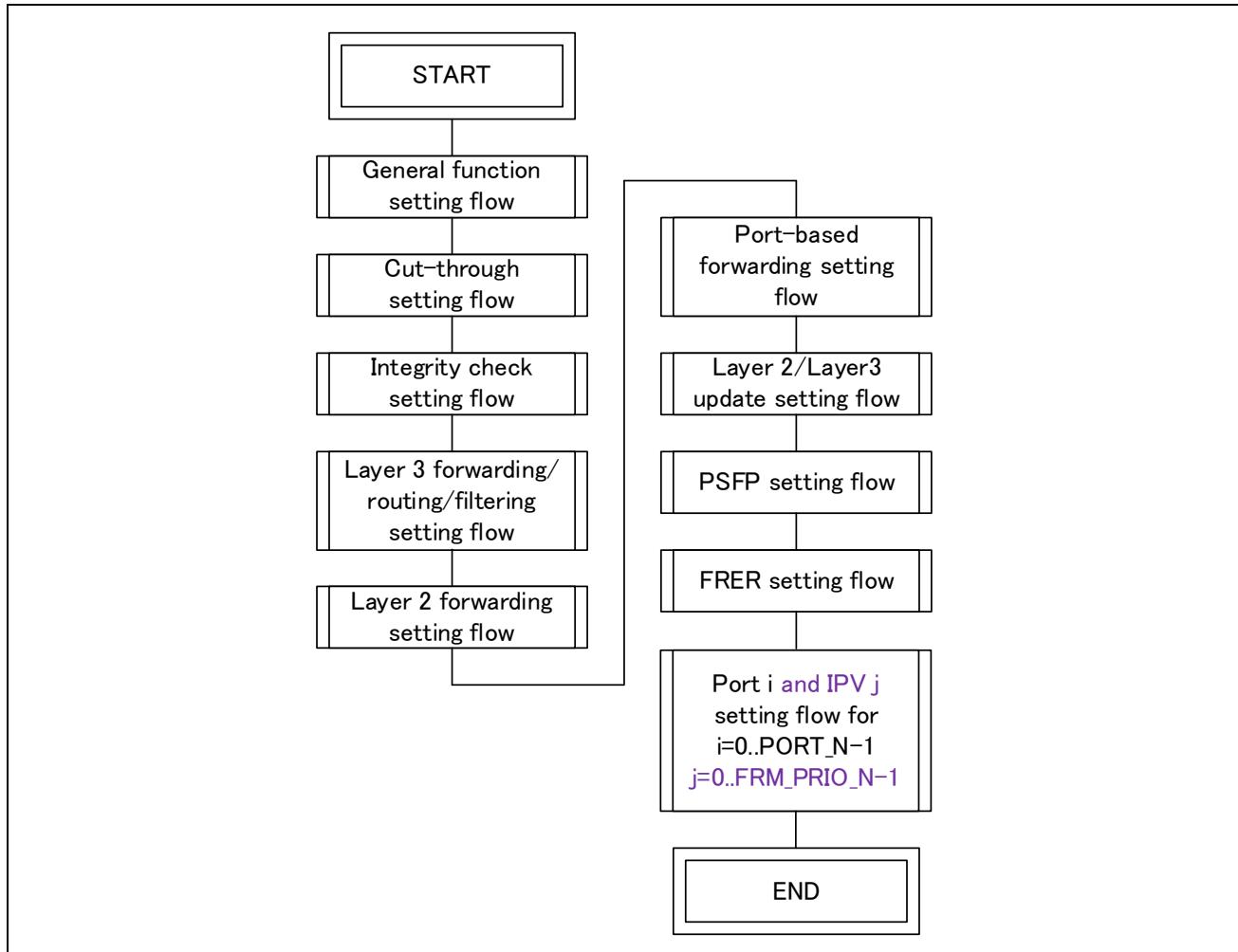


Fig 4.40: Full setting flow

4.1.12.2 General function setting flow

General function setting flow is described in Fig 4.41.

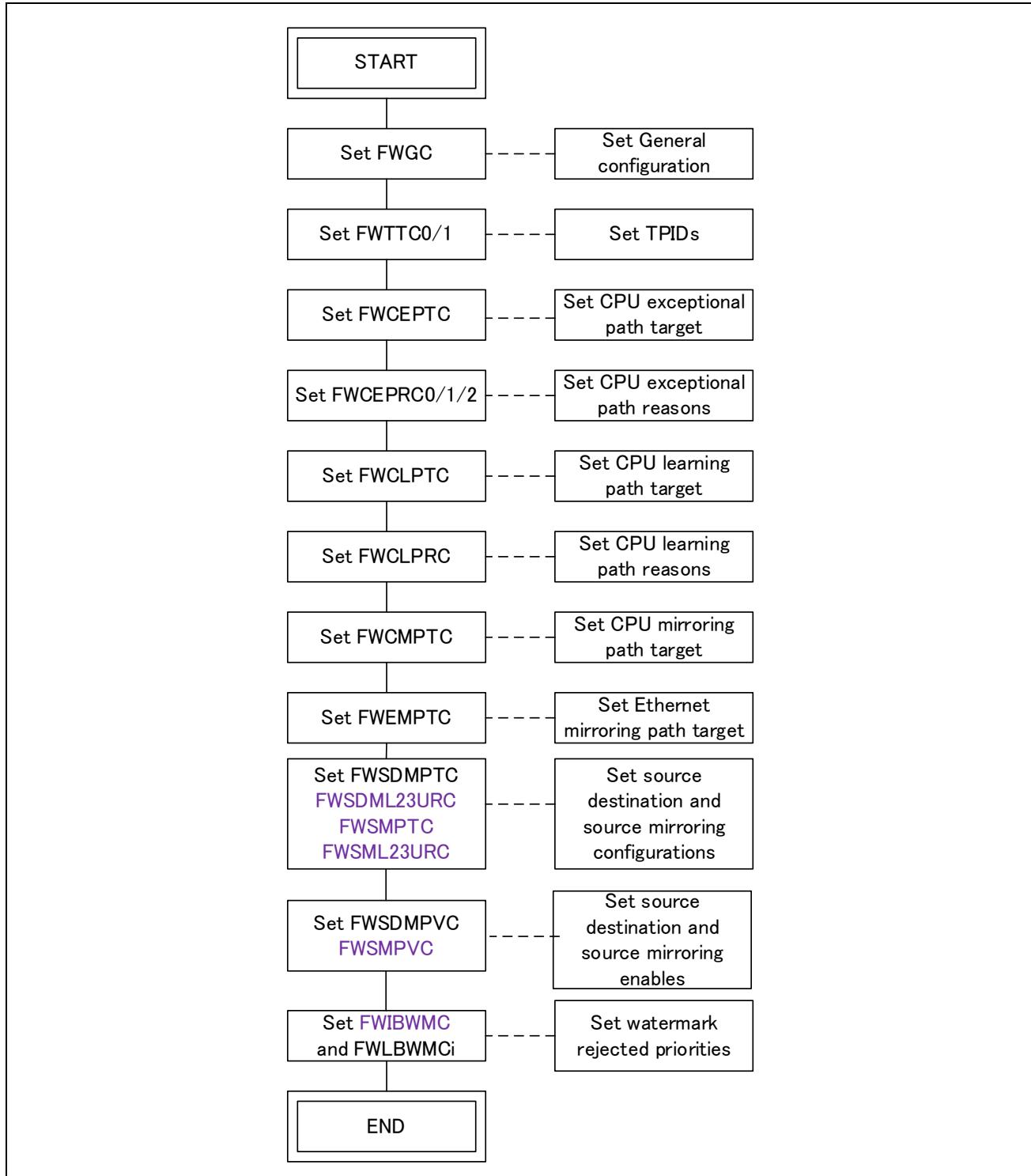


Fig 4.41: General function setting flow

4.1.12.3 Cut-through setting flow

Cut-through setting flow is described in Fig 4.42.

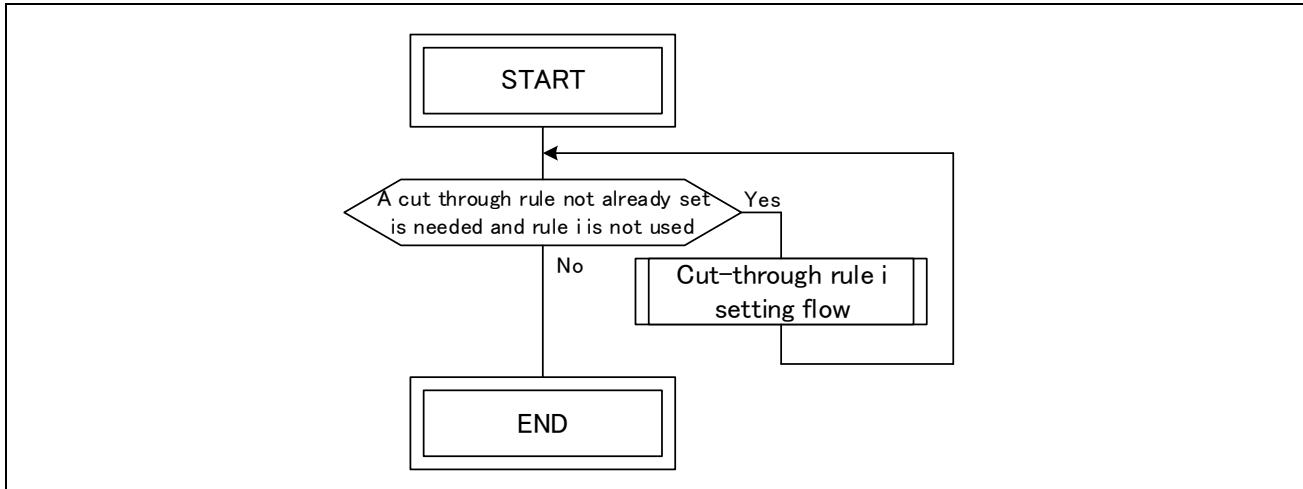


Fig 4.42: Cut-through setting flow

4.1.12.4 Integrity check setting flow

Integrity check setting flow is described in Fig 4.43.

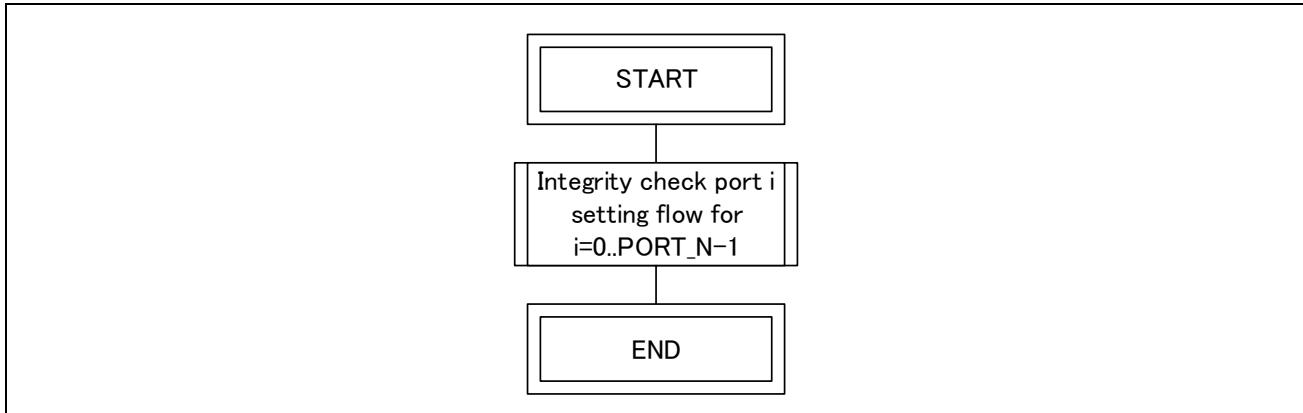


Fig 4.43: Integrity check setting flow

4.1.12.5 Two-byte filter i setting flow

Two-byte filter i setting flow is described in Fig 4.44.

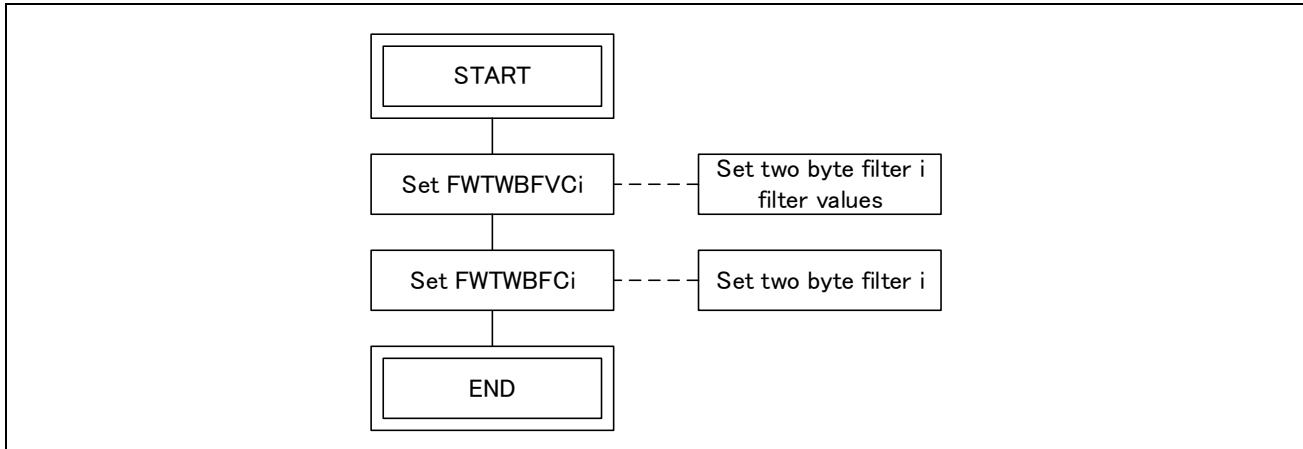


Fig 4.44: Two-byte filter i setting flow

4.1.12.6 Three-byte filter i setting flow

Three-byte filter i setting flow is described in Fig 4.45.

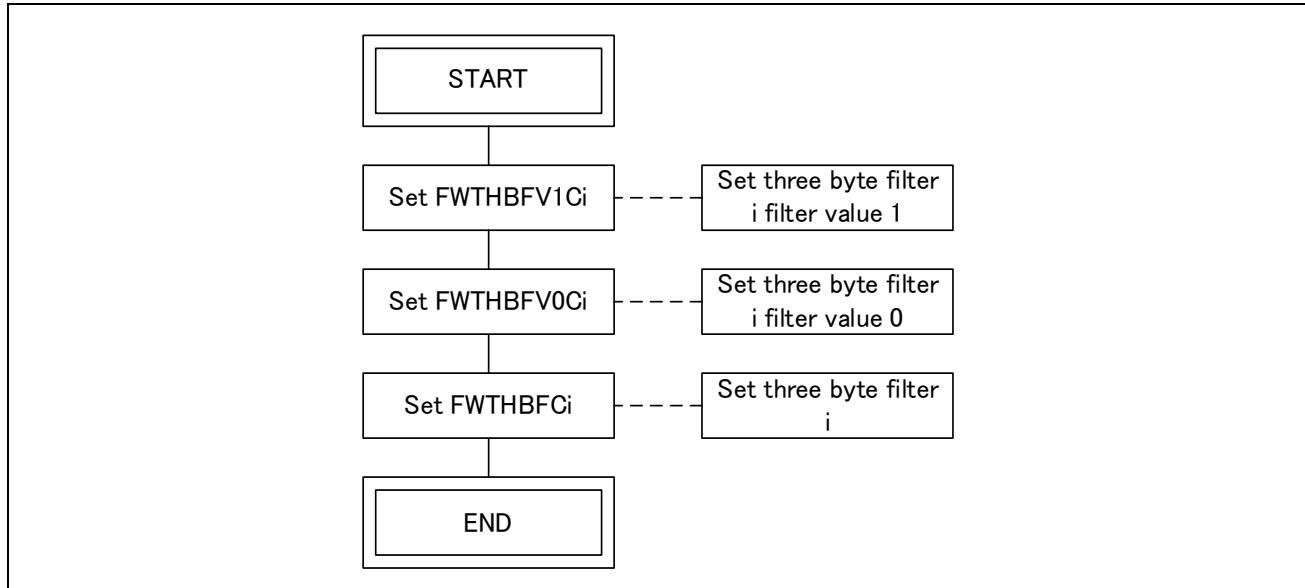


Fig 4.45: Three-byte filter i setting flow

4.1.12.7 Four-byte filter i setting flow

Four-byte filter i setting flow is described in Fig 4.46.

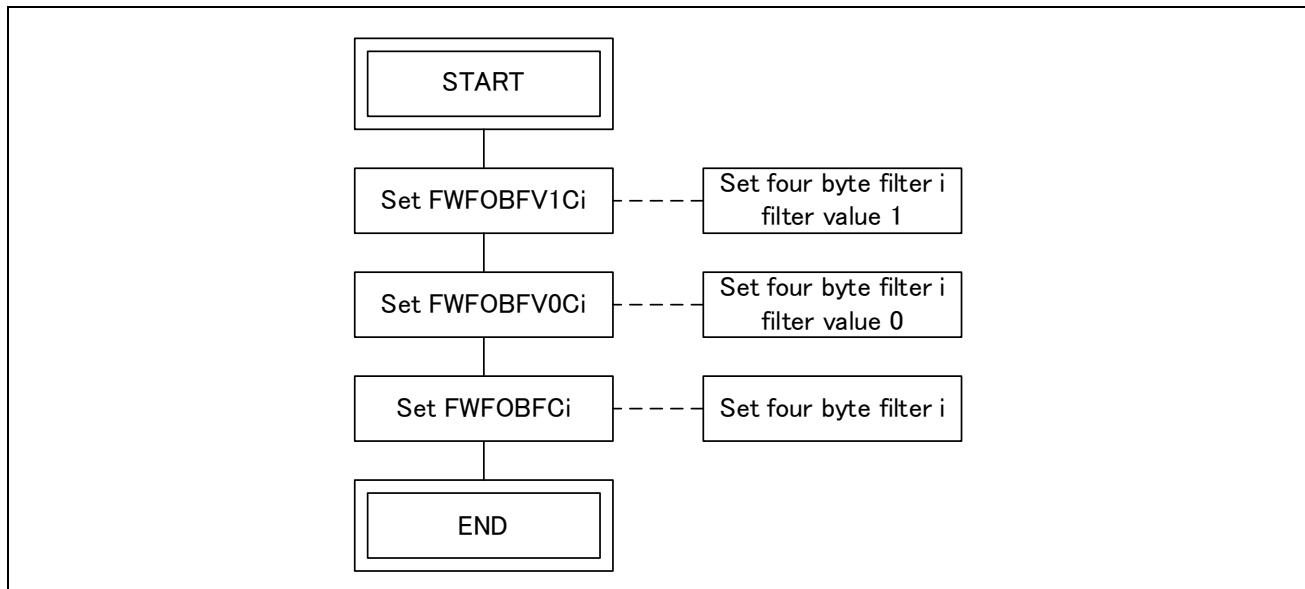


Fig 4.46: Four-byte filter i setting flow

4.1.12.8 Range filter i setting flow

Range filter i setting flow is described in Fig 4.47.

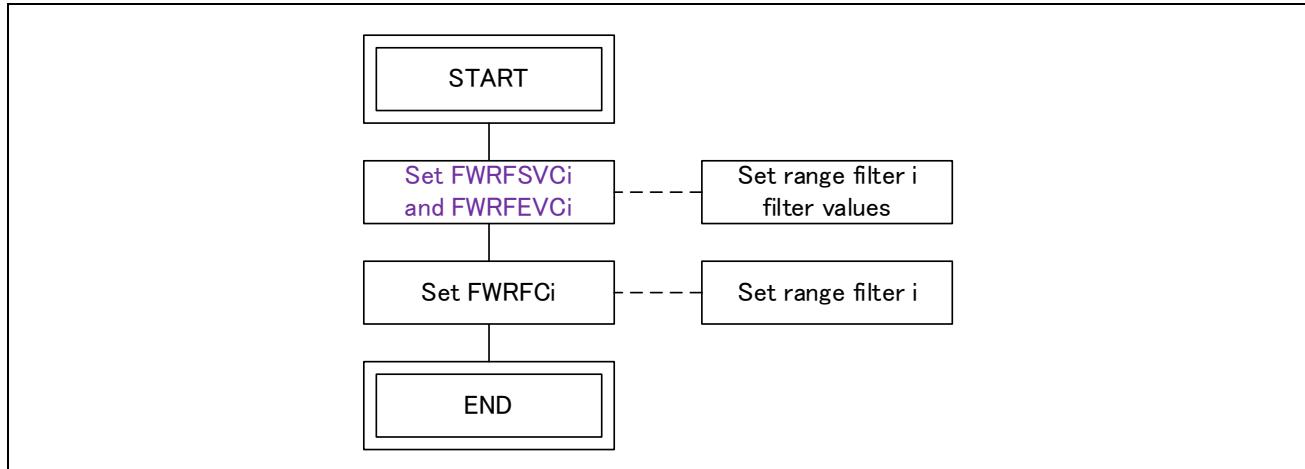


Fig 4.47: Range filter i setting flow

4.1.12.9 L3/L2 stream filter setting flow

L3/L2 stream filter setting flow is described in Fig 4.48.

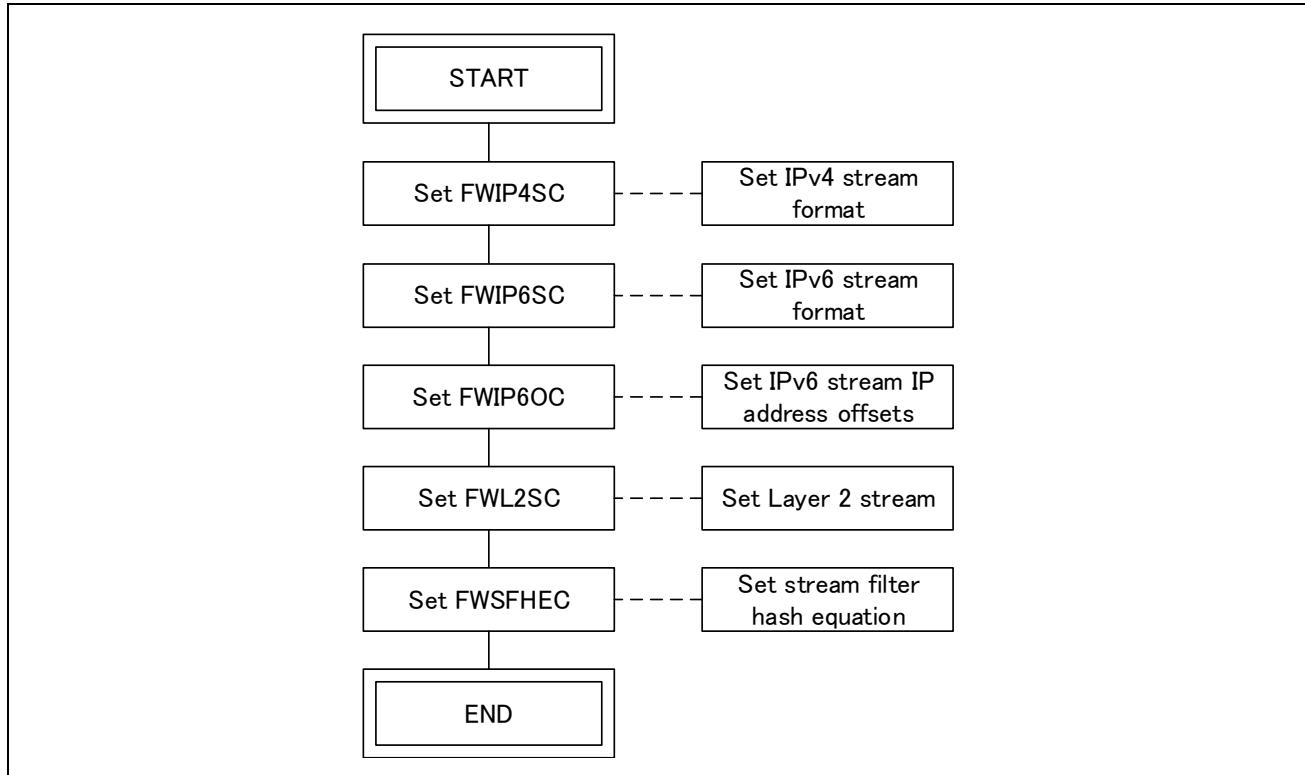


Fig 4.48: L3/L2 stream filter setting flow

4.1.12.10 Layer 3 forwarding/routing/filtering setting flow

Layer 3 forwarding/routing/filtering setting flow is described in Fig 4.49.

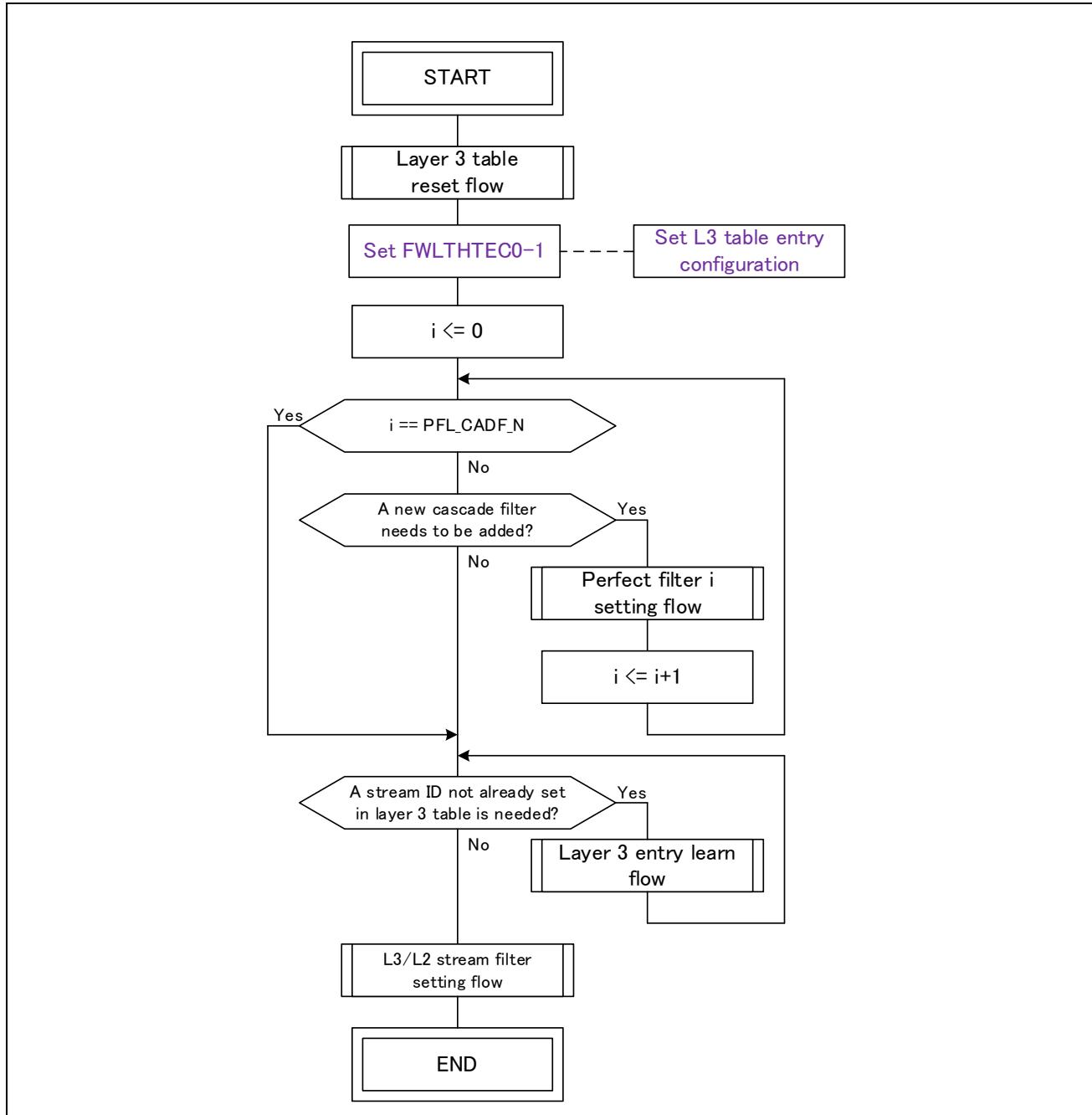


Fig 4.49: Layer 3 forwarding/routing/filtering setting flow

4.1.12.11 Layer 2 forwarding setting flow

Layer 2 forwarding setting flow is described in Fig 4.50.

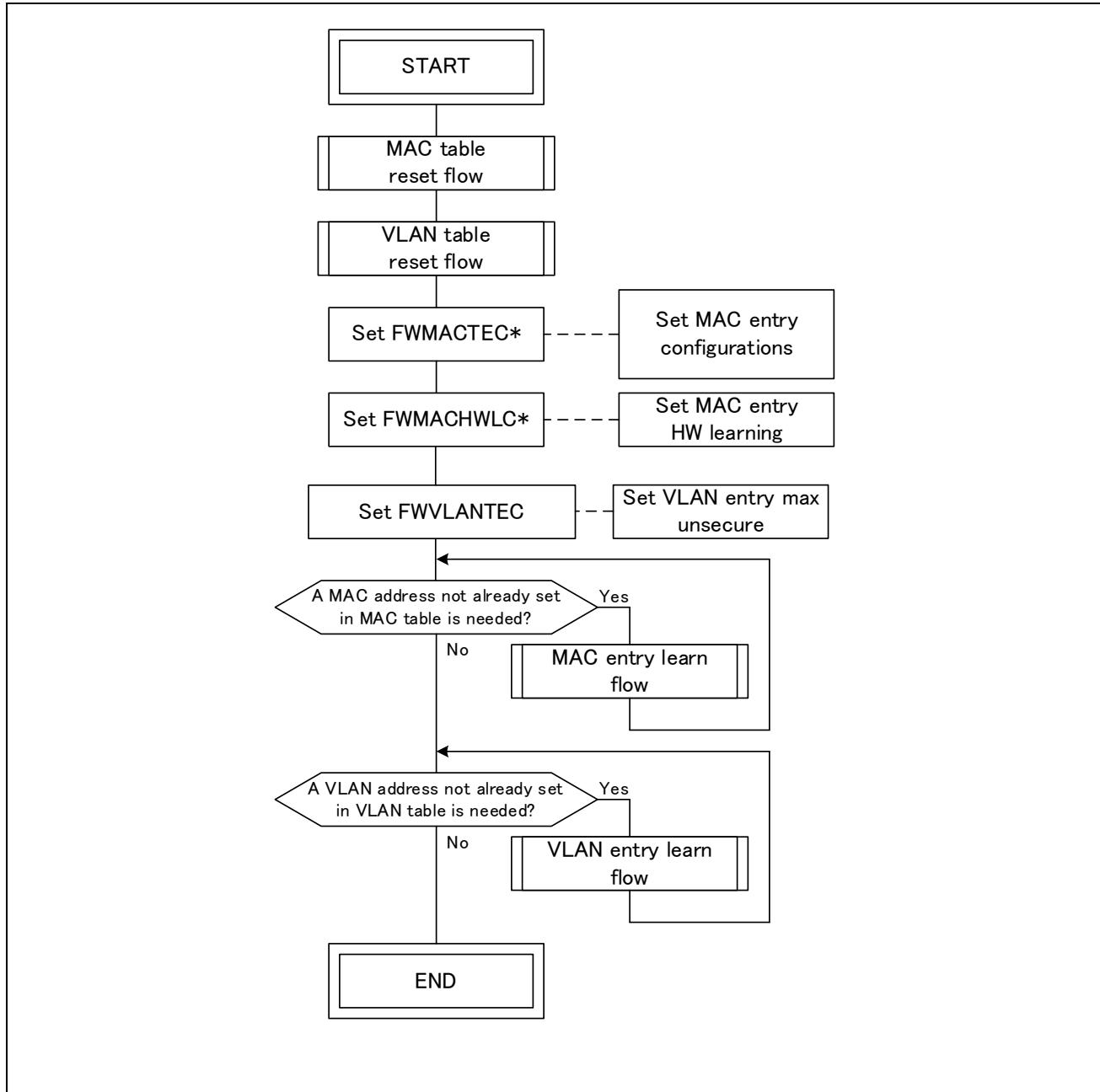


Fig 4.50: Layer 2 forwarding setting flow

4.1.12.12 Port-based forwarding setting flow

Port-based forwarding setting flow is described in Fig 4.51.

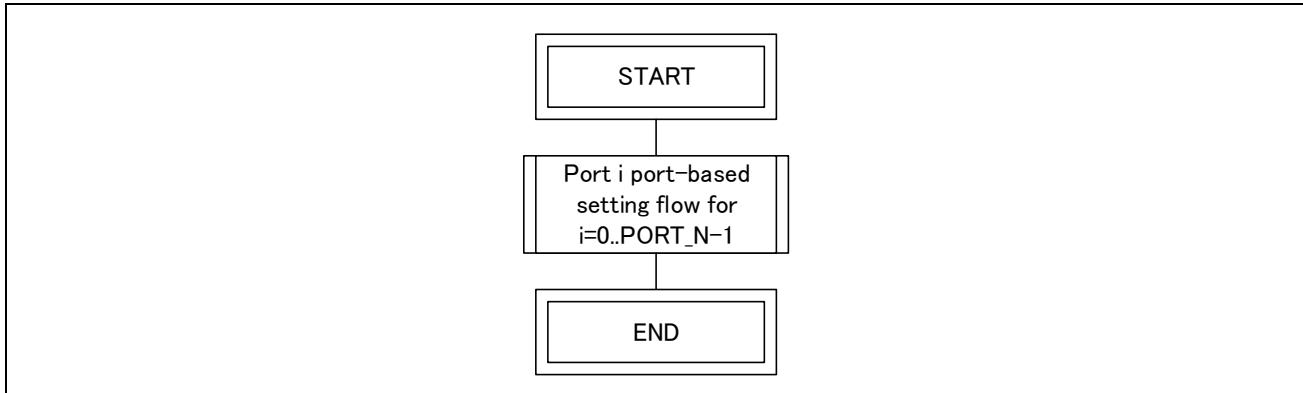


Fig 4.51: Port-based forwarding setting flow

4.1.12.13 Layer 2/Layer3 update setting flow

Layer 2/Layer3 update setting flow is described in Fig 4.52.

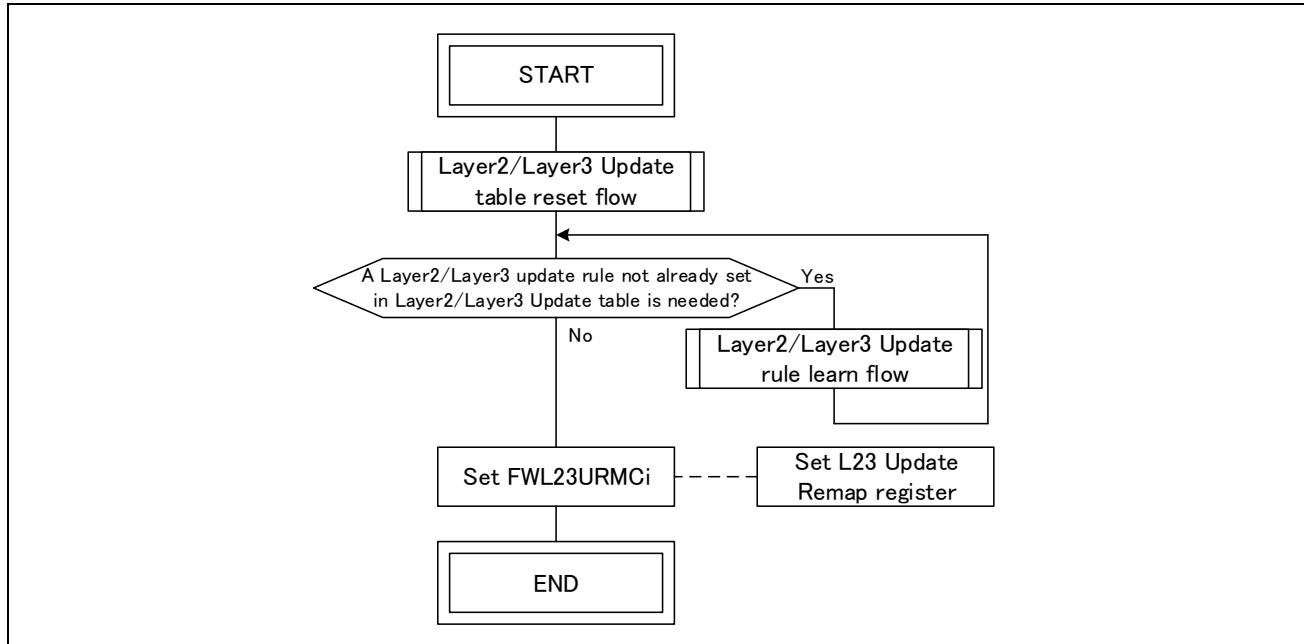


Fig 4.52: Layer 2/Layer3 update setting flow

4.1.12.14 PSFP setting flow

PSFP setting flow is described in Fig 4.53.

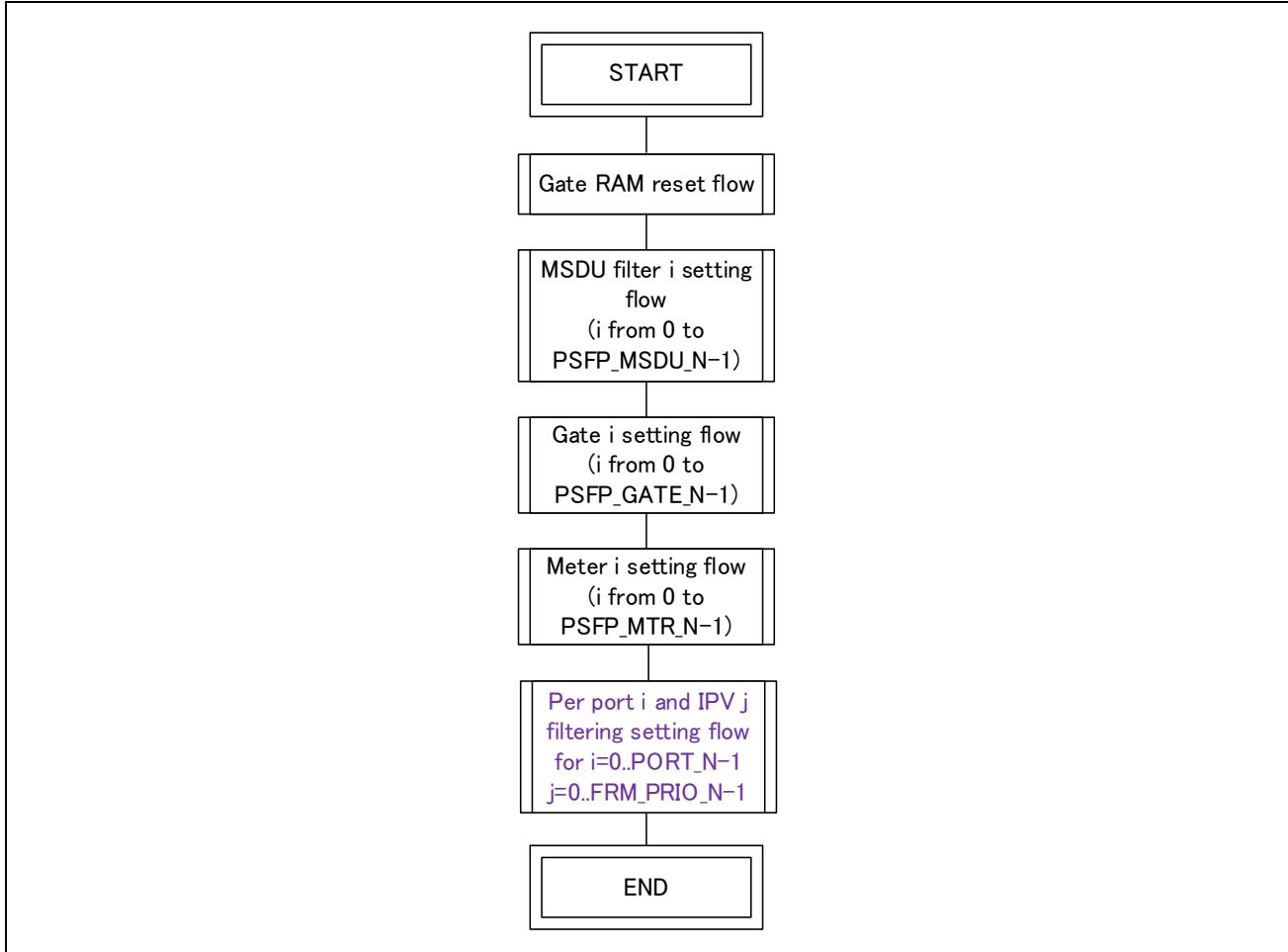


Fig 4.53: PSFP setting flow

4.1.12.15 FRER setting flow

FRER setting flow is described in Fig 4.54.

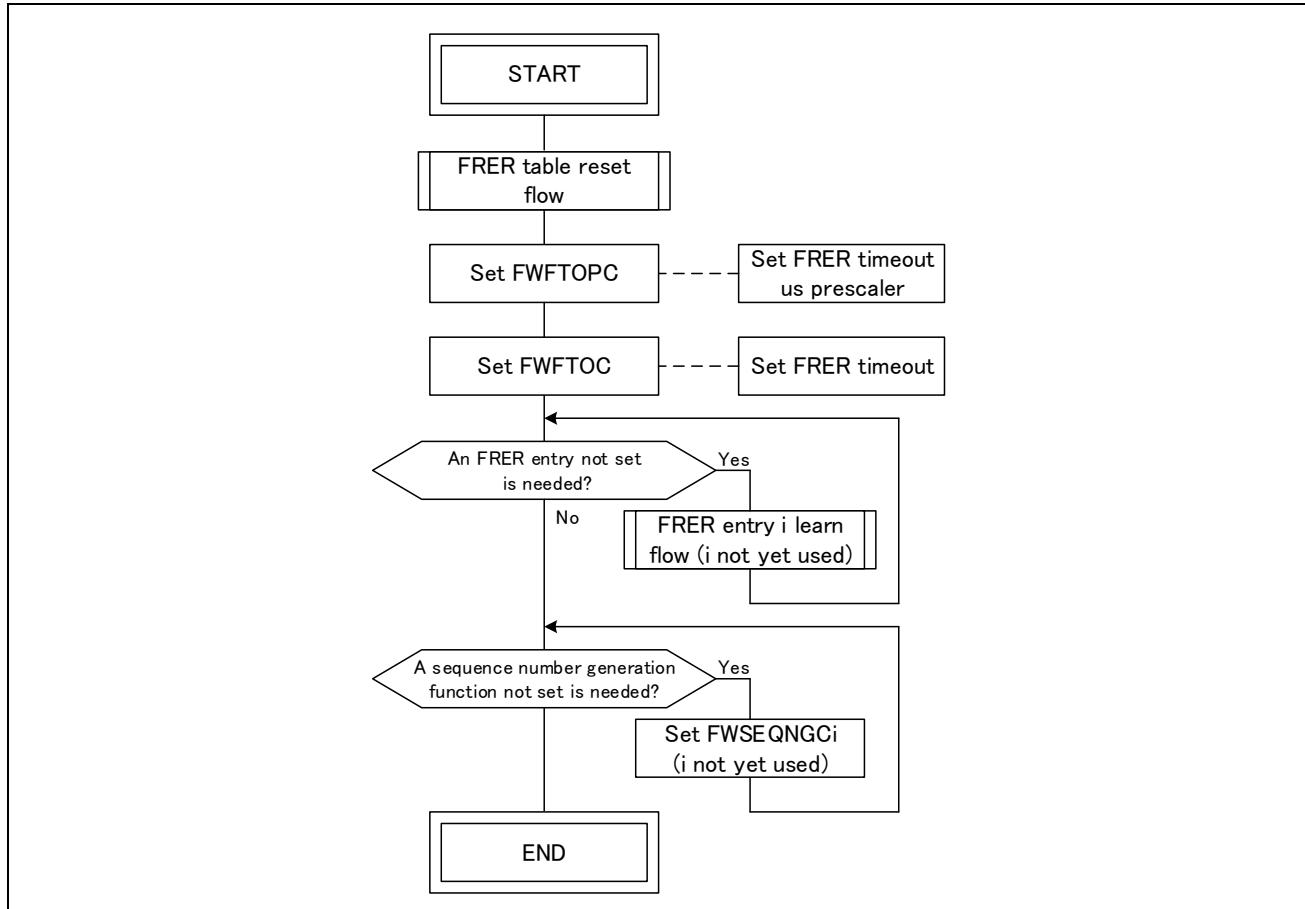


Fig 4.54: FRER setting flow

4.1.13 Register writable without software flow after initialization

This section describes registers that have not been described so far. These registers can be changed dynamically.
(However, it is necessary that the initial settings such as the clock enabling have been completed.)

5. Functional details

5.1 General functionalities

General functionalities are separated in several types:

- Descriptors.
- R-switch modes.
- R-switch TPIDs.
- R-switch debug functions.
- R-switch watermark.

5.1.1 Descriptors

To forward a frame to one or several port, the forwarding emits descriptors through the descriptor bus. All descriptor emitted by the forwarding engine shall follow the descriptor format described in Table 5-1. In following sections when a function emits a descriptor it will be explained using the field name. Only fields that are not determined by the input local descriptor or the input frame will be explained.

Table 5-1: Descriptor field

Field name FDESCR.	Bit width	Field explanation	Values
DV	PORT_N	Values: - Bit i set to 1'b0: Descriptor not valid for port i - Bit i set to 1'b1: Descriptor valid for port i	Depends on descriptor. Will be explained per descriptor in following sections.
SEC	1	Values: - 1'b0: Descriptor is unsecure - 1'b1: Descriptor is secure	Depends on descriptor. Will be explained per descriptor in following sections.
CSD	PORT_GWCA_N* AXI_CHAIN_W	Bit [AXI_CHAIN_W*(i+1)-1:AXI_CHAIN_W*i] (written as FDESCR.CSDi) define the CPU Sub destination for GWCA number i (CPU Sub destination is equivalent to AXI descriptor queue number)	Depends on descriptor. Will be explained per descriptor in following sections.
IPV	3	Internal priority value before agent internal priority remapping	Depends on descriptor. Will be explained per descriptor in following sections.
SPN	PORT_W	Port number from which the frame came from	Set to the source agent port number given by mfw_spn_fwd pin
TPL	FRM_TPL_W	Input frame total payload length.	Set to the TPL value given by agent through local descriptors
MINFO	24	Meta-information associated to a frame for CPU forwarding	Depends on descriptor. Will be explained per descriptor in following sections.
RV	1	Routing valid. Informs agents that routing rules should be fetched to forwarding engine through L23 update bus to update frame information	Depends on descriptor. Will be explained per descriptor in following sections.
RN	LTH_RRULE_W	Routing number. Informs agents that routing number should be used when FDESCR.RV is set	Depends on descriptor. Will be explained per descriptor in following sections.
VCTRL	FRM_VCTRL_W	VLAN control information.	Set to the VCTRL value given by agent through local descriptors

Field name FDESCR.	Bit width	Field explanation	Values
RTGI	1	R-TAG in	Set to the RTGI value given by agent through local descriptors
SEQN	16	Frame sequence number	Depends on descriptor. Will be explained per descriptor in following sections.
FI	1	Values: - 1'b0: Input frame does not contain its FCS - 1'b1: Input frame contains its FCS	Set to the FI value given by agent through local descriptors
FW	1	Values: - 1'b0: If input frame contains its FCS, it was correct when given to the switch - 1'b1: If input frame contains its FCS, it was incorrect when given to the switch	Set to the FW value given by agent through local descriptors

5.1.2 R-Switch modes

R-switch modes define the general behavior of the switch using **FWGC** registers.

Functions:

- **FWGC.SVM** register sets the VLAN format that will be used by the forwarding engine. Depending on this setting all the agents should convert ethernet frames in the required format (for format conversion refer to GWCA specification document [GWCA]).

5.1.3 R-switch TPIDs

R-switch TPIDs for C-TAG, S-TAG and R-TAG [801.2Q] [801.2CB] can be set by the user using **FWTTC0** and **FWTTC1** registers.

Functions:

- **FWTTC0** register sets the S-TAG and C-TAG TPIDs [801.2Q].
- **FWTTC1** register sets the R-TAG TPID [801.2CB].
- **FWTTC0** and **FWTTC1** register reset values are as per defined in IEEE standards [801.2Q] [801.2CB].

5.1.4 R-switch frame input priority

Any incoming frame will have an input priority given by forwarding engine depending on switch mode **FWGC.SVM**, and the incoming priority settings in **FWPBFC0i** register and the frame format. Fig 5.1 describes frame input priority assignment for a frame coming from port i (the ToS DSCP field decoding is fixed in hardware and described in Table 5-2).

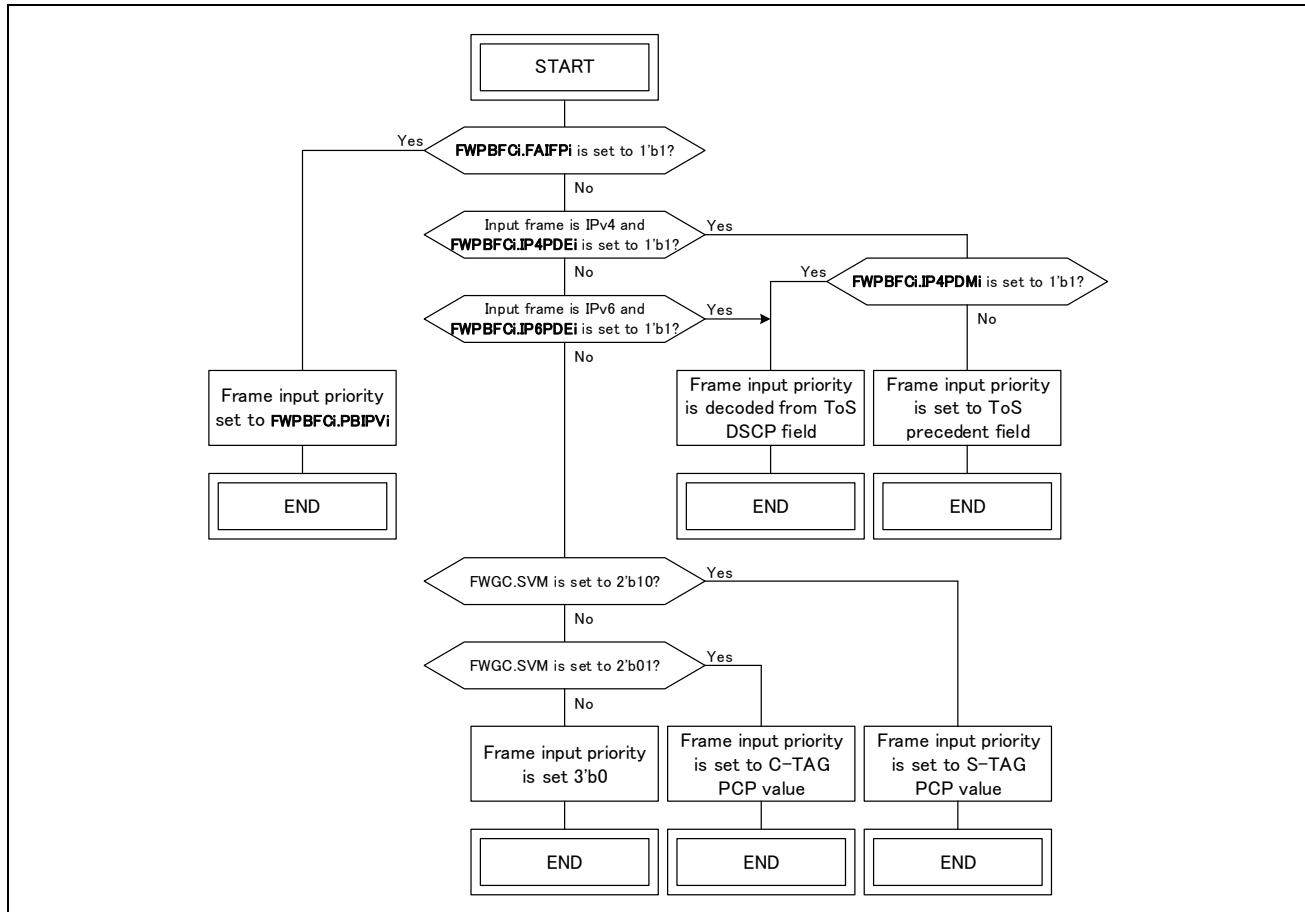


Fig 5.1: Frame input priority assignment for port i

Restrictions:

- HW: For cut-through forwarding, ToS and DSCP are not considered as frame input priority. frame input priority is always extracted from S-TAG, S-TAG or set to 0.

Table 5-2: DSCP to priority mapping

DSCP values in decimal	Frame input priority
56	7
48	6
40, 46	5
32, 34, 36, 38	4
24, 26, 28, 30	3
16, 18, 20, 22	2
8, 10, 12, 14	1
Others	0

5.1.5 R-switch debug functions

5.1.5.1 CPU Exceptional path

Exceptional path is used to forward faulty frames to CPU for diagnosis using **FWCEPTC** and **FWCEPRC0/1/2** registers. When a frame is selected by exceptional path an exceptional descriptor is emitted.

Functions:

- **FWCEPTC** register sets the target to which type of faulty frames will be forwarded. The target is common for multiple errors.
- **FWCEPRC0/1/2** registers set which error frame will be forwarded to the exceptional path. If any one condition is satisfied, this error frame will be forwarded to the exception path.

Note:

- For exceptional path descriptor formats and associated error details refer to section 5.2.3.2 (Integrity exceptional descriptor), 5.2.4.3 (Direct exceptional descriptor), 5.2.5.5(4) (Layer 3 exceptional descriptor), 5.2.6.4(4) (Layer 2 exceptional descriptor), 5.2.7.3 (port based exceptional descriptor) and 5.2.5.5(5) (Filter exceptional descriptor)

5.1.5.2 CPU learning path

Learning path is used to forward frames containing an unknown field to CPU for learning using **FWCLPTC** and **FWCLPRC** registers for the CPU to learn it. Learning can also be done by hardware using **FWPC0i** register and can be monitored using **FWEIS0i** interrupt register. Table 5-3 sums-up the field that can be learned in software (corresponding frames will be forwarded to learning path) and Table 5-4. Any frame sent to learning path will be sent using learning descriptor described in section 5.1.5.2(1).

"CPU learning path" will be occurred regardless of the priority (RP) of forwarding (whatever is selected in Forwarding). "CPU learning path" is an independent (separate from forwarding) path. Therefore, it will always be executed if the condition is satisfied.

Restrictions:

- HW: Any frame rejected by Watermark is not analyzed for learning. As a result, learning path is deactivated and hardware learning does not happen.

Functions:

- **FWCLPTC** register sets the target to which unknown frames will be forwarded.
- **FWCLPRC** registers set which field should be unknown for a frame to be forwarded to the learning path.
- **FWPC0i** registers sets for which fields hardware learning should happen.
- **FWEIS0i** interrupt register notifies that a field couldn't be learnt in hardware.

Table 5-3: Software learning summary table

Field to learn	Learning type	Learning detection conditions for a frame coming from port i	Learning enable bit in FWCLPRC register	Hardware learning possible
Stream ID	Learning	FWLTHTIM.LTHTR and FWPC0i.LTHTAi is set At least a stream ID is valid Stream ID is not set in layer 3 table	USIDL	No
Destination MAC	Learning	FWMACTIM.MACTR and FWPC0i.MACDSAi is set Destination MAC is not set in MAC table	UDMACLF	No
Source MAC	Learning	FWMACTIM.MACTR and FWPC0i.MACSSAi is set Source MAC is a unicast address Source MAC is not set in MAC table	USMACLF	Yes Refer to Table 5-4
Source MAC port	Migration	FWMACTIM.MACTR and FWPC0i.MACSSAi are set Source MAC is a unicast address Source MAC is set in MAC table MAC.DV[i] is not set	UPSMACLF	Yes Refer to Table 5-4
VLAN	Learning	FWVLANTIM.VLANTR and FWPC0i.VLANSAi is set VLAN is valid VLAN ID is not set in VLAN table	UVLANLF	No

Table 5-4: Hardware learning summary table

Field to learn	Learning type	Hardware learning enable bit in FWPC0i register for port i	Hardware learning fail interrupt in FWEIS0i register for port i	Hardware learning condition	Hardware learning disable condition (For certain frames HW learning can be disabled)
Source MAC	Learning	MACHLAi	SMHLFSi	Same as SW learning refer to Table 5-3	FWPC0i.MACDSAi is set Destination MAC is set in MAC table MAC.HLD is set Or FWPC0i.VLANSAi is set VLAN is valid VLAN ID is set in VLAN table VLAN.HLD is set Or FDESCR.HLD (Applied forwarding rule with HLD) is set. (Example FWPBFC1i.PBHLDi) Or Any errors with FWMACHWLC0.MACTHWLFC3-0 .
Source MAC port	Migration	MACHMAi	SMHMFSi	Same as SW learning refer to Table 5-3	FWPC0i.MACDSAi is set Destination MAC is set in MAC table MAC.HLD is set Or FWPC0i.VLANSAi is set VLAN is valid VLAN ID is set in VLAN table VLAN.HLD is set Or FDESCR.HLD (Applied forwarding rule with HLD) is set. (Example FWPBFC1i.PBHLDi) Or Any errors with FWMACHWLC0.MACTHWLFC3-0 .

Notes:

- A multicast MAC address is an address with bit 40 set to 1.

(1) Learning descriptor

Learning descriptor fields are described in Table 5-5.

Table 5-5: Learning descriptor fields

Field name FDESCR.	Values
DV	Learning descriptors are forwarded to GWCA number FWCLPTC.LPCS (port number PORT_TIME_N+FWCLPTC.LPCS)
SEC	FWCLPTC.LPSL
CSDj	FWCLPTC.LPCSD
IPV	FWCLPTC.LPIPV
MINFO	Refer to Fig 5.2 and Table 5-6
RV	1'b0
RN	ALL0
SEQN	Set to corresponding normal descriptor sequence number

Byte	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	RSV						FWDC[3:0]	
1	VL	SMPL	SML	DML	RSV			SIDL
2	RSV			SMHMF	SMHLF	SMHM	SMHL	

Fig 5.2: Learning descriptor MINFO format

Table 5-6: Learning descriptor MINFO field explanation

Field name FDESCR.	Bit width	Field explanation	Values
FWDC	4	ForWarDing Code Present in all descriptors, allows to identify the type of forwarding	Fixed to 13 for Learning descriptors
SIDL	1	Stream ID Learn	Refer to section 5.1.5.2
DML	1	Destination MAC Learn	Refer to section 5.1.5.2
SML	1	Source MAC Learn	Refer to section 5.1.5.2
SMPL	1	Source MAC Port Learn (migration)	Refer to section 5.1.5.2
VL	1	VLAN Learn	Refer to section 5.1.5.2
SMHL	1	Source MAC Hardware Learn *	Refer to section 5.1.5.2
SMHM	1	Source MAC Hardware Migration *	Refer to section 5.1.5.2
SMHLF	1	Source MAC Hardware Learn Fail *	Refer to section 5.1.5.2
SMHMF	1	Source MAC Hardware Migration Fail *	Refer to section 5.1.5.2

[notes]

* : "Hardware Learn/Migration" will set regardless of "Hardware Learn/Migration Fail". (If "Hardware Learn Fail" is set, "Hardware Learn" is always set.)

5.1.5.3 Mirroring paths

Forwarding engine contains 3 mirroring paths:

- CPU mirroring path
- Ethernet mirroring path
- Source-destination mirroring path

(1) CPU mirroring path

CPU Mirroring path is used to copy frames to a CPU for monitoring purpose using **FWCMPTC** and **FWCMPL23URC** register. Table 5-7 describes CPU mirroring selection conditions depending on the forwarding mechanism selected by forwarding flow. When a frame is selected for CPU mirroring, a mirroring descriptor is emitted (5.1.5.3(5)).

Functions:

- **FWCMPTC** and **FWCMPL23URC** register sets the target to which mirrored frames will be forwarded and layer2/layer3 update.

Table 5-7: CPU mirroring selection conditions

Descriptor selected by forwarding flow	Mirroring selection conditions
Cut-through normal descriptor (Fig 5.10)	Cut-through rule corresponding FWCTTC1i.CTCMEi is set.
Layer 3 normal descriptor (Fig 5.42, Fig 5.43)	L3.CME is set for stream ID
Layer 2 normal descriptor (Fig 5.51, Fig 5.52)	if { MAC.CME is set for destination MAC or VLAN.CME is set} when MAC destination address and VLAN ID are both found and MAC.SL = VLAN.SL . if MAC.CME is set for destination MAC when MAC destination only is found or if MAC destination address and VLAN ID are both found and MAC.SL & !VLAN.SL . if VLAN.CME is set when VLAN ID only is found or if MAC destination address and VLAN ID are both found and !MAC.SL & VLAN.SL ,
Port based normal descriptor (Fig 5.55, Fig 5.56)	If FWPBFC0i.PBCMEi is set for incoming frame source port.

(2) Ethernet mirroring path

Ethernet Mirroring path is used to copy frames to an ethernet agent for monitoring purpose using **FWEMPTC** and **FWEMPL23URC** register. Table 5-8 describes Ethernet mirroring selection conditions depending on the forwarding mechanism selected by forwarding flow. When a frame is selected for Ethernet mirroring, a mirroring descriptor is emitted (5.1.5.3(5)).

Functions:

- **FWEMPTC** and **FWEMPL23URC** register sets the target to which mirrored frames will be forwarded and layer2/layer3 update.

Table 5-8: Ethernet mirroring selection conditions

Descriptor selected by forwarding flow	Mirroring selection conditions
Cut-through normal descriptor (Fig 5.10)	Cut-through rule corresponding FWCTTC1i.CTEMEi is set.
Layer 3 normal descriptor (Fig 5.42, Fig 5.43)	L3.EME is set for stream ID
Layer 2 normal descriptor (Fig 5.51, Fig 5.52)	if { MAC.EME is set for destination MAC or VLAN.EME is set} when MAC destination address and VLAN ID are both found and MAC.SL = VLAN.SL . if MAC.EME is set for destination MAC when MAC destination only is found or if MAC destination address and VLAN ID are both found and MAC.SL & !VLAN.SL . if VLAN.EME is set when VLAN ID only is found or if MAC destination address and VLAN ID are both found and !MAC.SL & VLAN.SL ,
Port based normal descriptor (Fig 5.55, Fig 5.56)	If FWPBFC0i.PBEMEI is set for incoming frame source port.

(3) Source-destination Mirroring path

Source-destination mirroring path targets **the destination port and source port**. “Source-destination Mirroring” frames are affected by filtering (Example Acceptance list filtering, some error filtering and Source port filtering). In other words, even if the original frame is rejected by filter, the mirror frame will be rejected.

Mirroring path is used to copy frames to an Ethernet port or a CPU for monitoring purpose using **FWSDMPTC** and **FWSDMPVC** register. When a frame is selected for Source-destination mirroring, a mirroring descriptor is emitted (5.1.5.3(5)).

Functions:

- **FWSDMPTC** register sets the target to which mirrored frames will be forwarded.
- **FWSDMPL23URC** register sets the Layer2/Layer3 update functions for mirroring frames.
- **FWSDMPVC** register sets the source from which should come and the destination where should go a frame to be mirrored.
- A frame is selected for source-destination mirroring if the descriptor selected by forwarding flow is {Layer 3 normal descriptor (Fig 5.42, Fig 5.43) or Layer 2 normal descriptor (Fig 5.51, Fig 5.52) or Port based normal descriptor (Fig 5.55, Fig 5.56)}, if the frame source port is set in **FWSDMPVC.SDMSV** register and if **FDESCR.DV** & **FWSDMPVC.SDMDV** is not null.

(4) Source Mirroring path

Source mirroring path targets **only the source port**. “Source Mirroring” frames are **not** affected by filtering (Excluding ATS). In other words, even if the original frame is rejected by filter, the mirror frame will **not** be rejected. Therefore, there is no destination port setting.

Mirroring path is used to copy frames to an Ethernet port or a CPU for monitoring purpose using **FWSMPTC** and **FWSMPVC** register. When a frame is selected for Source mirroring, a mirroring descriptor is emitted (5.1.5.3(5)).

Functions:

- **FWSMPTC** register sets the target to which mirrored frames will be forwarded.
- **FWSMPL23URC** register sets the Layer2/Layer3 update functions for mirroring frames.
- **FWSMPVC.SMSV** register sets the source from which should come a frame to be mirrored.
- A frame is selected for source mirroring if the descriptor selected by forwarding flow is {Layer 3 normal descriptor (Fig 5.42, Fig 5.43) or Layer 2 normal descriptor (Fig 5.51, Fig 5.52) or Port based normal descriptor (Fig 5.55, Fig 5.56)}, if the frame source port is set in **FWSMPVC.SMSV** register is not null.

Restrictions:

- This function cannot use with Cut-through forwarding.

(5) Mirroring descriptor

Mirroring descriptor fields are described in Table 5-9.

Table 5-9: Mirroring descriptor fields

Field name FDESCR.	Values for CPU mirroring	Values for Ethernet mirroring	Values for Source-destination mirroring	Values for Source mirroring
DV	Mirroring descriptors are forwarded to GWCA number FWMPTC.CMPCS (port number PORT_TIME_N+ FWMPTC.CMPCS)	Mirroring descriptors are forwarded to TSNA number FWEMPTC.EMPPS (port number FWEMPTC.EMPPS)	Mirroring descriptors are forwarded to port number FWSDMPTC.SDMPPS	Mirroring descriptors are forwarded to port number FWSMPTC.SMPPS
SEC	FWMPTC.CMPSL	FWEMPTC.EMPSL	FWSDMPTC.SDMPSL	FWSMPTC.SMPSL
CSDj	FWMPTC.CMPCSD	All0	FWSDMPTC.SDMPCSD	FWSMPTC.SMPCSD
IPV	If FWMPTC.CMPIPU is set, FWMPTC.CMPIPV If FWMPTC.CMPIPU is not set, same IPV as normal descriptor	If FWEMPTC.EMPIPU is set, FWEMPTC.EMPIPV If FWEMPTC.EMPIPU is not set, same IPV as normal descriptor	If FWSDMPTC.SDMPIPU is set, FWSDMPTC.SDMPIPV If FWSDMPTC.SDMPIPU is not set, same IPV as normal descriptor	If FWSMPTC.SMPIPU is set, FWSMPTC.SMPIPV If FWSMPTC.SMPIPU is not set, same IPV as normal descriptor. If "FWSMPTC.SMPIPU" is not set and "Either error descriptor", PCP value in the frame. "Either error descriptor" means "Unknown Filtering" or "Source Source Source Port Filtering". In the case of other filtering, since the table is hit, the IPV is determined by the table information (same control as normal descriptor). Also, if multiple errors overlap, "Either error descriptor" takes precedence.
MINFO	Refer to Fig 5.3 and Table 5-10	Refer to Fig 5.3 and Table 5-10	Refer to Fig 5.3 and Table 5-10	Refer to Fig 5.3 and Table 5-10
RV	If FWMPL23URC.CMRV == 2'b00, same as original frame. If FWMPL23URC.CMRV == 2'b01, 1'b0. If FWMPL23URC.CMRV == 2'b10, 1'b1.	If FWEMPL23URC.EMRV == 2'b00, same as original frame. If FWEMPL23URC.EMRV == 2'b01, 1'b0. If FWEMPL23URC.EMRV == 2'b10, 1'b1.	If FWSDMPL23URC.SDMRV == 2'b00, same as original frame. If FWSDMPL23URC.SDMRV == 2'b01, 1'b0. If FWSDMPL23URC.SDMRV == 2'b10, 1'b1.	If FWSMPL23URC.SMRV == 2'b00, same as original frame. If FWSMPL23URC.SMRV == 2'b01, 1'b0. If FWSMPL23URC.SMRV == 2'b10, 1'b1.
RN	If FWMPL23URC.CMRV == 2'b00, same as original frame. If FWMPL23URC.CMRV == 2'b01, All 0. If FWMPL23URC.CMRV == 2'b10, FWMPL23URC.CMRN .	If FWEMPL23URC.EMRV == 2'b00, same as original frame. If FWEMPL23URC.EMRV == 2'b01, All 0. If FWEMPL23URC.EMRV == 2'b10, FWEMPL23URC.EMRN .	If FWSDMPL23URC.SDMRV == 2'b00, same as original frame. If FWSDMPL23URC.SDMRV == 2'b01, All 0. If FWSDMPL23URC.SDMRV == 2'b10, FWSDMPL23URC.SDMRN .	If FWSMPL23URC.SMRV == 2'b00, same as original frame. If FWSMPL23URC.SMRV == 2'b01, All 0. If FWSMPL23URC.SMRV == 2'b10, FWSMPL23URC.SMRN .
SEQN	Set to corresponding normal descriptor sequence number	Set to corresponding normal descriptor sequence number	Set to corresponding normal descriptor sequence number	Set to corresponding normal descriptor sequence number

Byte	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0				
0	RSV				FWDC[3:0]							
1	NDFB[7:0]											
2	RSV											

Fig 5.3: Mirroring descriptor MINFO format

Table 5-10: Mirroring descriptor MINFO field explanation

Field name FDESCR.	Bit width	Field explanation	Values
FWDC	4	ForWarding Code Present in all descriptors, allows to identify the type of forwarding	Fixed to 14 for Mirroring descriptors
NDFB	8	Normal Descriptor First Byte	Set to mirrored frame corresponding normal descriptor FDESCR.MINFO[7:0] value If Source mirroring, undefined (don't care) will be stored here.

5.1.6 Watermark

R-switch watermark defines the switch behavior in case of overflow using **FWLBWMCi** and **FWCEPRC2** registers and can be monitored using **FWEIS0i** interrupt register.

R-Switch have two type of watermark functions “IPV Based Watermark” and “Level Based Watermark”.

Functions:

- **FWIBWMC** is used to change frame discard operation for “IPV based watermark [COMA]”.
- **FWLBWMCi** is used to set which frame should be discarded by “Global/Per-Port level-based watermark [COMA]”.
- **FWCEPRC2** register enables exceptional path for error descriptors.
- **FWEIS0i** interrupt register notifies that a frame coming from port i has been rejected because of watermark.
- Watermark uses has frame priority the IPV value given by forwarding mechanism before filtering (PSFP gate filtering update is not taken in account). This correspond to the **FDESCR.IPV** in the normal descriptor emitted by the selected forwarding.
- Watermark uses as DEI value the value extracted from the input frame which is the S-TAG DEI value when **FWGC.SVM** is set to 2'b10, the C-TAG DEI value when **FWGC.SVM** is set to 2'b01, and 1'b0 when **FWGC.SVM** is set to 2'b00.

Cautions:

- SW: The watermark is an indispensable functionality for switch QoS behavior definition, it is not advised to disable it.

Notes:

- Error frames are not going through watermark.

(1) Watermark errors

Table 5-11 describes the Watermark errors. Instead of being discarded by forwarding engine, an error frame can be forwarded to exceptional path using Watermark exceptional descriptor described in section 5.1.6(2) by setting corresponding error exceptional bit. For error set conditions, refer to corresponding error interrupt register explanations.

Table 5-11: Watermark Errors

Error	Error name	Error interrupt	Error exceptional bit
WMCF	WaterMark Critical Filtering	FWEIS0i.WMCFSi	FWCEPRC2.FWMFEF
WMFF	WaterMark Flush Filtering	FWEIS0i.WMFFSi	FWCEPRC2.FWMFEF
WMISF	WaterMark IPV Secure Filtering	FWEIS0i.WMISFSi	FWCEPRC2.FWMFEF
WMIUF	WaterMark IPV Unsecure Filtering	FWEIS0i.WMIUFSi	FWCEPRC2.FWMFEF

(2) Watermark exceptional descriptor

Watermark exceptional descriptor fields are described in Table 5-12.

Table 5-12: Watermark exceptional descriptor fields

Field name FDESCR.	Values
DV	Exceptional descriptors are forwarded to GWCA number FWCEPTC.EPCS (port number PORT_TIME_N+FWCEPTC.EPCS)
SEC	FWCEPTC.EPSL
CSDj	FWCEPTC.EPCSD
IPV	FWCEPTC.EPIPV
MINFO	Refer to Fig 5.4 and Table 5-13
RV	1'b0
RN	ALL0
SEQN	Set to frame input sequence number

Byte	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	RSV					FWDC[3:0]		
1	RSV			WMIUF	WMISF	WMFF	WMCF	
2	RSV							

Fig 5.4: Watermark exceptional descriptor MINFO format

Table 5-13: Watermark exceptional descriptor MINFO field explanation

Field name FDESCR.	Bit width	Field explanation	Values
FWDC	4	ForWarDing Code Present in all descriptors, allows to identify the type of forwarding	Fixed to 4 for Watermark exceptional descriptors
WMCF	1	WaterMark Critical Filtering	Refer to section 5.1.6(1)
WMFF	1	WaterMark Flush Filtering	Refer to section 5.1.6(1)
WMISF	1	WaterMark IPV Secure Filtering	Refer to section 5.1.6(1)
WMIUF	1	WaterMark IPV Unsecure Filtering	Refer to section 5.1.6(1)

5.1.7 Self-recovery

ECC processing (1bit correction, 2bit notification) is possible for TCAM/CAM during Read operation. However, TCAM/CAM cannot process ECC during Search operation. Therefore, it is necessary to recover the state of TCAM/CAM periodically.

5.1.7.1 L3/L2 stream table recovery

L3/L2 stream table recovery function is used to recovery the correctable (ECC 1bit errored) entries and remove the uncorrectable (ECC 2bit errored) entries using **FWLTHREUSPC** and **FWLTHREC** registers. This result can be monitored using **FWLTHREM** registers and **FWMIS0.LTHEDRS** interrupt register. L3/L2 stream table recovery function thanks to follow algorithms for all entries.

Functions:

- **FWLTHREUSPC** register sets a prescaler to create a 1Hz for recovery.
- **FWLTHREC** register sets/enables the recovery function
- **FWMIS0.LTHEDRS** and **FWLTHREM** can be used to keep track in SW of the recovered L3/L2 stream entry addresses. These registers should be used only in polling mode (**FWLTHREC.LTHREPM** set).
- **FWLTHTEM1** will be updated after 3 clk cycle of setting **FWLTHREUSPC.LTHREUSP**.
- In polling mode if **FWMIS0.LTHEDRS** bit is not cleared, further L3/L2 stream entry delete by self-recovery will not happen until it is cleared.

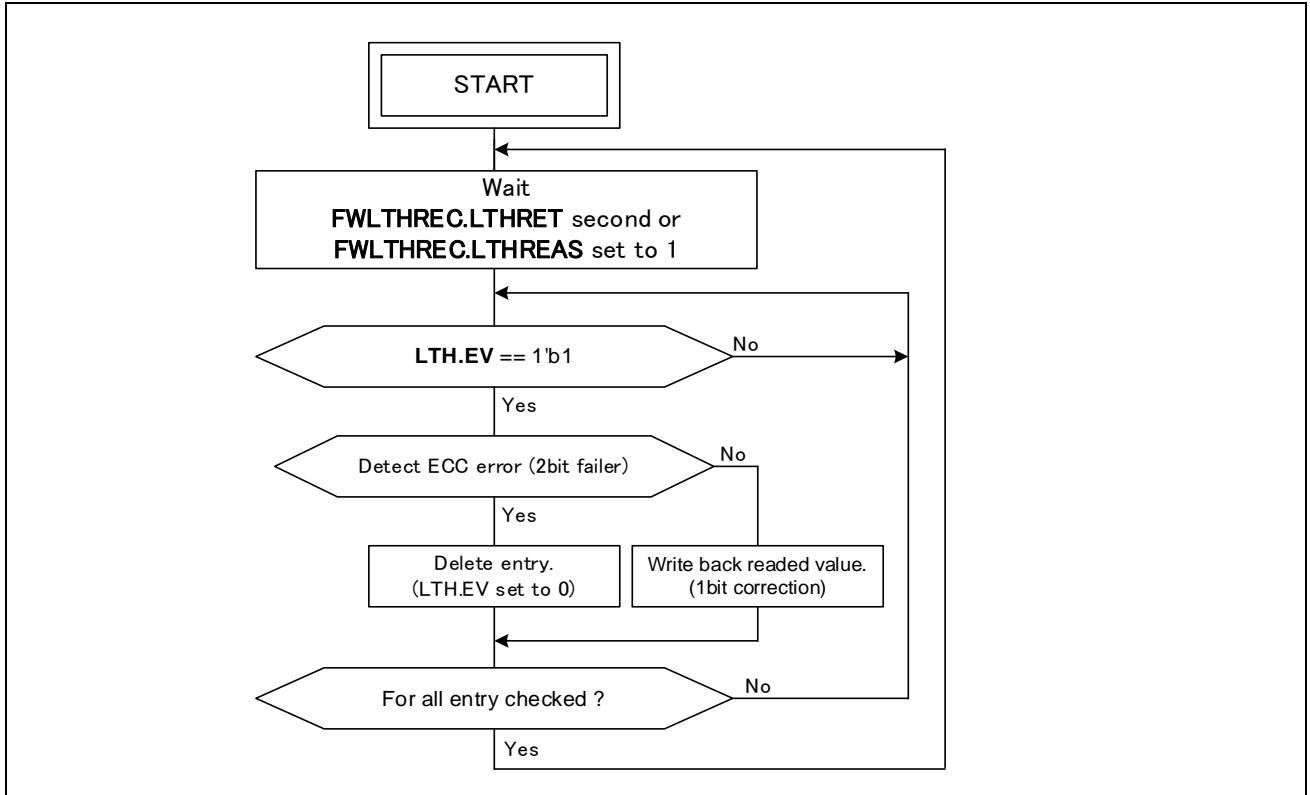


Fig 5.5: L3/L2 stream table recovery algorithm

5.1.7.2 MAC table recovery

MAC table recovery function is used to recover the correctable (ECC 1bit errored) entries and remove the uncorrectable (ECC 2bit errored) entries using **FWMACREUSPC** and **FWMACREC** registers. This result can be monitored using **FWMACREM** registers and **FWMIS0.MACEDRS** interrupt register. MAC table recovery function thanks to follow algorithms for all entries.

“Aging” has priority than “Self-recovery”, and “Self-recovery” pauses while “Aging” is running.

Functions:

- **FWMACREUSPC** register sets a prescaler to create a 1Hz for recovery.
- **FWMACREC** register sets/enables the recovery function
- **FWMIS0.MACEDRS** and **FWMACREM** can be used to keep track in SW of the recovered MAC entry addresses. These registers should be used only in polling mode (**FWMACREC.MACREPM** set).
- **FWMACTEM** and **MACDEN** will be updated after 3 clk cycle of setting **FWLTHREUSPC.LTHREUSP**.
- In polling mode if **FWMIS0.MACEDRS** bit is not cleared, further MAC entry delete by self-recovery will not happen until it is cleared.
-

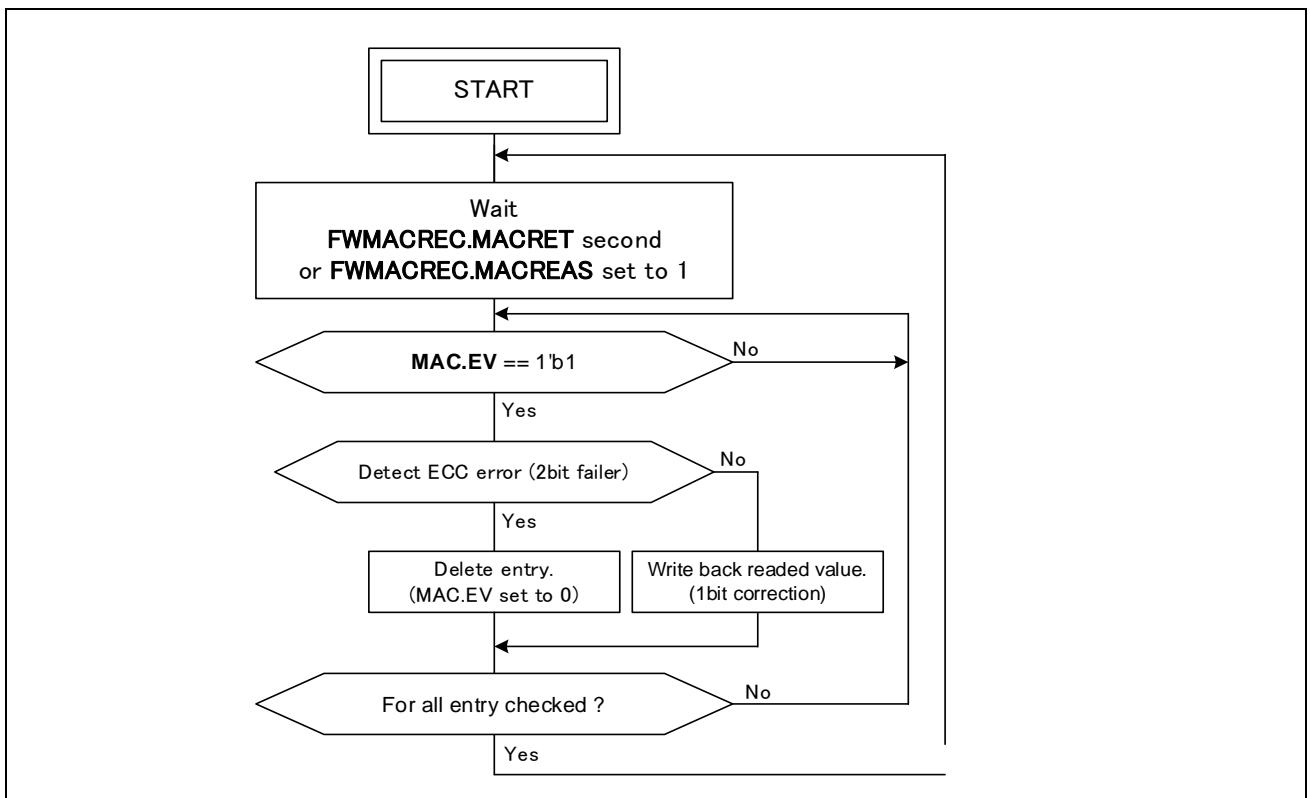


Fig 5.6: MAC table recovery algorithm

5.2 Forwarding/Routing

Forwarding engine contains different types of filtering/routing/filtering which are:

- Cut-through forwarding
- Integrity check filtering
- Direct descriptor forwarding
- Layer 3 forwarding/routing/filtering
- Layer 2 forwarding/routing/filtering
- Port based forwarding
- Layer2/Layer3 Update

5.2.1 General detail for forwarding arbitration

Forwarding arbitration block received forwarding information from cut-through forwarding block, integrity check block, direct descriptor forwarding block, L3 forwarding block, L2 forwarding block and port based forwarding block. Forwarding arbitration block arbitrate with each forwarding information and select one forwarding information confirmed by equipped forwarding priority decision rule. Detailed arbitration block diagram is shown in follow.

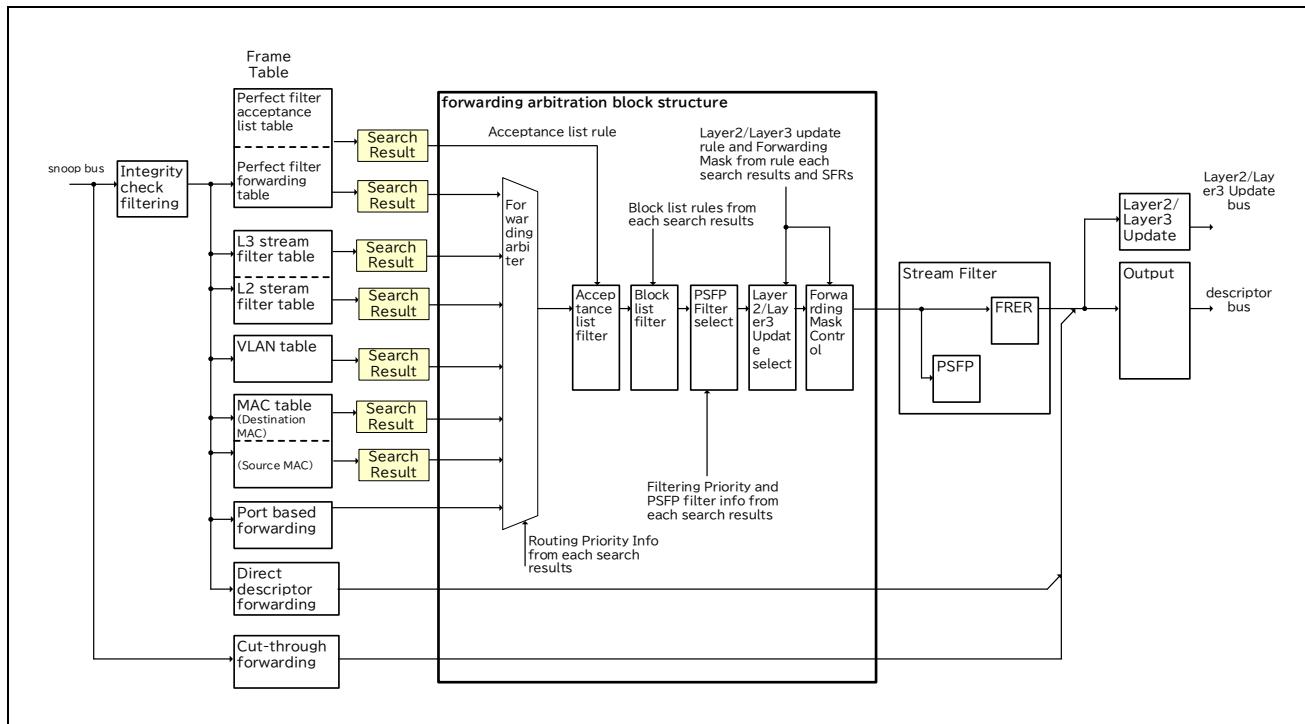


Fig 5.7: Forwarding arbitration block diagram

(1) Forwarding arbiter

Cut-through is highest forwarding priority, therefor Cut-through will ignore all even integrity check. integrity check is second priority, therefor it filters all but Cut-through. Direct descriptor is third priority but ignore forwarding arbitration.

When Cut-through, integrity check and direct forwarding are not existed, L3 forwarding, L2 forwarding and port-based forwarding got forwarding priority. The order of forwarding arbitration priority is Secure Perfect(Cascade) filter, Secure L3 stream, Secure L2 stream, Secure L2 DMAC&VLAN, Secure L2 DMAC, Secure L2 VLAN, Secure port-based forwarding, Unsecure Perfect(Cascade) filter, Unsecure L3 stream, Unsecure L2 stream, Unsecure L2 DMAC&VLAN, Unsecure L2 DMAC, Unsecure L2 VLAN and Unsecure port-based forwarding. This is hardware-pre-implemented forwarding priority order.

Although arbitration between each forwarding inputs are controlled by above hardware-pre-implemented method, except of Cut-through, integrity check and direct forwarding, forwarding priority is adjustable by **routing priority (RP)** value which each forwarding information have. Except of Cut-through, integrity check and direct forwarding, each forwarding inputs have routing priority value. Forwarding arbiter select one input forwarding information with highest **routing priority (RP)** value. If there are multiple input forwarding information with same highest priority value, above hardware-pre-implemented order is used.

(2) Acceptance list control

After forwarding arbitration, one input forwarding information is selected.

Perfect filter Stream ID (on L3 table) outputs two kind of forwarding information: normal information and acceptance list control dedicated information. The former is used to forwarding control described above and the latter is used to control acceptance list control.

When **acceptance list (FDESCR.AL)** dedicated information is available and the bit of Source Lock Vector which associated by source port number is set, forwarding arbitration result (select one forwarding information) is accepted (not blocked) and forwarded to next block. But secure forwarding descriptors (**FDESCR**) will not be accepted/overwritten by unsecure acceptance list descriptor (**L3(Acceptance)**).

This inbound feature can be enabled by **FWPC1i.PFALE[0]i** from Source Port i. Irrespective of the type of forwarding, if **FWPC1i.PFALE[0]i** is set the frame will be rejected if it does not find a match in perfect filter rule with (**L3.AL = 1** and **L3.SLV[Source port number] = 1**). But "Cut-through forwarding" and "Direct descriptor forwarding" will bypass Acceptance list filtering.

This outbound feature can be enabled by **FWPC1i.PFALE[1]i** from Source Port i. Irrespective of the type of forwarding, if **FWPC1i.PFALE[1]i** is set the frame will be rejected if it does not find a match in perfect filter rule with (**L3(Acceptance).AL = 1** and **L3(Acceptance).DLV[Destination port number] = 1**). But "Cut-through forwarding" and "Direct descriptor forwarding" will bypass Acceptance list filtering.

For example, "**L3(Acceptance).DLV[Destination port number]**" (parameter PORT_N = 4)

Case1. FDESCR.DV = 4'b0001 and L3.DLV = 4'b0001, this frame will be forwarded.

Case2. FDESCR.DV = 4'b0001 and L3.DLV = 4'b0000, this frame will be rejected by acceptance list filtering.

Case3. FDESCR.DV = 4'b0011 and L3.DLV = 4'b0011, this frame will be forwarded.

Case4. FDESCR.DV = 4'b0011 and L3.DLV = 4'b0000, this frame will be rejected by acceptance list filtering.

Case5. FDESCR.DV = 4'b0011 and L3.DLV = 4'b0001, this frame will be forwarded only Port0.

In this case of Case2 and Case4, "No target filtering" is also satisfied in addition to the conditions of "Block list filtering". (Because all of destination are restricted)

Other rules **L3(Acceptance).***** are used to overwrite selected forwarding descriptor (**FDESCR.*****) "Overwrite function". This overwrite function will be valid by enabled source port on **L3(Acceptance).SLV[Source port number] == 1'b1**. This overwrite function is also effective for those without base rules (Example, **DMAC.RV**, **PB.MSDUV**, etc).

(3) Block list control

Each L3 and L2 forwarding information are included **block list (FDESCR.BL/SBL/DBL)** control value. If **block list (FDESCR.BL/SBL/DBL)** control value is set and the bit of Source Lock Vector which associated by source port number is set, block list control function is available.

If any block list control function is available, forwarding arbitration result is dropped (a descriptor has been rejected). But secure forwarding descriptors (**FDESCR**) will not be rejected by unsecure block list descriptor.

This feature can be enabled by **FWPC1i.BLEi** from source Port i. Irrespective of the type of forwarding (Port Based forwarding, Layer 2 forwarding, Layer 3 forwarding), if **FWPC1i.BLEi** is set the frame will be filtered if it does not find a match in any filter rule with **BL = 1**. But "Cut-through forwarding" and "Direct descriptor forwarding" will bypass Block list filtering. If **FWPC1i.BLEi** is set to 1'b1 (block list is enabled) and **DESCR.BL/SBL/DBL = 1** (block list entry), then only **DESCR.SLV[i]** and **DESCR.SL** are valid for Block list Filter and other fields such as (**DESCR.RP**, **DESCR.DV**, ...etc.) are invalid.

Since this function is located after "Forwarding Arbiter" and "Acceptance list control". The frames forwarded in "Forwarding Arbiter" and the frames allowed in "Acceptance list control" can be also discarded. Irrespective of the block lists used by the block list filtering, only the selected forwarding/routing type (by "Forwarding Arbiter") blocklist filtering counter will be incremented.

(4) PSFP filtering info selection

Each forwarding information include PSFP filtering indications (PSFP MSDU, PSFP METER, PSFP GATE), and **filtering priority (FDESCR.FP)** value. Like as **routing priority (FDESCR.RP)** in forwarding arbitration, PSFP filtering indications are selected by forwarding information which have highest **filtering priority (FDESCR.FP)** value. If there are multiple forwarding information have same highest **filtering priority (FDESCR.FP)** value, PSFP filtering indication information are selected following order : Secure per Source PORT and IPV* (**FWPIFPIij** register), Secure L2 VLAN, Secure L2 SMAC, Secure L2 DMAC, Secure L2 stream, Secure L3 stream, Secure Perfect(Cascade) filter, Unsecure per Source PORT and IPV* (**FWPIFPIij** register), Unsecure L2 VLAN, Unsecure L2 SMAC, Unsecure L2 DMAC, Unsecure L2 stream, Unsecure L3 stream, Unsecure Perfect(Cascade) filter.

If set to **FWGC.FPM** = 1'b1, PSFP filtering info is selected by **routing priority (FDESCR.RP)** with **filtering priority (FDESCR.FP)** selection disabled. * : IPV means... PCP value in the frame (Example : PCP value with **MAC.IPU == 0**) or IPV value (Example : **MAC.IPV** value with **MAC.IPU == 1**).

(5) L23U info selection

Layer 3 and Layer2-VLAN forwarding information include L23 update rule indication. If forwarding arbitration select L3 forwarding information and selected forwarding information does not have included L23 update indication, L23 update indication is replaced to L23 update information in VLAN forwarding information. This replacing feature can be enabled by **FWPC3i.L23UOEi**.

(6) Forwarding Mask Control

When acceptance list control is passed and block list control is not applied, arbitrated forwarding information is forwarded to PSFP / FRER filtering block. This forwarding operation can be masked by register setting (L3: **FWPC1i.LTHFMi**, L2: **FWPC2i.LTWFMi**) or forwarding information (**VLAN**).

Additionally, when arbitration operation selects L3 forwarding information, forwarding mask operation can be disabled depending on validity of L23 update information. This feature can be enabled by **FWPC3i.LTHFMDi**.

5.2.2 Cut-through forwarding

Cut-through forwarding is used to forward high priority frames without storing them in the local memory to suppress the frame reception time impact on the latency. Under the condition of R-switch insure a best latency (no busy traffic on MFWD and no TAG frame) of

[RSW2.*] 1us*"PHY clock 4 cycle"(ns), 4.6us*"PHY clock 4 cycle"(ns) and 46us*"PHY clock 4 cycle"(ns) at respectively 10/5/2.5/1Gbps, 100Mbps and 10Mbps [TSNA].

[RSW3.*] 189ns, 347ns, 566ns, 893ns, 7.76us and 77.2us at respectively 10G, 5G, 2.5G, 1G, 100M and 10M bps. [TSNA].

Restriction: [RSW3.*] When using Cut-through with PHY 10Gbps, the clock frequency must be 600MHz or higher. This is caused by not being able to read from 512bit Fabric in time, regardless of the number of ports. If this constraint is violated, TSLS of RMAC will be set.

Depending on the setting conditions, the value may be smaller than these.

Generally, "Cut-through" only checks 6 bytes (Destination MAC Address) of a frame head and starts frame forwarding after this check immediately. Since internal data bus width in this switch is wider than 6 bytes, it needs more data bytes to start frame forwarding. Because of this logic, "Cut-through" forwarding time of this switch needs above times.

The Cut-through forwarding block diagram is represented in Fig 5.8.

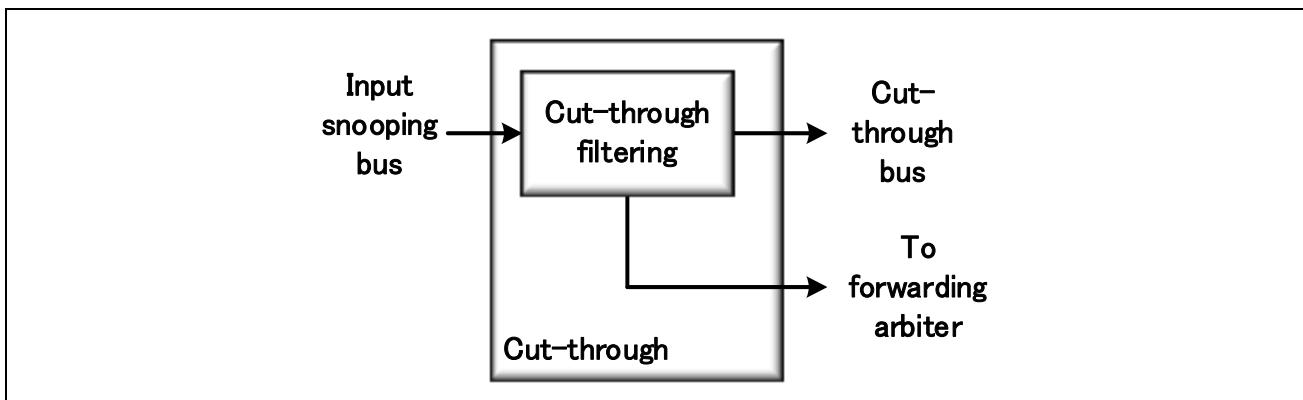


Fig 5.8: Cut-through forwarding block diagram

The Cut-through forwarding function has one functional block:

- Cut-through filtering: This function filters incoming frame first beat of data to select set frames for cut-through forwarding, creates the cut-through bus protocol destined to time agents [TSNA] and send required information to forwarding arbiter to apply store and forward to cut-through frames.

Notes:

- Forwarding arbiter contains the forwarding flow. The forwarding flow is explained per forwarding type. For Cut-through, related Forwarding flow is described in Fig 5.10

Restrictions:

- HW: The usage "From-one-to-one between same PHY speed" is recommended. So in case of forwarding engine back pressure, it can happen that cut-through frames are cut in the middle and lost.
- HW: P-frames cannot be forwarded by cut-through.
- HW: Watermark is not applied on Cut-through frames.

- HW: Cut-through frames can be ingress tagging by **FWGC.SVM** and **[TSNA] EAVCC.VIM** but not affected due to egress tagging **[TSNA] EAVCC.VEM**. But, Cut-through forwarding should not be set for ingress ports in Port-based VLAN mode because cut-through can only forward frame as they were received (**[TSNA] EAVCC.VIM** set to 1'b0). **FWCTGC0i.CTVCTRLi** and **FWCTGC0i.CTRTGli** controls how the frame will be transmitted out from DUT and Frames matching a cut-Through rule number should match the corresponding **FWCTGC0i.CTVCTRLi** and **FWCTGC0i.CTRTGli**.
- HW: Cut-through frames cannot be “Ethernet Agent Ingress/Egress C/S-TAG DEI 0/1 Remapping Configuration”. Please set default values for EAICD0RC, EAICD1RC, EAISD0RC, EAISD1RC, EAEC0RC, EAEC1RC, EAESD0RC and EAESD1RC [TSNA]. Restriction on remapping registers during cut-through transfer affects the transfer of “non-Cut-through transfer”.
- HW: L23 update is not applied on Cut-through frames.
- HW: Data padding applied on Cut-through frames.
- HW: Cut-through frames can be shaped using TAS but not CBS.
- HW: Cut-through frames will be forward in cut-through mode as there are received and will not be updated.
- HW: For cut-through, only mirroring set in **FWCTTC1/2i** register is available. All other debugging and mirroring are disabled.
- HW: Cut-through frames will not be filtered by [RMAC] MAC Address filtering on Reception. Because [TSNA] and [GWCA] reception filter information are ignored.
For example, a frame which is having a nibble alignment error ([TSNA] reception filter information) is ignored by cut through forwarding. And a frame is transmitted out by padding bits of data to complete a byte.
- SW: All the cut-through registers which are not captured under the security level in IP spec will be only accessible by the APB secure interface.

5.2.2.1 Cut-through filtering

Cut-through filtering is used to identify cut-through frames using **FWCTGC0i/1i** and **FWCTSC0/1/2/3/4i** registers. Cut-through filtering and register utilization are summarized in Fig 5.9.

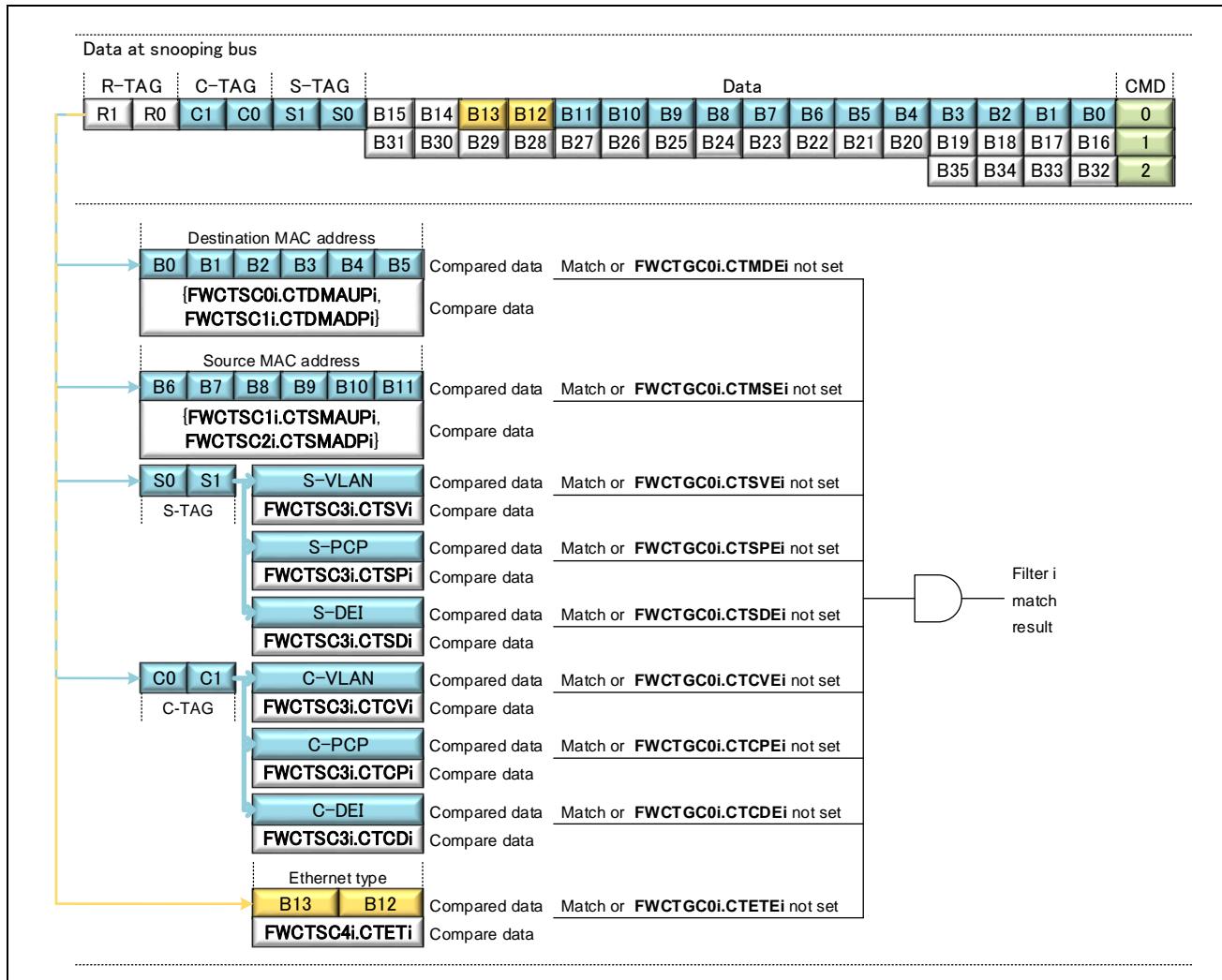


Fig 5.9: Cut-through filtering

Functions:

- A cut-through rule can only match frames from corresponding source port **FWCTSC4i.CTSPNi**.
- If several Cut-through rules match the same frame, the Cut-through rules with the highest number will be selected.
- A cut-through rule is only valid when corresponding **FWCTTC0i.CTDVi** is different than All0.
- A cut-through matching frames is forwarded by cut-through and store and forward independently from any error that could have happened in the ingress agent.
- For register FWCTGC0i bit 0-8 set to 0 (all fields compare match is disabled), Cut through becomes "port based cut through" by FWCTTC0i.CTDVi.

5.2.2.2 Cut-through forwarding

Cut-through forwarding function creates the cut-through bus protocol destined to time agents [TSNA] using **FWCTTC0i**, **FWCTGC0i/1i** registers. It is used to send frames while receiving them to reduce latency through cut-through bus.

Functions:

- **FWCTTC0i** register is to determine the target port for cut-through. All ports set in **FWCTTC0i.CTDVi[PORT_TIME_N-1:0]** and not set in **FWCTTC0i.CTDFMi** are targeted for rule i cut-through forwarding. Any frame received from an agent with an error will still be forwarded/mirrored by cut-through forwarding.
- **FWCTGC1i.CTMTi**, **FWCTGC0i.CTVCTRLi**, and **FWCTGC0i.CTFIi** registers are respectively used as Maximum Time on the PHY, VLAN control and FCS in for the matching cut-through frame.
- **FWCTGC1i.CTMTi**, **FWCTGC0i.CTVCTRLi**, **FWCTGC0i.CTRTGli** and **FWCTGC0i.CTFIi** registers are affected only “Cut through forwarding” but not “Store and forward forwarding” and “Mirroring”.

Restrictions:

- HW: Ethernet timestamping functionalities are not available during cut-through forwarding [TSNA]. E.g. while forwarding frames to RMAC [RMAC], the ethernet agent will fix “Timestamp capture”, “Insert egress timestamp” and “Calculate residence time” TX interface bit to 1'b0.
- HW: For cut-through forwarding, all(From & To) PHY speeds have to be the same[TSNA] [RMAC].
- SW: FWCTGC0i.CTRTGli and FWCTGC0i.CTVCTRLi should always correspond to the ingress frame format. If they do not correspond, errors can happen.

5.2.2.3 Store and forward forwarding

Store and forward forwarding function apply store and forward to cut-through frames using **FWCTTC0/1/2i**. Cut-through forwarding flow for Store and forward forwarding is described in Fig 5.10.

Functions:

- **FWCTTC0i** register is to determine the target port for store and forward. All ports set in **FWCTTC0i.CTDVi[PORT_TIME_N-1:0]** and set in **FWCTTC0i.CTDFMi** are targeted for rule i store and forward forwarding, so are ports set in FWCTTC0i.CTDVi[PORT_N-1:PORT_TIME_N]. Any frame received from an agent with an error will still be forwarded/mirrored in store and forward mode.
- **FWCTTC1/2i** registers sets the forwarding information.

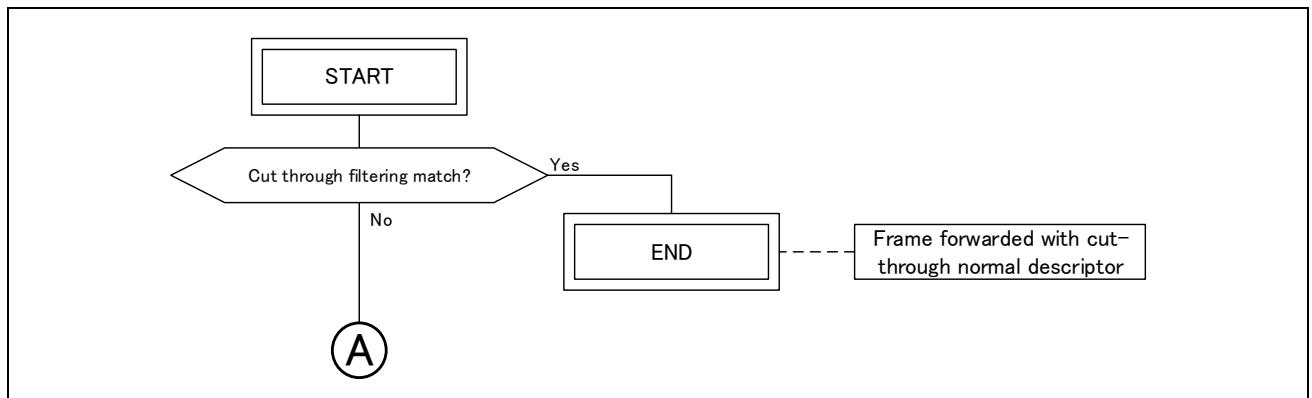


Fig 5.10: Cut-through forwarding flow

Note:

- Link A links to Fig 5.13.

(1) Cut-through normal descriptor

Cut-through normal descriptor fields for a frame matching cut-through rule number i are described in Table 5-14.

Table 5-14: Cut-through normal descriptor fields

Field name FDESCR.	Values
DV	{FWCTTC0i.CTDVi[PORT_N-1:PORT_TIME_N], {FWCTTC0i.CTDVi[PORT_TIME_N-1] & FWCTTC0i.CTDFMi}}
SEC	1'b1
CSDj	FWCTTC2ji.CTCSDji
IPV	if FWCTTC1i.CTIPUi is set, set to FWCTTC1i.CTIPVi if FWCTTC1i.CTIPUi not set and FWGC.SVM is set to 2'b10, set to frame input S-TAG PCP if FWCTTC1i.CTIPUi not set and FWGC.SVM is set to 2'b01, set to frame input C-TAG PCP if FWCTTC1i.CTIPUi not set and FWGC.SVM is set to 2'b00, set to frame input 3'd0
MINFO	Refer to Fig 5.11 and Table 5-15
RV	1'b0
RN	ALL0
SEQN	Set to frame input sequence number

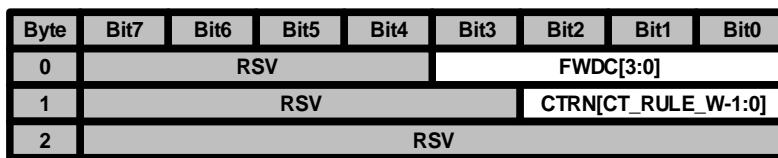


Fig 5.11: Cut-through normal descriptor MINFO format

Table 5-15: Cut-through normal descriptor MINFO field explanation

Field name FDESCR.	Bit width	Field explanation	Values
FWDC	4	ForWarding Code Present in all descriptors, allows to identify the type of forwarding	Fixed to 0 for Cut-through normal descriptors
CTRN	CT_RULE_W	Cut-through rule number	Set to the cut-through rule number which forwarded the frame
RSV	--	Reserved field	Set to 0

5.2.3 Integrity check filtering

Integrity check is used to check if a frame can be forwarded or if it contains an error. The Integrity check block diagram is represented in Fig 5.8. Integrity check flow is described in Fig 5.13.

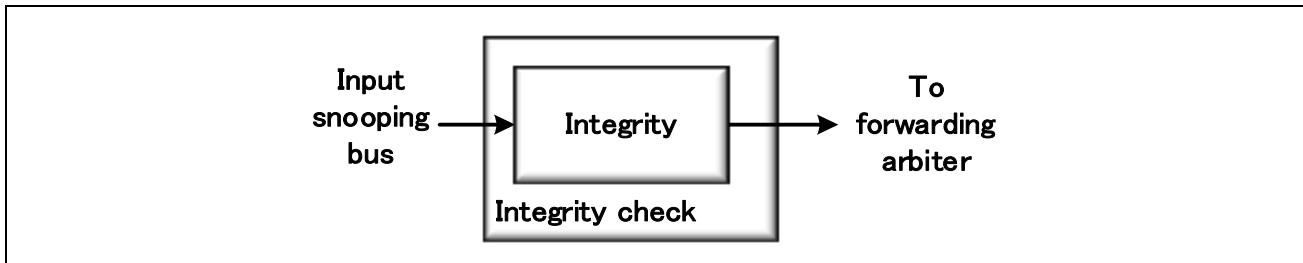


Fig 5.12: Integrity check block diagram

The Integrity check function has one functional block:

- Integrity: The ether type of TAGs (C-TAG, SC-TAG, CR-TAG and SCR-TAG) are ignored and the next ether type field are extracted. However, invalid frames are judged to have no header, and the first ether type field is the extract. For example S-TAG, "first ether type field" = ether type of S-TAG. For example CC-TAG, "first ether type field" = ether type of 2nd C-TAG.
- Integrity: This functions check if an error has been received from the input agent or if incoming frames don't respect the required format.
- Integrity check for both IPv4 filtering and IPv6 filtering will happen based on ether type field. i.e Ether type is only used for parsing frame type in MFWD integrity check and is irrespective of header length (IHL) or TPL size of the required frame type.
- Integrity check for layer 4 header filtering will be happened incorrectly when received frame does not included layer 4 header fully because of frame length is shorter. In this case, Integrity check for layer 4 header is executed by forcing the non-receiving field value of layer 4 header is all zero.
- Integrity check for layer 4 header filtering will happen based on ether type field and following conditions.
[IPv4] After IHL*4 bytes header.
[IPv6] After 40 bytes header.

Notes:

- Forwarding arbiter contains the forwarding flow. The forwarding flow is explained per forwarding type. For integrity check, related Forwarding flow is described in Fig 5.13.

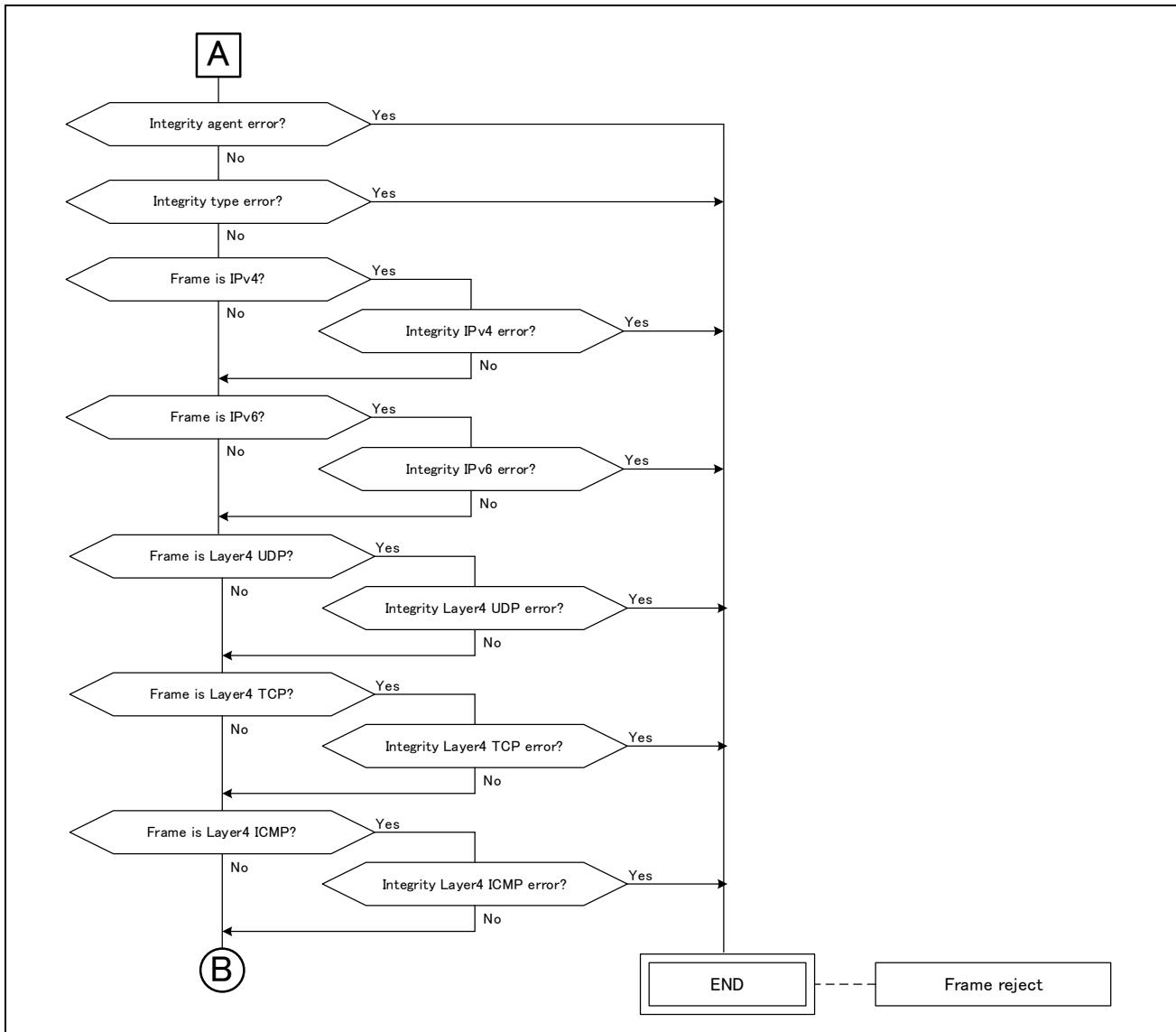


Fig 5.13: Integrity check flow

Note:

- Integrity check errors are described in 5.2.3.1.
- Link A is linked from Fig 5.10.
- Link B links to Fig 5.15.

5.2.3.1 Integrity check errors

Table 5-16 describes the Integrity check errors. Instead of being discarded by forwarding engine, an error frame can be forwarded to exceptional path using Integrity exceptional descriptor described in section 5.2.3.2 by setting its corresponding error exceptional bit.

If any “Integrity agent errors” is valid, “Integrity IPv4 errors”, “Integrity IPv6 errors” and “Integrity Layer 4 errors” are invalid according to Fig 5.13. (“Integrity agent errors” is controlled with higher priority than “Integrity IPv4 errors”, “Integrity IPv6 errors” and “Integrity Layer 4 errors”.). Therefore, if “Integrity agent errors” is valid, the “Integrity IPv4 errors”, “Integrity IPv6 errors” and “Integrity Layer 4 errors” counter and MINFO will not be updated even if the “Integrity IPv4 errors”, “Integrity IPv6 errors” and “Integrity Layer 4 errors” condition is met.

R-Switch integrity check functions don't support extension header on IPv6.

If multiple errors happen for the same frame (for example : TFE (TAG filtering error) , EC0 (RMAC Frame filtering error) , EC1 (Oversize error)), SAEF will be updated for all these errors as each signal is independent. And if exceptional path is set for any of these errors, then Frame will be forwarded via exceptional path.

Table 5-16: Integrity check Errors

Error	Error name	Error interrupt/Explanation	Error exceptional bit
Integrity agent errors			
GTFE	GWCA TAG filtering error	Happens when a frame is received from a GWCA and LDESCR.SAEF[0] is set [GWCA]	FWCEPRC0.GTTEF
GCKSE	GWCA CheckSum Error	Happens when a frame is received from a GWCA and LDESCR.SAEF[1] is set [GWCA] This function will not be affected by FWICETC1i.ICDMi .	FWCEPRC0.GCKSEEF
GAREE	GWCA AXI RAM ECC Error	Happens when a frame is received from a GWCA and LDESCR.SAEF[2] is set [GWCA]	FWCEPRC0.GAREEEF
GAXE	GWCA AXI Error	Happens when a frame is received from a GWCA and LDESCR.SAEF[3] is set [GWCA]	FWCEPRC0.GAXEEF
GSEGE	GWCA Sequence Error	Happens when a frame is received from a GWCA and LDESCR.SAEF[4] is set [GWCA]	FWCEPRC0.GSEQEEF
GDNE	GWCA Descriptor Number Error	Happens when a frame is received from a GWCA and LDESCR.SAEF[6] is set [GWCA]	FWCEPRC0.GDNEEF
ETFE	Ethernet TAG filtering Error	Happens when a frame is received from an Ethernet agent and LDESCR.SAEF[0] is set [TSNA]	FWCEPRC0.ETTEF
ECKSE	Ethernet CheckSum Error	Happens when a frame is received from an Ethernet agent and LDESCR.SAEF[1] is set [TSNA] This function will not be affected by FWICETC1i.ICDMi .	FWCEPRC0.ECKSEEF
EPHYE	Ethernet TAG PHY Error	Happens when a frame is received from an Ethernet agent and LDESCR.SAEF.EC0 is set to 4'd1 [TSNA]	FWCEPRC0.EPHYEEF
EPCRCE	Ethernet PCH CRC Error	Happens when a frame is received from an Ethernet agent and LDESCR.SAEF.EC0 is set to 4'd2 [TSNA]	FWCEPRC0.EPCRCEEF
ENIBE	Ethernet Nibble Error	Happens when a frame is received from an Ethernet agent and LDESCR.SAEF.EC0 is set to 4'd3 [TSNA]	FWCEPRC0.ENIBEEF
EFCSE	Ethernet FCS Error	Happens when a frame is received from an Ethernet agent and LDESCR.SAEF.EC0 is set to 4'd4 [TSNA]	FWCEPRC0.EFCSEEF
EFFME	Ethernet Final Fragment Missing Error	Happens when a frame is received from an Ethernet agent and LDESCR.SAEF.EC0 is set to 4'd5 [TSNA]	FWCEPRC0.EFFMEEF

Error	Error name	Error interrupt/Explanation	Error exceptional bit
ECFSE	Ethernet C-Fragment SMD Error	Happens when a frame is received from an Ethernet agent and LDESCR.SAEF.EC0 is set to 4'd6 [TSNA]	FWCEPRC0.ECFSEEF
ECFFCE	Ethernet C-Fragment FRAG_COUNT Error	Happens when a frame is received from an Ethernet agent and LDESCR.SAEF.EC0 is set to 4'd7 [TSNA]	FWCEPRC0.ECFFCEF
ERFF	Ethernet RMAC Frame Filtered	Happens when a frame is received from an Ethernet agent and LDESCR.SAEF.EC0 is set to 4'd8 [TSNA]	FWCEPRC0.ERFFEF
ERPOO	Ethernet Reception Partially Out of Operation	Happens when a frame is received from an Ethernet agent and LDESCR.SAEF.EC0 is set to 4'd9 [TSNA]	FWCEPRC0.ERPOOEF
EMACSE	Ethernet MACsec Error	Happens when a frame is received from an Ethernet agent and LDESCR.SAEF.EC0 is set to 4'd10 [TSNA]	FWCEPRC0.EMACSEEF
EBOE	Ethernet Buffer Overflow Error	Happens when a frame is received from an Ethernet agent and LDESCR.SAEF.EC1 is set to 2'd1 [TSNA]	FWCEPRC0.EBOEEF
EUE	Ethernet Undersize Error	Happens when a frame is received from an Ethernet agent and LDESCR.SAEF.EC1 is set to 2'd2 [TSNA]	FWCEPRC0.EUEEF
EOE	Ethernet Oversize Error	Happens when a frame is received from an Ethernet agent and LDESCR.SAEF.EC1 is set to 2'd3 [TSNA]	FWCEPRC0.EOEEF
Integrity Type errors			
TYPEF	Type Filtering	FWEIS0i.ICFSi	FWCEPRC0.ICTFEF
Integrity IPv4 errors			
IP4F	IPv4 Filtering	FWEIS0i.ICFSi	FWCEPRC0.ICIP4FEF
Integrity IPv6 errors			
IP6F	IPv6 Filtering	FWEIS0i.ICFSi	FWCEPRC0.ICIP6FEF
Integrity Layer 4 errors			
L4F	Layer 4 Filtering	FWEIS0i.ICFSi	FWCEPRC0.ICL4FEF

5.2.3.2 Integrity exceptional descriptor

Integrity exceptional descriptor fields are described in Table 5-17.

Table 5-17: Integrity exceptional descriptor fields

Field name FDESCR.	Values
DV	Exceptional descriptors are forwarded to GWCA number FWCEPTC.EPCS (port number PORT_TIME_N+FWCEPTC.EPCS)
SEC	FWCEPTC.EPSL
CSDj	FWCEPTC.EPCSD
IPV	FWCEPTC.EPIPV
MINFO	Refer to Fig 5.14 and Table 5-18
RV	1'b0
RN	ALL0
SEQN	Set to frame input sequence number

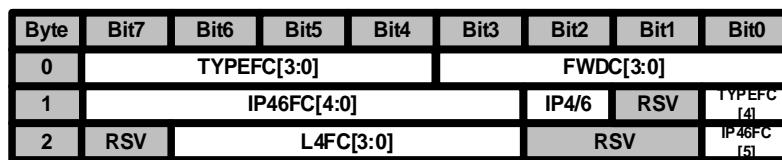


Fig 5.14: Integrity exceptional descriptor MINFO format

Table 5-18: Integrity exceptional descriptor MINFO field explanation

Field name FDESCR.	Bit width	Field explanation	Values
FWDC	4	ForWarDing Code Present in all descriptors, allows to identify the type of forwarding	Fixed to 1 for Integrity exceptional descriptors
TYPEF	none	Type filtering (FDESCR.TYPEFC != 0)	Refer to section 5.2.3.1
TYPEFC	5	Type filtering code	0 : no filtering 25, 24, ... 2, 1 : filtered by (i = any) ETDFEi7, ETDFEi6, ETDFEi5, ETDFEi4, ETDFEi3, ETDFEi2, ETDFEi1, ETDFEi0, RSV, OTFEi, PTPFEi, MSFEi, ECFEi, PPFEi, EOLFEi, ESPFEi, EFCFEi, IP6FEi, SRPFEi, AVTPFEi, WOLFEi, ARPFEi, IP4FEi, EUSFEi, ESFEi Restriction: - HW: If multiple errors are detected, only the highest number is reported.
IP4F	none	IPv4 filtering (FDESCR.IP46FC != 0)	Refer to section 5.2.3.1
IP6F	none	IPv6 filtering (FDESCR.IP46FC != 0)	Refer to section 5.2.3.1
IP4/6	1	IPv4 or IPv6 frame	0 : IPv4 frame and filtering 1 : IPv6 frame and filtering

Field name FDESCR.	Bit width	Field explanation	Values
IP46FC	6	<p>FDESCR.IP4/6 = 0 : IPv4 filtering code</p> <p>FDESCR.IP4/6 = 1 : IPv6 filtering code</p>	<p>0 : no filtering</p> <p>[IPv4] 40, 39, 38, 37, ... 2, 1 : filtered by (i = any)</p> <p>FWIP4TLCCi.IP4TLMXVi, FWIP4TLCCi.IP4TLMVVi, IP4SOLDAFEi0, IP4SDBDAFEi0, IP4SNDAFEi0, IP4SUDAFEi0, IP4SOLSAFEi0, IP4SDBSAFEi0, IP4SNSAFEi0, IP4SUSAFei0, IP4WTLFi, IP4OTLFi, IP4UTLFi, IP4IFFFei, IP4FFFFei, RSV, IP4WBHLFEi, IP4OLSAFEi, IP4OWSAFEi, IP4SSDAFEi, IP4OSAFEi, IP4LSAFEi, IP4USAFei, IP4BSAFEi, IP4MSAFEi, IP4ODAFEi, IP4LDAFEi, IP4UDAFEi, IP4BDAFEi, IP4MDAFEi, IP4UUDAFEi, IP4OTHFEi, IP4ICMPFEi, IP4UDPFEi, IP4TCPFEi, IP4TLNFEi, IP4MFFFei, RSV, IP4WVFEi, IP4WHLFEi [IPv6] 34, 33, 32, 31, ... 2, 1 : filtered by (i = any)</p> <p>FWIP6PLCCi.IP6PLFMXVi, FWIP6PLCCi.IP6PLFMVVi, IP6SOLDAFEi0, IP6SDBDAFEi0, IP6SNDAFEi0, IP6SUDAFEi0, IP6SOLSAFEi0, IP6SDBSAFEi0, IP6SNSAFEi0, IP6SUSAFeij IP6OPLFE, IP6UPLFE, RSV, IP6OLSAFEi, IP6OWSAFEi, IP6SSDAFEi, IP6USAFei, IP6LSAFEi, IP6MSAFEi, IP6LLSAFEi, IP6ULSAFEi, IP6UDAFEi, IP6LDAFEi, IP6MDAFEi, IP6LLDAFEi, IP6ULDAFEi, IP6UUDAFEi, IP6OTHFEi, IP6ICMPFEi, IP6UDPFEi, IP6TCPFEi, IP6HLNFEi, RSV, IP6WVFEi</p> <p>Restriction:</p> <p>HW: If multiple errors are detected, only the highest number is reported.</p>
L4F	none	Layer 4 filtering (FDESCR.L4FC != 0)	Refer to section 5.2.3.1
L4FC	4	Layer 4 filtering code	<p>0 : no filtering</p> <p>12, 11, 10, 9, ... 2, 1 : filtered by (i = any)</p> <p>FWICL4THLCi.L4THLFMXVi, FWICL4THLCi.L4THLFMVVi, L4N9FEi, L4N8FEi, L4N7FEi, L4N6FEi, L4N5FEi, L4N4FEi, L4N3FEi, L4N2FEi, L4N1FEi, L4N0FEi</p>
RSV	--	Reserved field	Set to 0

5.2.4 Direct descriptor forwarding

Direct descriptor forwarding is used to forward local direct descriptors (**LDESCR.FMT** [GWCA] set to 1'b1) received from a slow interface [GWCA] using **FWPC1i** and **FWCEPRC0** register and can be monitored using **FWEIS0i** interrupt register. Direct descriptor forwarding flow is described in Fig 5.15.

Functions:

- **FWPC1i.DDEi** register is used to enable direct descriptor reception from port i.
- **FWPC1i.DDSLi** register is used to enable secure direct descriptor reception from port i when direct descriptor reception from port I is enabled.
- **FWCEPRC0** register enables exceptional path for error descriptors.
- **FWEIS0i** interrupt register notifies that a direct descriptor has been rejected.

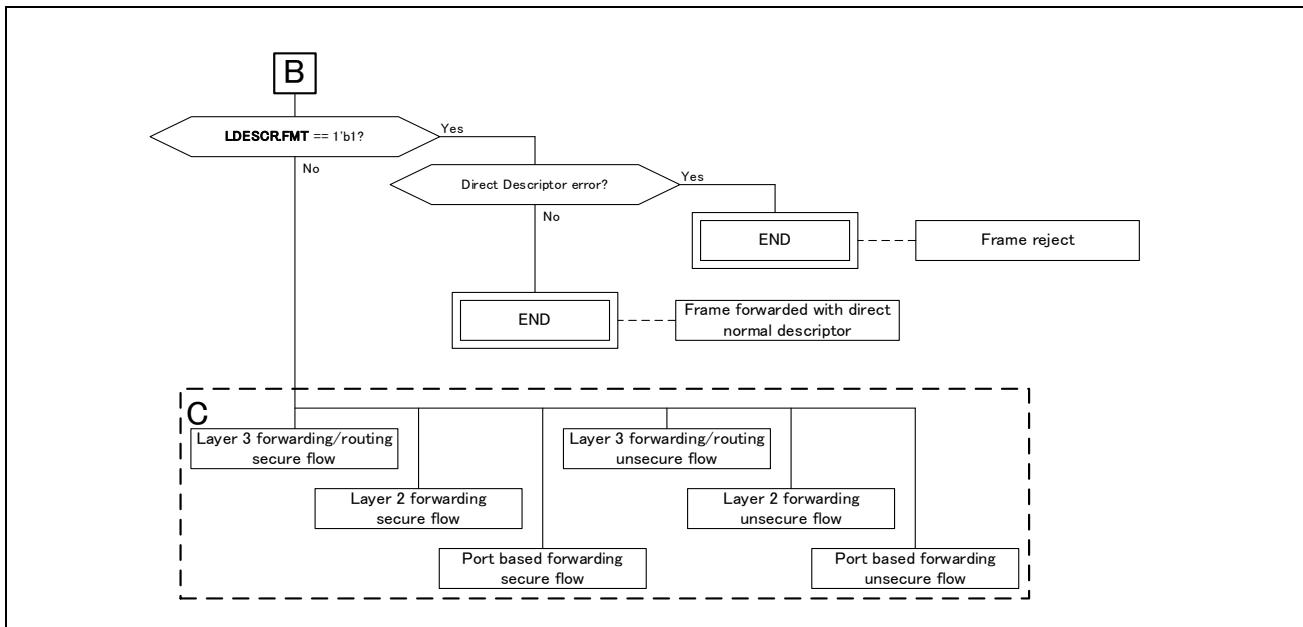


Fig 5.15: Direct descriptor forwarding flow

Note:

- Direct descriptor errors are described in section 5.2.4.1.
- Direct normal descriptor format is described in section 5.2.4.2.
- Link B is linked from Fig 5.13.
- Link C links to Fig 5.42: Layer 3 forwarding/routing secure flow, Fig 5.43: Layer 3 forwarding/routing unsecure flow, Fig 5.51: Layer 2 forwarding secure flow, Fig 5.52: Layer 2 forwarding unsecure flow, Fig 5.55: Port based forwarding secure flow, Fig 5.56: Port based forwarding unsecure flow.

They are processed in parallel and forwarding with the highest effective RP is applied. If the RP values are the same, the priority is controlled as follows:

Layer 3 forwarding/routing secure flow(Cascade filter > L3 stream filter > L2 stream filter) > Layer 2 forwarding secure flow(MAC&VLAN or MAC or VLAN) > Port based forwarding secure flow > Layer 3 forwarding/routing unsecure flow(Cascade filter > L3 stream filter > L2 stream filter) > Layer 2 forwarding unsecure flow(MAC&VLAN or MAC or VLAN) > Port based forwarding unsecure flow

5.2.4.1 Direct Descriptor forwarding errors

Table 5-19 describes the Direct descriptor forwarding errors. Instead of being discarded by forwarding engine, an error frame can be forwarded to exceptional path using Direct exceptional descriptor described in section 5.2.4.3 by setting corresponding error exceptional bit. For error set conditions, refer to corresponding error interrupt register explanations.

Table 5-19: Direct descriptor Errors

Error	Error name	Error interrupt	Error exceptional bit
DDE	Direct Descriptor Error	FWEIS0i.DDESi	FWCEPRC0.DDEEF
DDSF	Direct Descriptor Security Filtering	FWEIS0i.DDSESi	FWCEPRC0.DDFSFEF
DDFF	Direct Descriptor Format Security Filtering	FWEIS0i.DDFESi	FWCEPRC0.DDFEEF
NTF	No Target Filtering	FWEIS0i.DDNTFSi	FWCEPRC2.DDNTFEF

5.2.4.2 Direct normal descriptor

Direct normal descriptor fields are described in Table 5-20. For **LDESCR** explanation, refer to GWCA specification [GWCA].

Table 5-20: Direct normal descriptor fields

Field name FDESCR.	Values
DV	LDESCR.DV
SEC	LDESCR.SEC
CSD	LDESCR.CSD
IPV	LDESCR.IPV
MINFO	Refer to Fig 5.16 and Table 5-21
RV	LDESCR.RV
RN	if LDESCR.RV is set, set to LDESCR.RN if LDESCR.RV is not set, set to 0
SEQN	Set to frame input sequence number

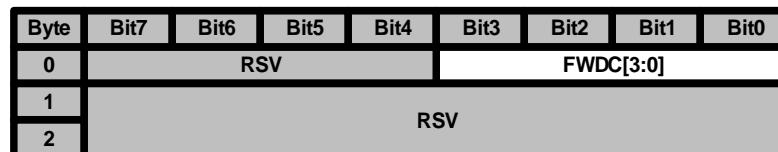


Fig 5.16: Direct normal descriptor MINFO format

Table 5-21: Direct normal descriptor MINFO field explanation

Field name FDESCR.	Bit width	Field explanation	Values
FWDC	4	ForWarDing Code Present in all descriptors, allows to identify the type of forwarding	Fixed to 2 for Direct normal descriptors
RSV	--	Reserved field	Set to 0

5.2.4.3 Direct exceptional descriptor

Direct exceptional descriptor fields are described in Table 5-22.

Table 5-22: Direct exceptional descriptor fields

Field name FDESCR.	Values
DV	Exceptional descriptors are forwarded to GWCA number FWCEPTC.EPCS (port number PORT_TIME_N+FWCEPTC.EPCS)
SEC	FWCEPTC.EPSL
CSDj	FWCEPTC.EPCSD
IPV	FWCEPTC.EPIPV
MINFO	Refer to Fig 5.17 and Table 5-23
RV	1'b0
RN	ALL0
SEQN	Set to frame input sequence number

Byte	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	RSV							FWDC[3:0]
1	RSV				NTF	DDFF	DDSF	DDF
2					RSV			

Fig 5.17: Direct exceptional descriptor MINFO format

Table 5-23: Direct exceptional descriptor MINFO field explanation

Field name FDESCR.	Bit width	Field explanation	Values
FWDC	4	ForWarDing Code Present in all descriptors, allows to identify the type of forwarding	Fixed to 3 for Direct exceptional descriptors
DDF	1	Direct Descriptor Filtered	Refer to section 5.2.4.1
DDSF	1	Direct Descriptor Security Filtered	Refer to section 5.2.4.1
DDFF	1	Direct Descriptor Format Filtered	Refer to section 5.2.4.1
NTF	1	No Target Filtered	Refer to section 5.2.4.1

5.2.5 Layer 3 forwarding/routing/filtering

The Layer 3 forwarding/routing/filtering block diagram is represented in Fig 5.18. This block is denominated by “L3”, but it contains all the stream-based functions of the forwarding engine, even the Layer 2 streams.

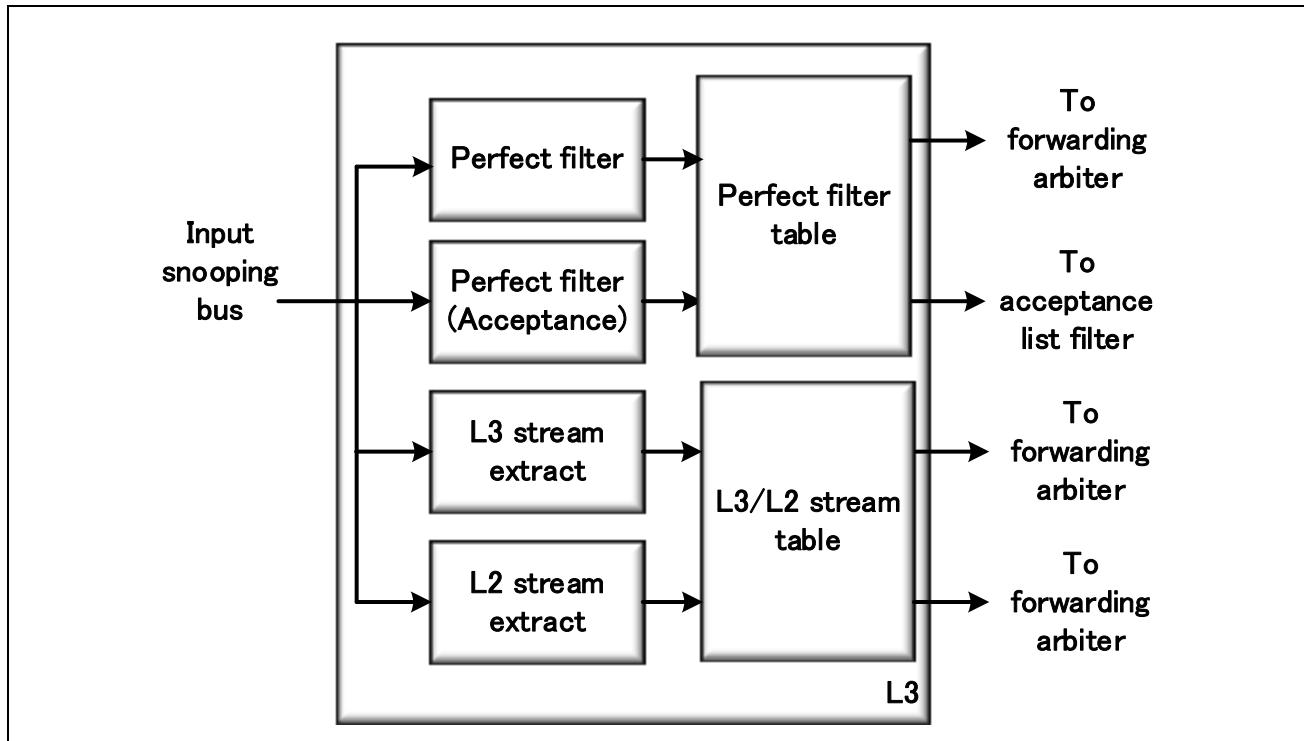


Fig 5.18: Layer 3 forwarding/routing/filtering block diagram

The Layer 3 forwarding/routing/filtering function is separated in four functional blocks:

- Perfect filter: This block snoops all the needed information from the Forwarding engine snooping bus and create a user defined stream.
- Perfect filter (Acceptance): This block snoops all the needed information from the Forwarding engine snooping bus and create a user defined stream.
- L3 stream extract: This block snoops all the needed information from the Forwarding engine snooping bus and create an L3 stream.
- L2 stream extract: This block snoops all the needed information from the Forwarding engine snooping bus and create a L2 stream.
- Perfect filter table: This block handles the stream meta information such as forwarding, routing and filtering information. The total number of this table is PFL_CADF_N. This table can divide into for Filtering (Acceptance list) and for Forwarding by **FWLTHTEC0.PFFALA** and **FWLTHTEC0.PFFALAA**.
- L3/L2 stream table: This block handles the stream meta information such as forwarding, routing and filtering information. The total number of this table is LTH_STREAM_N. This table is shared by L3/L2 stream.

Notes:

- Forwarding arbiter contains the forwarding flow. The forwarding flow is explained per forwarding type. For Layer 3 forwarding/routing/filtering, related Forwarding flow is described in Fig 5.42, Fig 5.43 and Fig 5.60.

5.2.5.1 Perfect filter

The perfect filter is used to identify streams. This filter has the advantage to be flexible and can identify a stream without any statistic error but, because of its high cost, is available in a limited number (PFL_CADF_N streams available).

The Perfect filter block diagram is represented in Fig 5.19.

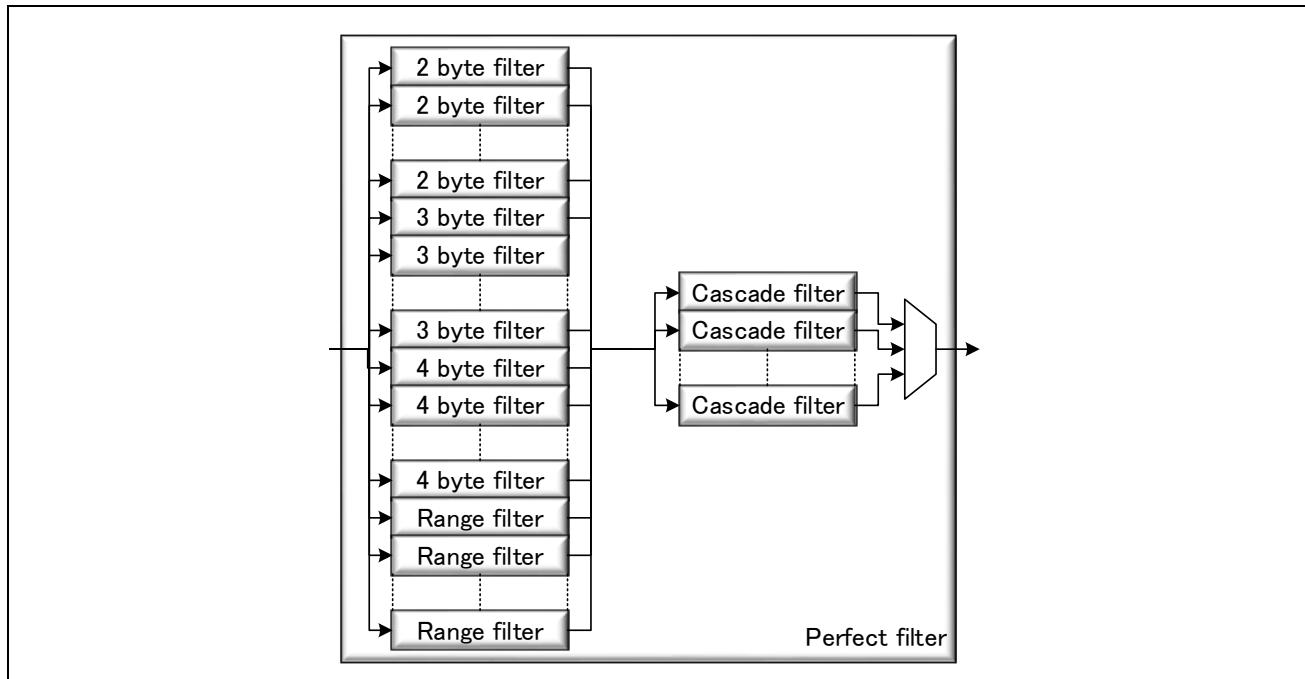


Fig 5.19: Perfect filter block diagram

The perfect filtering happens in two steps:

- The first step is done by 2-byte, 3-byte, 4-byte and range filters. Each one of these filters is independent from others but only able to filter a precise part of a frame.
- The second step is done by Cascade filters. Each one of the cascade filters can associate PFL_CFMF_N filtering results from the first step to create a stream ID.

Restrictions:

- HW: All frames smaller than 49 bytes (received with no command 1 from snooping bus, the 49 bytes are not including the TAG saved in the TAG RAM) will be considered has unknown frames by the perfect filter.

(1) 2-byte filters

A 2-byte filter aims at filtering a specific portion of a frame and happens in two steps, the data extraction and the filtering.

(a) Data extraction for filtering

A 2-byte filter has two modes to extract the data from a frame. Fig 5.20 describes these modes using examples.

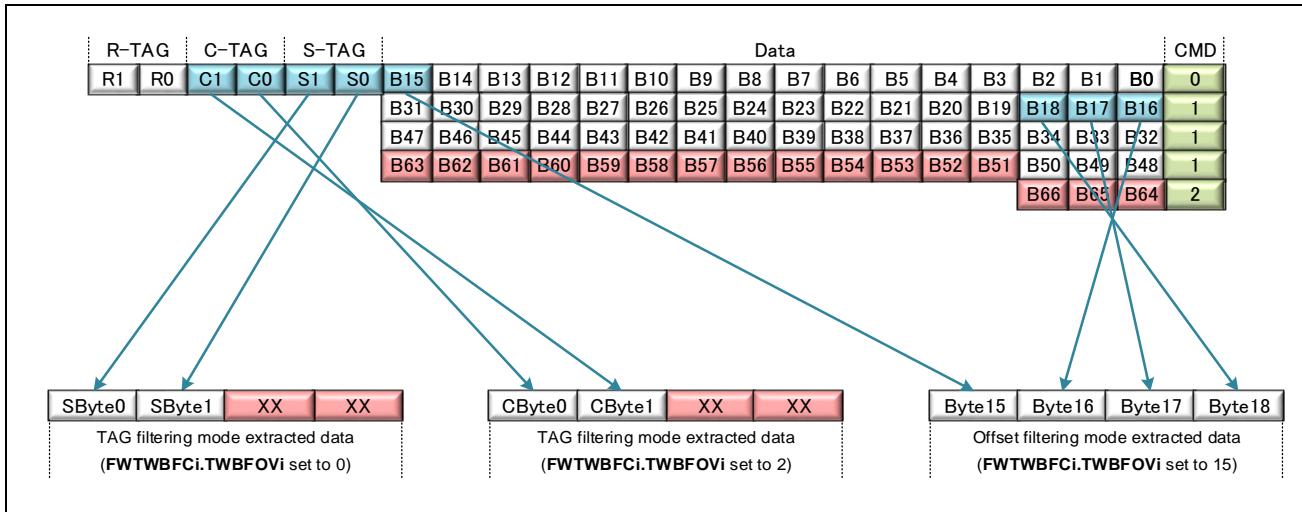


Fig 5.20: 2-byte filter data extraction for filtering

In Offset filtering mode (**FTWTWBFCi.TWBFMi == 1'b0**):

- Data bytes from byte **FTWTWBFCi.TWBFOVi** to byte **FTWTWBFCi.TWBFOVi+3** are extracted for filtering.

In TAG filtering mode (**FTWTWBFCi.TWBFMi == 1'b1**):

- If **FTWTWBFCi.TWBFOVi** is set to 0, VLAN S-TAG is extracted for filtering.
- If **FTWTWBFCi.TWBFOVi** is set to 2, VLAN C-TAG is extracted for filtering.

Restrictions:

- HW: The data for filtering in 2-byte filters can only be extracted until the first three bytes in the penultimate beat of data (first three bytes of the last time CMD is equal to 1. In Fig 5.20, the bytes colored in red are the none-extractable bytes for filtering). I.e., the offset filtering will only be effective if the offset value is set until the last byte of the antepenultimate beat of data (the last before last time CMD is equal to 1. Byte 47 in Fig 5.20).
- HW: A filter with a setting that should use non-extractable data for filtering will always unmatched.
- HW: In TAG filtering mode, if S-TAG or C-TAG is not present in the frame for filtering, the value 0 will be extracted by the filter.

(b) Extracted data filtering

A 2-byte filter has three modes to filter extracted data. Fig 5.21 describes these modes.

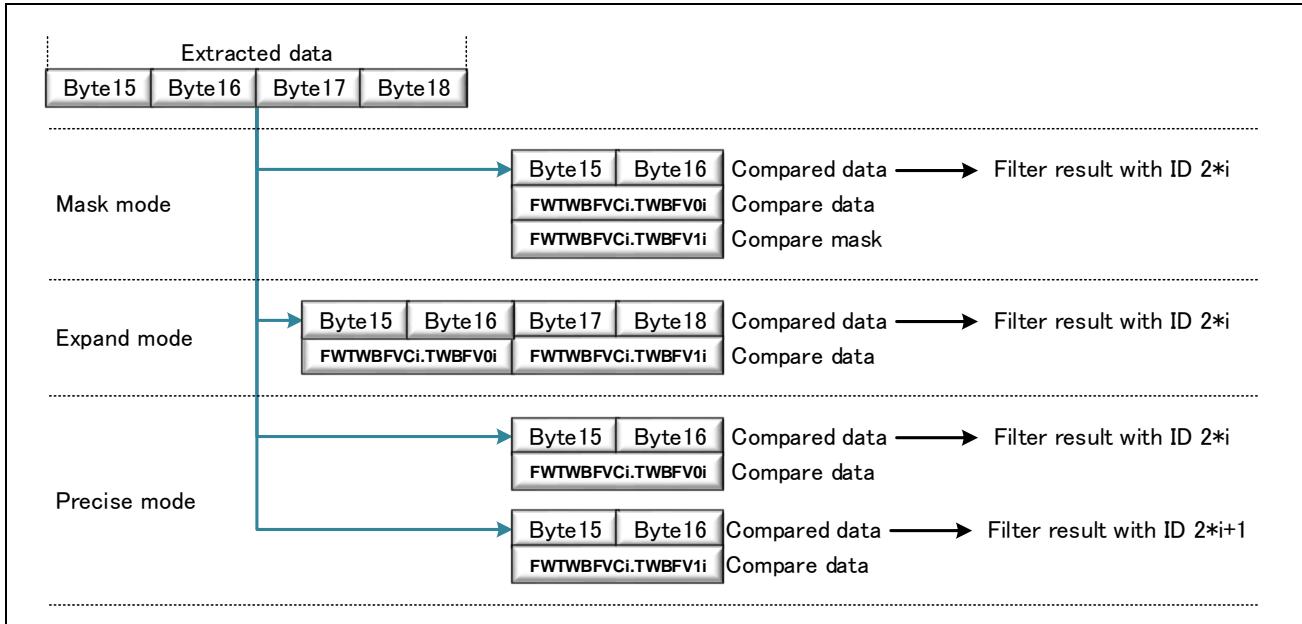


Fig 5.21: 2-byte filter data extraction for filtering

In mask mode (**FWTWFBCi.TWBFUMi** == 2'b00):

- The first two bytes of the extracted data are compared to **FWTWFVCi.TWBFV0i** using **FWTWFVCi.TWBFV1i** as a mask (when a bit is set to 1, the corresponding bit is not used for comparison). The result is associated to 2^*i filter ID.

In Expand mode (**FWTWFBCi.TWBFUMi** == 2'b01):

- The four-byte extracted data is compared to **{FWTWFVCi.TWBFV0i, FWTWFVCi.TWBFV1i}**. The result is associated to 2^*i filter ID.

In Precise mode (**FWTWFBCi.TWBFUMi** == 2'b10):

- The first two bytes of the extracted data are compared to **FWTWFVCi.TWBFV0i**. The result is associated to 2^*i filter ID.
- The first two bytes of the extracted data are compared to **FWTWFVCi.TWBFV1i**. The result is associated to 2^*i+1 filter ID.

(2) 3-byte filters

A 3-byte filter aims at filtering a specific portion of a frame and happens in two steps, the data extraction and the filtering.

(a) Data extraction for filtering

A 3-byte filter has one mode to extract the data from a frame. Fig 5.22 describes this mode using an example.

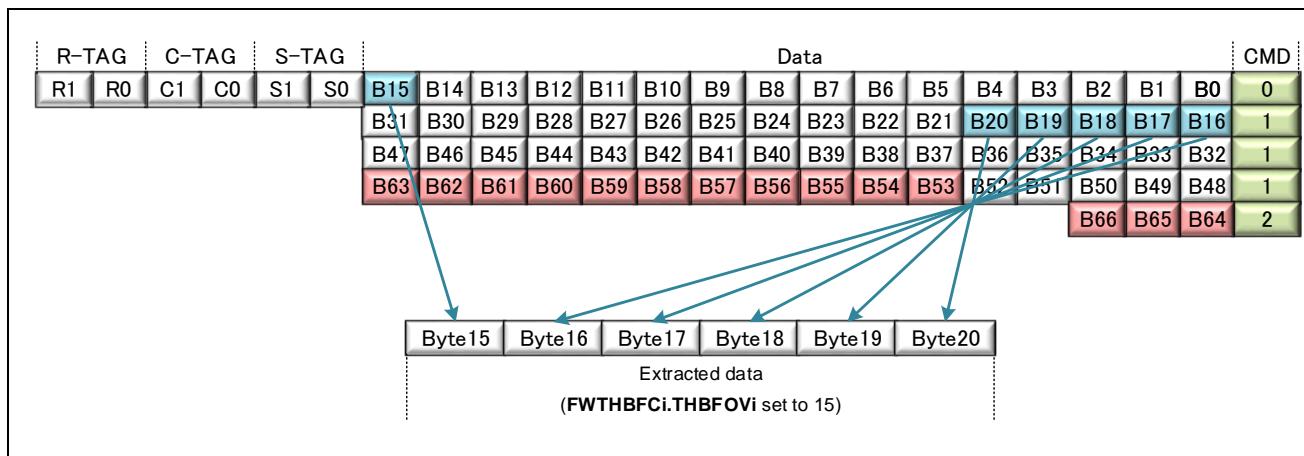


Fig 5.22: 3-byte filter data extraction for filtering

For 3-byte filters:

- Data bytes from byte **FWTHBFci.THBFOVi** to byte **FWTHBFci.THBFOVi+5** are extracted for filtering.

Restrictions:

- HW: The data for filtering in 3-byte filters can only be extracted until the first five bytes in the penultimate beat of data (first five bytes of the last time CMD is equal to 1. In Fig 5.22, the bytes colored in red are the none-extractible bytes for filtering). I.e. the offset filtering will only be effective if the offset value is set until the last byte of the antepenultimate beat of data (the last before last time CMD is equal to 1. Byte 47 in Fig 5.22).
 - HW: A filter with a setting that should use non-extractible data for filtering will always unmatched.

(b) Extracted data filtering

A 3-byte filter has three modes to filter extracted data. Fig 5.23 describes these modes.

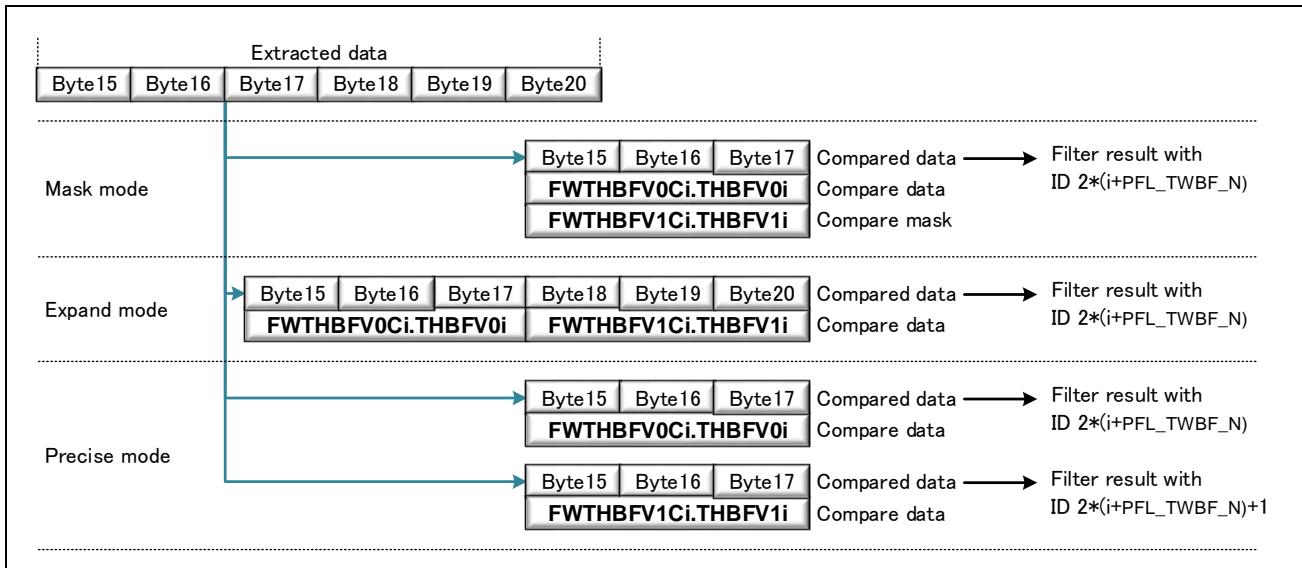


Fig 5.23: 3-byte filter data extraction for filtering

In mask mode (**FWTHBFCi.THBFDUMi == 2'b00**):

- The first three bytes of the extracted data are compared to **FWTHBFV0Ci.THBFDUMi** using **FWTHBFV1Ci.THBFDUMi** as a mask (when a bit is set to 1, the corresponding bit is not used for comparison). The result is associated to $2^*(i + PFL_TWBF_N)$ filter ID.

In Expand mode (**FWTHBFCi.THBFDUMi == 2'b01**):

- The six-byte extracted data is compared to **{FWTHBFV0Ci.THBFDUMi, FWTHBFV1Ci.THBFDUMi}**. The result is associated to $2^*(i + PFL_TWBF_N)$ filter ID.

In Precise mode (**FWTHBFCi.THBFDUMi == 2'b10**):

- The first three bytes of the extracted data are compared to **FWTHBFV0Ci.THBFDUMi**. The result is associated to $2^*(i + PFL_TWBF_N)$ filter ID.
- The first three bytes of the extracted data are compared to **FWTHBFV1Ci.THBFDUMi**. The result is associated to $2^*(i + PFL_TWBF_N)+1$ filter ID.

(3) 4-byte filters

A 4-byte filter aims at filtering a specific portion of a frame and happens in two steps, the data extraction and the filtering.

(a) Data extraction for filtering

A 4-byte filter has one mode to extract the data from a frame. Fig 5.24 describes this mode using an example.

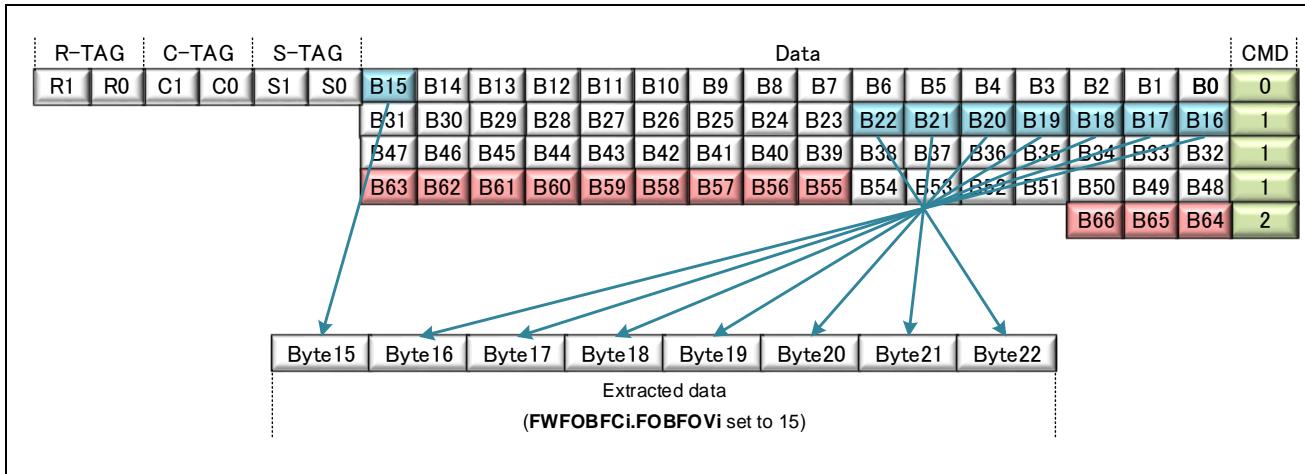


Fig 5.24: 4-byte filter data extraction for filtering

For 4-byte filters:

- Data bytes from byte **FWFOBFCi.FOBFOVi** to byte **FWFOBFCi.FOBFOVi+7** are extracted for filtering.

Restrictions:

- HW: The data for filtering in 4-byte filters can only be extracted until the first seven bytes in the penultimate beat of data (first seven bytes of the last time CMD is equal to 1. In Fig 5.24, the bytes colored in red are the none-extractable bytes for filtering). I.e. the offset filtering will only be effective if the offset value is set until the last byte of the antepenultimate beat of data (the last before last time CMD is equal to 1. Byte 47 in Fig 5.24).
- HW: A filter with a setting that should use non-extractable data for filtering will always unmatched.

(b) Extracted data filtering

A 4-byte filter has three modes to filter extracted data. Fig 5.25 describes these modes.

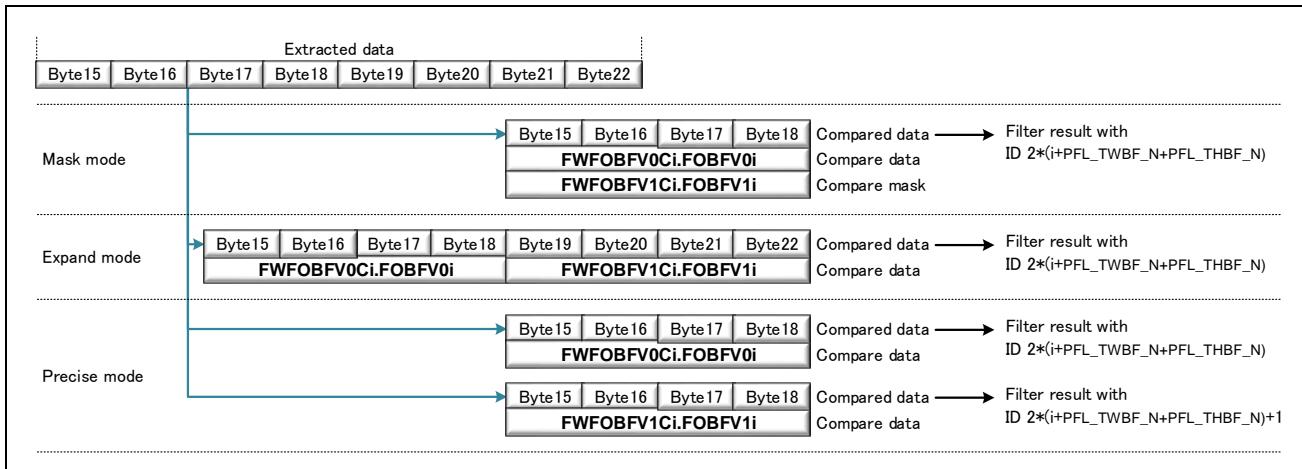


Fig 5.25: 4-byte filter data extraction for filtering

In mask mode (**FWFOBFCi.FOBFUMi** == 2'b00):

- The first four bytes of the extracted data are compared to **FWFOBFV0Ci.FOBFV0i** using **FWFOBFV1Ci.FOBFV1i** as a mask (when a bit is set to 1, the corresponding bit is not used for comparison). The result is associated to $2*(i + PFL_TWBF_N + PFL_THBF_N)$ filter ID.

In Expand mode (**FWFOBFCi.FOBFUMi** == 2'b01):

- The eight-byte extracted data is compared to **{FWFOBFV0Ci.FOBFV0i, FWFOBFV1Ci.FOBFV1i}**. The result is associated to $2*(i + PFL_TWBF_N + PFL_THBF_N)$ filter ID.

In Precise mode (**FWFOBFCi.FOBFUMi** == 2'b10):

- The first three bytes of the extracted data are compared to **FWFOBFV0Ci.FOBFV0i**. The result is associated to $2*(i + PFL_TWBF_N + PFL_THBF_N)$ filter ID.
- The first three bytes of the extracted data are compared to **FWFOBFV1Ci.FOBFV1i**. The result is associated to $2*(i + PFL_TWBF_N + PFL_THBF_N)+1$ filter ID.

(4) Range filters

A Range filter aims at filtering a specific portion of a frame and happens in two steps, the data extraction and the filtering.

(a) Data extraction for filtering

A Range filter has two modes to extract the data from a frame. Fig 5.26 describes these modes using examples.

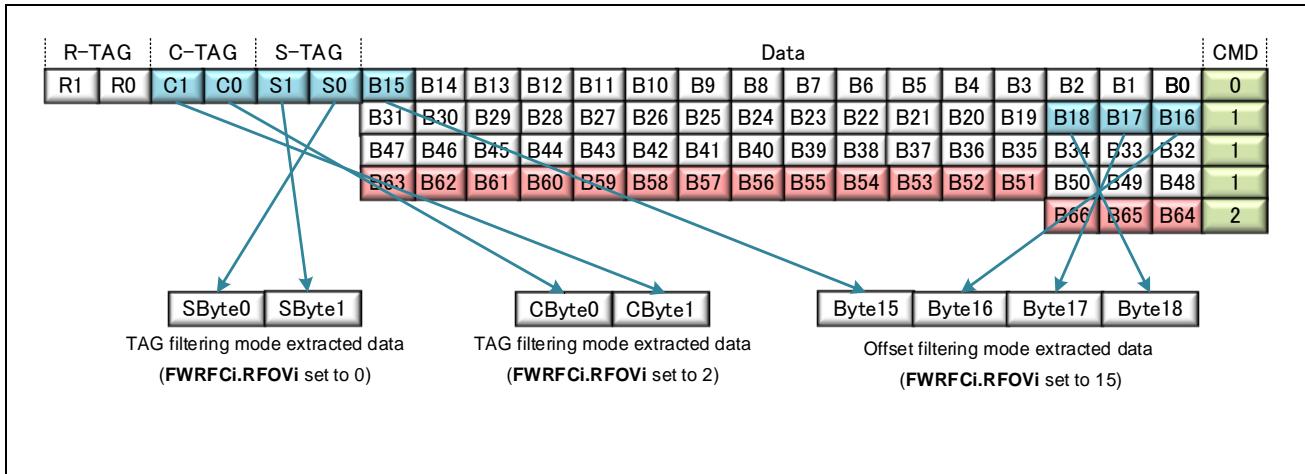


Fig 5.26: Range filter data extraction for filtering

In Offset filtering mode (**FWRFCi.RFOMi** == 1'b0):

- Data bytes from byte **FWRFCi.RFOVi** to byte **FWRFCi.RFOVi** +3 are extracted for filtering.

In TAG filtering mode (**FWRFCi.RFOMi** == 1'b1):

- If **FWRFCi.RFOVi** is set to 0, VLAN S-TAG VID are extracted for filtering (PCP and DEI are fixed to 0).
- If **FWRFCi.RFOVi** is set to 2, VLAN C-TAG VID are extracted for filtering (PCP and DEI are fixed to 0).

Restrictions:

- HW: PCP and DEI values in C-TAGs and S-TAGs are ignored by the range filter (Set to 0).
- HW: The data for filtering in range filters can only be extracted until the first three bytes in the penultimate beat of data (the last before last time CMD is equal to 1. In Fig 5.26, the bytes colored in red are the non-extractable bytes for filtering). I.e. the offset filtering will only be effective if the offset value is set until the last byte of the antepenultimate beat of data (the last before last time CMD is equal to 1. Byte 47 in Fig 5.26).
- HW: A filter with a setting that should use non-extractable data for filtering will always unmatched.

(b) Extracted data filtering

A Range filter has one mode to filter extracted data. Fig 5.21 describes this mode.

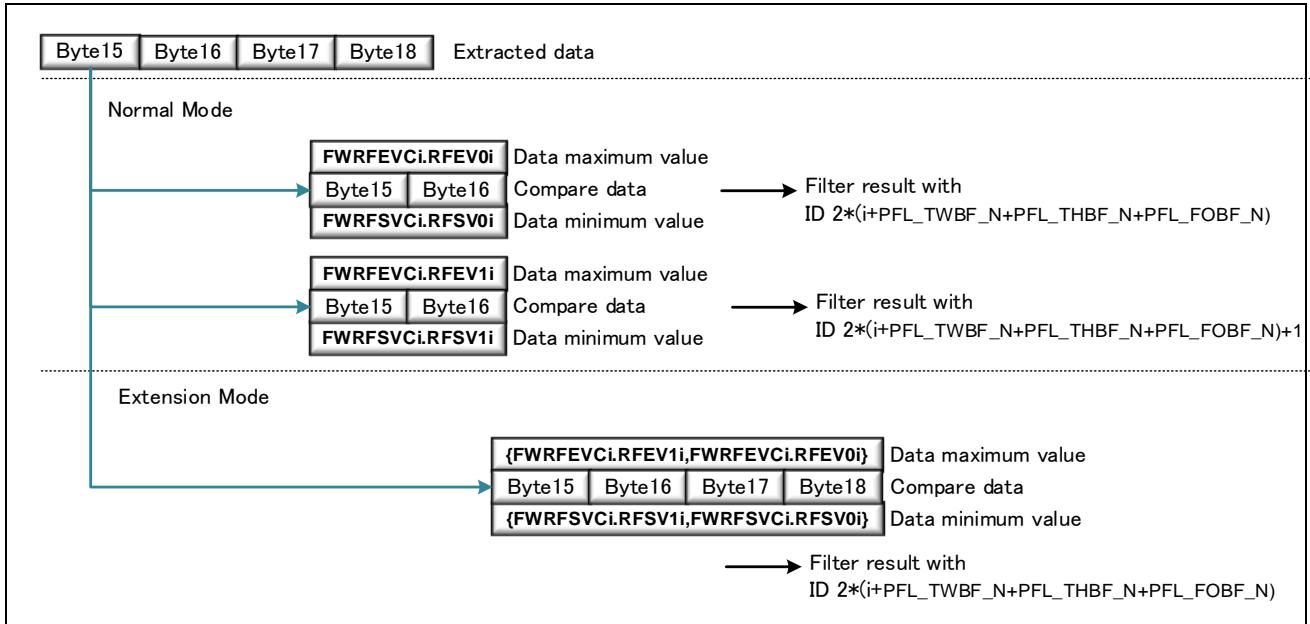


Fig 5.27: Range filter data extraction for filtering

For Range filters:

In Normal mode (**FWRFCi.RFEMi** == 1'b0):

- The two-byte extracted data is checked to be included from **FWRFSVCi.RFSV0i** to **FWRFEVCI.RFEV0i**. The result is associated to $2*(i + PFL_TWBF_N + PFL_THBF_N + PFL_FOBF_N)$ filter ID.
- The two-byte extracted data is checked to be included from **FWRFSVCi.RFSV1i** to **FWRFEVCI.RFEV1i**. The result is associated to $2*(i + PFL_TWBF_N + PFL_THBF_N + PFL_FOBF_N) + 1$ filter ID.

In Extension mode (**FWRFCi.RFEMi** == 1'b1):

- The four-byte extracted data is checked to be included in **{FWRFSVCi.RFSV1i, FWRFSVCi.RFSV0i}** from **{FWRFEVCI.RFEV1i, FWRFEVCI.RFEV0i}**. The result is associated to $2*(i + PFL_TWBF_N + PFL_THBF_N + PFL_FOBF_N)$ filter ID.

(5) Cascade filters

A Cascade filter aims at gathering several filter results (from 2-byte, 3-byte, 4byte and Range filters) to regroup them to create a stream ID. The number of cascade filters defines the number of possible stream IDs in the perfect filter (PFL_CADF_N).

Functions:

- **FWCFMCij** register is used to map until PFL_CFMF_N filters results to cascade filter i.
- **FWCFCi.CFEFFVi** and **FWCFCi.CFPFFVi** registers are used to select from which port the stream is expected and with which type of frame (p or e).
- **FWCFCi.CFMMi** register is used to select filter match mode. In All (AND) Match mode (**FWCFCi.CFMMi == 1'b0**), the Cascade filter will be matched with all valid conditions of **FWCFMCij** has been established. In Partial (OR) Match mode (**FWCFCi.CFMMi == 1'b1**), the Cascade filter will be matched with at least one valid conditions of **FWCFMCij** has been established.
- If a cascade filter matches a frame, a frame format vector [0] of 8 bits equal to 1'b1 is associated to the frame.

Cascade filter stream ID:

- When cascade filter i matches a frame, the stream ID associated to this frame will be a 136-bit stream ID equal to {frame format vector,128'di}.
- If several "enabled cascade filters (that associated valid stream IDs)" match the same frame, the highest number will be selected.

(6) Perfect filter utilization example

Fig 5.28 contains an example of perfect filter utilization. In this example, the user wants to filter a frame which:

- Has a stream ID based on MAC destination address, and VLAN C-TAG.
- Has a MAC destination address equal to 'hAABBCCDDEEFF'.
- Has a VLAN C-TAG equal to ABCD.
- Is known to be an IPv4 frame (IPv4 type is added in filtering for security).

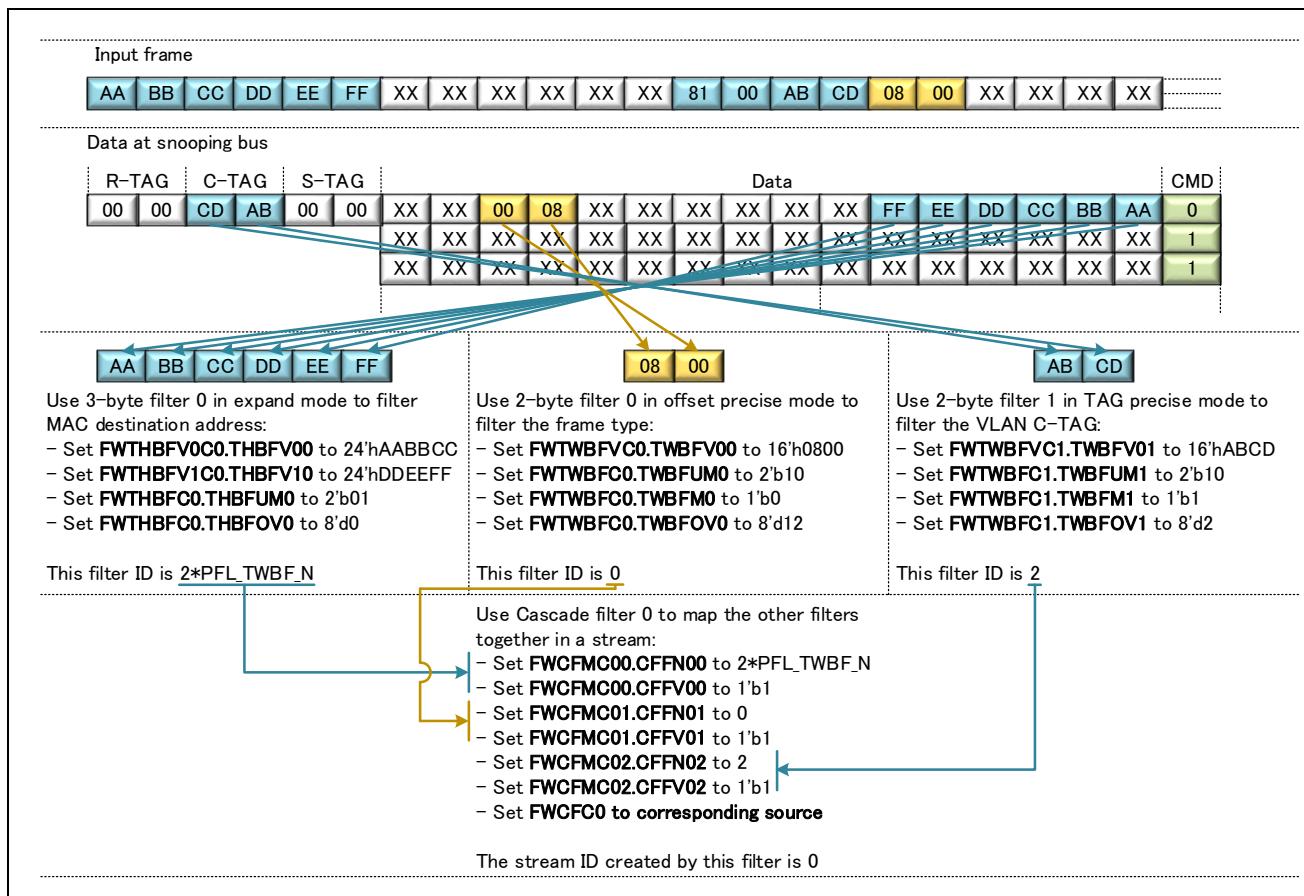


Fig 5.28: Perfect filter utilization example

5.2.5.2 L3 stream filter

The L3 stream filter is used to identify streams. The block diagram is represented in Fig 5.29.

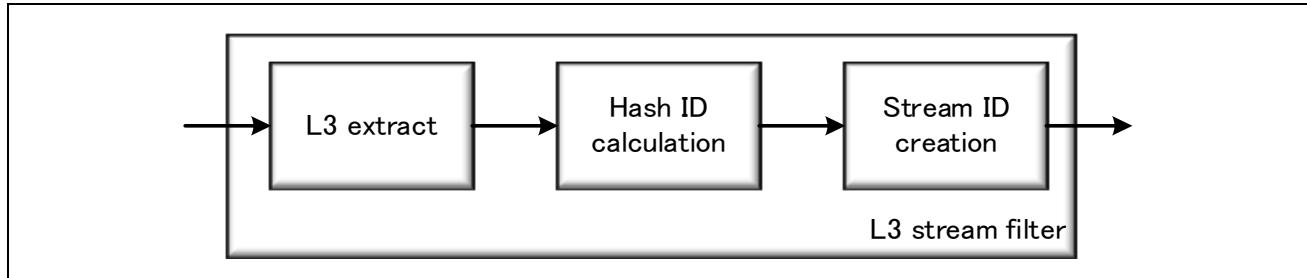


Fig 5.29: L3 stream filter block diagram

The L3 stream filtering happens in Three steps:

- The first step is done by L3 extract. It consists in extracting all the possible field for the IPv4/IPv6 stream ID creation.
- The second step is done by Hash ID calculation. It consists in calculating the hash ID associated to each frame depending on the extracted data and the fields chosen by user for Hash.
- The third step is done by Stream ID creation. It consists in the stream ID assembling depending on the fields chosen by user.
- If several L3 stream filters match the same frame, the L3 stream filter with the highest entry number (learned address) will be selected.

(1) L3 extract

The L3 extract is used to extract the Stream IDs from IPv4 and IPv6 frames to create their associated stream ID. The extraction happens on six formats which are IPv4, IPv4/TCP, IPv4/UDP, IPv6, IPv6/TCP and IPv6/UDP.

Restrictions:

(a) IPv4 detection and data extraction

Fig 5.30 describes how IPv4 detection and data extraction happens. This data extraction happens only if the frame format decode condition are satisfied and if **FWPC0i.IP4OEi** is set for the corresponding source port. In this case, a frame format vector [1] of 8 bits equal to 1'b1 is associated to the frame.

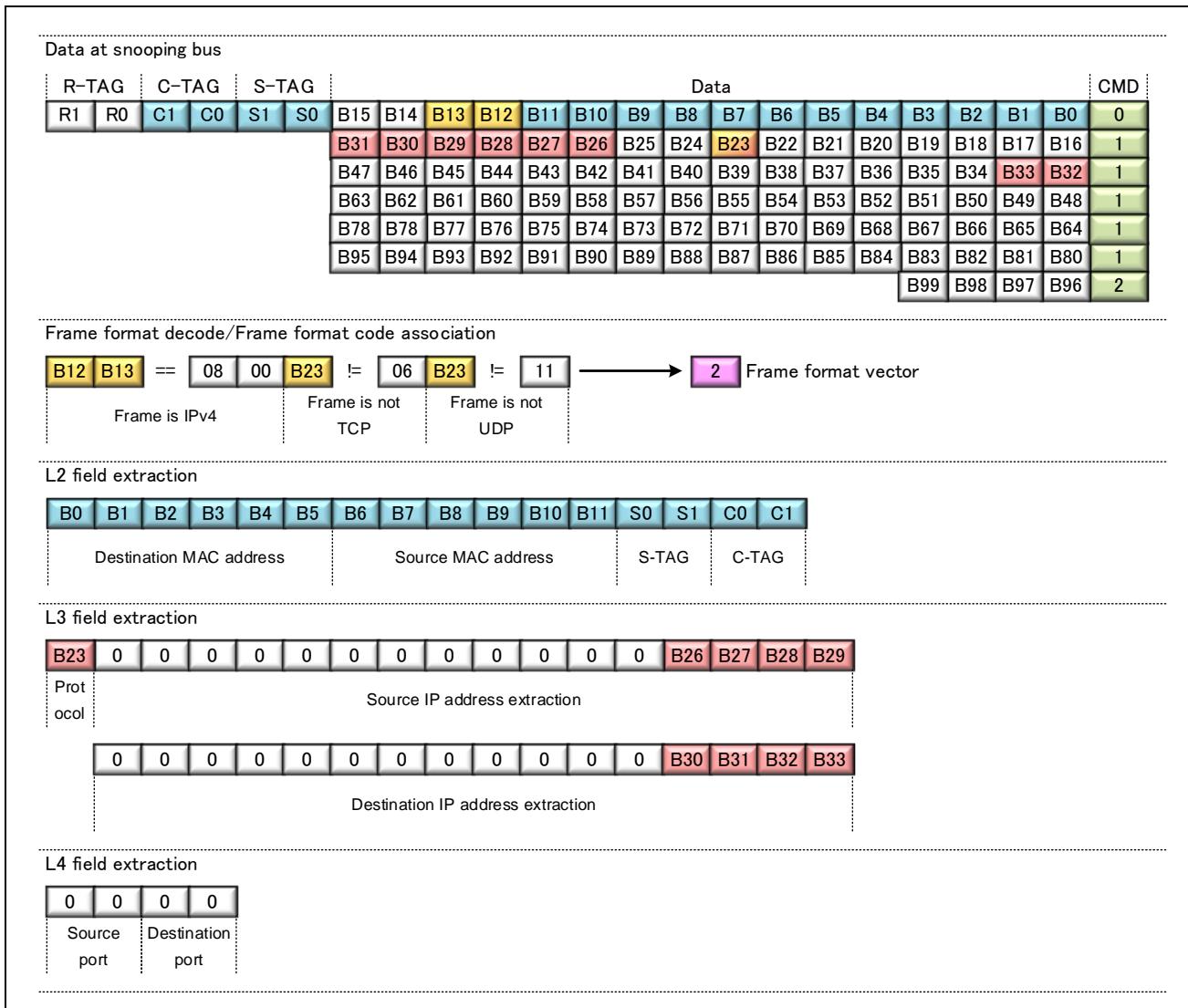


Fig 5.30: IPv4 detection and data extraction

(b) IPv4/UDP detection and data extraction

Fig 5.31 describes how IPv4/UDP detection and data extraction happens. This data extraction happens only if the frame format decode condition are satisfied and if **FWPC0i.IP4UEi** is set for the corresponding source port. In this case, a frame format vector [2] of 8 bits equal to 1'b1 is associated to the frame.

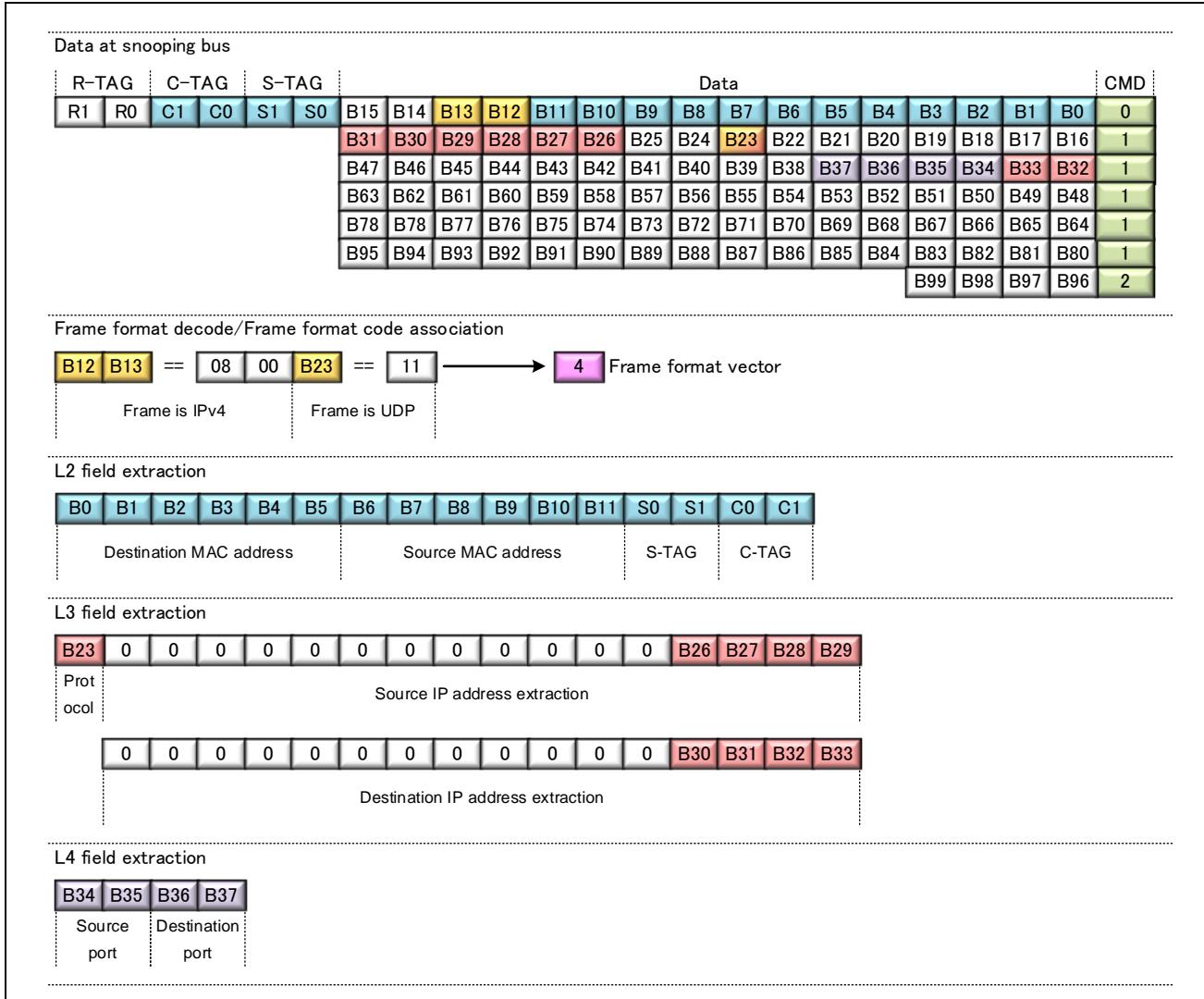


Fig 5.31: IPv4/UDP detection and data extraction

Function:

- The L4 extraction function takes in account the IPv4 HeaderLength (IHL) field. Fig 5.31 only describes the case where HeaderLength (IHL) is equal to 5 (default value). If HeaderLength (IHL) is less than 5, L4 field extraction is not supported.

(c) IPv4/TCP detection and data extraction

Fig 5.32 describes how IPv4/TCP detection and data extraction happens. This data extraction happens only if the frame format decode condition are satisfied and if **FWPC0i.IP4TEi** is set for the corresponding source port. In this case, a frame format vector [3] of 8 bits equal to 1'b1 is associated to the frame.

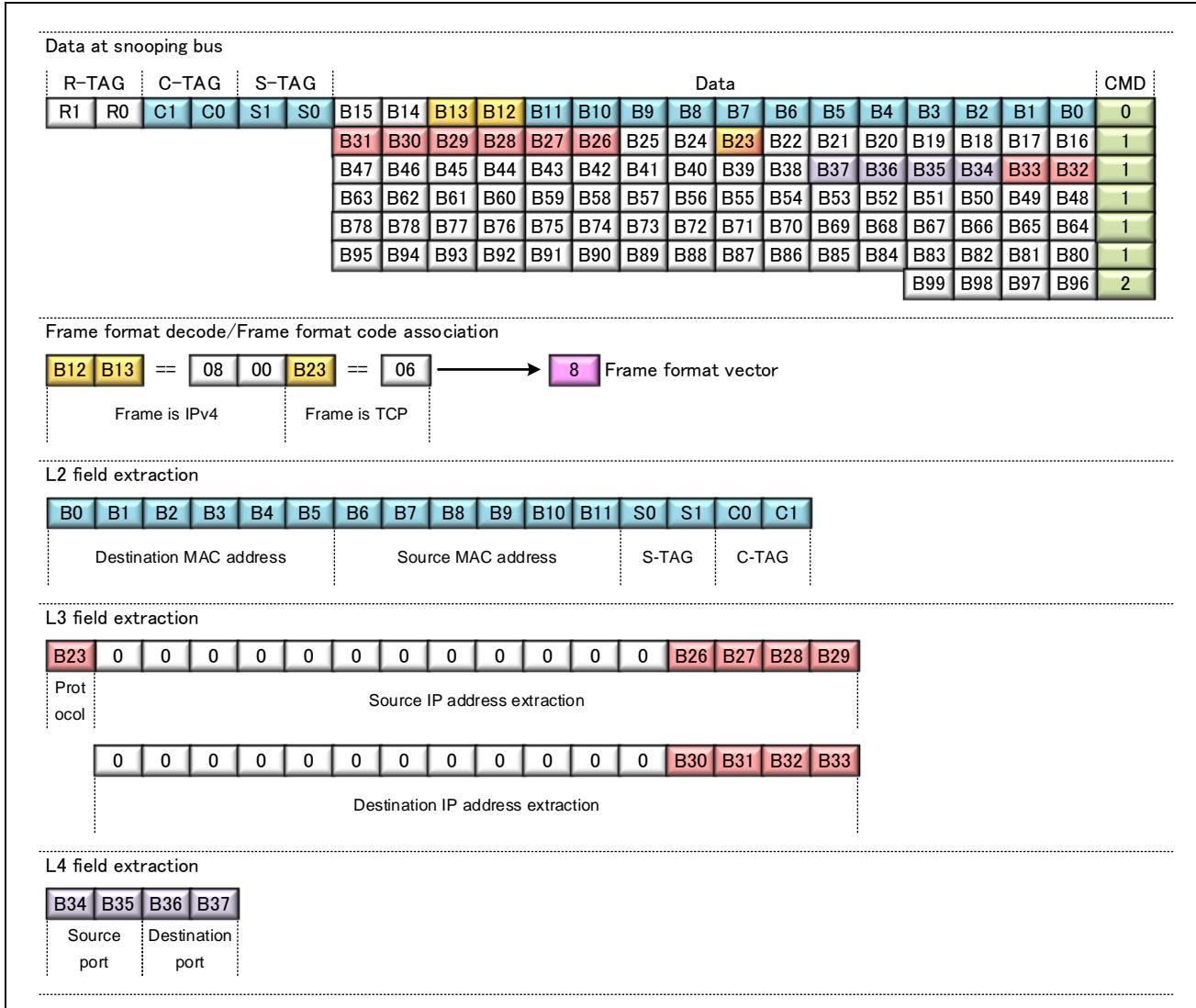


Fig 5.32: IPv4/TCP detection and data extraction

Function:

- The L4 extraction function takes in account the IPv4 HeaderLength (IHL) field. Fig 5.32 only describes the case where HeaderLength (IHL) is equal to 5 (default value). If HeaderLength (IHL) is less than 5, L4 field extraction is not supported.

(d) IPv6 detection and data extraction

Fig 5.33 describes how IPv6 detection and data extraction happens. This data extraction happens only if the frame format decode condition are satisfied and if **FWPC0i.IP6OEi** is set for the corresponding source port. In this case, a frame format vector [4] of 8 bits equal to 1'b1 is associated to the frame.

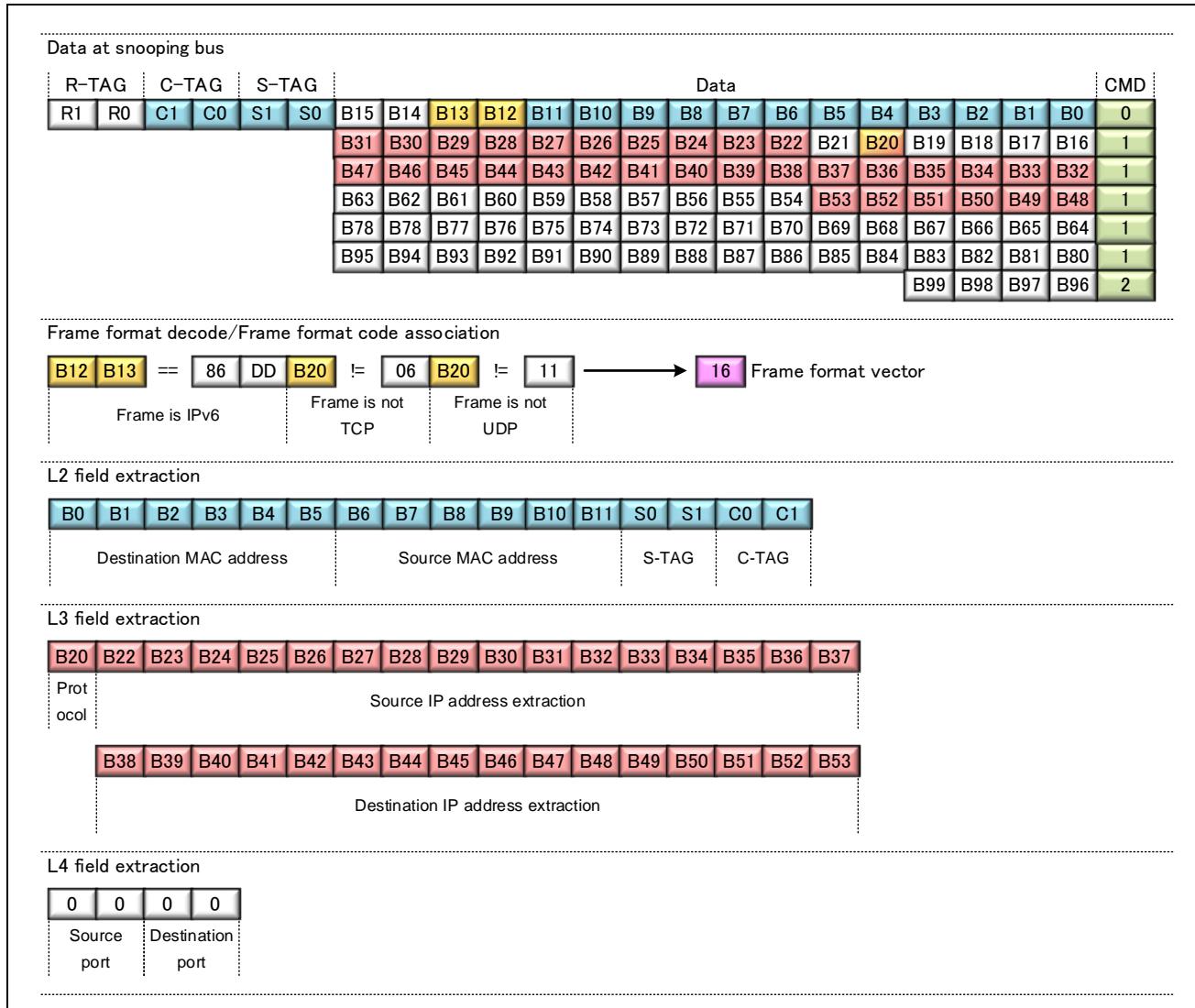


Fig 5.33: IPv6 detection and data extraction

(e) IPv6/UDP detection and data extraction

Fig 5.34 describes how IPv6/UDP detection and data extraction happens. This data extraction happens only if the frame format decode condition are satisfied and if **FWPC0i.IP6UEi** is set for the corresponding source port. In this case, a frame format vector [5] of 8 bits equal to 1'b1 associated to the frame.

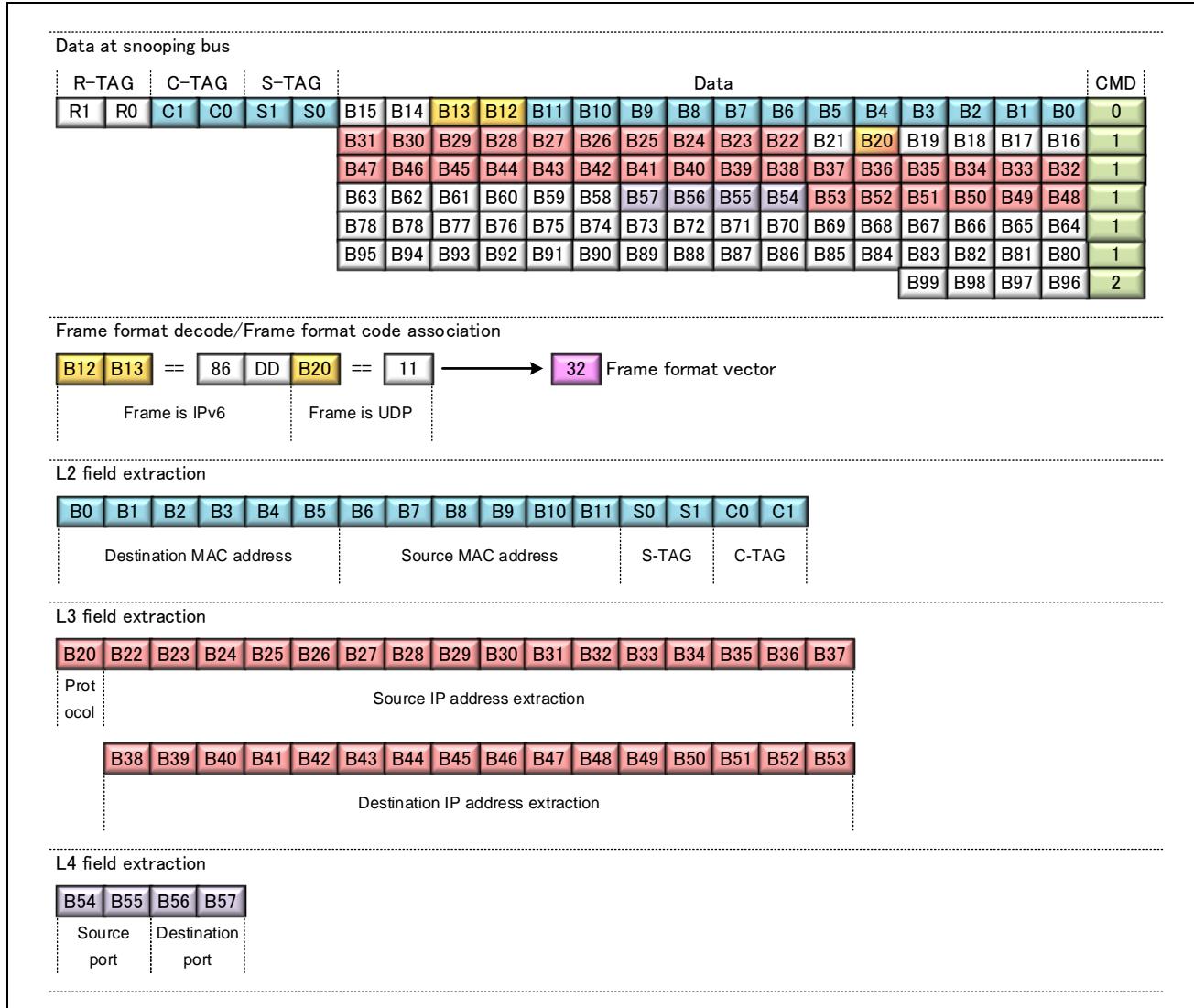


Fig 5.34: IPv6/UDP detection and data extraction

(f) IPv6/TCP detection and data extraction

Fig 5.35 describes how IPv6/TCP detection and data extraction happens. This data extraction happens only if the frame format decode condition are satisfied and if **FWPC0i.IP6TEi** is set for the corresponding source port. In this case, a frame format vector [6] of 8 bits equal to 1'b1 associated to the frame.

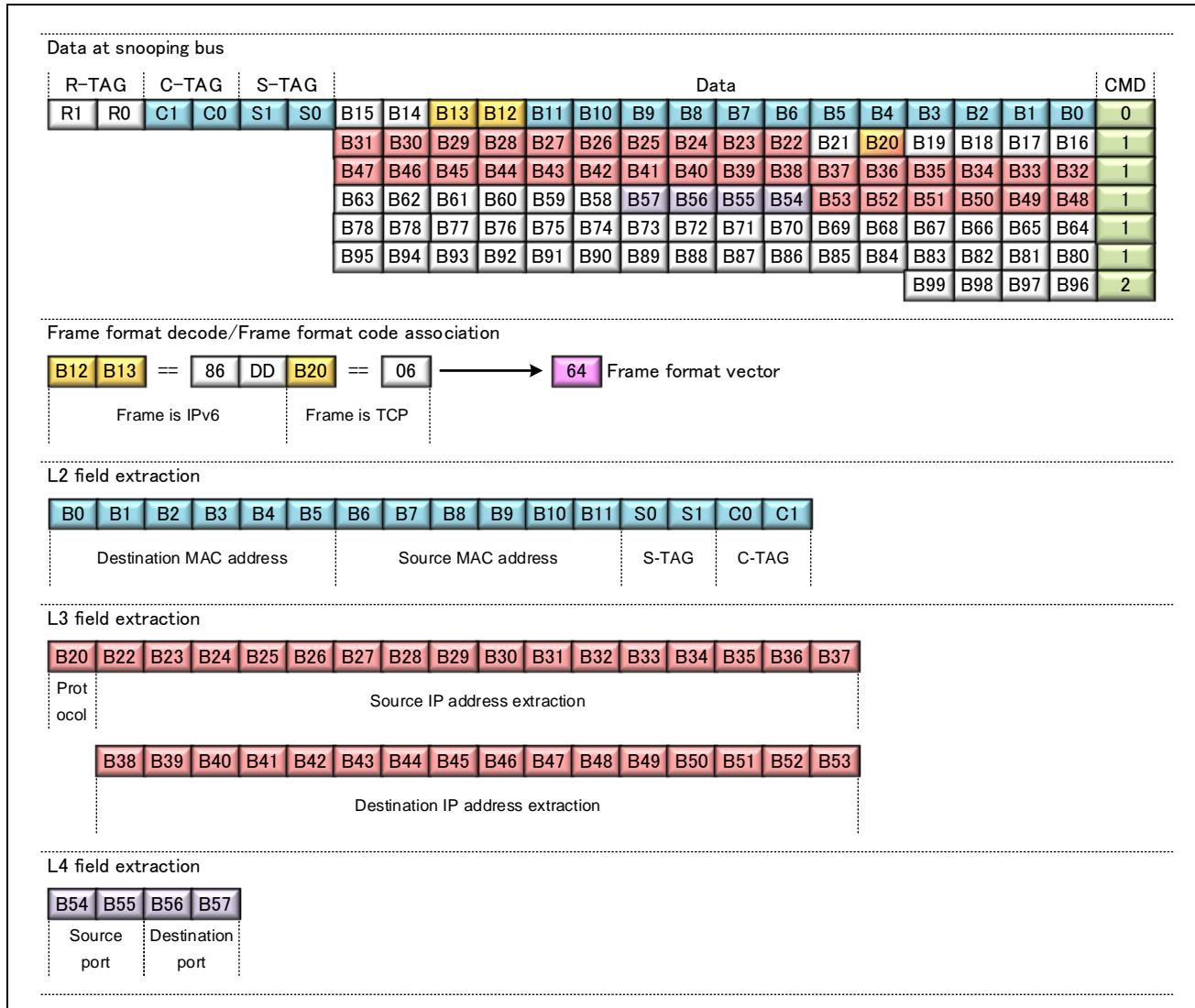


Fig 5.35: IPv6/TCP detection and data extraction

(2) Hash ID calculation

The Hash ID calculation is used to select the interesting fields for the Hash ID (security purpose) and to calculate the hash ID.

(a) Hash equation

Refer to **FWSFHEC** register explanation.

(b) IPv4 Hash ID calculation

The IPv4 Hash ID calculation is done depending on extracted fields in Hash extract. The calculation is described in Fig 5.36.



Fig 5.36: IPv4 Hash ID calculation

Functions:

- In Fig 5.36, The C-TAG and S-TAG masking is represented done at once, but masking is possible independently on PCP, DEI and VID.
- Setting all the field inclusion bits for Hash to 0 will fix the Hash ID to 0 in the stream (FWIP4SC.IP4IDPTH/IP4ISPTH/IP4IPH/IP4IIDH/IP4IISDH/IP4ICDH/IP4ICPH/IP4ICVH/IP4ISDH/IP4ISPH/IP4ISVH/IP4IMSH/IP4IMDH).
- Setting the hash equation to 0 will fix the Hash ID to 0 in the stream (FWSFHEC.IP4HE).

(c) IPv6 Hash ID calculation

The IPv6 Hash ID calculation is done depending on extracted fields in Hash extract. The calculation is described in Fig 5.37.

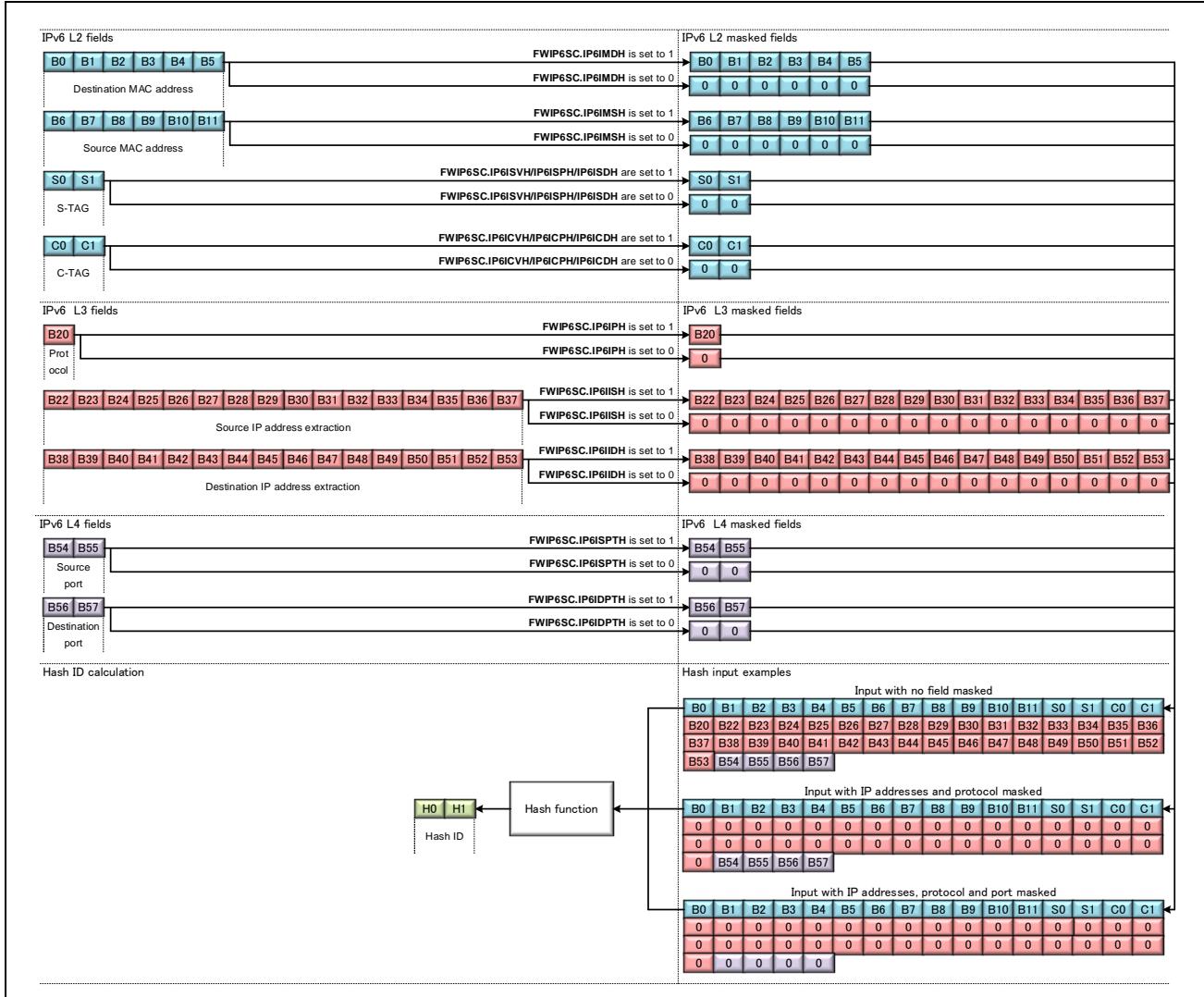


Fig 5.37: IPv6 Hash ID calculation

Functions:

- In Fig 5.37, The C-TAG and S-TAG masking is represented done at once, but masking is possible independently on PCP, DEI and VID.
- Setting all the field inclusion bits for Hash to 0 will fix the Hash ID to 0 in the stream (**FWIP6SC.IP6IDPTH/IP6ISPTH/IP6IPH/IP6IIDH/IP6IISH/IP6ICDH/IP6ICPH/IP6ICVH/IP6ISDH/IP6ISPH/IP6ISVH/IP6IMSH/IP6IMDH**)
- Setting the hash equation to 0 will fix the Hash ID to 0 in the stream (**FWSFHEC.IP6HE**)

(3) Stream ID creation

(a) IPv4 Stream ID creation

The IPv4 Stream ID is assembled from some of the extracted fields in L3 extract, the Hash ID calculated and the frame format vector. The stream ID creation is described in Fig 5.38.

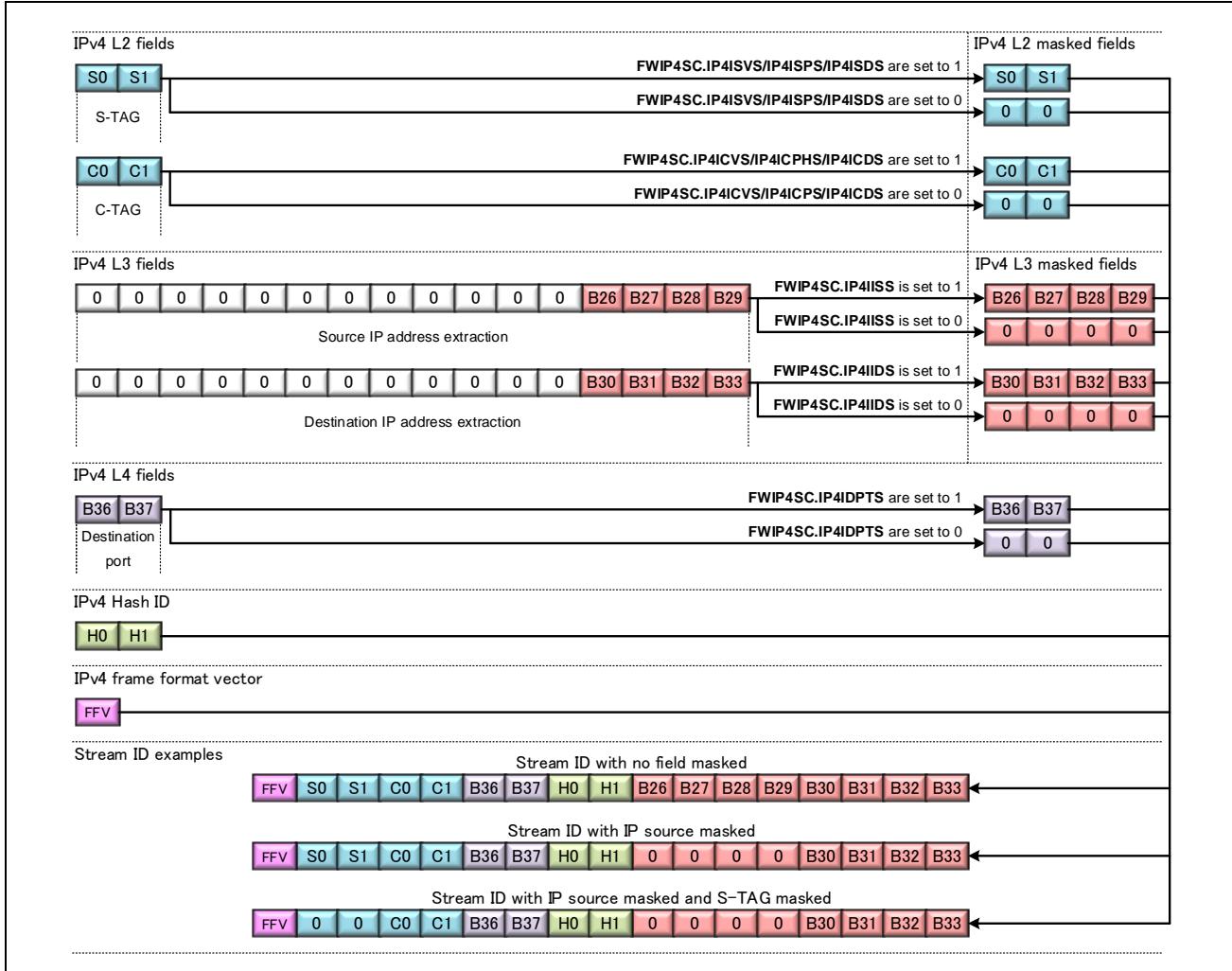


Fig 5.38: IPv4 Stream ID creation

Functions:

- In Fig 5.38, The C-TAG and S-TAG masking is represented done at once, but masking is possible independently on PCP, DEI and VID.
- The Stream ID field (FWLTHTL2-9) should be configured as 0 related to disabled part(bits) with "Stream in (FWIP4SC. IP4IDPTS/IP4IIDS/IP4ISSL/IP4ICDS/IP4ICPS/IP4ICVTS/IP4ISDS/IP4ISPS/IP4ISVS) = 0x0"

(b) IPv6 Stream ID creation

The IPv6 Stream ID is assembled from some of the extracted fields in L3 extract, the Hash ID calculated and the frame format vector. The stream ID creation is described in Fig 5.39.

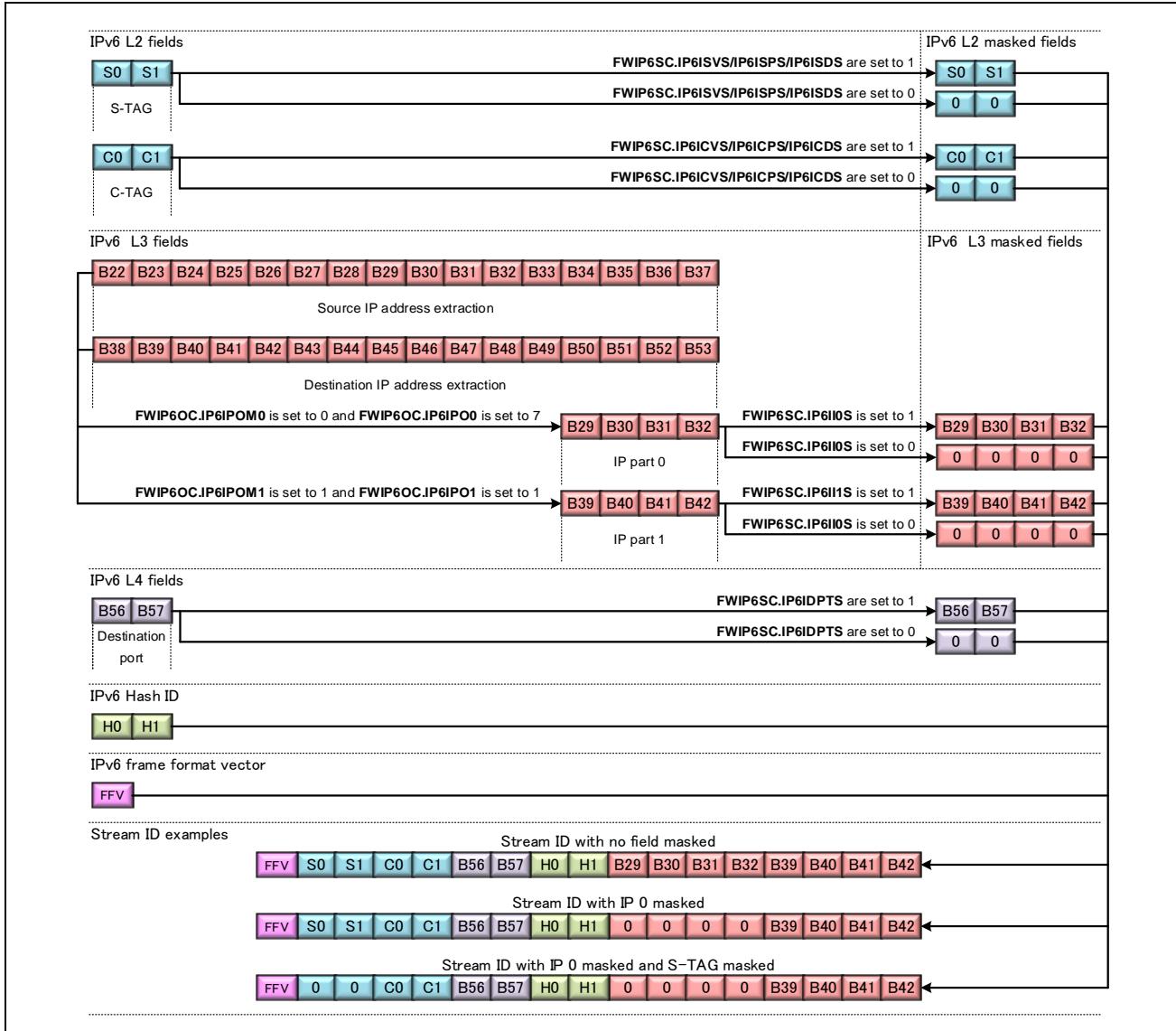


Fig 5.39: IPv6 Stream ID creation

Functions:

- In Fig 5.39, The C-TAG and S-TAG masking is represented done at once, but masking is possible independently on PCP, DEI and VID.
- In Fig 5.39, IP 0 is extracted from IPv6 source IP address and IP 1 is extracted from destination IP address, but it both can extract their 4 bytes from any of the IP addresses. This setting is done through **FWIP6OC** register.
- The Stream ID field (FWLTHTL2-9) should be configured as 0 related to disabled part(bits) with "Stream in (FWIP6SC. IP6IDPTS/IP6I1S/IP6I0S/IP6ICDS/IP6ICPS/IP6ICVS/IP6ISDS/IP6ISPS/IP6ISVS) = 0x0"

(4) Software Hash ID calculation

Because hash ID calculation is complex to implement in software, a hardware accelerator is available for hash ID calculation. Fig 5.40 gives software hash ID calculation examples.

IPv4 Data at snooping bus															SFR setting for IPv4							
R-TAG	C-TAG	S-TAG	Data												CMD	B0	B1	B2	B3			
R1	R0	C1	C0	S1	S0	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0
						B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16	1
						B47	B46	B45	B44	B43	B42	B41	B40	B39	B38	B37	B36	B35	B34	B33	B32	1
						B63	B62	B61	B60	B59	B58	B57	B56	B55	B54	B53	B52	B51	B50	B49	B48	1
						B78	B78	B77	B76	B75	B74	B73	B72	B71	B70	B69	B68	B67	B66	B65	B64	1
						B95	B94	B93	B92	B91	B90	B89	B88	B87	B86	B85	B84	B83	B82	B81	B80	1
																	B99	B98	B97	B96	2	

IPv6/TCP data at snooping bus															SFR setting for IPv6/TCP							
R-TAG	C-TAG	S-TAG	Data												CMD	B0	B1	B2	B3			
R1	R0	C1	C0	S1	S0	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0
						B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16	1
						B47	B46	B45	B44	B43	B42	B41	B40	B39	B38	B37	B36	B35	B34	B33	B32	1
						B63	B62	B61	B60	B59	B58	B57	B56	B55	B54	B53	B52	B51	B50	B49	B48	1
						B78	B78	B77	B76	B75	B74	B73	B72	B71	B70	B69	B68	B67	B66	B65	B64	1
						B95	B94	B93	B92	B91	B90	B89	B88	B87	B86	B85	B84	B83	B82	B81	B80	1
																	B99	B98	B97	B96	2	

Fig 5.40: Software hash ID calculation example

Restrictions:

- SW: For software hash ID calculation, the software should set to 0 the fields that are masked by the Hash ID calculation function.

5.2.5.3 L2 stream filter

The L2 stream filter is used to create a stream based on L2 fields. This stream creating happens only if **FWPC0i.L2SEI** is set for the corresponding source port. In this case, a frame format vector [7] of 8 bits equal to 1'b1s associated to the frame. Fig 5.41 describes how the L2 stream ID is created.

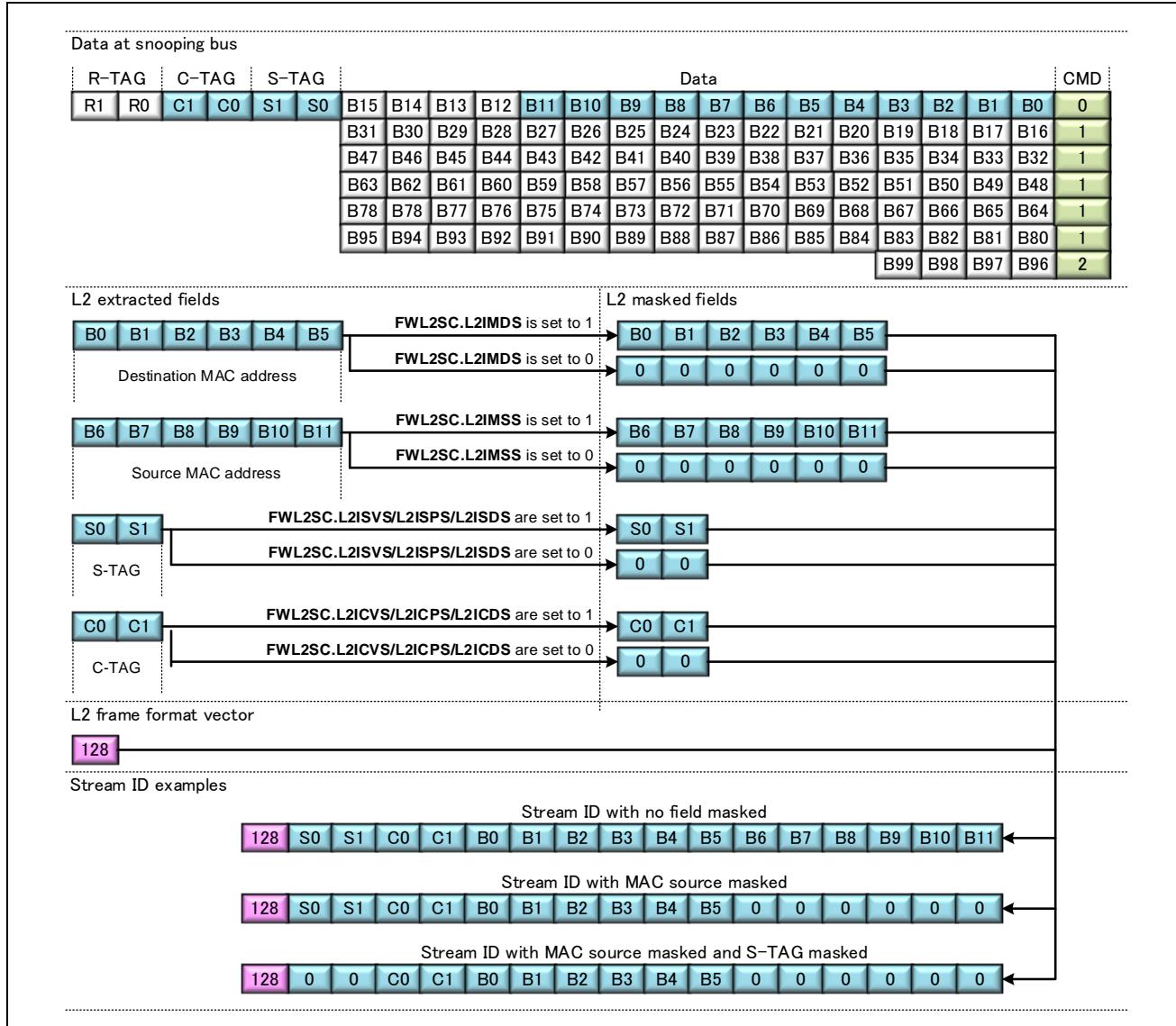


Fig 5.41: L2 stream ID creation

Functions:

- In Fig 5.41, The C-TAG and S-TAG masking is represented done at once, but masking is possible independently on PCP, DEI and VID.
- If several L2 stream filters match the same frame, the L2 stream filter with the highest entry number (learned address) will be selected.
- A frame which didn't match a cascade filter, an L3 stream filter or the L2 stream filter is considered an unknown frame.
- The Stream ID field (FWLTHTL2-9) should be configured as 0 related to disabled part(bits) with "Stream in (FWL2SC.L2ICDS/L2ICPS/L2ICVS/L2ISDS/L2ISPS/L2ISVS/L2IMSS/L2IMDS) = 0x0"

5.2.5.4 Layer 3 forwarding/routing/filtering table

L3 table aims at searching/learning/reading Cascade filter and L3/L2 stream table rules.

L3 table is divided in the following items:

- Rule format: Determines what information will be stored along with the stream ID in the table.
- SW Learning: Function to add/suppress an entry from the L3 table by software.
- SW Searching: Function to find the forwarding/routing/filtering information related to a stream by software.
- SW Reading: Function to read the entries in the L3 table by software.
- HW searching: Function to find the forwarding/routing/filtering information related to a stream by forwarding mechanism.

(1) Rule format

The L3 table is used to store L3 rules. A L3 rule contains the information the frame forwarding, routing and filtering. Perfect with AL=0, L3 stream and L2 stream fields in this table, if quoted, will be written **L3.{Field name}**. Perfect with AL=1 fields in this table, if quoted, will be written **AL.{Field name}**. Table 5-24 describes fields contained in a L3 rule. If FWPC1i.BLEi is enabled and FDESCR.BL=1, then only FDESCR.SL and FDESCR.SLV[i] are valid for Block list filter.

Table 5-24: L3 rule format

Field name	Field size (bit)	Field Explanation
EV	1	<p>Entry Valid</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Entry is not valid - 1'b1: Entry is valid
SID	136	Stream ID of the entry. The stream ID is created in perfect filter or L3/L2 stream filter (respectively refer to section 5.2.5.1(5), section 5.2.5.2(3) and section 5.2.5.3)
SIDM	128	<p>Stream ID compare mask of the entry for forwarding and SW search. The stream ID mask is created in L3/L2 stream filter.</p> <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: This bit cannot be enabled by "Perfect filter".
SL	1	<p>Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Entry is unsecure - 1'b1: Entry is secure
FP	4	<p>Filtering Priority</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: Priority for filtering (MSDU, GATE and Meter) arbitration. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If FWGC.FPM is 1'b1, this value is invalid. (not use Filtering Priority, use Routing Priority) - HW: If AL is 1'b1, this is invalid. - HW: If BL is 1'b1, this is invalid.
RP	4	<p>Routing Priority</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: Priority for forwarding/routing arbitration. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If AL is 1'b1, this is invalid. - HW: If BL is 1'b1, this is invalid.
AL	1	<p>Acceptance List</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: This entry will be used by forwarding/routing. - 1'b1: This entry will be used by filtering as follow. <p>Frames from source port i matching this entry will be accepted (not filtered) by Acceptance list filtering if FWPC1i.PFALEi[0] == 1'b1.</p> <p>Frames for destination port i matching this entry will be accepted (not filtered) by Acceptance list filtering if FWPC1i.PFALEi[1] == 1'b1.</p> <p>This bit will be no functions if FWPC1i.PFALEi[1:0] == 2'b00. (All frames will be not filtered by Acceptance list filtering.)</p> <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: This bit can only be enabled only "Perfect filter".

Field name	Field size (bit)	Field Explanation
BL	1	<p>Block List</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: No function. - 1'b1: Frames from source port i matching this entry will be filtered by Block list filtering if FWPC1i.PFBLE == 1'b1. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If AL is 1'b1, this is invalid.
MSDUV	1	<p>MSDU Valid</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Frames matching this entry will be ignored by PSFP MSDU filter. - 1'b1: If AL is 1'b0, Frames matching this entry will be processed by PSFP MSDU filter. <p>If AL is 1'b1, FDESCR.MSDUV will be set to 1'b1 and FDESCR.MSDUN will be overwritten with AL.MSDUN. However, Secure descriptors(FDESCR.SL=1) will not be overwritten by Unsecure descriptors(AL.SL=0).</p> <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
MSDUN	PSFP_MSDU_W	<p>MSDU Number</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: If corresponding entry L3.MSDUV value is set to 1, frames matching this entry will be processed by PSFP MSDU filter number L3.MSDUN. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
GATEV	1	<p>GATE Valid</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Frames matching this entry will be ignored by PSFP Gate filter. - 1'b1: If AL is 1'b0, Frames matching this entry will be processed by PSFP Gate filter. <p>If AL is 1'b1, FDESCR.GATEV will be set to 1'b1 and FDESCR.GATEN will be overwritten with AL.GATEN. However, Secure descriptors(FDESCR.SL=1) will not be overwritten by Unsecure descriptors(AL.SL=0).</p> <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
GATEN	PSFP_GATE_W	<p>GATE Number</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: If corresponding entry L3.GATEV value is set to 1, frames matching this entry will be processed by PSFP Gate filter number L3.GATEN. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
MTRV	1	<p>MeTeR Valid</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Frames matching this entry will be ignored by PSFP Meter filter. - 1'b1: If AL is 1'b0, Frames matching this entry will be processed by PSFP Meter filter. <p>If AL is 1'b1, FDESCR.MTRV will be set to 1'b1 and FDESCR.MTRN will be overwritten with AL.MTRN. However, Secure descriptors(FDESCR.SL=1) will not be overwritten by Unsecure descriptors(AL.SL=0).</p> <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.

Field name	Field size (bit)	Field Explanation
MTRN	PSFP_MTR_W	<p>MeTeR Number</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: If corresponding entry L3.MTRV value is set to 1, frames matching this entry will be processed by PSFP MSDU filter number L3.MTRN. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
FRERV	1	<p>FRER Valid</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Frames matching this entry will be ignored by FRER individual recovery. - 1'b1: If AL is 1'b0, Frames matching this entry will be processed by FRER individual recovery. <p>If AL is 1'b1, FDESCR.FRERV will be set to 1'b1 and FDESCR.FRERN will be overwritten with AL.FRERN. However, Secure descriptors(FDESCR.SL=1) will not be overwritten by Unsecure descriptors(AL.SL=0).</p> <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
FRERN	FRER_RECE_W	<p>FRER Number</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: If corresponding entry L3.FRERV value is set to 1, frames matching this entry will be processed by FRER entry number L3.FRERN for individual recovery. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
HLD	1	<p>Hardware Learn Disable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Source MAC hardware learning is enabled. - 1'b1: If AL is 1'b0, Source MAC hardware learning is disabled. <p>If AL is 1'b1, FDESCR.HLD will be set to 1'b1. However, Secure descriptors(FDESCR.SL=1) will not be overwritten by Unsecure descriptors(AL.SL=0).</p> <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
RV	1	<p>Routing Valid</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Frames matching this entry will be ignored by routing. - 1'b1: If AL is 1'b0, Frames matching this entry will be processed by routing. <p>If AL is 1'b1, FDESCR.RV will be set to 1'b1 and FDESCR.RN will be overwritten with AL.RN. However, Secure descriptors(FDESCR.SL=1) will not be overwritten by Unsecure descriptors(AL.SL=0).</p> <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
RN	LTH_RRULE_W	<p>Routing Number</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: If corresponding entry L3.RV value is set to 1, frames matching this entry will be processed by routing rule number L3.RN. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.

Field name	Field size (bit)	Field Explanation
SLV	PORT_N	<p>Source Lock Vector</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Frames matching this entry coming from source port i are rejected by source port lock error. - Bit i set to 1'b1: Frames matching this entry coming from source port i are forwarded/routed. <p>Notes:</p> <ul style="list-style-type: none"> - This value will be enabling for rules per input port for "Forwarding rule", "Acceptance list" and "Block list" - This value will be enabling for rules per input port for "Overwrite function" - This function will be used by Acceptance list filtering with FWPC1i.PFALEi[0] == 1'b1.
DLV	PORT_N	<p>Destination Lock Vector (for acceptance list filtering only)</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Frames matching this entry forwarding for destination port i are rejected by acceptance list filtering. - Bit i set to 1'b1: Frames matching this entry forwarding for destination port i are forwarded/routed. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: This bit is only present in "Perfect filter". - HW: If AL is 1'b0, this is invalid. <p>Notes:</p> <ul style="list-style-type: none"> - This value will be enabling for rules per output port for "Acceptance list". - This function will be used by Acceptance list filtering with FWPC1i.PFALEi[1] == 1'b1.
DV	PORT_N	<p>Destination Vector</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: If AL is 1'b0, ports to where the frame should be sent. - HW: If AL is 1'b1 and AL.DV is all 0, no functions. - If AL is 1'b1 and AL.DV is not all 0, FDESCR.DV will be overwritten with this value (AL.DV). However, Secure descriptors (FDESCR.SL=1) will not be overwritten by Unsecure descriptors (AL.SL=0). <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
CSD	PORT_GWCA_N* AXI_CHAIN_W	<p>CPU Sub-Destinations</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: If AL is 1'b0, CPU Sub-Destinations the frame should be sent. - HW: If AL is 1'b1 and AL.DV is all 0, no functions. - If AL is 1'b1 and AL.DV is not all 0, FDESCR.CSD will be overwritten with this value (AL.DV). However, Secure descriptors (FDESCR.SL=1) will not be overwritten by Unsecure descriptors (AL.SL=0). <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
CME	1	<p>CPU Mirroring Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: CPU mirroring is disabled. - 1'b1: If AL is 1'b0, CPU mirroring is enabled. <p>If AL is 1'b1, FDESCR.CME will be set to 1'b1. However, Secure descriptors (FDESCR.SL=1) will not be overwritten by Unsecure descriptors (AL.SL=0).</p> <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.

Field name	Field size (bit)	Field Explanation
EME	1	<p>Ethernet Mirroring Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Ethernet mirroring is disabled. - 1'b1: If AL is 1'b0, Ethernet mirroring is enabled. <p>If AL is 1'b1, FDESCR.EME will be set to 1'b1. However, Secure descriptors(FDESCR.SL=1) will not be overwritten by Unsecure descriptors(AL.SL=0).</p> <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
IPU	1	<p>Internal Priority Update</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Frames matching this entry will not have their internal priority updated. - 1'b1: If AL is 1'b0, frames matching this entry will have their internal priority updated. <p>If AL is 1'b1, FDESCR.IPU will be set to 1'b1 and FDESCR.IPV will be overwritten with AL.IPV. However, Secure descriptors(FDESCR.SL=1) will not be overwritten by Unsecure descriptors(AL.SL=0).</p> <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
IPV	3	<p>Internal Priority Value</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: If corresponding entry L3.IPU value is set to 1, frames matching this entry will have their priority updated to L3.IPV. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.

(2) SW Learning

Learning is used to add/remove an entry in the L3 table. Table 5-25 describes register used to learn a stream ID in the Layer 3 table. Table 5-26 describes the learn results.

Table 5-25: L3 learn registers

Register name	Field name/corresponding field in L3 table	Field explanation
Perfect filter table: {FWLTHTL2.LTHSLP1, FWLTHTL3.LTHSLP2, FWLTHTL4.LTHSLP3, FWLTHTL5.LTHSLP4} L3/L2 stream filter table: FWLTHTL0.LTHELA	L3 table address	Not present in L3 table because this is table address.
FWLTHTL1.LTHED	Entry delete	Not present in L3 table, used to select between learning an entry and deleting an entry
FWLTHTL1.LTHFPL	L3.FP	Refer to section 5.2.5.4(1)
FWLTHTL1.LTHRPL	L3.RP	Refer to section 5.2.5.4(1)
Perfect filter table: If ({FWLTHTL2.LTHSLP1, FWLTHTL3.LTHSLP2, FWLTHTL4.LTHSLP3, FWLTHTL5.LTHSLP4} > FWLTHTEC0.PFFALA) or (FWLTHTEC0.PFFALAA == 1'b1), set to 1'b1 If ({FWLTHTL2.LTHSLP1, FWLTHTL3.LTHSLP2, FWLTHTL4.LTHSLP3, FWLTHTL5.LTHSLP4} <= FWLTHTEC0.PFFALA) and (FWLTHTEC0.PFFALAA == 1'b0), set to 1'b0 L3/L2 stream filter table: None (be fixed to 0)	L3.AL	Refer to section 5.2.5.4(1)
FWLTHTL1.LTHBLL	L3.BL	Refer to section 5.2.5.4(1)
FWLTHTL1.LTHHLDL	L3.HLD	Refer to section 5.2.5.4(1)
Perfect filter table: ~FWSCRCA.CFRSL[{FWLTHTL2.LTHSLP1, FWLTHTL3.LTHSLP2, FWLTHTL4.LTHSLP3, FWLTHTL5.LTHSLP4}] L3/L2 stream filter table: FWLTHTL0.LTHELA >= FWLTHTEC1.LTHTUENC	L3.SL	Refer to section 5.2.5.4(1)
{FWLTHTL1.LTHSLP0, FWLTHTL2.LTHSLP1, FWLTHTL3.LTHSLP2, FWLTHTL4.LTHSLP3, FWLTHTL5.LTHSLP4}	L3.SID	Refer to section 5.2.5.4(1)
{FWLTHTL6.LTHSMLP0, FWLTHTL7.LTHSMLP1, FWLTHTL8.LTHSMLP2, FWLTHTL9.LTHSMLP3}	L3.SIDM	Refer to section 5.2.5.4(1)
FWLTHTL10.LTHMSDUVL	L3.MSDUV	Refer to section 5.2.5.4(1)
FWLTHTL10.LTHMSDUNL	L3.MSDUN	Refer to section 5.2.5.4(1)
FWLTHTL10.LTHGATEVL	L3.GATEV	Refer to section 5.2.5.4(1)
FWLTHTL10.LTHGATENL	L3.GATEN	Refer to section 5.2.5.4(1)
FWLTHTL11.LTHMTRVL	L3.MTRV	Refer to section 5.2.5.4(1)
FWLTHTL11.LTHMTRNL	L3.MTRN	Refer to section 5.2.5.4(1)
FWLTHTL11.LTHFRERVL	L3.FRERV	Refer to section 5.2.5.4(1)
FWLTHTL11.LTHFRERNL	L3.FRERN	Refer to section 5.2.5.4(1)
FWLTHTL12.LTHRVL	L3.RV	Refer to section 5.2.5.4(1)

Register name	Field name/corresponding field in I3 table	Field explanation
FWLTHTL12.LTHRNL	L3.RN	Refer to section 5.2.5.4(1)
FWLTHTL12.LTHSLVL	L3.SLV	Refer to section 5.2.5.4(1)
FWLTHTL13i.LTHCSDLi	L3.CSD[AXI_CHAIN_W*(i+1)-1:AXI_CHAIN_W*i]	Refer to section 5.2.5.4(1)
FWLTHTL14.LTHDVL	L3.DV	Refer to section 5.2.5.4(1)
FWLTHTL14.LTHCMEL	L3.CME	Refer to section 5.2.5.4(1)
FWLTHTL14.LTHEMEL	L3.EME	Refer to section 5.2.5.4(1)
FWLTHTL14.LTHIPUL	L3.IPU	Refer to section 5.2.5.4(1)
FWLTHTL14.LTHIPVUL	L3.IPV	Refer to section 5.2.5.4(1)
FWLTHTL15.LTHDLVL	L3.DLV	Refer to section 5.2.5.4(1)

Table 5-26: L3 learn result

Register name	Field name/corresponding field in I3 table	Field explanation
FWLTHTLR.LTHLF	Learning fail	Learning fail with happen in one of the following conditions: - The Layer 3 table is not ready (FWLTHTIM.LTHTR is not set)
FWLTHTLR.LTHLSF	Learning security fail	Security fail with happen in one of the following conditions: - [Perfect filter table] The learn action is done by the unsecure APB and the corresponding entry for learning is a table of secure area (FWSCRCA.CFRSL [{ FWLTHTL2.LTHSLP1 , FWLTHTL3.LTHSLP2 , FWLTHTL4.LTHSLP3 , FWLTHTL5.LTHSLP4}]) is set to 1'b0). - [L3/L2 stream table] The learn action is done by the unsecure APB and the corresponding entry for learning is already in the table and is a secure area (FWLTHTL0.LTHELA >= FWLTHTEC1.LTHTUENC is set).
FWLTHTLR.LTHLEF	Learning ECC fail	ECC fail with happen in one of the following conditions: - [Perfect filter table] When an ECC error happens while learning an entry. The learning algorithm learns entries such a way that the algorithm will never be broken by an ECC error. Some entries will be unreachable because of the ECC error and be considered as not found while being searched but most of the entries will still operate normally. - [L3/L2 stream table] No ECC error happens.
FWLTHTLR.LTHLOF	Learning overwrite fail	Overwrite fail with happen in one of the following conditions: - This learn failed because it tried to overwrite an existing Entry.

(3) SW Searching

Searching is used to find the information related to a stream ID. Table 5-27 describes register used to search a stream ID in the Layer 3 table. Table 5-28 describes the search results.

Table 5-27: L3 search registers

Register name	Field name/corresponding field in I3 table	Field explanation
{ FWLHTS0.LTHSSP0 , FWLHTS1.LTHSSP1 , FWLHTS2.LTHSSP2 , FWLHTS3.LTHSSP3 , FWLHTS4.LTHSSP4} }	L3.SID	Refer to section 5.2.5.4(1)

Table 5-28: L3 search result

Register name	Field name/corresponding field in I3 table	Field explanation
FWLHTSR0.LTHFPS	L3.FP	Refer to section 5.2.5.4(1)
FWLHTSR0.LTHRPS	L3.RP	Refer to section 5.2.5.4(1)
Perfect filter table: FWLHTSR6.LTHMCHAS > FWLTHTEC0.PFFALA	L3.AL	Refer to section 5.2.5.4(1)
L3/L2 stream filter table: None (be fixed to 0)		
FWLHTSR0.LTHBLS	L3.BL	Refer to section 5.2.5.4(1)
FWLHTSR0.LTHHLDs	L3.HLD	Refer to section 5.2.5.4(1)
FWLHTSR0.LTHSLS	L3.SL	Refer to section 5.2.5.4(1)
FWLHTSR0.LTHSNF	Search not found	Search failed because the searched stream ID is not in the table
FWLHTSR0.LTHSEF	Search ECC Fail	Search failed because of an ECC error

Register name	Field name/corresponding field in L3 table	Field explanation
FWLHTTSR1.LTHMSDUVS	L3.MSDUV	Refer to section 5.2.5.4(1)
FWLHTTSR1.LTHMSDUNS	L3.MSDUN	Refer to section 5.2.5.4(1)
FWLHTTSR1.LTHGATEVS	L3.GATEV	Refer to section 5.2.5.4(1)
FWLHTTSR1.LTHGATENS	L3.GATEN	Refer to section 5.2.5.4(1)
FWLHTTSR2.LTHMTRVS	L3.MTRV	Refer to section 5.2.5.4(1)
FWLHTTSR2.LTHMTRNS	L3.MTRN	Refer to section 5.2.5.4(1)
FWLHTTSR3.LTHFRERVS	L3.FRERV	Refer to section 5.2.5.4(1)
FWLHTTSR3.LTHFRERNNS	L3.FRERN	Refer to section 5.2.5.4(1)
FWLHTTSR3.LTHSLVS	L3.SLV	Refer to section 5.2.5.4(1)
FWLHTTSR3.LTHRVS	L3.RV	Refer to section 5.2.5.4(1)
FWLHTTSR3.LTHRNS	L3.RN	Refer to section 5.2.5.4(1)
FWLHTTSR4i.LTHCSDSi	L3.CSD[AXI_CHAIN_W*(i+1)-1:AXI_CHAIN_W*i]	Refer to section 5.2.5.4(1)
FWLHTTSR5.LTHDVS	L3.DV	Refer to section 5.2.5.4(1)
FWLHTTSR5.LTHCMES	L3.CME	Refer to section 5.2.5.4(1)
FWLHTTSR5.LTHEMES	L3.EME	Refer to section 5.2.5.4(1)
FWLHTTSR5.LTHIPUS	L3.IPU	Refer to section 5.2.5.4(1)
FWLHTTSR5.LTHIPVS	L3.IPV	Refer to section 5.2.5.4(1)
FWLHTTSR6.LTHDLVS	L3.DLV	Refer to section 5.2.5.4(1)
FWLHTTSR7.LTHMCHAS	L3 table address (Address with the highest number in the range FWLHTTS5.LTHTSSA to FWLHTTS5.LTHTSEA)	Not present in L3 table because this is table address.

Restrictions:

- HW: If the unsecure APB accesses to a secure entry for searching, It will be not found.

(4) SW Reading

Reading is used to dump the Layer 3 table content. This function cannot be used to read a specific entry because it is not possible for the software to know at which address an entry can be found in the Layer 3 RAM. Table 5-29 describes register used to read an entry in the Layer 3 table. Table 5-30 describes the read results.

Table 5-29: L3 read registers

Register name	Field name/corresponding field in I3 table	Field explanation
FWLTHTR.LTHSRS	Read select	Select that Perfect table or L3/L2 stream table.
FWLTHTR.LTHAR	L3 table Read address	Address that will be used to read an entry in the Layer 3 table

Table 5-30: L3 read result

Register name	Field name/corresponding field in I3 table	Field explanation
FWLTHTRR0.LTHREF	Read ECC fail	Read failed because of an ECC error
FWLTHTRR0.LTHEVR	L3.EV	The read address holds a valid entry Only if this bit is set when reading an address, the corresponding entry and the following registers in this table are valid. Refer to section 5.2.5.4(1)
FWLTHTRR1.LTHFPR	L3.FP	Refer to section 5.2.5.4(1)
FWLTHTRR1.LTHRPR	L3.RP	Refer to section 5.2.5.4(1)
Perfect filter table: FWLTHTR.LTHAR > FWLTHTEC0.PFFALA	L3.AL	Refer to section 5.2.5.4(1)
L3/L2 stream filter table: None (be fixed to 0)		
FWLTHTRR1.LTHBLR	L3.BL	Refer to section 5.2.5.4(1)
FWLTHTRR1.LTHHLDR	L3.HLD	Refer to section 5.2.5.4(1)
FWLTHTRR1.LTHSLR	L3.SL	Refer to section 5.2.5.4(1)
{FWLTHTRR1.LTHSRP0, FWLTHTRR2.LTHSRP1, FWLTHTRR3.LTHSRP2, FWLTHTRR4.LTHSRP3, FWLTHTRR5.LTHSRP4}	L3.SID	Refer to section 5.2.5.4(1)
{FWLTHTRR6.LTHSMRP0, FWLTHTRR7.LTHSMRP1, FWLTHTRR8.LTHSMRP2, FWLTHTRR9.LTHSMRP3}	L3.SIDM	Refer to section 5.2.5.4(1)
FWLTHTRR10.LTHMSDUVR	L3.MSDUV	Refer to section 5.2.5.4(1)
FWLTHTRR10.LTHMSDUNR	L3.MSDUN	Refer to section 5.2.5.4(1)
FWLTHTRR10.LTHGATEVR	L3.GATEV	Refer to section 5.2.5.4(1)
FWLTHTRR10.LTHGATENR	L3.GATEN	Refer to section 5.2.5.4(1)
FWLTHTRR11.LTHMTRVR	L3.MTRV	Refer to section 5.2.5.4(1)
FWLTHTRR11.LTHMTRNR	L3.MTRN	Refer to section 5.2.5.4(1)
FWLTHTRR11.LTHFRERVR	L3.FRERV	Refer to section 5.2.5.4(1)
FWLTHTRR11.LTHFRERNR	L3.FRERN	Refer to section 5.2.5.4(1)
FWLTHTRR12.LTHSLVR	L3.SLV	Refer to section 5.2.5.4(1)
FWLTHTRR12.LTHRVR	L3.RV	Refer to section 5.2.5.4(1)

Register name	Field name/corresponding field in I3 table	Field explanation
FWLTHTRR12.LTHRNR	L3.RN	Refer to section 5.2.5.4(1)
FWLTHTRR13i.LTHCSDRI	L3.CSD[AXI_CHAIN_W*(i+1)-1:AXI_CHAIN_W*i]	Refer to section 5.2.5.4(1)
FWLTHTRR14.LTHDVR	L3.DV	Refer to section 5.2.5.4(1)
FWLTHTRR15.LTHDLVR	L3.DLV	Refer to section 5.2.5.4(1)
FWLTHTRR10.LTHCMER	L3.CME	Refer to section 5.2.5.4(1)
FWLTHTRR10.LTHEMER	L3.EME	Refer to section 5.2.5.4(1)
FWLTHTRR10.LTHIPUR	L3.IPU	Refer to section 5.2.5.4(1)
FWLTHTRR10.LTHIPVR	L3.IPV	Refer to section 5.2.5.4(1)

Restrictions:

- HW: If the unsecure APB accesses to a secure entry for reading, the read will return all0 for read fields.

5.2.5.5 Layer 3 forwarding/routing/filtering

Layer 3 forwarding/routing/filtering is used to forward local ethernet descriptors (**LDESCR.FMT** [GWCA] set to 1'b0) received from agents using **FWPC0i/FWPC1i** and **FWCEPRC2** register and can be monitored using **FWEIS0i** interrupt register. Layer 3 forwarding/routing/filtering searches received valid stream IDs (section 5.2.5.1(5), section 5.2.5.2(3)(a) and section 5.2.5.2(3)(b)) in the layer 3 table to extract corresponding entry fields (section 5.2.5.4(1)). Depending on the entry fields, Layer 3 forwarding/routing/filtering will forward/route/filter frames following Layer 3 forwarding/routing secure flow in Fig 5.42, Layer 3 forwarding/routing unsecure flow in Fig 5.43 and Layer 3 filtering flow in Fig 5.60.

Functions:

- **FWPC0i.LTHTAI** register is used to activate layer 3 table for frames received from port i.
- **FWPC0i.LTHTDDMi** register is used to disable “L3 stream filter” (not Perfect filter and L2 stream filter) for frames received from port i with Destination MAC address NOT matched Port MAC address as in [RMAC] and [GWCA].
- **FWPC0i.LTHRUSi** register is used to reject unknown streams received from port i.
- **FWPC0i.LTHRUSSI** register is used to reject secure unknown streams received from port i.
- **FWPC1i.LTHFMI** register is used to set to which ports frames received from port i can be forwarded.
- **FWCEPRC2** register enables exceptional path for error descriptors.
- **FWEIS0** interrupt register notifies that an ethernet descriptor has been rejected because of an error.
- **FWGC.LTHUFRP** register is used to setting filtering priority. If in case “L3 stream forwarding and L2 stream filtering” or “L3 stream filtering and L2 stream forwarding” happens together in a same frame with same RP value in both case (**L3S.RP/L2S.RP == FWGC.LTHUFRP**), filtering will get the priority.

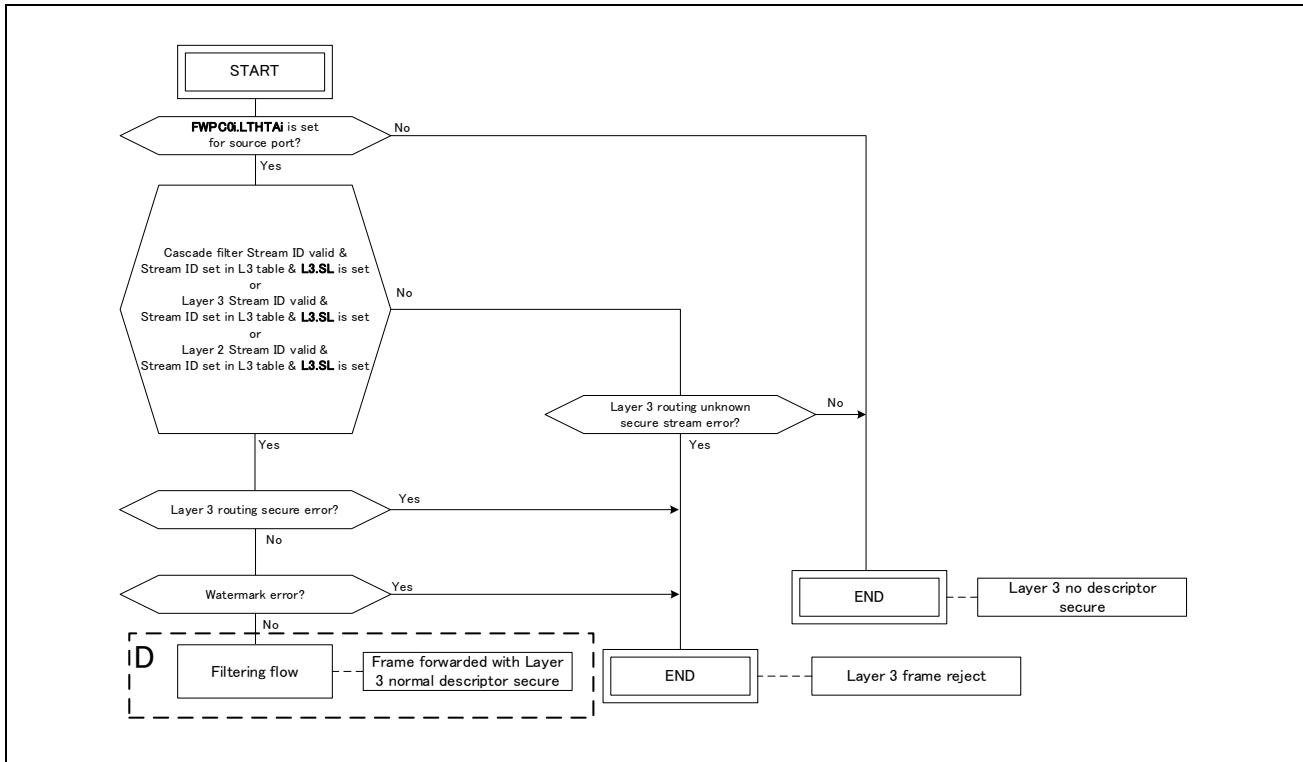


Fig 5.42: Layer 3 forwarding/routing secure flow

Notes:

- Layer 3 routing secure errors and Layer 3 routing unknown secure stream errors are described in section 5.2.5.5(1).
- Watermark errors are described in section 5.1.6(1).
- Link D links to Fig 5.59: Filtering flow

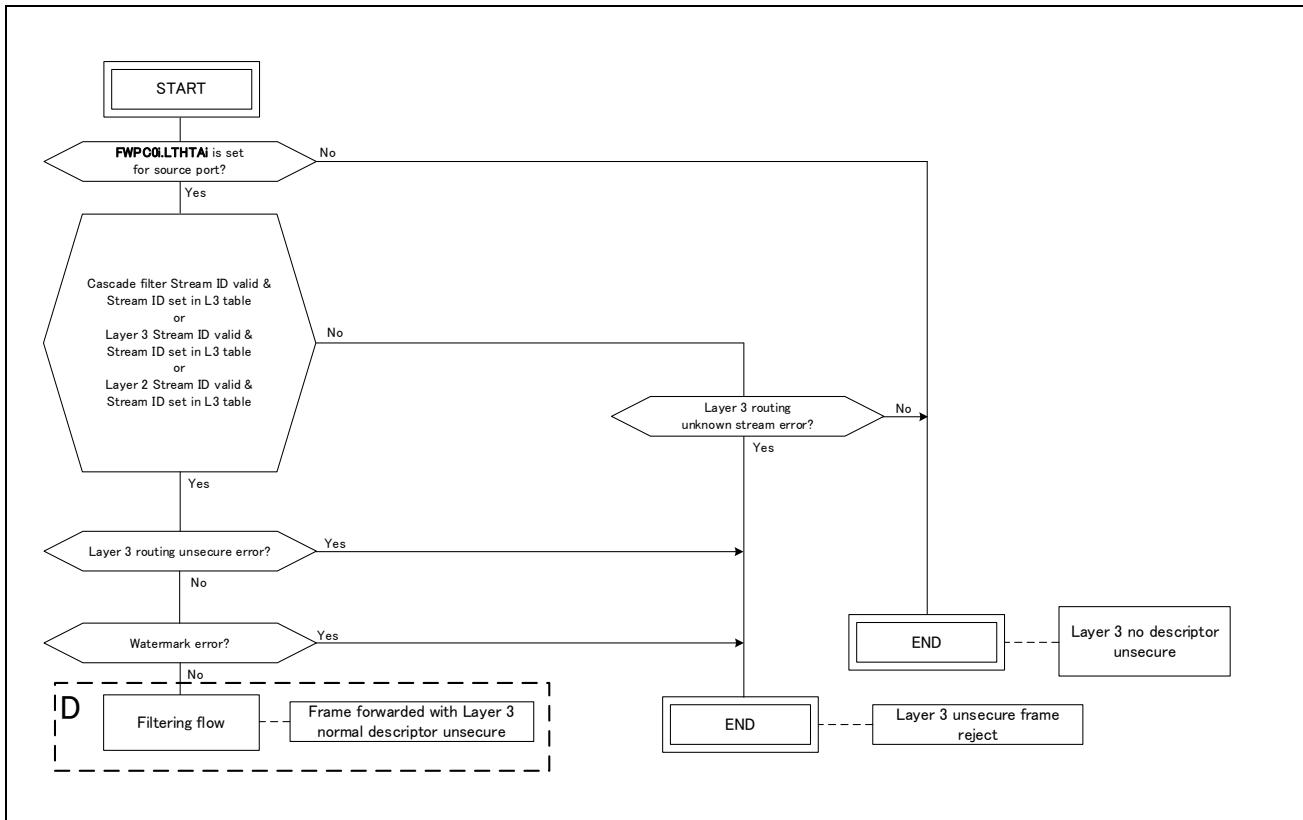


Fig 5.43: Layer 3 forwarding/routing unsecure flow

Notes:

- Layer 3 routing errors and Layer 3 routing unknown stream errors are described in section 5.2.5.5(1).
- Watermark errors are described in section 5.1.6(1).
- Link D links to Fig 5.59: Filtering flow

(1) Layer 3 routing errors

Table 5-31 describes the Layer 3 routing errors. Instead of being discarded by forwarding engine, an error frame can be forwarded to exceptional path using Layer 3 exceptional descriptor described in section 5.2.5.5(4) by setting corresponding error exceptional bit. For error set conditions, refer to corresponding error interrupt register explanations.

Table 5-31: Layer 3 routing Errors

Error	Error name	Error interrupt	Error exceptional bit
Layer 3 routing secure errors			
SNTF	Secure No Target Filtering	FWEIS0i.LTHNTFSi	FWCEPRC2.FLTHNTFEF
SSPF	Secure Source Port Filtering	FWEIS0i.LTHSPFSi	FWCEPRC2.FLTHSLFEF
SUF	Secure Unknown filtering	FWEIS0i.LTHUFSi	FWCEPRC2.FLTHUFEF
SALF	Secure Acceptance List Filtering	FWEIS0i.LTHALFSi	FWCEPRC1.FALFEF
SBLF	Secure Block List Filtering	FWEIS0i.LTHBLFSi	FWCEPRC1.FBLFEF
Layer 3 routing errors			
NTF	No Target Filtering	FWEIS0i.LTHNTFSi	FWCEPRC2.FLTHNTFEF
SPF	Source Port Filtering	FWEIS0i.LTHSPFSi	FWCEPRC2.FLTHSLFEF
FSF	Format Security Filtering	FWEIS0i.LTHFSFSi	FWCEPRC2.FLTHFSFEF
UF	Unknown filtering	FWEIS0i.LTHUFSi	FWCEPRC2. FLTHUFEF
ALF	Acceptance List Filtering	FWEIS0i.LTHALFSi	FWCEPRC1.FALFEF
BLF	Block List Filtering	FWEIS0i.LTHBLFSi	FWCEPRC1.FBLFEF

(2) Layer 3 filtering errors

Table 5-32 describes the Filter errors. Instead of being discarded by forwarding engine, an error frame can be forwarded to exceptional path using Filter exceptional descriptor described in section 5.2.5.5(5) by setting corresponding error exceptional bit. For error set conditions, refer to corresponding error interrupt register explanations.

Table 5-32: Filtering Errors

Error	Error name	Error interrupt	Error exceptional bit
MSDUF	MSDU filtered	FWEIS2.PMFS	FWCEPRC1.FMSDUFEF
GATEF	GATE filtered	FWEIS3.PGFS	FWCEPRC1.FGATEFEF
MTRF	MeTeR filtered	FWEIS50/51/52/53.PMRFS	FWCEPRC1.FMTRFEF
IFRERF	Individual FRER Filtered	FWEIS60/61/62/63.FFS for no sequence error or stuck error FWEIS70/71/72/73.FOORS for out of range error	FWCEPRC1.FIFFEF
SFRERF	Sequence FRER Filtered	FWEIS60/61/62/63.FFS for no sequence error FWEIS70/71/72/73.FOORS for out of range error No interrupt if a frame is discarded because it was a duplicate	FWCEPRC1.FSFFEF

(3) Layer 3 normal descriptor

Layer 3 normal descriptor fields are described in Table 5-33.

Table 5-33: Layer 3 normal descriptor fields

Field name FDESCR.	Values
DV	L3.DV & !FWPC1i.LTHFMI & !VLAN.FMI
SEC	L3.SL
CSD	L3.CSD
IPV	if L3.IPU is set, set to L3.IPV if L3.IPU is not set, set to the frame input priority (section 5.1.4)
MINFO	Refer to Fig 5.44 and Table 5-34
RV	L3.RV
RN	L3.RN
HLD	L3.HLD
RP	If Layer 3 forwarding errors (described by FWGC.LTHUFRP), FWGC.LTHUFRP. Else L3.RP.
FP	L3.FP
SEQN	Set to frame input sequence number if L3.RN is not mapped to a sequence number generation function (refer to section 5.3.2.2)

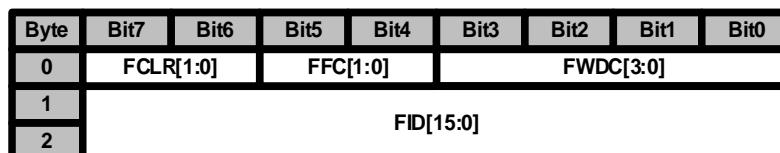


Fig 5.44: Layer 3 normal descriptor MINFO format

Table 5-34: Layer 3 normal descriptor MINFO field explanation

Field name FDESCR.	Bit width	Field explanation	Values
FWDC	4	ForWarDing Code Present in all descriptors, allows to identify the type of forwarding	Fixed to 5 for Layer 3 normal descriptors
FFC	2	Frame Format Code	Set to 0 for perfect filter forwarding Set to 1 for IPv4 forwarding Set to 2 for IPv6 forwarding Set to 3 for Layer 2 stream forwarding
FCLR	2	Frame CoLoR	Set to 0 when frame has no color Set to 1 when frame is green Set to 2 when frame is yellow Set to 3 when frame is red Refer to section 5.3.1.3 for color attribution

Field name FDESCR.	Bit width	Field explanation	Values
FID	16	Frame IDentifier	For Cascade filter stream id, set to the cascade filter number that matched. For L3 stream ID, set to the hash ID inserted in the stream ID. For L2 stream, set to All0.

(4) Layer 3 exceptional descriptor

Layer 3 exceptional descriptor fields are described in Table 5-35.

Table 5-35: Layer 3 exceptional descriptor fields

Field name FDESCR.	Values
DV	Exceptional descriptors are forwarded to GWCA number FWCEPTC.EPCS (port number PORT_TIME_N+FWCEPTC.EPCS)
SEC	FWCEPTC.EPSL
CSDj	FWCEPTC.EPCSD
IPV	FWCEPTC.EPIPV
MINFO	Refer to Fig 5.45 and Table 5-36
RV	1'b0
RN	ALL0
SEQN	Set to frame input sequence number

Byte	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	SBLF	SALF	FFC[1:0]		FWDC[3:0]			
1	ALF	FSF	UF	SPF	NTF	SUF	SSPF	SNTF
2	RSV							BLF

Fig 5.45: Layer 3 exceptional descriptor MINFO format

Table 5-36: Layer 3 exceptional descriptor MINFO field explanation

Field name FDESCR.	Bit width	Field explanation	Values
FWDC	4	ForWarDing Code Present in all descriptors, allows to identify the type of forwarding	Fixed to 6 for Layer 3 exceptional descriptors
FFC	2	Frame Format Code	Set to 0 for perfect filter forwarding Set to 1 for IPv4 forwarding Set to 2 for IPv6 forwarding Set to 3 for Layer 2 stream forwarding Restrictions: - HW: This field is not valid when Secure Unknown filtering or Unknown filtering happened.
SALF	1	Secure Acceptance List Filtering	Refer to section 5.2.5.5(1)
SBLF	1	Secure Block List Filtering	Refer to section 5.2.5.5(1)
SNTF	1	Secure No Target Filtering	Refer to section 5.2.5.5(1)
SSPF	1	Secure Source Port Filtering	Refer to section 5.2.5.5(1)
SUF	1	Secure Unknown filtering	Refer to section 5.2.5.5(1)
NTF	1	No Target Filtering	Refer to section 5.2.5.5(1)
SPF	1	Source Port Filtering	Refer to section 5.2.5.5(1)
FSF	1	Format Security Filtering	Refer to section 5.2.5.5(1)
UF	1	Unknown filtering	Refer to section 5.2.5.5(1)
ALF	1	Acceptance List Filtering	Refer to section 5.2.5.5(1)

Field name FDESCR.	Bit width	Field explanation	Values
BLF	1	Block List Filtering	Refer to section 5.2.5.5(1)

(5) Layer 3 filter exceptional descriptor

Layer 3 filter exceptional descriptor fields are described in Table 5-37.

Table 5-37: Filter exceptional descriptor fields

Field name FDESCR.	Values
DV	Exceptional descriptors are forwarded to GWCA number FWCEPTC.EPCS (port number PORT_TIME_N+FWCEPTC.EPCS)
SEC	FWCEPTC.EPSL
CSDj	FWCEPTC.EPCSD
IPV	FWCEPTC.EPIPV
MINFO	Refer to Fig 5.46 and Table 5-38
RV	1'b0
RN	ALL0
SEQN	Set to frame input sequence number

Byte	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
0	FCLR[1:0]		FFC[1:0]		FWDC[3:0]					
1	RSV		FLC[1:0]		RSV	MTRF	GATEF	MSDUF		
2	RSV	SFOOR	SFNOSEQ	SFRERF	FSTUCK	IFOOR	IFNOSEQ	IFRERF		

Fig 5.46: Filter exceptional descriptor MINFO format

Table 5-38: Filter exceptional descriptor MINFO field explanation

Field name FDESCR.	Bit width	Field explanation	Values
FWDC	4	ForWarDing Code Present in all descriptors, allows to identify the type of forwarding	Fixed to 15 for Filter exceptional descriptors
FLC	2	Frame Layer Code	Set to 0 for Port based Filter exceptional forwarding Set to 1 for Layer 2 Filter exceptional forwarding Set to 2 for Layer 3 Filter exceptional forwarding
FFC	2	Frame Format Code	If FLC == 2'h0 : - Set to 0. If FLC == 2'h1 : (Same as FL2C) - Set to 0 for "MAC destination address and VLAN ID are both found and MAC.SL = VLAN.SL" - Set to 1 for "MAC destination only is found or if MAC destination address and VLAN ID are both found and MAC.SL & !VLAN.SL" - Set to 2 for "VLAN ID only is found or if MAC destination address and VLAN ID are both found and !MAC.SL & VLAN.SL" If FLC == 2'h2 : (Same as FFC) - Set to 0 for perfect filter forwarding - Set to 1 for IPv4 forwarding - Set to 2 for IPv6 forwarding - Set to 3 for Layer 2 stream forwarding

Field name FDESCR.	Bit width	Field explanation	Values
FCLR	2	Frame CoLoR	Set to 0 when frame has no color Set to 1 when frame is green Set to 2 when frame is yellow Set to 3 when frame is red Refer to section 5.3.1.3 for color attribution
MSDUF	1	MSDU Filtered	Refer to section 5.2.5.5(2)
GATEF	1	GATE Filtered	Refer to section 5.2.5.5(2)
MTRF	1	MeTeR Filtered	Refer to section 5.2.5.5(2)
IFRERF	1	Individual FRER Filtered	Refer to section 5.2.5.5(2)
IFNOSEQ	1	Individual FRER NO SEQuence	Refer to section 5.2.5.5(2)
IFOOR	1	Individual FRER Out Of Range (For match algorithm, this flag is set for Out of order error)	Refer to section 5.2.5.5(2)
FSTUCK	1	FRER Stuck	Refer to section 5.2.5.5(2)
SFRERF	1	Sequence FRER Filtered	Refer to section 5.2.5.5(2)
SFNOSEQ	1	Sequence FRER NO SEQuence	Refer to section 5.2.5.5(2)
SFOOR	1	Sequence FRER Out Of Range (For match algorithm, this flag is set for Out of order error)	Refer to section 5.2.5.5(2)

5.2.6 Layer 2 forwarding/routing/filtering

The Layer 2 forwarding block diagram is represented in Fig 5.47.

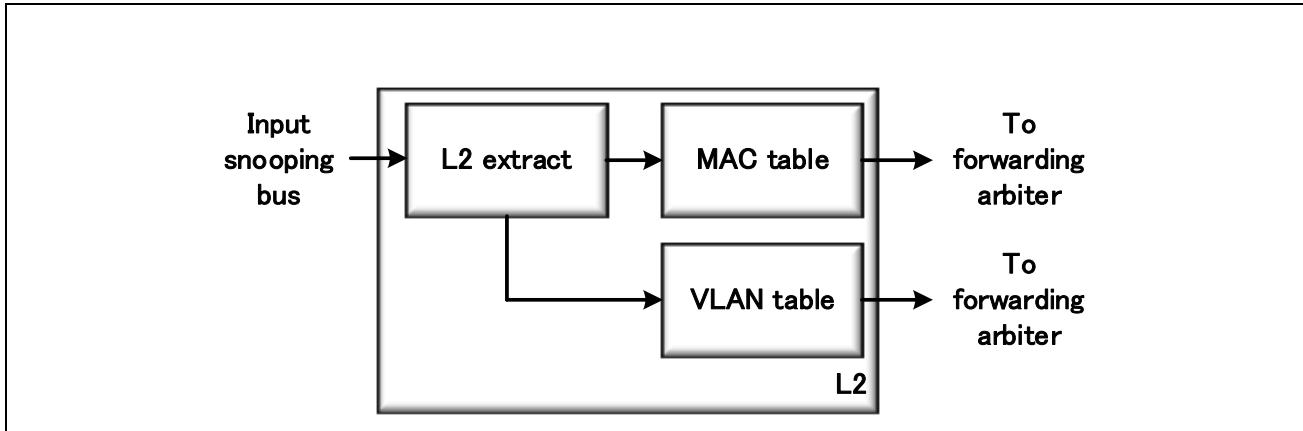


Fig 5.47: Layer 2 forwarding block diagram

The Layer 2 forwarding function is separated in three functional blocks:

- L2 extract: This block snoops all the needed information from the Forwarding engine snooping bus and extract the MAC destination, MAC source addresses and the VLAN ID from frames.
- MAC table: This block handles the MAC addresses meta information such as forwarding and routing information.
- VLAN table: This block handles the VLAN ID meta information such as forwarding and routing information.

Notes:

- Forwarding arbiter contains the forwarding flow. The forwarding flow is explained per forwarding type. For Layer 3 forwarding/routing/filtering, related Forwarding flow is described in Fig 5.51 and Fig 5.52.

5.2.6.1 L2 extract

The L2 extract is used to extract the source and destination MAC addresses and the VLAN ID all frames.

Fig 5.48 describes MAC addresses and VLAN ID extraction happen. MAC addresses extraction always happens. VLAN extraction only happen when **FWGC.SVM** is different than 2'b00, If VLAN ID extraction doesn't happen, all VLANs are considered has unknown.

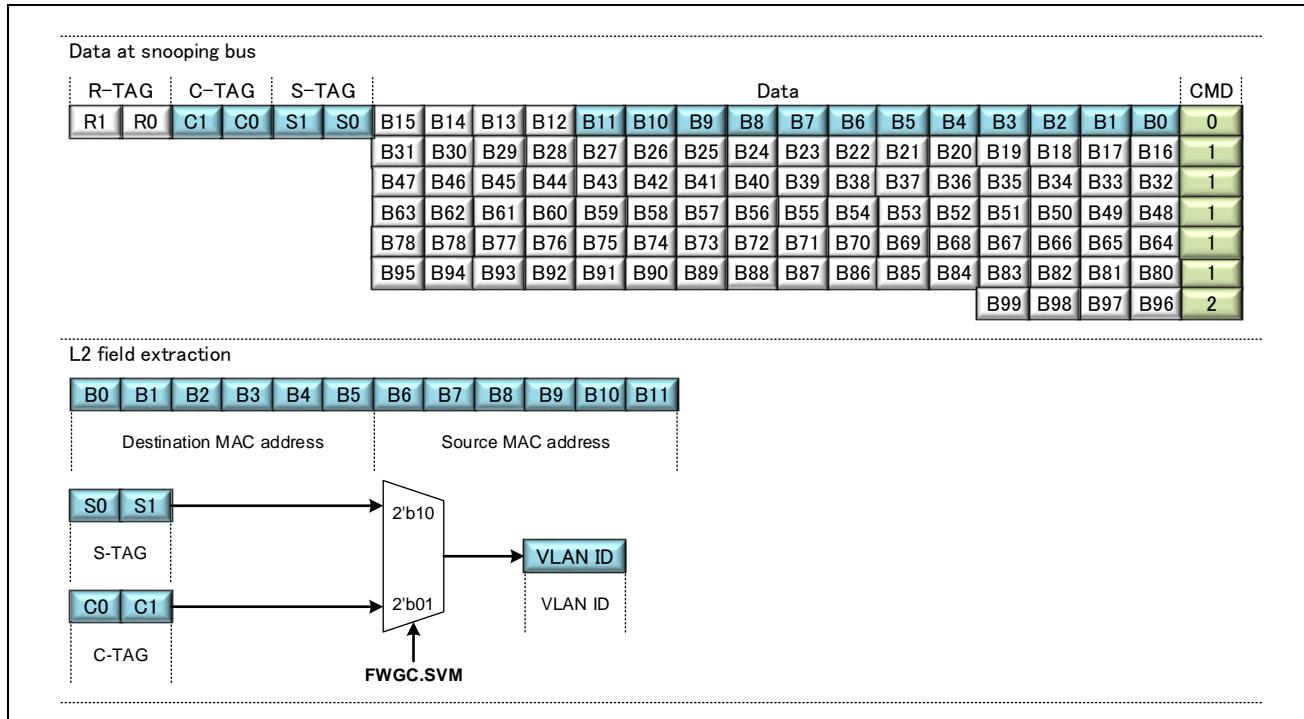


Fig 5.48: MAC address and VLAN ID extraction

5.2.6.2 MAC table

MAC table aims at searching/learning/reading MAC rules.

MAC table is divided in the following items:

- Rule format: Determines what information will be stored along with the MAC address in the table.
- SW Learning: Function to add/suppress an entry from the MAC table by software.
- SW Searching: Function to find the forwarding information related to a MAC address by software.
- SW Reading: Function to read the entries in the MAC table by software.
- HW Searching: Function to find the forwarding information related to a MAC address by forwarding mechanism.
- HW Learning: Function to learn unicast MAC source addresses by forwarding mechanism.
- HW aging: Function used to suppress unused dynamic MAC addresses.
- If several MAC table match a frame searching, the MAC table with the highest entry number (learned address) will be selected.
-

(1) Rule format

The MAC table is used to store MAC rules. A MAC rule contains the information for the frame forwarding. All the fields in this table about Destination MAC, if quoted, will be written **DMAC.{Field name}**. All the fields in this table about Source MAC, if quoted, will be written **SMAC.{Field name}**. All the fields in this table about Destination and Source MAC, if quoted, will be written **MAC.{Field name}**. Table 5-39 describes fields contained in a MAC rule.

Table 5-39: MAC rule format

Field name	Field size (bit)	Field Explanation
EV	1	<p>Entry Valid</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Entry is not valid - 1'b1: Entry is valid
MA	48	MAC Address of the entry. The MAC address is extracted by L2 extract (refer to section 5.2.6.1). This address is in big endian.
SL	1	<p>Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Entry is unsecure - 1'b1: Entry is secure
FP	4	<p>Filtering Priority</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: Priority for filtering (MSDU, GATE and Meter) arbitration. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If FWGC.FPM is 1'b1, this value is invalid. (not use Filtering Priority, use Routing Priority) - HW: If SBL or DBL is 1'b1, this is invalid.
RP	4	<p>Routing Priority</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: Priority for forwarding/routing arbitration. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: For Source MAC, this is invalid. - HW: If SBL or DBL is 1'b1, this is invalid.
SBL	1	<p>Block List for Source MAC address</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Entry is used to forwarding. - 1'b1: Entry is used to Block list filtering. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: For Destination MAC, this is invalid.
DBL	1	<p>Block List for Destination MAC address</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Entry is used to forwarding. - 1'b1: Entry is used to Block list filtering. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: For Source MAC, this is invalid.
MSDUV	1	<p>MSDU Valid</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Frames matching this entry will be ignored by PSFP MSDU filter. - 1'b1: Frames matching this entry will be processed by PSFP MSDU filter. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If SBL or DBL is 1'b1, this is invalid.

Field name	Field size (bit)	Field Explanation
MSDUN	PSFP_MSDU_W	<p>MSDU Number</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: If corresponding entry MAC.MSDUV value is set to 1, frames matching this entry will be processed by PSFP MSDU filter number MAC.MSDUN. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If SBL or DBL is 1'b1, this is invalid.
GATEV	1	<p>GATE Valid</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Frames matching this entry will be ignored by PSFP Gate filter. - 1'b1: Frames matching this entry will be processed by PSFP Gate filter. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If SBL or DBL is 1'b1, this is invalid.
GATEN	PSFP_GATE_W	<p>GATE Number</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: If corresponding entry MACGATEV value is set to 1, frames matching this entry will be processed by PSFP Gate filter number MAC.GATEN. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If SBL or DBL is 1'b1, this is invalid.
MTRV	1	<p>MeTeR Valid</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Frames matching this entry will be ignored by PSFP Meter filter. - 1'b1: Frames matching this entry will be processed by PSFP Meter filter. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If SBL or DBL is 1'b1, this is invalid.
MTRN	PSFP_MTR_W	<p>MeTeR Number</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: If corresponding entry MAC.MTRV value is set to 1, frames matching this entry will be processed by PSFP MSDU filter number MAC.MTRN. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If SBL or DBL is 1'b1, this is invalid.
FRERV	1	<p>FRER Valid</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Frames matching this entry will be ignored by FRER individual recovery. - 1'b1: Frames matching this entry will be processed by FRER individual recovery. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: For Source MAC, this is invalid. - HW: If DBL is 1'b1, this is invalid.
FRERN	FRER_RECE_W	<p>FRER Number</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: If corresponding entry MAC.FRERV value is set to 1, frames matching this entry will be processed by FRER entry number MAC.FRERN for individual recovery. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: For Source MAC, this is invalid. - HW: If DBL is 1'b1, this is invalid.

Field name	Field size (bit)	Field Explanation
HLD	1	<p>Hardware Learn Disable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Source MAC hardware learning is enabled for frames containing MAC.MAC as destination MAC address. - 1'b1: Source MAC hardware learning is disabled for frames containing MAC.MAC as destination MAC address. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: For Source MAC, this is invalid. - HW: If SBL or DBL is 1'b1, this is invalid.
DSLV	PORT_N	<p>Destination Source Lock Vector</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Frames with a destination MAC matching this entry coming from port i are rejected by source port lock error. - Bit i set to 1'b1: Frames with a destination MAC matching this entry coming from port i are forwarded/routed. <p>Notes:</p> <ul style="list-style-type: none"> - This value will be enabling for rules per input port for "Forwarding rule" and "Block list" <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: For Source MAC, this is invalid.
SSLV	PORT_N	<p>Source Source Lock Vector</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Frames with a source MAC matching this entry coming from port i are rejected by source port lock error. - Bit i set to 1'b1: Frames with a source MAC matching this entry coming from port i are forwarded/routed. <p>Notes:</p> <ul style="list-style-type: none"> - This value will be enabling for rules per input port for "Filtering" and "Block list" <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: For Destination MAC, this is invalid.
DV	PORT_N	<p>Destination vector</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: Ports to where the frame should be sent. - hogehoge <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If DBL is 1'b1, this is invalid.
CSD	PORT_GWCA_N* AXI_CHAIN_W	<p>CPU Sub-Destinations</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: CPU Sub-Destinations the frame should be sent. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: For Source MAC, this is invalid. - HW: If DBL is 1'b1, this is invalid.
CME	1	<p>CPU Mirroring Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: CPU mirroring is disabled. - 1'b1: CPU mirroring is enabled. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: For Source MAC, this is invalid. - HW: If DBL is 1'b1, this is invalid.

Field name	Field size (bit)	Field Explanation
EME	1	<p>Ethernet Mirroring Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Ethernet mirroring is disabled. - 1'b1: Ethernet mirroring is enabled. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: For Source MAC, this is invalid. - HW: If DBL is 1'b1, this is invalid.
IPU	1	<p>Internal Priority Update</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Frames matching this entry will not have their internal priority updated. - 1'b1: Frames matching this entry will have their internal priority updated. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: For Source MAC, this is invalid. - HW: If DBL is 1'b1, this is invalid.
IPV	3	<p>Internal Priority Value</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: If corresponding entry MAC.IPU value is set to 1, frames matching this entry will have their priority updated to MAC.IPV. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: For Source MAC, this is invalid. - HW: If DBL is 1'b1, this is invalid.
DE	1	<p>Dynamic Entry</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Entry is static. Migration and aging cannot be applied to the entry. - 1'b1: Entry is dynamic. Migration and aging can be applied to the entry. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: For Destination MAC, this is invalid.
AB	1	<p>Aging Bit:</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Entry has been searched as a MAC source address by forwarding mechanism since previous aging. The entry shouldn't be deleted during next aging. - 1'b1: Entry hasn't been searched as a MAC source address by forwarding mechanism since previous aging. The entry should be deleted during next aging if it is not searched as a MAC source address by forwarding mechanism before. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: For Destination MAC, this is invalid.

(2) SW Learning

Learning is used to add/remove an entry in the MAC table. Table 5-40 describes register used to learn an entry in the MAC table. Table 5-41 describes the learn results.

Table 5-40: MAC learn registers

Register name	Field name/corresponding field in MAC table	Field explanation
FWMACCTL0.MACELA	MAC table address	Not present in MAC table because this is table address.
FWMACCTL1.MACED	Entry delete	Not present in MAC table, used to select between learning an entry and deleting an entry
FWMACCTL1.MACFPL	MAC.FP	Refer to section 5.2.6.2(1).
FWMACCTL1.MACRPL	MAC.RP	Refer to section 5.2.6.2(1).
FWMACCTL1.MACSBL	MAC.SBL	Refer to section 5.2.6.2(1).
FWMACCTL1.MACDBLL	MAC.DBL	Refer to section 5.2.6.2(1).
FWMACCTL1.MACHLDL	MAC.HLD	Refer to section 5.2.6.2(1).
FWMACCTL1.MACDEL	MAC.DE	Refer to section 5.2.6.2(1).
FWMACCTL0.MACELA >= FWMACTEC0.MACTUENC	MAC.SL	Refer to section 5.2.6.2(1).
FWMACCTL2.MACMSDUVL	MAC.MSDUV	Refer to section 5.2.6.2(1).
FWMACCTL2.MACMSDUNL	MAC.MSDUN	Refer to section 5.2.6.2(1).
FWMACCTL2.MACGATEVL	MAC.GATEV	Refer to section 5.2.6.2(1).
FWMACCTL2.MACGATENL	MAC.GATEN	Refer to section 5.2.6.2(1).
FWMACCTL3.MACMTRVL	MAC.MTRV	Refer to section 5.2.6.2(1).
FWMACCTL3.MACMTRNL	MAC.MTRN	Refer to section 5.2.6.2(1).
FWMACCTL3.MACFRERVL	MAC.FRERV	Refer to section 5.2.6.2(1).
FWMACCTL3.MACFRERNL	MAC.FRERN	Refer to section 5.2.6.2(1).
FWMACCTL4.MACDSLVL	MAC.DSLV	Refer to section 5.2.6.2(1).
FWMACCTL4.MACSSLVL	MAC.SSLV	Refer to section 5.2.6.2(1).
{FWMACCTL5.MACMALP0, FWMACCTL6.MACMALP1}	MAC.MA	Refer to section 5.2.6.2(1).
FWMACCTL7i.MACCSDLi	MAC.CSD[AXI_CHAIN_W*(i+1)-1:AXI_CHAIN_W*i]	Refer to section 5.2.6.2(1).
FWMACCTL8.MACDVL	MAC.DV	Refer to section 5.2.6.2(1).
FWMACCTL8.MACCME	MAC.CME	Refer to section 5.2.6.2(1).
FWMACCTL8.MACEMEL	MAC.EME	Refer to section 5.2.6.2(1).
FWMACCTL8.MACIPUL	MAC.IPU	Refer to section 5.2.6.2(1).
FWMACCTL8.MACIPVL	MAC.IPV	Refer to section 5.2.6.2(1).

Table 5-41: MAC learn result

Register name	Field name/corresponding field in MAC table	Field explanation
FWMACTLR.MACLF	Learning fail	Learning failed with happen in one of the following conditions: - The MAC table is not ready (FWMACTIM.MACTR is not set)
FWMACTLR.MACLDF	Learning dynamic fail	Learning failed with happen in one of the following conditions: - The NOT deleting (FWMACCTL1.MACED == 1'b0) entry is MAC table address of HW learning (from FWMACHWLC0.MACTHWLSA to FWMACHWLC0.MACTHWLEA).
FWMACTLR.MACLSF	Learning security fail	Security fail with happen in one of the following conditions: - The learn action is done by the unsecure APB and the corresponding entry for learning is a table of secure area (FWMACCTL0.MACELA >= FWMACTEC0.MACTUENC).

Register name	Field name/corresponding field in MAC table	Field explanation
FWMACTLR.MACLOF	Learning overwrite fail	Overwrite fail with happen in one of the following conditions: - This learn failed because it tried to overwrite an existing Entry.

(3) SW Searching

Searching is used to find the information related to a MAC address. Table 5-42 describes register used to search an MAC address in the MAC table. Table 5-43 describes the search results.

Table 5-42: MAC search registers

Register name	Field name/corresponding field in MAC table	Field explanation
{FWMACTS0.MACMASP0, FWMACTS1.MACMASP1}	MAC.MA	Refer to section 5.2.6.2(1).

Table 5-43: MAC search result

Register name	Field name/corresponding field in MAC table	Field explanation
FWMACTSR0.MACFPS	MAC.FP	Refer to section 5.2.6.2(1).
FWMACTSR0.MACRPS	MAC.RP	Refer to section 5.2.6.2(1).
FWMACTSR0.MACSBLS	MAC.SBL	Refer to section 5.2.6.2(1).
FWMACTSR0.MACDBLS	MAC.DBL	Refer to section 5.2.6.2(1).
FWMACTSR0.MACHLDS	MAC.HLD	Refer to section 5.2.6.2(1).
FWMACTSR0.MACDENTS	MAC.DE	Refer to section 5.2.6.2(1).
FWMACTSR0.MACSLS	MAC.SL	Refer to section 5.2.6.2(1).
FWMACTSR0.MACSNF	Search not found.	Search failed because the searched MAC address is not in the table
FWMACTSR0.MACSEF	Search ECC Fail	Search failed because of an ECC error
FWMACTSR1.MACDSLVS	MAC.DSLV	Refer to section 5.2.6.2(1).
FWMACTSR1.MACSSLVS	MAC.SSLV	Refer to section 5.2.6.2(1).
FWMACTSR2i.MACCSDSi	MAC.CSD[AXI_CHAIN_W*(i+1)-1:AXI_CHAIN_W*i]	Refer to section 5.2.6.2(1).
FWMACTSR3.MACCMES	MAC.CME	Refer to section 5.2.6.2(1).
FWMACTSR3.MACEMES	MAC.EME	Refer to section 5.2.6.2(1).
FWMACTSR3.MACIPUS	MAC.IPU	Refer to section 5.2.6.2(1).
FWMACTSR3.MACIPVS	MAC.IPV	Refer to section 5.2.6.2(1).
FWMACTSR3.MACDV5	MAC.DV	Refer to section 5.2.6.2(1).
FWMACTSR4.MACMSDUVS	MAC.MSDUV	Refer to section 5.2.6.2(1).
FWMACTSR4.MACMSDUNS	MAC.MSDUN	Refer to section 5.2.6.2(1).
FWMACTSR4.MACGATEVS	MAC.GATEV	Refer to section 5.2.6.2(1).
FWMACTSR4.MACGATENS	MAC.GATEN	Refer to section 5.2.6.2(1).
FWMACTSR5.MACMTRVS	MAC.MTRV	Refer to section 5.2.6.2(1).
FWMACTSR5.MACMTRNS	MAC.MTRN	Refer to section 5.2.6.2(1).
FWMACTSR5.MACFRERVS	MAC.FRERV	Refer to section 5.2.6.2(1).
FWMACTSR5.MACFRERNNS	MAC.FRERN	Refer to section 5.2.6.2(1).
FWMACTSR6.MACMCHAS	MAC table address (Address with the highest number in the range FWMACTS2.MACTSSA to FWMACTS2.MACTSEA)	Not present in MAC table.

Restrictions:

- HW: If the unsecure APB accesses to a secure entry for searching, It will be not found.

(4) SW Reading

Reading is used to dump the MAC table content. This function cannot be used to read a specific entry because it is not possible for the software to know at which address an entry can be found in the MAC RAM.

Table 5-44: MAC read registers

Register name	Field name/corresponding field in MAC table	Field explanation
FWMACCTR.MACAR	Read MAC table address	Address that will be used to read an entry in the Layer 2 table

Table 5-45: MAC read result

Register name	Field name/corresponding field in MAC table	Field explanation
FWMACTRR0.MACREF	Read ECC fail	Read failed because of an ECC error
FWMACTRR0.MACEVR	MAC.EV	The read address holds a valid entry Only if this bit is set when reading an address, the corresponding entry and the following registers in this table are valid. Refer to section 5.2.6.2(1).
FWMACTRR1.MACFPR	MAC.FP	Refer to section 5.2.6.2(1).
FWMACTRR1.MACRPR	MAC.RP	Refer to section 5.2.6.2(1).
FWMACTRR1.MACABR	MAC.AB	Refer to section 5.2.6.2(1).
FWMACTRR1.MACSBLR	MAC.SBL	Refer to section 5.2.6.2(1).
FWMACTRR1.MACDBLR	MAC.DBL	Refer to section 5.2.6.2(1).
FWMACTRR1.MACHLDR	MAC.HLD	Refer to section 5.2.6.2(1).
FWMACTRR1.MACDER	MAC.DE	Refer to section 5.2.6.2(1).
FWMACTRR1.MACSLR	MAC.SL	Refer to section 5.2.6.2(1).
FWMACTRR2.MACMSDUVS	MAC.MSDUV	Refer to section 5.2.6.2(1).
FWMACTRR2.MACMSDUNS	MAC.MSDUN	Refer to section 5.2.6.2(1).
FWMACTRR2.MACGATEVS	MAC.GATEV	Refer to section 5.2.6.2(1).
FWMACTRR2.MACGATENS	MAC.GATEN	Refer to section 5.2.6.2(1).
FWMACTRR3.MACMTRVS	MAC.MTRV	Refer to section 5.2.6.2(1).
FWMACTRR3.MACMTRNS	MAC.MTRN	Refer to section 5.2.6.2(1).
FWMACTRR3.MACFRERVS	MAC.FRERV	Refer to section 5.2.6.2(1).
FWMACTRR3.MACFRERN	MAC.FRERN	Refer to section 5.2.6.2(1).
FWMACTRR4.MACDSLVR	MAC.DSLV	Refer to section 5.2.6.2(1).
FWMACTRR4.MACSSLVR	MAC.SSLV	Refer to section 5.2.6.2(1).
{FWMACTRR5.MACMAR0, FWMACTRR6.MACMAR1}	MAC.MA	Refer to section 5.2.6.2(1).
FWMACTRR7i.MACCSDR <i>i</i>	MAC.CSD[AXI_CHAIN_W*(i+1)-1:AXI_CHAIN_W*i]	Refer to section 5.2.6.2(1).
FWMACTRR8.MACCMER	MAC.CME	Refer to section 5.2.6.2(1).
FWMACTRR8.MACEMER	MAC.EME	Refer to section 5.2.6.2(1).
FWMACTRR8.MACIPUR	MAC.IPU	Refer to section 5.2.6.2(1).
FWMACTRR8.MACIPVR	MAC.IPV	Refer to section 5.2.6.2(1).
FWMACTRR8.MACDVR	MAC.DV	Refer to section 5.2.6.2(1).

Restrictions:

- HW: If the unsecure APB accesses to a secure entry for reading, the read will return all0 for read fields.

(5) HW learning/migration

MAC HW learning/migration conditions and settings are described in section 5.1.5.2. Table 5-46 describes to what value the MAC entry fields will be set while learning in hardware a frame coming from port i.

Hardware learning/migration should not happen when a frames with “watermark rejecting”, “cut-through forwarding”, “integrity check rejecting”, “direct descriptor forwarding”.

On the other hand for L1(Port based)/L2(MAC VLAN)/L3(Stream) forwarding, HW learning/migration will valid. Hardware learning/migration should not happen when a frames with any one of following conditions.

- Source MAC multicast address
- VLAN.HLD == 1'b1 (Before overwriting by **L3(Acceptance).HLD**)
- DMAC.HLD == 1'b1 (Before overwriting by **L3(Acceptance).HLD**)
- DESCRIPTOR.HLD == 1'b1 (After overwriting by **L3(Acceptance).HLD**)
- Additional conditions by **FWMACHWLC0.MACTHWLFC0/1/2/3**

HW learning targeted empty area from **FWMACHWLC0.MACTHWLSA** to **FWMACHWLC0.MACTHWLEA**. HW migration targeted all area of MAC tables (**MAC.DE** == 1'b1).

HW learning/migration are limited “all port by **FWMACHWLC0.MACTHWLSA - FWMACHWLC0.MACTHWLEA**” or “per port by **FWMACHWLC2i.MACDELNPPi**” and will be detected “HW learning/migration fail”. Migration and Learning will be constrained by the same conditions. This is because an abnormality has occurred in the Source port, and this is a control that should be stopped even if it is possible.

Table 5-46: MAC hardware learning/migration values

Field name	Field Explanation
MAC.EV	1'b1
MAC.FP	4'h0
MAC.RP	4'h0
MAC.AB	1'b0
MAC.SBL	1'b0
MAC.DBL	1'b0
MAC.HLD	1'b0
MAC.DE	1'b1
MAC.SL	1'b0
MAC.MSDUV	1'b0
MAC.MSDUN	All 0
MAC.GATEV	1'b0
MAC.GATEN	All 0
MAC.MTRV	1'b0
MAC.MTRN	All 0
MAC.FRERV	1'b0
MAC.FRERN	All 0
MAC.DSLV	All 1
MAC.SSLV	All 1
MAC.MA	Incoming frame Source MAC address
MAC.CSD	All 0
MAC.CME	1'b0
MAC.EME	1'b0
MAC.IPU	1'b0
MAC.IPV	3'b0

Field name	Field Explanation
MAC.DV	<code>{{{PORT_N-1}{1'b0}},1'b1} << i (2)</code>

(6) HW Aging

MAC HW aging function is used to remove the unused MAC addresses conditions using **FWMACAGUSPC** and **FWMACAGC** registers and can be monitored using **FWMACAGM0/1** registers and **FWMIS0.MACADAS** interrupt register. MAC HW aging function thanks to two algorithms, the aging algorithm described in Fig 5.49 and the MAC source address search algorithm described in Fig 5.50.

Functions:

- **FWMACAGUSPC** register sets a prescaler to create a 1Hz for aging.
- **FWMACAGC** register sets/enables the aging function
- **FWMIS0.MACADAS** and **FWMACAGM0/1** can be used to keep track in SW of the aged MAC addresses. These registers should be used only in polling mode (**FWMACAGC.MACAGPM** set).
- In polling mode if **FWMIS0.MACADAS** bit is not cleared, further aging or dynamic entry delete will not happen until it is cleared.

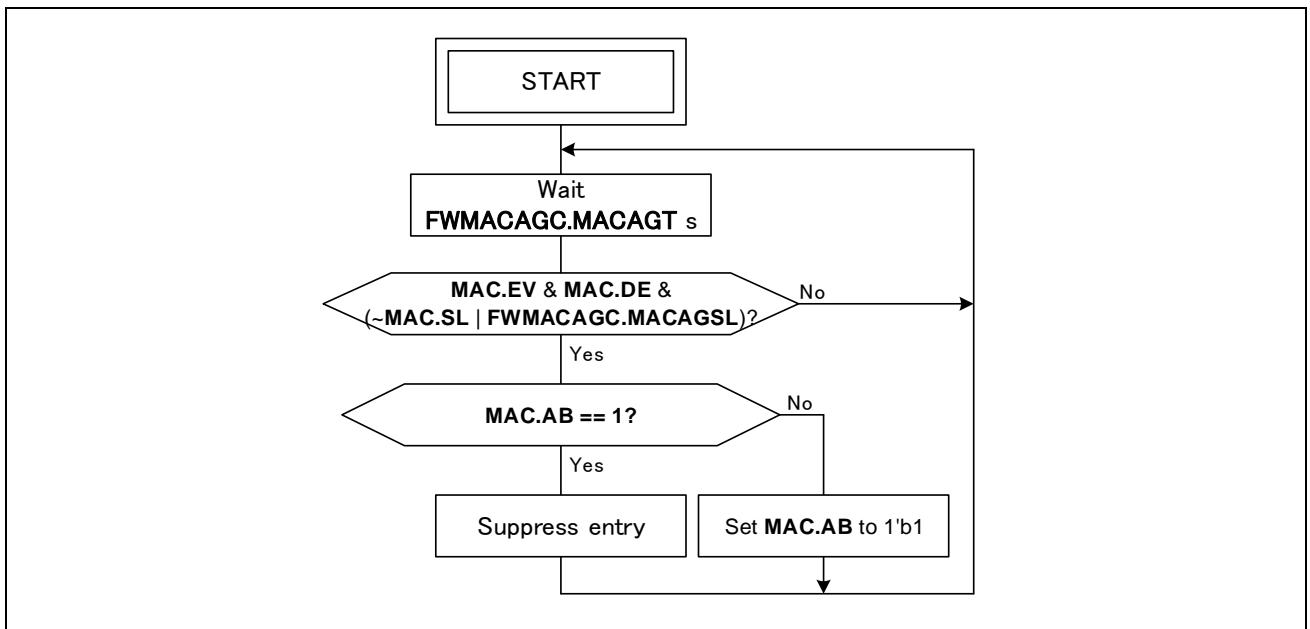


Fig 5.49: MAC aging algorithm

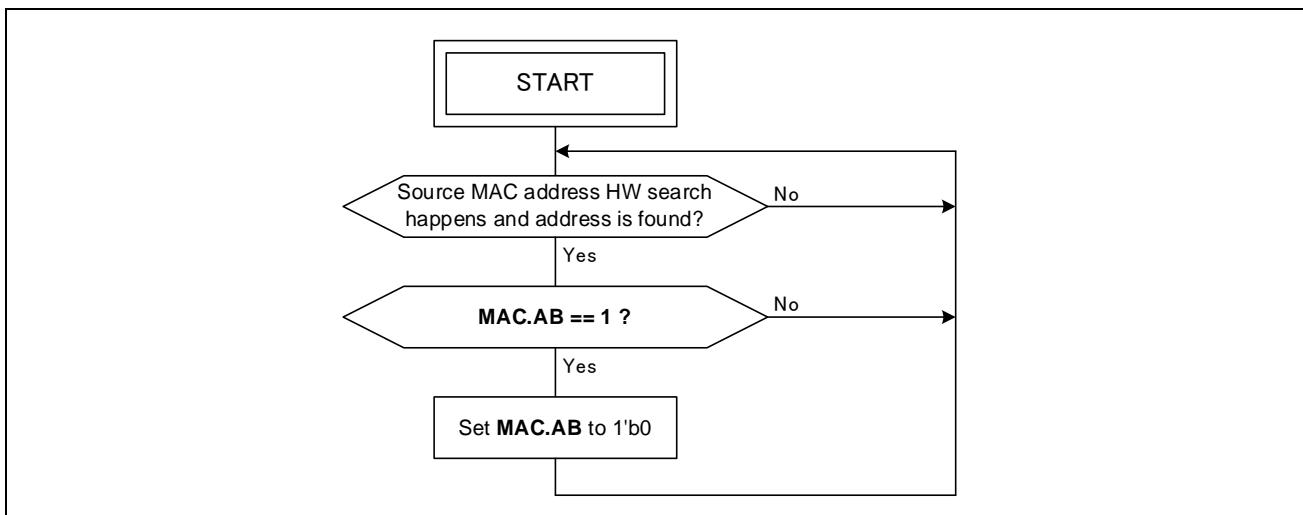


Fig 5.50: MAC source address search algorithm

5.2.6.3 VLAN table

VLAN hash aims at searching/learning VLAN rules. The VLAN ID to VLAN RAM address mapping is a 1:1 mapping so no hash is needed for VLAN handling.

VLAN table is divided in the following items:

- Rule format: Determines what information will be stored in a VLAN rule. The VLAN ID is not stored in a VLAN rule.
- SW Learning: Function to add/suppress an entry from the VLAN table by software.
- SW Searching: Function to find the forwarding information related to a VLAN ID by software.
- HW Searching: Function to find the forwarding information related to a VLAN ID by forwarding mechanism.

(1) Rule format

The VLAN table is used to store VLAN rules. A VLAN rule contains the information for the frame forwarding. All the fields in this table, if quoted, will be written **VLAN.{Field name}**. Table 5-39 describes fields contained in a VLAN rule.

Table 5-47: VLAN rule format

Field name	Field size (bit)	Field Explanation
EV	1	<p>Entry Valid</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Entry is not valid - 1'b1: Entry is valid
SL	1	<p>Security Level</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Entry is unsecure - 1'b1: Entry is secure
FP	4	<p>Filtering Priority</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: Priority for filtering (MSDU, GATE and Meter) arbitration. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If FWGC.FPM is 1'b1, this value is invalid. (not use Filtering Priority, use Routing Priority) - HW: If BL is 1'b1, this is invalid.
RP	4	<p>Routing Priority</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: Priority for forwarding/routing arbitration. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
BL	1	<p>Block List</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Entry is used to forwarding. - 1'b1: Entry is used to Block list filtering.
MSDUV	1	<p>MSDU Valid</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Frames matching this entry will be ignored by PSFP MSDU filter. - 1'b1: Frames matching this entry will be processed by PSFP MSDU filter. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.

Field name	Field size (bit)	Field Explanation
MSDUN	PSFP_MSDU_W	<p>MSDU Number</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: If corresponding entry VLAN.MSDUV value is set to 1, frames matching this entry will be processed by PSFP MSDU filter number VLAN.MSDUN. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
GATEV	1	<p>GATE Valid</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Frames matching this entry will be ignored by PSFP Gate filter. - 1'b1: Frames matching this entry will be processed by PSFP Gate filter. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
GATEN	PSFP_GATE_W	<p>GATE Number</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: If corresponding entry VLAN.GATEV value is set to 1, frames matching this entry will be processed by PSFP Gate filter number VLAN.GATEN. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
MTRV	1	<p>MeTeR Valid</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Frames matching this entry will be ignored by PSFP Meter filter. - 1'b1: Frames matching this entry will be processed by PSFP Meter filter. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
MTRN	PSFP_MTR_W	<p>MeTeR Number</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: If corresponding entry VLAN.MTRV value is set to 1, frames matching this entry will be processed by PSFP MSDU filter number VLAN.MTRN. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
FRERV	1	<p>FRER Valid</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Frames matching this entry will be ignored by FRER individual recovery. - 1'b1: Frames matching this entry will be processed by FRER individual recovery. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
FRERN	FRER_RECE_W	<p>FRER Number</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: If corresponding entry VLAN.FRERV value is set to 1, frames matching this entry will be processed by FRER entry number VLAN.FRERN for individual recovery. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
RV	1	<p>Routing Valid</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Frames matching this entry will be ignored by routing. - 1'b1: Frames matching this entry will be processed by routing. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.

Field name	Field size (bit)	Field Explanation
RN	LTH_RRULE_W	<p>Routing Number</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: If corresponding entry VLAN.RV value is set to 1, frames matching this entry will be processed by routing rule number VLAN.RN. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
FM	PORT_N	<p>Forwarding Mask vector</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: Bit i set to 1'b1: Frames forwarded by Layer 3 or Layer 2 forwarding cannot be forwarded to port i. (same as forwarding mask) <p>Secure VLAN.FM can mask Secure-L2.DV, Unsecure-L2.DV, Secure-L3.DV and Unsecure-L3.DV.</p> <p>Unsecure VLAN.FM can mask Unsecure-L2.DV and Unsecure-L3.DV.</p> <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
HLD	1	<p>Hardware Learn Disable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Source MAC hardware learning is enabled for frames containing corresponding VLAN ID. - 1'b1: Source MAC hardware learning is disabled for frames containing corresponding VLAN ID. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
SLV	PORT_N	<p>Source Lock Vector</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Frames with a VLAN ID matching this entry coming from port i are rejected by source port lock error. - Bit i set to 1'b1: Frames with a VLAN ID matching this entry coming from port i are forwarded/routed. <p>Notes:</p> <ul style="list-style-type: none"> - This value will be enabling for rules per input port for "Forwarding rule" and "Block list"
DV	PORT_N	<p>Destination vector</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: Ports to where the frame should be sent. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
CSD	PORT_GWCA_N* AXI_CHAIN_W	<p>CPU Sub-Destinations</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: CPU Sub-Destinations the frame should be sent <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
CME	1	<p>CPU Mirroring Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: CPU mirroring is disabled. - 1'b1: CPU mirroring is enabled. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.

Field name	Field size (bit)	Field Explanation
EME	1	<p>Ethernet Mirroring Enable</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Ethernet mirroring is disabled. - 1'b1: Ethernet mirroring is enabled. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
IPU	1	<p>Internal Priority Update</p> <p>Values:</p> <ul style="list-style-type: none"> - 1'b0: Frames matching this entry will not have their internal priority updated. - 1'b1: Frames matching this entry will have their internal priority updated. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.
IPV	3	<p>Internal Priority Value</p> <p>Functions:</p> <ul style="list-style-type: none"> - HW: If corresponding entry VLAN.IPU value is set to 1, frames matching this entry will have their priority updated to VLAN.IPV. <p>Restrictions:</p> <ul style="list-style-type: none"> - HW: If BL is 1'b1, this is invalid.

(2) SW Learning

Learning is used to add/remove an entry in the VLAN table. Table 5-48 describes register used to learn an entry in the VLAN table. Table 5-49 describes the learn results.

Table 5-48: VLAN learn registers

Register name	Field name/corresponding field in VLAN table	Field explanation
FWVLANTL0.VLANED	Entry delete	Not present in L3 table, used to select between learning an entry and deleting an entry
FWVLANTL0.VLANFPL	VLAN.FP	Refer to section 5.2.6.3(1).
FWVLANTL0.VLANRPL	VLAN.RP	Refer to section 5.2.6.3(1).
FWVLANTL0.VLANBLL	VLAN.BL	Refer to section 5.2.6.3(1).
FWVLANTL0.VLANHLDL	VLAN.HLD	Refer to section 5.2.6.3(1).
FWVLANTL0.VLANSLL	VLAN.SL	Refer to section 5.2.6.3(1).
FWVLANTL1.VLANVIDL	VLAN ID	Correspond to the address of the learnt entry.
FWVLANTL2.VLANMSDUVL	VLAN.MSDUV	Refer to section 5.2.6.3(1).
FWVLANTL2.VLANMSDUNL	VLAN.MSDUN	Refer to section 5.2.6.3(1).
FWVLANTL2.VLANGATEVL	VLAN.GATEV	Refer to section 5.2.6.3(1).
FWVLANTL2.VLANGATENL	VLAN.GATEN	Refer to section 5.2.6.3(1).
FWVLANTL3.VLANMTRVL	VLAN.MTRV	Refer to section 5.2.6.3(1).
FWVLANTL3.VLANMTRNL	VLAN.MTRN	Refer to section 5.2.6.3(1).
FWVLANTL3.VLANFRERVL	VLAN.FRERV	Refer to section 5.2.6.3(1).
FWVLANTL3.VLANFRERNL	VLAN.FRERN	Refer to section 5.2.6.3(1).
FWVLANTL4.VLANSLVL	VLAN.SLV	Refer to section 5.2.6.3(1).
FWVLANTL4.VLANRVL	VLAN.RV	Refer to section 5.2.6.3(1).
FWVLANTL4.VLANRNL	VLAN.RN	Refer to section 5.2.6.3(1).
FWVLANTL5.VLANFMVL	VLAN.FM	Refer to section 5.2.6.3(1).
FWVLANTL6i.VLANCSDi	VLAN.CSD[AXI_CHAIN_W*(i+1)-1:AXI_CHAIN_W*i]	Refer to section 5.2.6.3(1).
FWVLANTL7.VLANCSEL	VLAN.CME	Refer to section 5.2.6.3(1).
FWVLANTL7.VLANEMEL	VLAN.EME	Refer to section 5.2.6.3(1).
FWVLANTL7.IPUL	VLAN.IPU	Refer to section 5.2.6.3(1).
FWVLANTL7.VLANIPVL	VLAN.IPV	Refer to section 5.2.6.3(1).
FWVLANTL7.VLANDVL	VLAN.DV	Refer to section 5.2.6.3(1).

Table 5-49: VLAN learn result

Register name	Field name/corresponding field in VLAN table	Field explanation
FWVLANTLR.VLANLF	Learning fail	<p>Learning fail will happen in one of the following conditions:</p> <ul style="list-style-type: none"> - The VLAN table is not ready (FWVLANTIM.VLANTR is not set) - The learning function is used to delete an entry (FWVLANTL0.VLANED set for learning) and the entry is not found in the VLAN table)

Register name	Field name/corresponding field in VLAN table	Field explanation
FWVLANTLR.VLANLSF	Learning security fail	<p>Security fail with happen in one of the following conditions:</p> <ul style="list-style-type: none"> - The learn entry is an unsecure entry (FWVLANTL0.VLANSLL not set for learning) and the unsecure entry number FWVLANTEM.VLANTUEN has reached the maximum unsecure entry number FWVLANTEC.VLANTMUE. - The learn action is done by the unsecure APB and the corresponding entry for learning is already in the table and is a secure entry (VLAN.SL is set). - The learn action is done by the secure APB which tries to learn an unsecure entry when the entry is already in the table, is secure (VLAN.SL is set) and when FWVLANTEM.VLANTUEN has reached the maximum unsecure entry number FWVLANTEC.VLANTMUE.
FWVLANTLR.VLANLEF	Learning ECC Fail	<p>ECC fail with happen in one of the following conditions:</p> <ul style="list-style-type: none"> - When an ECC error happens while learning an entry. The learning algorithm learns entries such a way that the algorithm will never be broken by an ECC error. Some entries will be unreachable because of the ECC error and be considered as not found while being searched but most of the entries will still operate normally.
FWVLANTLR.VLANLO	Learning overwrite	<p>Overwrite with happen in one of the following conditions:</p> <ul style="list-style-type: none"> - The learn VLAN is already present in the table an no error happened during learning.

(3) SW Searching

Searching is used to find the information related to a VLAN address. Table 5-50 describes register used to search a VLAN address in the VLAN table. Table 5-51 describes the search results. This function is not actually searching the address but only reading the address corresponding to the VLAN ID in the VLAN table

Table 5-50: VLAN search registers

Register name	Field name/corresponding field in VLAN table	Field explanation
FWVLANTS.VLANVIDS	VLAN ID	Address that should be read in VLAN table. Correspond to the VLAN ID

Table 5-51: VLAN search result

Register name	Field name/corresponding field in VLAN table	Field explanation
FWVLANTSRO.VLANCFPS	VLAN.FP	Refer to section 5.2.6.3(1).
FWVLANTSRO.VLANRPS	VLAN.RP	Refer to section 5.2.6.3(1).
FWVLANTSRO.VLANBLS	VLAN.BL	Refer to section 5.2.6.3(1).
FWVLANTSRO.VLANHLDs	VLAN.HLD	Refer to section 5.2.6.3(1).
FWVLANTSRO.VLANSLS	VLAN.SL	Refer to section 5.2.6.3(1).
FWVLANTSRO.VLANSEF	Search ECC Fail	Search failed because of an ECC error
FWVLANTSRO.VLANSNF	Search not found.	Search failed because the searched VLAN ID is not in the table
FWVLANTS1.VLANMSDUVS	VLAN.MSDUV	Refer to section 5.2.6.3(1).
FWVLANTS1.VLANMSDUNS	VLAN.MSDUN	Refer to section 5.2.6.3(1).
FWVLANTS1.VLANGATEVS	VLAN.GATEV	Refer to section 5.2.6.3(1).
FWVLANTS1.VLANGATENS	VLAN.GATEN	Refer to section 5.2.6.3(1).
FWVLANTS2.VLANMTRVS	VLAN.MTRV	Refer to section 5.2.6.3(1).
FWVLANTS2.VLANMTRNS	VLAN.MTRN	Refer to section 5.2.6.3(1).
FWVLANTS2.VLANFRERVS	VLAN.FRERV	Refer to section 5.2.6.3(1).
FWVLANTS2.VLANFRERNS	VLAN.FRERN	Refer to section 5.2.6.3(1).
FWVLANTS3.VLANSLVS	VLAN.SLV	Refer to section 5.2.6.3(1).
FWVLANTS3.VLANRVS	VLAN.RV	Refer to section 5.2.6.3(1).
FWVLANTS3.VLANRNS	VLAN.RN	Refer to section 5.2.6.3(1).
FWVLANTS4.VLANFMVS	VLAN.FM	Refer to section 5.2.6.3(1).
FWVLANTS5i.VLANCSDSi	VLAN.CSD[AXI_CHAIN_W*(i+1)-1:AXI_CHAIN_W*i]	Refer to section 5.2.6.3(1).
FWVLANTS6.VLANCMES	VLAN.CME	Refer to section 5.2.6.3(1).
FWVLANTS6.VLANEMES	VLAN.EME	Refer to section 5.2.6.3(1).
FWVLANTS6.VLANIPUS	VLAN.IPU	Refer to section 5.2.6.3(1).
FWVLANTS6.VLANIPVS	VLAN.IPV	Refer to section 5.2.6.3(1).
FWVLANTS6.VLANDVS	VLAN.DV	Refer to section 5.2.6.3(1).

Restrictions:

- HW: If the unsecure APB accesses to a secure entry for searching, it will be not found.

5.2.6.4 Layer 2 forwarding

Layer 2 forwarding is used to forward local ethernet descriptors (**LDESCR.FMT** [GWCA] set to 1'b0) received from agents using **FWPC0i** and **FWCEPRC2** register and can be monitored using **FWEIS0i** interrupt register. Layer 2 forwarding searches received MAC addresses (section 5.2.6.1) in the MAC table to extract corresponding entry fields (section 5.2.6.2(1)) and searches valid VLAN IDs (section 5.2.6.1) in the VLAN table to extract corresponding entry fields (section 5.2.6.3(1)). Depending on the entry fields, Layer 2 forwarding will forward frames following L2 forwarding secure flow in Fig 5.51 and L2 forwarding unsecure flow in Fig 5.52.

Functions:

- **FWPC0i.MACDSAi** register is used to activate MAC table for frames received from port i for destination MAC.
- **FWPC0i.MACRUDAi** register is used to reject unknown destination MAC received from port i.
- **FWPC0i.MACRUDSAi** register is used to reject secure unknown destination MAC received from port i.
- **FWPC0i.MACSSAi** register is used to activate MAC table for frames received from port i for source MAC.
- **FWPC0i.MACRUSAi** register is used to reject unknown source MAC received from port i.
- **FWPC0i.MACRUSSAi** register is used to reject secure unknown source MAC received from port i.
- **FWPC0i.VLANSAi** register is used to activate VLAN table for frames received from port i for source MAC.
- **FWPC0i.VLANRUi** register is used to reject unknown VLAN IDs received from port i.
- **FWPC0i.VLANRUSi** register is used to reject secure unknown VLAN IDs received from port i.
- **FWPC2i.LTHFMi** register is used to set to which ports frames received from port i can be forwarded.
- **FWCEPRC2** register enables exceptional path for error descriptors.
- **FWEIS0** interrupt register notifies that an ethernet descriptor has been rejected because of an error.
- **FWGC.LTWUFRP** register is used to setting filtering priority. If in case “MAC forwarding and VLAN filtering” or “MAC filtering and VLAN forwarding” happens together in a same frame with same RP value in both case (**MAC.RP/VLAN.RP == FWGC.LTWUFRP**), filtering will get the priority.

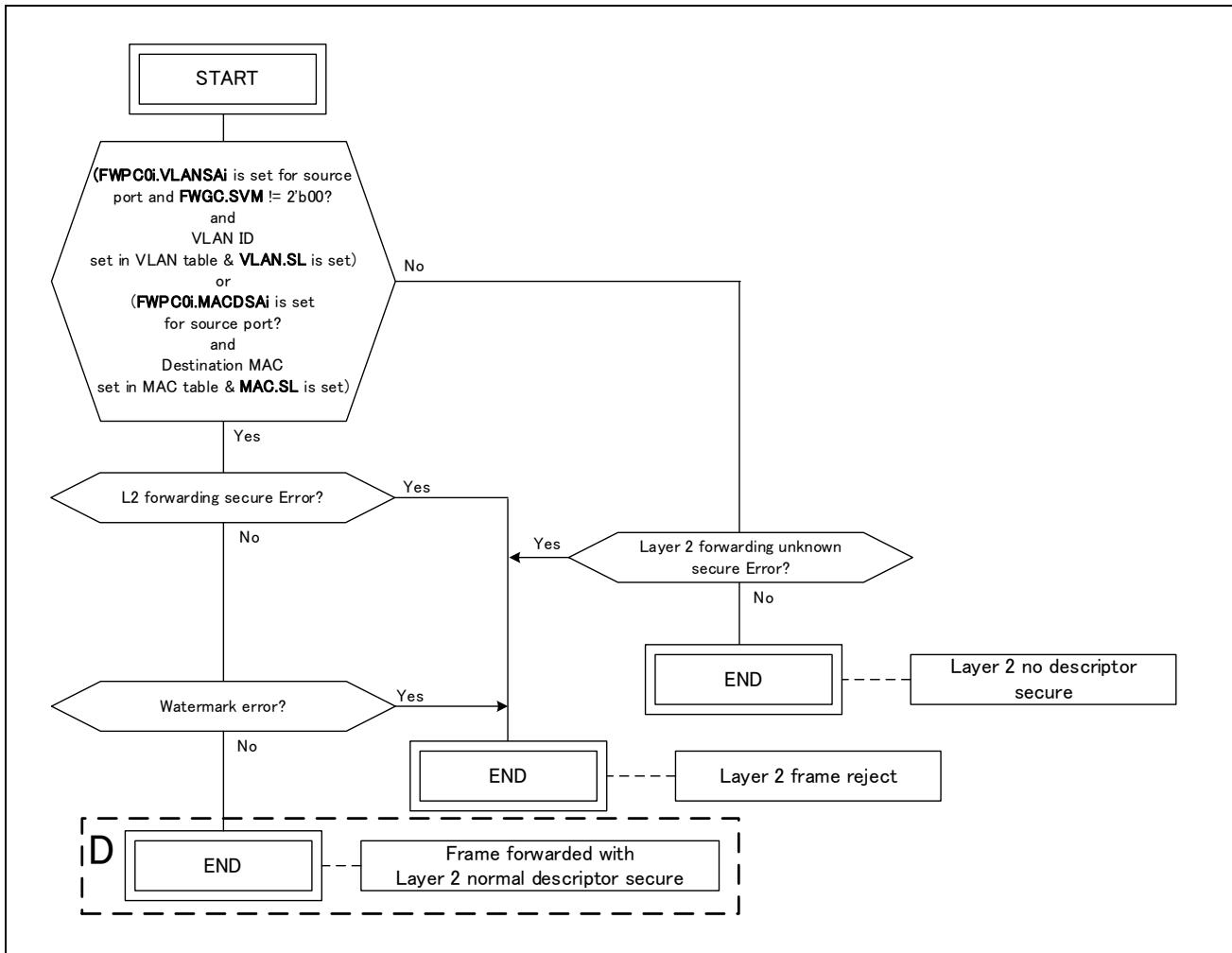


Fig 5.51: Layer 2 forwarding secure flow

Notes:

- Layer 2 forwarding secure errors are described in section 5.2.6.4(1).
- Layer 2 forwarding unknown secure Error means “Secure any unknown filtering” in section 5.2.6.4(1).
- Watermark errors are described in section 5.1.6(1).
- Link D links to Fig 5.59: Filtering flow

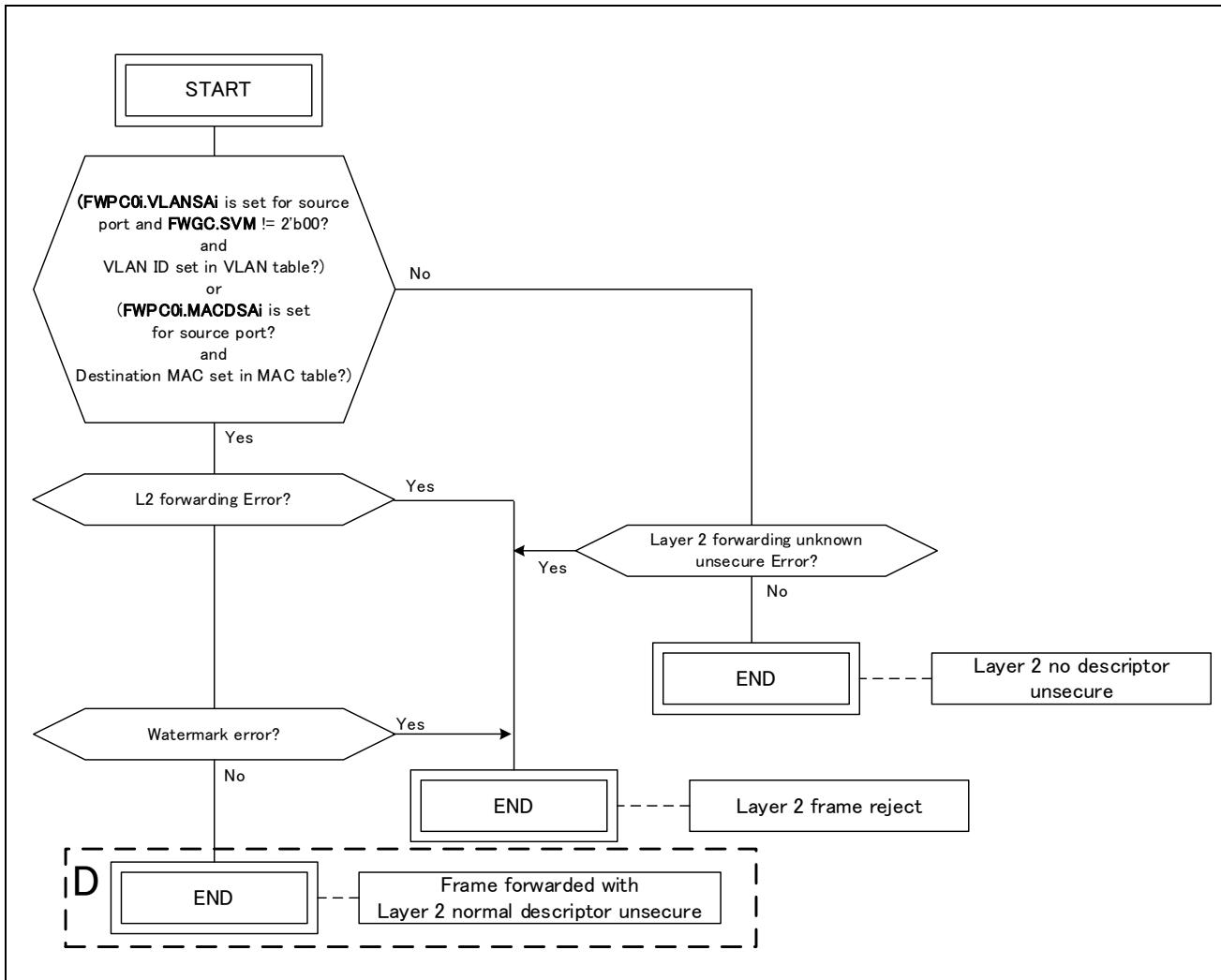


Fig 5.52: Layer 2 forwarding unsecure flow

Notes:

- Layer 2 forwarding errors are described in section 5.2.6.4(1).
- Layer 2 forwarding unknown secure Error means “Any unknown filtering” in section 5.2.6.4(1).
- Watermark errors are described in section 5.1.6(1).
- Link D links to Fig 5.59: Filtering flow

(1) Layer 2 forwarding errors

Table 5-52 describes the L2 forwarding errors. Instead of being discarded by forwarding engine, an error frame can be forwarded to exceptional path using Layer 2 exceptional descriptor described in section 5.2.6.4(4) by setting corresponding error exceptional bit. For error set conditions, refer to corresponding error interrupt register explanations.

If multiple errors occur (with the same priority), the error information and interrupts/status has the following restrictions.

- If SDUF, SSUF, SVUF or SSSPF are detected, SNTF, SDSPF, SVSPF, SALF, SBLF will be ignored.
- If DUF, SUF, VUF or SSPF are detected, NTF, DSPF, VSPF, FSF, ALF, BLF will be ignored.

Table 5-52: L2 forwarding Errors

Error	Error name	Error interrupt	Error exceptional bit
L2 forwarding secure errors			
SNTF	Secure No Target Filtering	FWEIS0i.LTWNTFSi	FWCEPRC2.FLTWNTFEF
SDSPF	Secure Destination Source Port Filtering	FWEIS0i.LTWDSPFSi	FWCEPRC2.FDMACSLFEF
SSSPF	Secure Source Source Port Filtering	FWEIS0i.LTWSSPFSi	FWCEPRC2.FSMACSLFEF
SVSPF	Secure VLAN Source Port Filtering	FWEIS0i.LTWVSPFSi	FWCEPRC2.FVLANSLFEF
SDUF	Secure Destination Unknown filtering	FWEIS0i.LTWDUFSi	FWCEPRC2.FDMACUFEF
SSUF	Secure Source Unknown filtering	FWEIS0i.LTWSUFSi	FWCEPRC2.FSMACUFEF
SVUF	Secure VLAN Unknown filtering	FWEIS0i.LTWVUFSi	FWCEPRC2.FVLANUFEF
SALF	Secure Acceptance List Filtering	FWEIS0i.LTWALFSi	FWCEPRC1.FALFEF
SBLF	Secure Block List Filtering	FWEIS0i.LTWBLFSi	FWCEPRC1.FBLFEF
L2 forwarding errors			
NTF	No Target Filtering	FWEIS0i.LTWNTFSi	FWCEPRC2.FLTWNTFEF
DSPF	Destination Source Port Filtering	FWEIS0i.LTWDSPFSi	FWCEPRC2.FDMACSLFEF
SSPF	Source Source Port Filtering	FWEIS0i.LTWSSPFSi	FWCEPRC2.FSMACSLFEF
VSPF	VLAN Source Port Filtering	FWEIS0i.LTWVSPFSi	FWCEPRC2.FVLANSLFEF
FSF	Format Security Filtering	FWEIS0i.LTWFSFSi	FWCEPRC2.FTWFSFEF
DUF	Destination Unknown filtering	FWEIS0i.LTWDUFSi	FWCEPRC2.FDMACUFEF
SUF	Source Unknown filtering	FWEIS0i.LTWSUFSi	FWCEPRC2.FSMACUFEF
VUF	VLAN Unknown filtering	FWEIS0i.LTWVUFSi	FWCEPRC2.FVLANUFEF
ALF	Acceptance List Filtering	FWEIS0i.LTWALFSi	FWCEPRC1.FALFEF
BLF	Block List Filtering	FWEIS0i.LTWBLFSi	FWCEPRC1.FBLFEF

(2) Layer 2 filtering errors

Same as 5.2.5.5(2).

(3) Layer 2 normal descriptor

For Layer 2 normal descriptor creation, only MAC table fields read from MAC table thanks to the destination MAC and VLAN table fields read from VLAN table are used. Layer 2 normal descriptor fields are described in Table 5-53.

If "MAC destination address and VLAN ID are both found and DMAC.SL != VLAN.SL", VLAN.RP or DMAC.RP whichever greater will be selected and if VLAN.RP == DMAC.RP, secure descriptor (DMAC.SL == 1'b1 or VLAN.SL == 1'b1) will be selected. If "MAC destination only is found" DMAC.RP will be selected or if "VLAN ID only is found" VLAN.RP will be selected.

If MAC source address found from MAC table, SMAC.FP and SMAC.PSFP (SMAC.MSDUV, SMAC.MSDUN, SMAC.GATEV, SMAC.GATEN, SMAC.MTRV, SMAC.MTRN) will be transmitted as a unique path for "PSFP filtering info selection".

Table 5-53: Layer 2 normal descriptor fields

Field name FDESCR.	Values if MAC destination address and VLAN ID are both found and MAC.SL == VLAN.SL or Layer 2 forwarding errors	Values if MAC destination only is found	Values if VLAN ID only is found
DV	DMAC.DV & VLAN.DV & !FWPC2i.LTWFMi & !VLAN.FMi	DMAC.DV & !FWPC2i.LTWFMi & !VLAN.FMi	VLAN.DV & !FWPC2i.LTWFMi & !VLAN.FMi
SEC	DMAC.SL	DMAC.SL	VLAN.SL
CSD	DMAC.CSD	DMAC.CSD	VLAN.CSD
IPV	if DMAC.IPU is set, set to DMAC.IPV if DMAC.IPU is not set and VLAN.IPU is set, set to VLAN.IPV if DMAC.IPU and VLAN.IPU both are not set, set to the frame input priority (section 5.1.4)	if DMAC.IPU is set, set to DMAC.IPV if DMAC.IPU is not set, set to the frame input priority (section 5.1.4)	if VLAN.IPU is set, set to VLAN.IPV if VLAN.IPU is not set, set to the frame input priority (section 5.1.4)
MINFO	Refer to Fig 5.53 and Table 5-54	Refer to Fig 5.53 and Table 5-54	Refer to Fig 5.53 and Table 5-54
RV	VLAN.RV	0	VLAN.RV
RN	VLAN.RN	All 0	VLAN.RN
HLD	Refer to Table 5-4	DMAC.HLD	VLAN.HLD
RP	If Layer 2 forwarding errors (described by FWGC.LTWUFRP), FWGC.LTWUFRP. Else, VLAN.RP or DMAC.RP whichever is greater. (SMAC.RP is invalid)	DMAC.RP	VLAN.RP
FP	If FWGC.FPM == 1'b1, VLAN.RP or DMAC.RP whichever is greater. If FWGC.FPM == 1'b0, VLAN.FP or DMAC.FP (or SMAC.FP) whichever is greater.	If FWGC.FPM == 1'b1, DMAC.FP. If FWGC.FPM == 1'b0, DMAC.FP (or SMAC.FP)	If FWGC.FPM == 1'b1, VLAN.FP. If FWGC.FPM == 1'b0, VLAN.FP (or SMAC.FP)
PSFP	If FWGC.FPM == 1'b1, selected by RP. If FWGC.FPM == 1'b0, selected by FP. (VLAN.MSDUV, VLAN.MSDUN, VLAN.GATEV, VLAN.GATEN, VLAN.MTRV, VLAN.MTRN) or (DMAC.MSDUV, DMAC.MSDUN, DMAC.GATEV, DMAC.GATEN, DMAC.MTRV, DMAC.MTRN) or (SMAC.MSDUV, SMAC.MSDUN, SMAC.GATEV, SMAC.GATEN, SMAC.MTRV, SMAC.MTRN) Example: *	(DMAC.MSDUV, DMAC.MSDUN, DMAC.GATEV, DMAC.GATEN, DMAC.MTRV, DMAC.MTRN) or (SMAC.MSDUV, SMAC.MSDUN, SMAC.GATEV, SMAC.GATEN, SMAC.MTRV, SMAC.MTRN)	(VLAN.MSDUV, VLAN.MSDUN, VLAN.GATEV, VLAN.GATEN, VLAN.MTRV, VLAN.MTRN) or (SMAC.MSDUV, SMAC.MSDUN, SMAC.GATEV, SMAC.GATEN, SMAC.MTRV, SMAC.MTRN)
FRER	VLAN.FRERV, VLAN.FRERN	DMAC.FRERV, DMAC.FRERN	VLAN.FRERV, VLAN.FRERN
SEQN	Set to frame input sequence number	Set to frame input sequence number	Set to frame input sequence number

* : [In case of] “DMAC and VLAN are both found” and “VLAN.FP = DMAC.FP” and “VLAN.RP = DMAC.RP” and “DMAC.SL = VLAN.SL” and “VLAN.MSDUV = 1, VLAN.MSDUN = 6” and “DMAC.MSDUV = 1, DMAC.MSDUN = 5”.

[Results]

If “FWGC.FPM == 1'b1 (FP are invalid)”, DMAC.MSDUV and DMAC.MSDUN are selected because default routing priority is high for DMAC.

If “FWGC.FPM == 1'b0 (FP are valid)”, VLAN.MSDUV and VLAN.MSDUN are selected because default filtering priority is high for VLAN.

Byte	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	FCLR[1:0]		FL2C[1:0]				FWDC[3:0]	
1								
2							RSV	

Fig 5.53: Layer 2 normal descriptor MINFO format

Table 5-54: Layer 2 normal descriptor MINFO field explanation

Field name FDESCR.	Bit width	Field explanation	Values
FWDC	4	ForWarDing Code Present in all descriptors, allows to identify the type of forwarding	Fixed to 9 for Layer 2 normal descriptors
FL2C	2	Forwarding layer 2 code Forwarding layer 2 code	if MAC destination address and VLAN ID are both found and MAC.SL = VLAN.SL , set to 0 if MAC destination only is found or if MAC destination address and VLAN ID are both found and MAC.SL & !VLAN.SL , set to 1 if VLAN ID only is found or if MAC destination address and VLAN ID are both found and !MAC.SL & VLAN.SL , set to 2
FCLR	2	Frame CoLoR Frame CoLoR	Set to 0 when frame has no color Set to 1 when frame is green Set to 2 when frame is yellow Set to 3 when frame is red Refer to section 5.3.1.3 for color attribution
RSV	--	Reserved field	Set to 0

(4) Layer 2 exceptional descriptor

Layer 2 exceptional descriptor fields are described.

Table 5-55: Layer 2 exceptional descriptor fields

Field name FDESCR.	Values
DV	Exceptional descriptors are forwarded to GWCA number FWCEPTC.EPCS (port number PORT_TIME_N+FWCEPTC.EPCS)
SEC	FWCEPTC.EPSL
CSDj	FWCEPTC.EPCSD
IPV	FWCEPTC.EPIPV
MINFO	Refer to Fig 5.54 and Table 5-56
RV	1'b0
RN	ALL0
SEQN	Set to frame input sequence number

Byte	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	RSV	SBLF	SAFL	FSF	FWDC[3:0]			
1	NTF	SVUF	SSUF	SDUF	SVSPF	SSSPF	SDSPF	SNTF
2	BLF	ALF	VUF	SUF	DUF	VSPF	SSPF	DSPF

Fig 5.54: Layer 2 exceptional descriptor MINFO format

Table 5-56: Layer 2 exceptional descriptor MINFO field explanation

Field name FDESCR.	Bit width	Field explanation	Values
FWDC	4	ForWarDing Code Present in all descriptors, allows to identify the type of forwarding	Fixed to 10 for Layer 2 exceptional descriptors
FSF	1	Format Security Filtering	Refer to section 5.2.6.4(1)
SAFL	1	Secure Acceptance List filtering	Refer to section 5.2.6.4(1)
SBLF	1	Secure Block List filtering	Refer to section 5.2.6.4(1)
SNTF	1	Secure No Target Filtering	Refer to section 5.2.6.4(1)
SDSPF	1	Secure Destination Source Port Filtering	Refer to section 5.2.6.4(1)
SSSPF	1	Secure Source Source Port Filtering	Refer to section 5.2.6.4(1)
SVSPF	1	Secure VLAN Source Port Filtering	Refer to section 5.2.6.4(1)
SDUF	1	Secure Destination Unknown filtering	Refer to section 5.2.6.4(1)
SSUF	1	Secure Source Unknown filtering	Refer to section 5.2.6.4(1)
SVUF	1	Secure VLAN Unknown filtering	Refer to section 5.2.6.4(1)
NTF	1	No Target Filtering	Refer to section 5.2.6.4(1)
DSPF	1	Destination Source Port Filtering	Refer to section 5.2.6.4(1)
SSPF	1	Source Source Port Filtering	Refer to section 5.2.6.4(1)
VSPF	1	VLAN Source Port Filtering	Refer to section 5.2.6.4(1)
DUF	1	Destination Unknown filtering	Refer to section 5.2.6.4(1)
SUF	1	Source Unknown filtering	Refer to section 5.2.6.4(1)
VUF	1	VLAN Unknown filtering	Refer to section 5.2.6.4(1)
ALF	1	Acceptance List filtering	Refer to section 5.2.6.4(1)

Field name FDESCR.	Bit width	Field explanation	Values
BLF	1	Block List filtering	Refer to section 5.2.6.4(1)

(5) Layer 2 Filter exceptional descriptor

Same as 5.2.5.5(5)

5.2.7 Port based forwarding

Port based forwarding aims at forwarding all frames from a port to other ones. It used **FWPBFC0i** and **FWPBFCSDCji** registers. Port based forwarding will forward frames following Port based forwarding secure flow in Fig 5.55 and Port based forwarding unsecure flow in Fig 5.56.

Functions:

- **FWPBFC0i** and **FWPBFCSDCji** registers are used to set forwarding information for frames coming from port i.

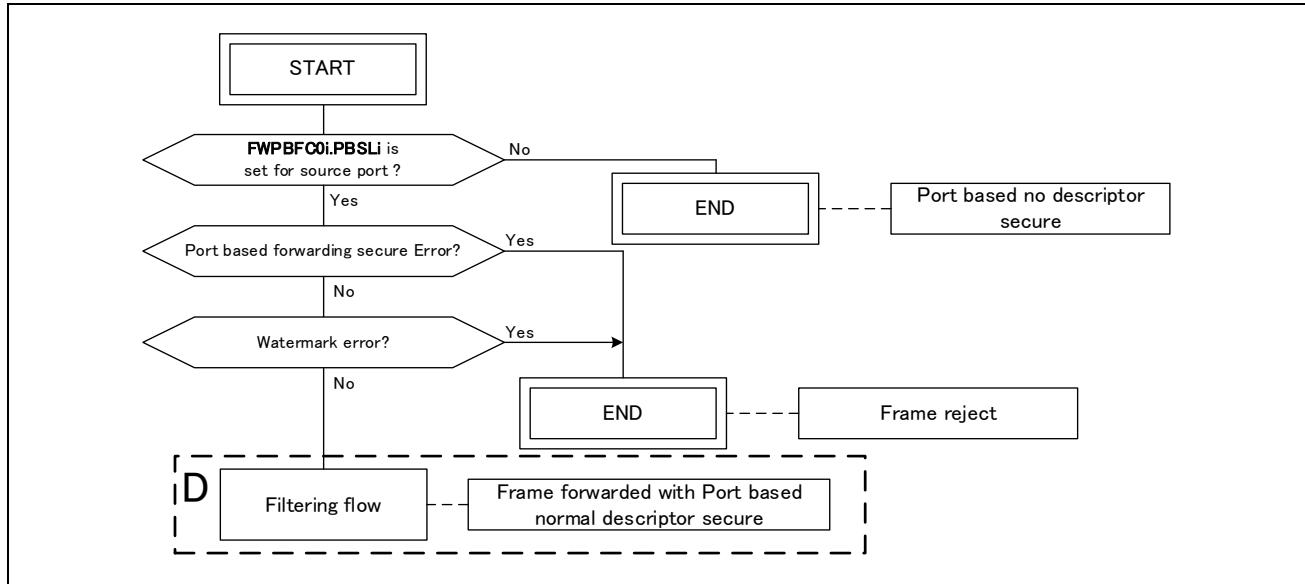


Fig 5.55: Port based forwarding secure flow

Notes:

- Port based forwarding secure errors are described in section Table 5-57.
- Watermark errors are described in section 5.1.6(1).
- Link D links to Fig 5.59: Filtering flow

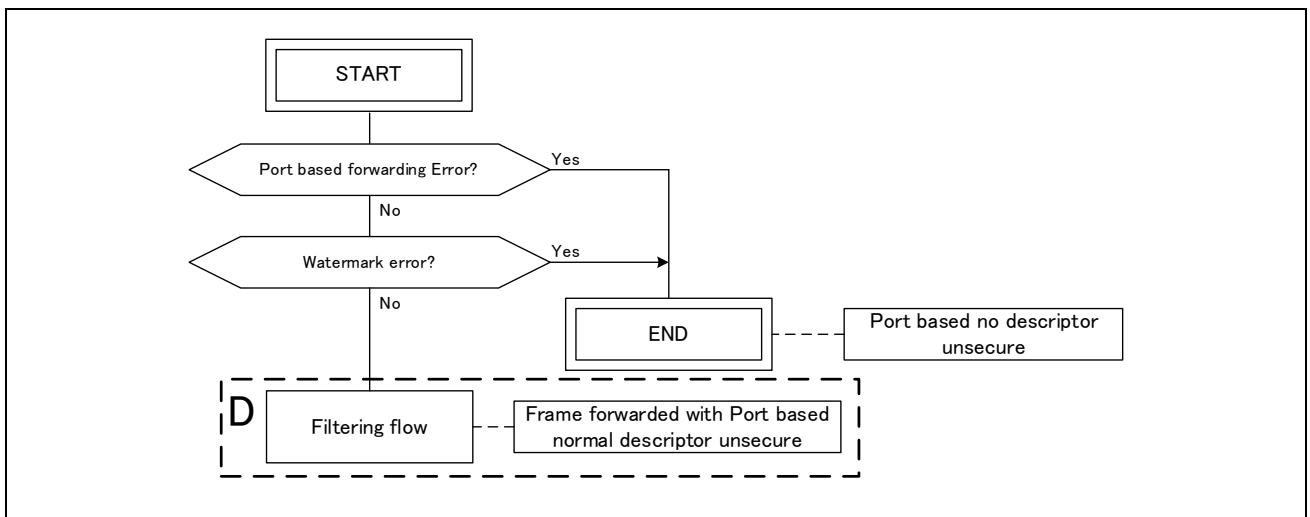


Fig 5.56: Port based forwarding unsecure flow

Notes:

- Port based forwarding errors are described in section Table 5-57.
- Watermark errors are described in section 5.1.6(1).
- Link D links to Fig 5.59: Filtering flow

5.2.7.1 Port based forwarding errors

Table 5-57 describes the Port based forwarding errors. Instead of being discarded by forwarding engine, an error frame can be forwarded to exceptional path using Port based exceptional descriptor described in section 5.2.7.3 by setting corresponding error exceptional bit. For error set conditions, refer to corresponding error interrupt register explanations.

Table 5-57: Port based forwarding Errors

Error	Error name	Error interrupt	Error exceptional bit
Port based forwarding secure errors			
SNTF	Secure No Target Filtering	FWEIS0i.PBNTFSi	FWCEPRC2.FPBNTFEF
SALF	Secure Acceptance List Filtering	FWEIS0i.PBALFSi	FWCEPRC1.FALFEF
SBLF	Secure Block List Filtering	FWEIS0i.PBBLFSi	FWCEPRC1.FBLFEF
Port based forwarding errors			
FSF	Format Security Filtering	FWEIS0i.PBFSSFSi	FWCEPRC2.FPBFSFEF
NTF	No Target Filtering	FWEIS0i.PBNTFSi	FWCEPRC2.FPBNTFEF
ALF	Acceptance List Filtering	FWEIS0i.PBALFSi	FWCEPRC1.FALFEF
BLF	Block List Filtering	FWEIS0i.PBBLFSi	FWCEPRC1.FBLFEF

5.2.7.2 Port based normal descriptor

Port based normal descriptor fields are described in Table 5-58.

Table 5-58: Port based normal descriptor fields

Field name FDESCR.	Values
DV	FWPBFC0i.PBDVi
SEC	FWPBFC0i.PBSLi
CSDj	FWPBFCSDCji.PBCSDji
IPV	if FWPBFC0i.PBIPUi is set, set to FWPBFC0i.PBIPVi if FWPBFC0i.PBIPUi is not set, set to the frame input priority (section 5.1.4)
MINFO	Refer to Fig 5.44 and Table 5-34
RV	1'b0
RN	ALL0
HLD	FWPBFC1i.HLDi
RP	FWPBFC1i.PBRPi
SEQN	Set to frame input sequence number

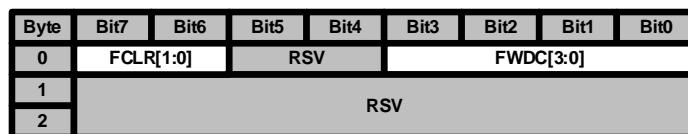


Fig 5.57: Port based normal descriptor MINFO format

Table 5-59: Port based normal descriptor MINFO field explanation

Field name FDESCR.	Bit width	Field explanation	Values
FWDC	4	ForWarDing Code Present in all descriptors, allows to identify the type of forwarding	Fixed to 11 for Port based normal descriptors
FCLR	2	Frame CoLoR	Set to 0 when frame has no color Set to 1 when frame is green Set to 2 when frame is yellow Set to 3 when frame is red Refer to section 5.3.1.3 for color attribution
RSV	--	Reserved field	Set to 0

5.2.7.3 Port based exceptional descriptor

Port based exceptional descriptor fields are described in Table 5-60.

Table 5-60: Port based exceptional descriptor fields

Field name FDESCR.	Values
DV	Exceptional descriptors are forwarded to GWCA number FWCEPTC.EPCS (port number PORT_TIME_N+FWCEPTC.EPCS)
SEC	FWCEPTC.EPSL
CSDj	FWCEPTC.EPCSD
IPV	FWCEPTC.EPIPV
MINFO	Refer to Fig 5.58 and Table 5-61
RV	1'b0
RN	ALL0
SEQN	Set to frame input sequence number

Byte	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	RSV			FSF				FWDC[3:0]
1	RSV	BLF		ALF	NTF	SBLF	SALF	SNTF
2				RSV				

Fig 5.58: Port based exceptional descriptor MINFO format

Table 5-61: Port based exceptional descriptor MINFO field explanation

Field name FDESCR.	Bit width	Field explanation	Values
FWDC	4	ForWarDing Code Present in all descriptors, allows to identify the type of forwarding	Fixed to 12 for Port based exceptional descriptors
FSF	1	Format Security Filtering	Refer to section 5.2.7.1
SNTF	1	Secure No Target Filtering	Refer to section 5.2.7.1
SALF	1	Secure Acceptance List Filtering	Refer to section 5.2.7.1
SBLF	1	Secure Block List Filtering	Refer to section 5.2.7.1
NTF	1	No Target Filtering	Refer to section 5.2.7.1
ALF	1	Acceptance List Filtering	Refer to section 5.2.7.1
BLF	1	Block List Filtering	Refer to section 5.2.7.1

5.2.7.4 Port based Filter exceptional descriptor

Same as 5.2.5.5(5)

5.2.8 Layer2/Layer3 Update

Layer2/Layer3 Update aims at updating frames before sending them. Agents will use the L23 update interface to fetch the update information from the forwarding engine and will automatically update the frames following the Layer2/Layer3 Update rule. Frames Layer2/Layer3 Update information fetching will happen for Layer 3 forwarding, VLAN forwarding , or mirroring frames with respectively **FDESCR.RV** set.

Layer2/Layer3 Update is divided in the following items:

- Rule format: Determines what information will be stored along with the stream ID in the table.
- Learning: Function to add/suppress a Layer2/Layer3 Update rule by software.
- Reading: Function to read a Layer2/Layer3 Update rule by software.
- Rule fetching: Function used by agents to read a Layer2/Layer3 Update rule.

5.2.8.1 Rule format

The Layer2/Layer3 Update RAM is used to store Layer2/Layer3 Update rules. A Layer2/Layer3 Update rule contains the information for the frame routing. All the fields in this table, if quoted, will be written **L23U.{Field name}**. Table 5-62 describes fields contained in a L3 rule.

Table 5-62: Layer2/Layer3 Update rule format

Field name	Field size (bit)	Field Explanation
RPV	PORT_N	<p>Routing Port Valid.</p> <p>Values:</p> <ul style="list-style-type: none"> - Bit i set to 1'b0: Routing rule won't apply for port i. - Bit i set to 1'b1: Routing rule will apply for port i. <p>Functions:</p> <ul style="list-style-type: none"> - If set to all0, this field will disable the corresponding routing entry. <p>In case RPV is 0 for an egress port, the frame is not updated and will be transmitted unmodified.</p>
TTLU	1	<p>TimeToLive update</p> <p>Functions:</p> <ul style="list-style-type: none"> - If this bit is set and the corresponding frame is detected as an IPv4 frame, the TTL field will be decremented by 1 and the header checksum will be updated accordingly. - If this bit is set and the corresponding frame is detected as an IPv6 frame, the HopLimit field will be decremented by 1.
MDAU	1	<p>MAC Destination Address Update</p> <p>Functions:</p> <ul style="list-style-type: none"> - If this bit is set, the rule corresponding frame MAC address will be updated to L23U.MDA.
MSAU	1	<p>MAC Source Address Update</p> <p>Functions:</p> <ul style="list-style-type: none"> - If this bit is set, the rule corresponding frame MAC address will be updated to corresponding agent MAC address.
CVIDU	1	<p>C-tag VLAN ID Update</p> <p>Functions:</p> <ul style="list-style-type: none"> - If this bit is set, the rule corresponding frame C-tag VLAN ID will be updated to L23U.CVID.
CPCPU	1	<p>C-tag PCP Update</p> <p>Functions:</p> <ul style="list-style-type: none"> - If this bit is set, the rule corresponding frame C-tag PCP will be updated to L23U.CPCP.

Field name	Field size (bit)	Field Explanation
CDEIU	1	<p>C-tag DEI Update</p> <p>Functions:</p> <ul style="list-style-type: none"> - If this bit is set, the rule corresponding frame C-tag DEI will be updated to L23U.CDEI.
SVIDU	1	<p>S-tag VLAN ID Update</p> <p>Functions:</p> <ul style="list-style-type: none"> - If this bit is set, the rule corresponding frame S-tag VLAN ID will be updated to L23U.SVID.
SPCPU	1	<p>S-tag PCP Update</p> <p>Functions:</p> <ul style="list-style-type: none"> - If this bit is set, the rule corresponding frame S-tag PCP will be updated to L23U.SPCP.
SDEIU	1	<p>S-tag DEI Update</p> <p>Functions:</p> <ul style="list-style-type: none"> - If this bit is set, the rule corresponding frame S-tag DEI will be updated to L23U.SDEI.
RTU	2	<p>R-TAG update</p> <p>Values:</p> <ul style="list-style-type: none"> - 2'b00: Frame received without R-TAG will be forwarded without R-TAG, Frame received with R-TAG will be forwarded with an R-TAG containing FDESCR.SEQN sequence number. - 2'b01: All frames will be forwarded with an R-TAG containing FDESCR.SEQN sequence number (used for sequence number generation, refer to section 5.3.2.2). - 2'b10: All frames will be forward without R-TAG (used to strip R-TAG after elimination, refer to section 5.3.2.3(1)).
TC	3	<p>TAG Configuration for tagging/un-tagging</p> <ul style="list-style-type: none"> - 3'h0: No function. - 3'h1: Tagging C-TAG of L23U.CVID/CPCP/CDEI for the NO-TAG frame. - 3'h2: Tagging S-TAG of L23U.SVID/SPCP/SCDEI for the C/CoS-TAG frame. Tagging SC-TAG of L23U.SVID/SPCP/SCDEI and L23U.CVID/CPCP/CDEI for the NO-TAG frame. - 3'h3: Tagging C-TAG of [GWCA/TSNA] port based TAG for the NO-TAG frame. - 3'h4: Tagging S-TAG of [GWCA/TSNA] port based TAG for the C/CoS-TAG frame. Tagging SC-TAG of [GWCA/TSNA] port based TAGs for the NO-TAG frame. - 3'h5: Un-tagging C-TAG and SC-TAG. - 3'h6: Un-tagging S-TAG.
MDA	48	<p>MAC Destination Address</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used to update MAC destination address.
CVID	12	<p>C-tag VLAN ID</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used to update C-tag VLAN ID.
CPCP	3	<p>C-tag PCP</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used to update C-tag PCP.
CDEI	1	<p>C-tag DEI</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used to update C-tag DEI.
SVID	12	<p>S-tag VLAN ID</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used to update S-tag VLAN ID.
SPCP	3	<p>S-tag PCP</p> <p>Functions:</p> <ul style="list-style-type: none"> - Used to update S-tag PCP.

Field name	Field size (bit)	Field Explanation
SDEI	1	<p>S-tag DEI</p> <p>Functions:</p> <ul style="list-style-type: none">- Used to update S-tag DEI.

5.2.8.2 SW Learning

Learning is used to add/remove an entry in the Layer2/Layer3 Update rule table. Table 5-63 describes register used to learn an entry in the Layer2/Layer3 Update rule table. Table 5-64 describes the learn results.

Table 5-63: Layer2/Layer3 Update rule learn registers

Register name	Field name/corresponding field in I23u table	Field explanation
FWL23URL0.L23RNL	Routing number Learn	Address that will be used to learn an entry in the Layer2/Layer3 Update rule table
FWL23URL0.L23RPVL	L23U.RPV	Refer to section 5.2.8.1
FWL23URL1.L23UTTLUL	L23U.TTLLU	Refer to section 5.2.8.1
FWL23URL1.L23UMDAUL	L23U.MDAU	Refer to section 5.2.8.1
FWL23URL1.L23UMSAUL	L23U.MSAU	Refer to section 5.2.8.1
FWL23URL1.L23UCVIDUL	L23U.CVIDU	Refer to section 5.2.8.1
FWL23URL1.L23UCPCPUL	L23U.CPCPU	Refer to section 5.2.8.1
FWL23URL1.L23UCDEIUL	L23U.CDEIU	Refer to section 5.2.8.1
FWL23URL1.L23USVIDUL	L23U.SVIDU	Refer to section 5.2.8.1
FWL23URL1.L23USPCPUL	L23U.SPCPU	Refer to section 5.2.8.1
FWL23URL1.L23USDEIUL	L23U.SDEIU	Refer to section 5.2.8.1
FWL23URL1.L23URTUL	L23U.RTU	Refer to section 5.2.8.1
FWL23URL1.L23UTCL	L23U.TC	Refer to section 5.2.8.1
FWL23URL1.L23UMDALP0/ FWL23URL2.L23UMDALP1	L23U.MDA	Refer to section 5.2.8.1
FWL23URL3.L23UCVIDL	L23U.CVID	Refer to section 5.2.8.1
FWL23URL3.L23UCPCPL	L23U.CPCP	Refer to section 5.2.8.1
FWL23URL3.L23UCDEIL	L23U.CDEI	Refer to section 5.2.8.1
FWL23URL3.L23USVIDL	L23U.SVID	Refer to section 5.2.8.1
FWL23URL3.L23USPCPL	L23U.SPCP	Refer to section 5.2.8.1
FWL23URL3.L23USDEIL	L23U.SDEI	Refer to section 5.2.8.1

Table 5-64: Layer2/Layer3 Update rule learn result

Register name	Field name/corresponding field in I23u table	Field explanation
FWL23URLR.L23ULF	Learning fail	Learning fail with happen in one of the following conditions: - The Layer2/Layer3 table is not ready (FWL23UTIM.L23UTR is not set)
FWL23URLR.L23ULSF	Learning security fail	Security fail with happen in one of the following conditions: - The learn action is done by the unsecure APB and the corresponding entry for learning is secure (corresponding FWSCR27/28/29/30/31/32/33/34.L23URSL[i] is not set).

5.2.8.3 SW Reading

Reading is used to read an entry in the Layer2/Layer3 Update rule table. Table 5-65 describes register used to read an entry in the Layer2/Layer3 Update rule table. Table 5-66 describes the read results.

Table 5-65: Layer2/Layer3 Update rule read registers

Register name	Field name/corresponding field in L23u table	Field explanation
FWL23URR.L23RNR	Routing number Read	Address that will be used to read an entry in the Layer2/Layer3 Update rule table

Table 5-66: Layer2/Layer3 Update rule read result

Register name	Field name/corresponding field in L23u table	Field explanation
FWL23URRR0.L23UREF	Read ECC fail	Reading failed because of an ECC error.
FWL23URRR0.L23URPVR	L23U.RPV	Refer to section 5.2.8.1
FWL23URRR1.L23UTTLUR	L23U.TTLU	Refer to section 5.2.8.1
FWL23URRR1.L23UMDAUR	L23U.MDAU	Refer to section 5.2.8.1
FWL23URRR1.L23UMSAUR	L23U.MSAU	Refer to section 5.2.8.1
FWL23URRR1.L23UCVIDUR	L23U.CVIDU	Refer to section 5.2.8.1
FWL23URRR1.L23UCPCPUR	L23U.CPCPU	Refer to section 5.2.8.1
FWL23URRR1.L23UCDEIUR	L23U.CDEIU	Refer to section 5.2.8.1
FWL23URRR1.L23USVIDUR	L23U.SVIDU	Refer to section 5.2.8.1
FWL23URRR1.L23USPCPUR	L23U.SPCPU	Refer to section 5.2.8.1
FWL23URRR1.L23USDEIUR	L23U.SDEIU	Refer to section 5.2.8.1
FWL23URRR1.L23URTUR	L23U.RTU	Refer to section 5.2.8.1
FWL23URRR1.L23UTCR	L23U.TC	Refer to section 5.2.8.1
FWL23URRR1.L23UMDARP0/ FWL23URRR2.L23UMDARP1/	L23U.MDA	Refer to section 5.2.8.1
FWL23URRR3.L23UCVIDR	L23U.CVID	Refer to section 5.2.8.1
FWL23URRR3.L23UCPCPR	L23U.CPCP	Refer to section 5.2.8.1
FWL23URRR3.L23UCDEIR	L23U.CDEI	Refer to section 5.2.8.1
FWL23URRR3.L23USVIDR	L23U.SVID	Refer to section 5.2.8.1
FWL23URRR3.L23USPCPR	L23U.SPCP	Refer to section 5.2.8.1
FWL23URRR3.L23USDEIR	L23U.SDEI	Refer to section 5.2.8.1

Restrictions:

- HW: If the unsecure APB accesses to a secure entry for reading, the read will return all0 for read fields.

5.2.8.4 HW Reading

Hardware reading is used by agents [GWCA][TSNA] to fetch the Layer2/Layer3 Update rule corresponding to a frame and update the frame. The read result is given to agents to perform Layer2/Layer3 update along with **L23U.ERR** which is used to notify to agents that an ECC error happened while reading the entry and that the corresponding data should be rejected.

5.2.8.5 Routing number remapping function

The routing number remapping function is used to change the routing number for a specific port using **FWL23URMCi** register. That way, different ports can use different Routing Rules for the same frame. It can be used for FRER during replication (section 5.3.2.1) to send a duplicated frame through several ports with a different stream ID.

Functions:

- When **FWL23URMCi.RMEi** is set, a frame from port **FWL23URMCi.RMSPNi** with **FDESCR.RV** set and **FDESCR.RN** equal to **FWL23URMCi.RMRNi** will be routed with rule number **FWL23URMCi.RMNRNi**.

5.3 Filtering

Forwarding engine allows frame filtering and shaping using the following functions:

- PSFP (Per Stream Filtering and Policing) [802.1Qci]
- ATS (Asynchronous Traffic Shaping) [802.1Qcr]
- FRER (Frame Replication and Elimination for Reliability) [802.1CB]

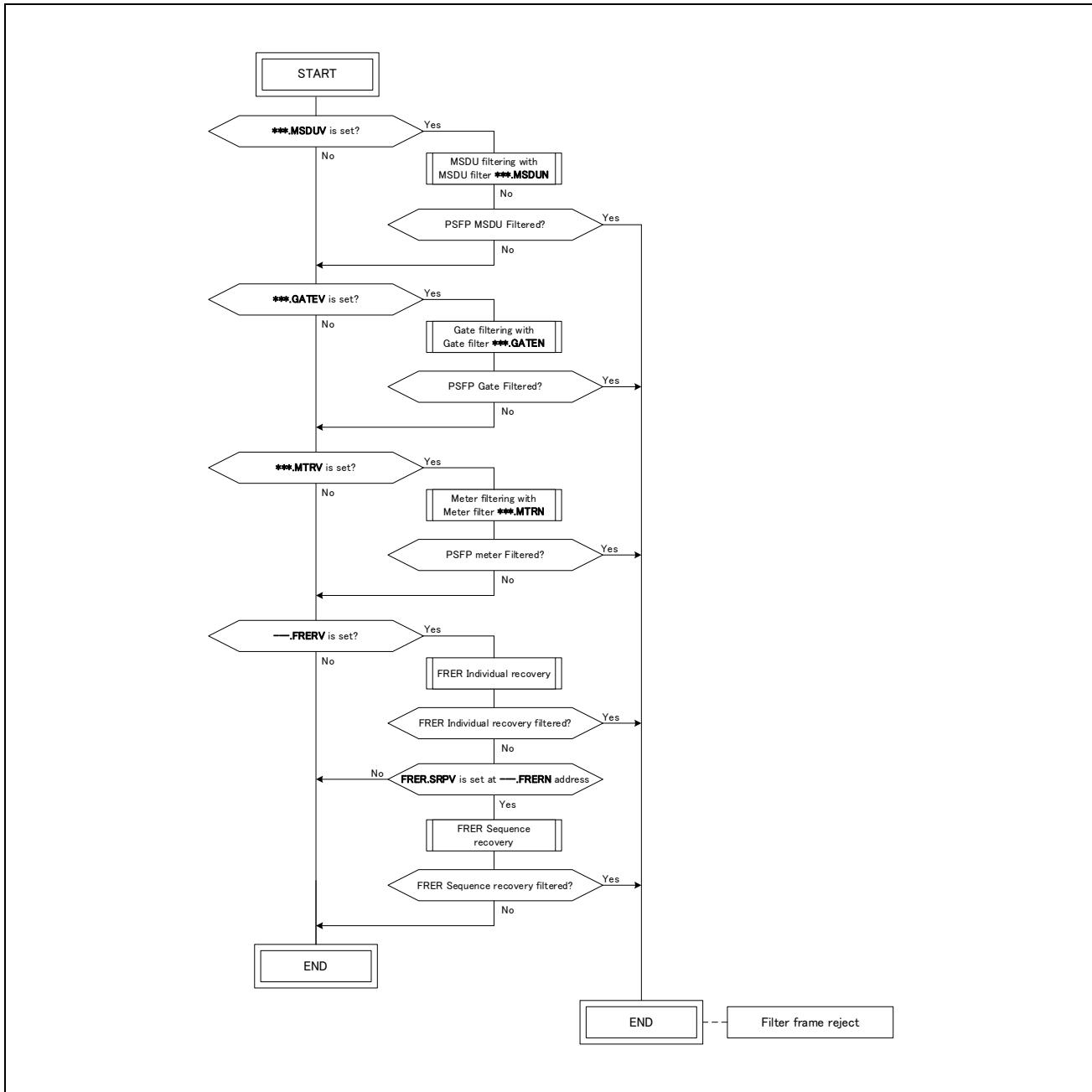


Fig 5.59: Filtering flow

Notes:

- *** is selected from the following. The rule with the highest valid FP(Filtering Priority) is selected.

L3, MAC, VLAN, FWPIFPlj.

If the FP values are the same, the priority is controlled as follows:

FWPIFPlj > VLAN > MAC > L3(L2 stream) > L3 stream > Cascade filter)

- --- is selected from the follow. The rule with the selected forwarding.

L3, MAC or VLAN

- Filter frame reject is described in section 5.2.5.5(2).
- MSDU filtering is described in Fig 5.60.
- Gate filtering is described in Fig 5.66.
- Meter filtering is described in Fig 5.67.
- Individual recovery is described in section 5.3.2.3(2)(e)5.3.2.3(2)(e).
- Sequence recovery is described in section 5.3.2.3(2)(f).

5.3.1 PSFP/ATS

PSFP functions is divided in three functions that happen sequential following forwarding flow in Fig 5.59:

- MSDU filter
- Gate filter
- Meter filter/ATS

5.3.1.1 MSDU filter

The MSDU filter aims at checking frame size using **FWPMFGCi** register and can be monitored using **FWEIS2** interrupt register. MSDU filtering flow for MSDU filter i is described in Fig 5.60.

Functions:

- **FWPMFGCi** is used to set MSDU filter number i maximum frame size and mode.
- **FWEIS2** interrupt register notifies that an ethernet descriptor has been rejected because of an error.

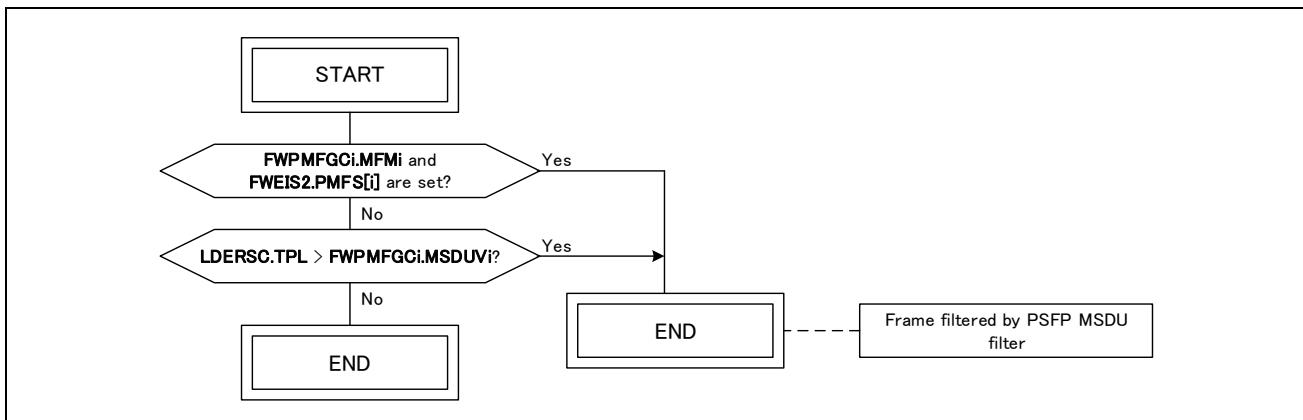


Fig 5.60: MSDU filtering flow for MSDU filter i

5.3.1.2 Gate filter

The Gate filter aims at checking the incoming timing of a frame using a scheduler and can also update a frame IPV value depending on its ingress timing using **FWPGFCi**, **FWPGFIGSCi**, **FWPGFENCi**, **FWPGFCSTC0i/1i**, **FWPGFCTCi**, **FWPGFHCCI**, **FWPGFGCi**, **FWPGFGL0/1**, **FWPGFGLR** registers and can be monitored using **FWPGFENMi**, **FWPGFCSTM0i/1i**, **FWPGFCTMi**, **FWPGFSMi**, **FWPGFGR**, **FWPGFRR0/1**, **FWPGFRIM** registers and **FWEIS3/4** interrupt registers.

Functions:

- **FWPGFCi** register is used to configure and enable Gate Filter i scheduler.
- **FWPGFIGSCi** register is used to set the initial gate states for Gate Filter scheduler i.
- **FWPGFENCi** register is used to set the number of entries used in Gate RAM by Gate Filter scheduler i.
- **FWPGFCSTC0i/1i** registers are used to set the cycle start time for Gate Filter scheduler i.
- **FWPGFCTCi** register is used to set the cycle time for Gate Filter scheduler i.
- **FWPGFHCCI** is used to set the Gate Filter scheduler i jitter caused by to the switch architecture.
- **FWPGFGCi**, register is used to set the filtering modes for Gate Filter i.
- **FWPGFGL0/1** and **FWPGFGLR** registers are used to write entries in the Gate RAM.
- **FWPGFENMi** register is used to monitor the number of entries used in the Gate RAM by Gate Filter i scheduler for the ongoing schedule.
- **FWPGFCSTM0i/1i** registers are used to monitor the next cycle start time for the ongoing schedule for Gate Filter i scheduler.
- **FWPGFCTMi** register is used to monitor the cycle time for the ongoing schedule for Gate Filter i scheduler.
- **FWPGFSMi** register is used to monitor Gate Filter i scheduler operation.
- **FWPGFGR** and **FWPGFRR0/1** registers are used to read entries in the PSFP Gate RAM.
- **FWPGFRIM** register is used to initialize Gate RAM entries to All0.
- **FWEIS3/4** interrupt registers notify that an error happened.

Restrictions:

- HW: Gate filtering will always be ignored for slow agents [GWCA].

(1) Gate filter scheduler general behavior

Each gate filter scheduler general behavior is the same as “TAS general behavior” function in TSNA. Refer to TSNA specification for more details [TSNA] (The correspondence between TSNA and Forwarding Engine registers/signals is described in Table 5-67).

Table 5-67: Descriptor store TSNA/Forwarding Engine register/signal correspondence

Register/signal name in TSNA [TSNA]	Register/signal name in Forwarding Engine for gate filter scheduler i
EATASC.TASE	FWPGFCi.GFEi
EATASC.TASCC	FWPGFCi.GCCI
EATASIGSC.TASCTIGS EATASIGSC.TASIGS	FWPGFIGSCI.GFIGSI Each gate filter scheduler only contains one gate of 4 bits (3 bits for IPV and 1 bit for gate state)
EATASENCi EATASCTENC	FWPGFENCi Each gate filter scheduler only contains one setting for entry number because it contains only one gate
EATASENMi EATASCTENM	FWPGFENMi
{EATASCSTC1, EATASCSTC0}	{FWPGFCSTC1i, FWPGFCSTC0i}
{EATASCSTM1, EATASCSTM0}	{FWPGFCSTM1i, FWPGFCSTM0i}
EAPASCTC	FWPGFCTCi
EAPASCTM	FWPGFCTMi

(a) Gate schedule

Gate schedule defines at which moment of a cycle a frame is allowed to be received. A Gate schedule should be learnt in the Gate RAM using Gate RAM learning functionality. Gate entry format, Gate entry learning function, Gate entry reading function and conversion between Gate schedule to a set of Gate entries are described in this section.

(b) Gate entry format

The Gate RAM is used to store gate entries which compose Gate schedules. A Gate entry contains the information of a gate state. All the fields in this table, if quoted, will be written **GATE.{Field name}**. Table 5-68 describes fields contained in a Gate entry.

Table 5-68: Gate entry format

Field name	Field size (bit)	Field Explanation
GS	4	Gate state Values for bit 0: - 1'b0: Gate state is closed - 1'b1: Gate state is opened Functions for bit [3:1]: - Gate state corresponding IPV value
GT	28	Gate time Functions: - Values of time in nanoseconds associated to the entry gate state GATE.GS

(c) Gate entry learning

Learning is used to overwrite entries in the Gate RAM. Table 5-69 describes register used to learn an entry in the Gate RAM. Table 5-70 describes the learn results.

Table 5-69: Gate entry learn registers

Register name	Field name/corresponding field in Gate RAM	Field explanation
FWPGFGL0.GFGAL	Entry address	Not present in Gate RAM, new entry will be written at this address
FWPGFGL1.GFGSL	GATE.GS	Refer to section 5.3.1.2(1)(b)
FWPGFGL1.GFGSL	GATE.GT	Refer to section 5.3.1.2(1)(b)

Table 5-70: Gate entry learn results

Register name	Field name/corresponding field in Gate RAM	Field explanation
FWPGFGLR.GLSF	Learning security fail	<p>Security fail with happen in one of the following conditions:</p> <ul style="list-style-type: none"> - The learn action is done by the unsecure APB and the gate entry is learnt to an address in a secure scheduler (corresponding FWSCR39.PGATERSL[i] is not set) - The learn action is done by the secure APB and the gate entry is learnt to an address in an unsecure scheduler (corresponding FWSCR39.PGATERSL[i] is set)

(d) Gate entry reading

Reading is used to read entries in the Gate RAM. Table 5-71 describes register used to read an entry in the Gate RAM. Table 5-72 describes the read results.

Table 5-71: Gate entry read registers

Register name	Field name/corresponding field in Gate RAM	Field explanation
FWPGFGR.GFGAR	Entry address	Not present in Gate RAM, entry will be read from this address

Table 5-72: Gate entry read result

Register name	Field name/corresponding field in Gate RAM	Field explanation
FWPGFGR1.GFGSR	Gate.GS	Refer to section 5.3.1.2(1)(b)
FWPGFGR1.GFGTR	Gate.GT	Refer to section 5.3.1.2(1)(b)
FWPGFGR0.GFREF	Reading ECC Fail	Reading failed because of an ECC error.

(e) Conversion between Gate schedule to a set of Gate entries

■ Schedule example

Fig 5.61 describes a basic schedule example for Gate scheduler i with basic gate behavior and recommendations about what not to do while designing a schedule.

FWPGFCTMi.GFOCTi					
① Gate state	Open	Close	Open	Close	
IPV	3	0	7	6	0
	②		③		②
(1) Frames are allowed in reception when Gate state is opened (2) When Gate state is closed, IPV should be set to 0 (3) It is possible to change the IPV value and keep gate state opened					

Fig 5.61: Schedule example and recommendations

Restrictions:

- SW: A Gate filter aims at checking that incoming frame shaped by a TAS module are coming in at the right timing. That is why a Gate schedule should be the same schedule than the TAS gate being verified.

■ Schedule setting

Fig 5.62 describes how to convert a schedule into a set of Gate entries and how to set the schedule corresponding register through two examples.

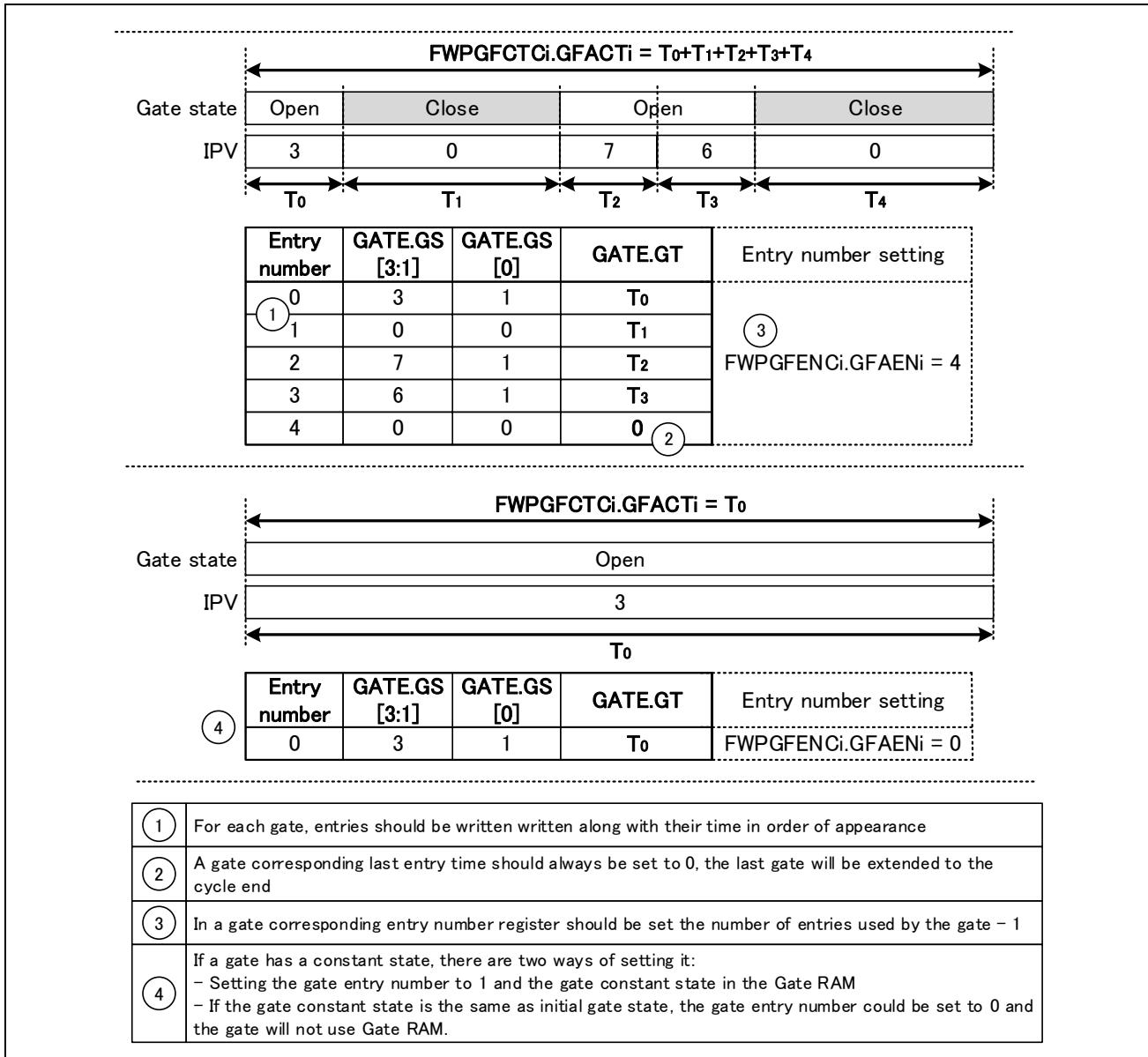


Fig 5.62: Schedule example

Restrictions:

- SW: Each gate time (T₀, T₁, T₂, T₃ in Fig 5.62) should be bigger or equal to 50ns (minimum gate time).

(2) Gate scheduler hardware calibration

Gate scheduler filtering happens at the input snooping bus of the forwarding engine. Because of that, there is an internal minimum latency and an internal maximum jitter (Fig 5.63) that should be taken in account while setting a Gate scheduler module. Latency calibration should be handled by SW and jitter calibration should be set by SW and will be handled by HW. In this section will be described how to calibrate a Gate scheduler module in latency and jitter from the PHY interface [RMAC], but, by adding, for example, the minimum latency and the maximum jitter from the previous IP TAS module, it can be possible to calibrate the Gate scheduler to it.

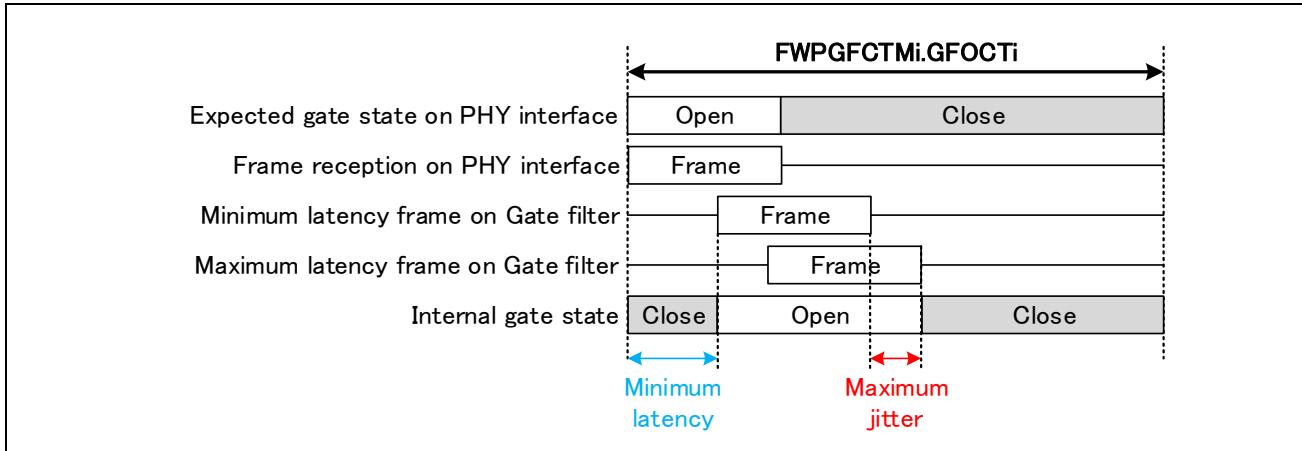


Fig 5.63: Minimum latency and maximum jitter

(a) Latency calibration

Because of the internal minimum latency, with a non-calibrated schedule a frame could be rejected because it would be considered as being received late on the PHY interface [RMAC]. To correct this phenomenon, the Gate schedule should always be late compared to the expected schedule of the minimum latency between the actual reception on the PHY interface and the Gate filtering (Fig 5.64). This minimum latency is described in Table 5-73. To calibrate the schedule, the software should always add the minimum latency to the cycle start time before setting it in **FWPGFCSTC0i/1i** registers.

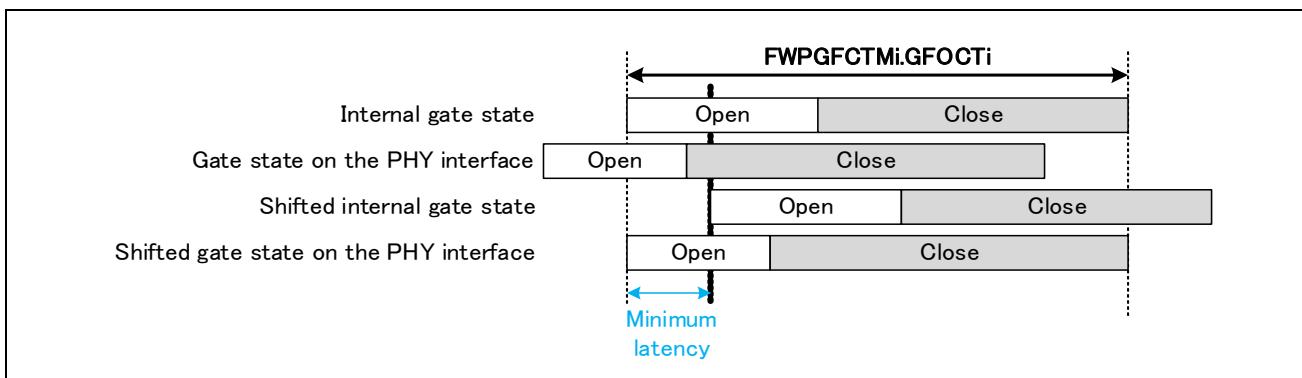


Fig 5.64: Minimum latency calibration

Table 5-73: Minimum latency values

PHY speed	Only E-frames are checked by corresponding gate
10Mbps	$4 * \text{clk_phy_rx_period}[ns] + 25 * \text{clk_period}[ns] + \text{fabricLatency}[ns] + \text{MACsecLatency}[ns]$
100Mbps	$5 * \text{clk_phy_rx_period}[ns] + 25 * \text{clk_period}[ns] + \text{fabricLatency}[ns] + \text{MACsecLatency}[ns]$
1Gbps	$9 * \text{clk_phy_rx_period}[ns] + 25 * \text{clk_period}[ns] + \text{fabricLatency}[ns] + \text{MACsecLatency}[ns]$
2.5Gbps	$6 * \text{clk_phy_rx_period}[ns] + 25 * \text{clk_period}[ns] + \text{fabricLatency}[ns] + \text{MACsecLatency}[ns]$
5Gbps	$8 * \text{clk_phy_rx_period}[ns] + 25 * \text{clk_period}[ns] + \text{fabricLatency}[ns] + \text{MACsecLatency}[ns]$
10Gbs	$14 * \text{clk_phy_rx_period}[ns] + 25 * \text{clk_period}[ns] + \text{fabricLatency}[ns] + \text{MACsecLatency}[ns]$
PHY speed	P-frames and E-frames or only P-frames are checked by corresponding gate
10Mbps	$4 * \text{clk_phy_rx_period}[ns] + 25 * \text{clk_period}[ns] + \text{fabricLatency}[ns] + \text{MACsecLatency}[ns]$
100Mbps	$5 * \text{clk_phy_rx_period}[ns] + 25 * \text{clk_period}[ns] + \text{fabricLatency}[ns] + \text{MACsecLatency}[ns]$
1Gbps	$5 * \text{clk_phy_rx_period}[ns] + 25 * \text{clk_period}[ns] + \text{fabricLatency}[ns] + \text{MACsecLatency}[ns]$
2.5Gbps	$5 * \text{clk_phy_rx_period}[ns] + 25 * \text{clk_period}[ns] + \text{fabricLatency}[ns] + \text{MACsecLatency}[ns]$
5Gbps	$5 * \text{clk_phy_rx_period}[ns] + 25 * \text{clk_period}[ns] + \text{fabricLatency}[ns] + \text{MACsecLatency}[ns]$
10Gbs	$5 * \text{clk_phy_rx_period}[ns] + 25 * \text{clk_period}[ns] + \text{fabricLatency}[ns] + \text{MACsecLatency}[ns]$

Where:

- clk_phy_rx_period is the clock clk_phy_rx period for the ethernet agent from which the data comes [TSNA].
- clk_period is the clock clk period.
- fabricLatency is the latency induced by the fabric. Refer to fabric specification document for calculation [FAB].
- $\text{MACsecLatency} = \text{Please refer to Latency_RX_MIN [MACsec]} (\text{If disabling MACsec, this is 0})$

(b) Jitter calibration

Because of the internal maximum jitter, with a non-calibrated schedule a frame could be rejected because it would be considered as being received late on the PHY interface [RMAC]. To correct this phenomenon, a Gate schedule opened gate should always be closed late compared to the expected close time of the maximum jitter (Fig 5.65). This maximum jitter should be calculated using equation (4) and converted in clock clk using equation (5) . To calibrate the schedule, software should set the maximum jitter in clocks in **FWPGFHCCi.GFJi** register.

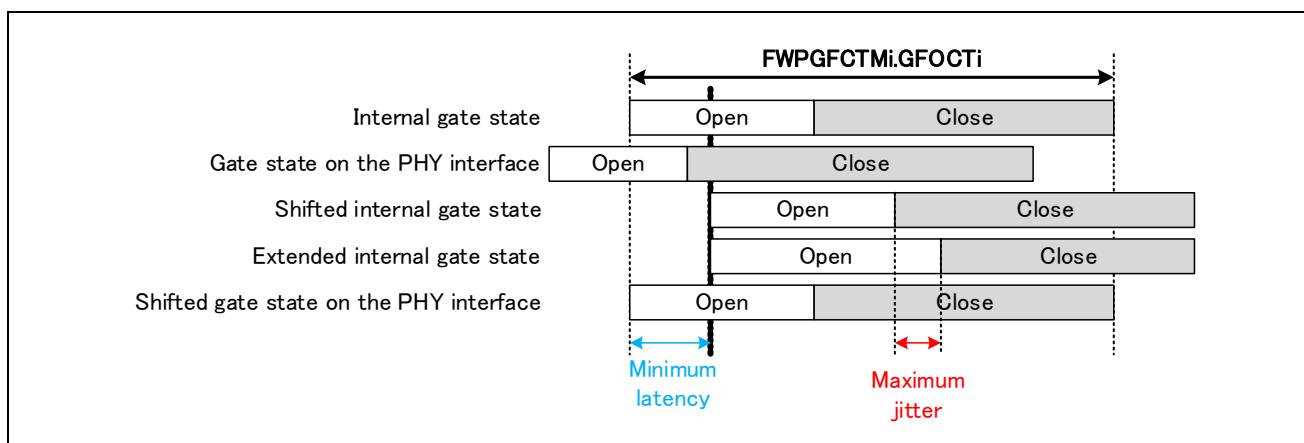


Fig 5.65: Maximum jitter calibration

$$(4) \text{ jitter}[ns] = \text{gateInternalJitter}[ns] + \text{fabricJitter}[ns] + \text{preemptionJitter}[ns] - \text{MACsecReduced}[ns] + \text{MACsecJitter}[ns] + \text{asynchronousJitter}[ns] + \text{gptpSyncJitter}[ns] + \text{clkDerivationJitter}[ns]$$

$$(5) jitter[clk] = jitter[ns] / clk_period[ns] + 1$$

Where:

- *gate_internal_jitter* is the jitter induced by Gate scheduler module and is equal to $2 * clk_period[ns]$ where *clk_period* is the clock clk period.
- *fabricJitter* is the jitter induced by the fabric. Refer to fabric specification document for calculation [FAB].
- *preemptionJitter* is the jitter induced by preemption and is equal to 15-byte time on the PHY interface (Time to transmit 15 bytes on the current PHY interface). This jitter can be set to 0 if the frames being checked by the corresponding are only E-frames.
- *MACsecReduced[ns]* = Actual transmitting time of "TAG and ICV adding by MACsec".
- *MACsecJitter[ns]* = Please refer to *Latency_RX_MAX – Latency_RX_MIN [MACsec]* (If disabling MACsec, this is 0)
- *asynchronousJitter* is the jitter induced by the asynchronous conversion in RMAC [RMAC] and is equal to *clk_period[ns] + clk_phy_rx_period* where *clk_period* is the clock clk period and *clk_phy_rx_periods* the clock *clk_phy_rx* period (*clk_phy_rx* correspond to the source TSNA *clk_phy_rx* clock [TSNA]).
- *gptpSyncJitter* is the jitter induced by gPTP synchronization between the gPTP master clock and the gPTP slave clock.
- *clkDerivationJitter* is the jitter induced by clock derivation between the gPTP clock *clk* and the PHY TX clock *clk_phy_rx* (*clk_phy_rx* correspond to the source TSNA *clk_phy_rx* clock [TSNA]) and is equal to *clkRelativeDerivation * maxGateTime[ns]* where *clkRelativeDerivation* is the clock derivation and *maxGateTime* is the longest opened gate in the Gate schedule. *clkRelativeDerivation* is equal to 0 when TAS corresponding gPTP timer is the master and the gPTP clock is phase synchronous to the RX PHY clock.
- *clk_period* is the clock clk period.

(3) Gate filtering

Gate filtering uses the schedule made by a Gate scheduler to determine if a frame reception timing is correct. Gate filtering flow for Gate filter i is described in Fig 5.66.

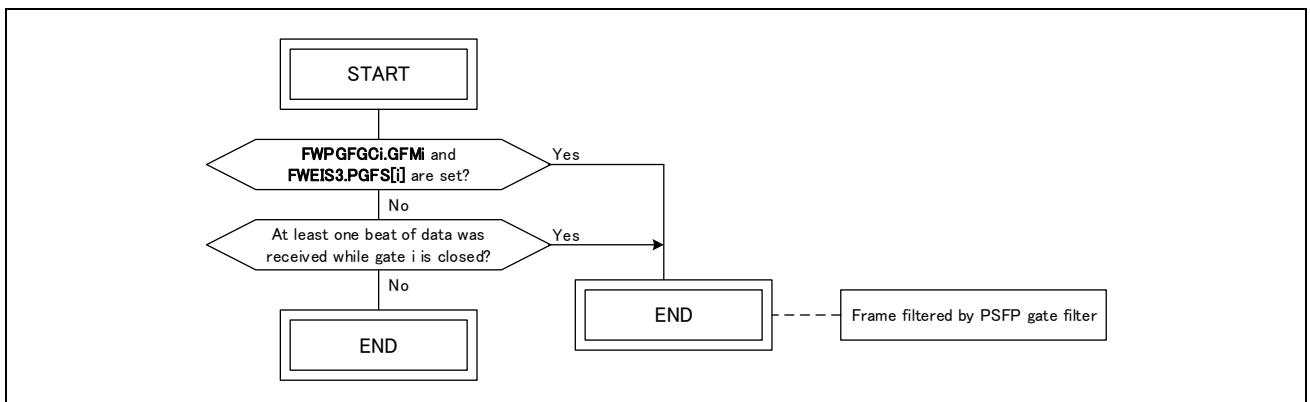


Fig 5.66: Gate filtering flow for Gate filter i

5.3.1.3 Meter filter/ATS

The meter filter aims at checking a stream throughput or, in ATS, at controlling a stream throughput using **FWPMTRFCi**, **FWPMTRCBSCi**, **FWPMTRCIRCi**, **FWPMTREBSCi**, **FWPMTREIRCi** registers and can be monitored using **FWPMTRFMi** register and, **FWEIS1.AREES** and **FWEIS50/51** interrupt registers. Meter filtering flow for meter i is described in Fig 5.67.

Functions:

- **FWPMTRFCi** register is used to set Meter filter i modes.
- **FWPMTRCBSCi** and **FWPMTRCIRCi** registers are used to set Meter filter i green bucket.
- **FWPMTREBSCi** and **FWPMTREIRCi** registers are used to set Meter filter i yellow bucket.
- **FWPMTRFMi** is used to monitor ATS shaper i.
- **FWEIS1.AREES** interrupt register notifies that a descriptor has been lost because of an ECC error.
- **FWEIS50/51/52/53** interrupt register notifies that an ethernet descriptor has been rejected because of an error.

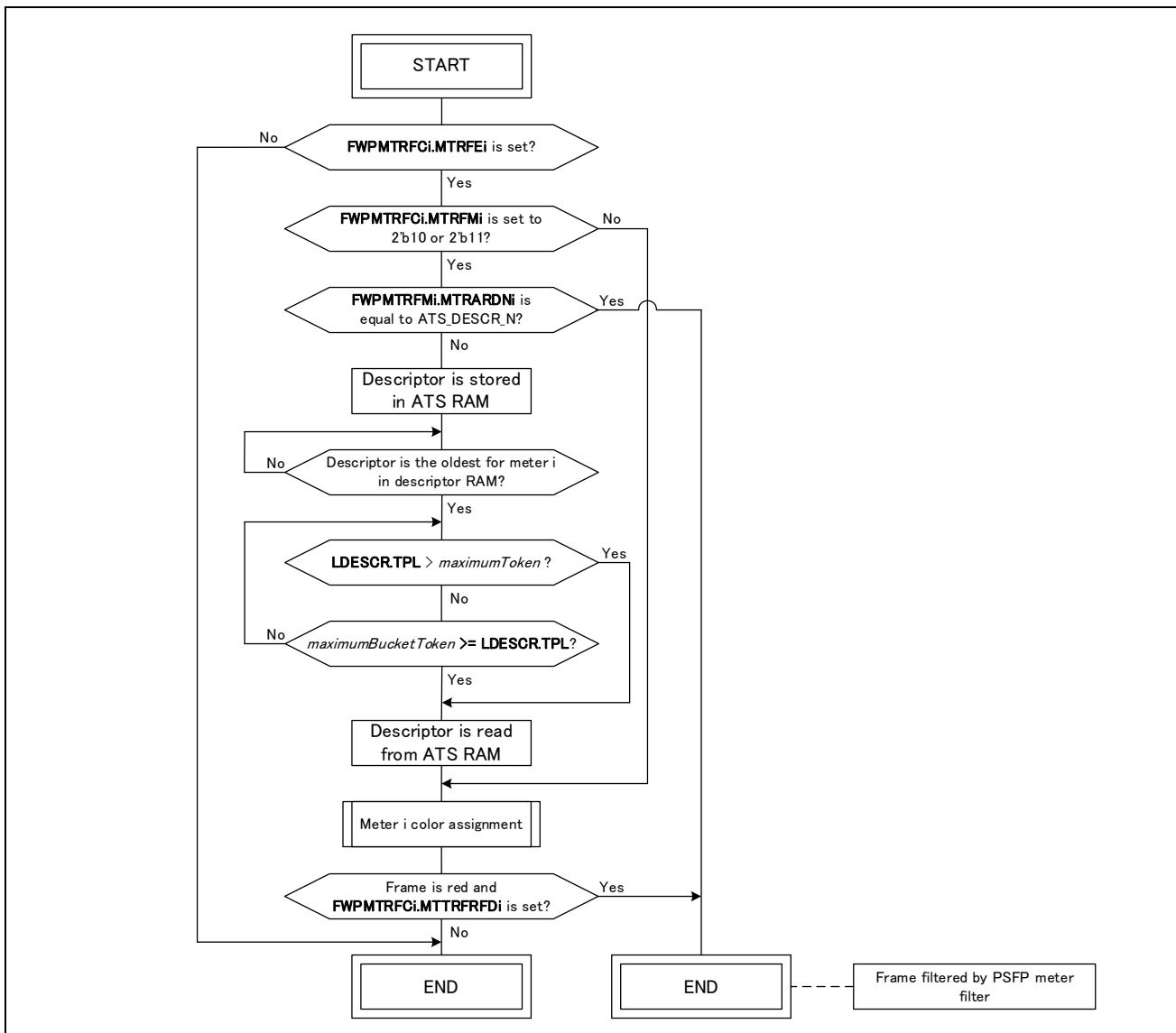


Fig 5.67: Meter filtering flow for meter i

Notes:

- For Meter i color assignment refer to Fig 5.68 and Fig 5.69
- In Fig 5.67, *maximumToken* is the maximum number of tokens that can be contained in one meter biggest bucket. For Double bucket meters, it corresponds to the maximum value between **FWPMTRCBSCi** and **FWPMTREBSCi** and for Single bucket meters, it corresponds to **FWPMTRCBSCi** value. Any frame rejected by "**LDESCR.TPL** [GWCA] > *maximumToken*" condition will be marked as red.
- In Fig 5.67, *maximumBucketToken* is, for a double bucket the maximum number between the number of tokens actually contained in the yellow bucket and the number of tokens actually contained in the green bucket, for a single bucket the number of tokens actually contained in the green bucket.
- In Fig 5.67, any frame rejected by "**FWPMTRFMi.MTRARDNi**" is equal to **ATS_DESCR_N**" conditions (meter corresponding ATS descriptor queue full) will have no color.

Recommendations:

- For every L3 rule mapped to a meter, it is recommended to map also an MSDU filter with a value smaller or equal to the meter corresponding *maximumToken* value. It will allow to know that whenever **FWEIS50/51/52/53.PMRFS[i]** is set, it is due to an ATS RAM overflow in ATS mode and due to a maximum throughput reached error in other modes and, not due to a frame format error (frame being too big for the corresponding meter).

(1) Double bucket meters

Double bucket meters aim at giving a color to a frame. Meters from meter number 0 to meter number PSFP_DMTR_N-1 are Double bucket meters.

(a) Double bucket color assignment

Double bucket meter i color assignment flow is described in Fig 5.68.

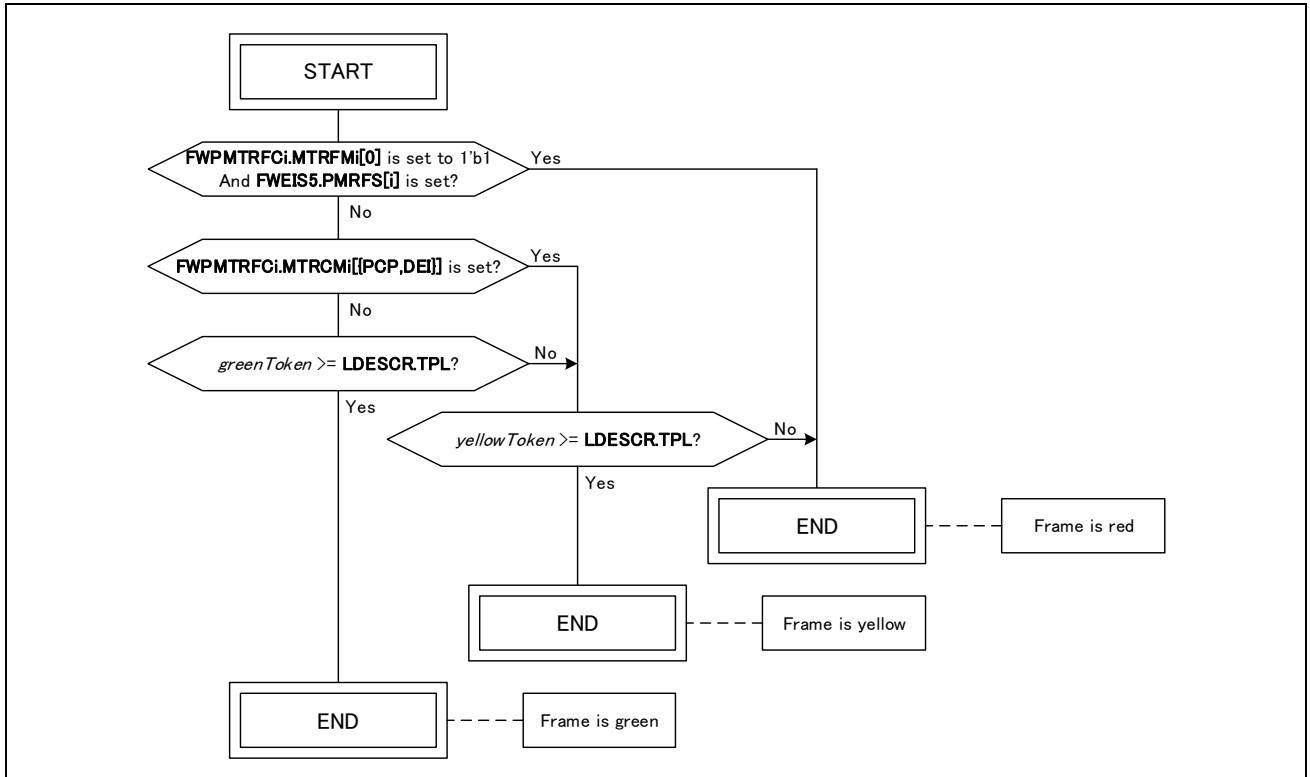


Fig 5.68: Double bucker meter i color assignment flow

In Fig 5.68:

- PCP and DEI are respectively the frame incoming S-TAG PCP and DEI values if **FWGC.SVM** is set to 2'b10, the frame incoming C-TAG PCP and DEI values if **FWGC.SVM** is set to 2'b01 and, 3'b0 and 1'b0 if **FWGC.SVM** is set to 2'b00.
- **greenToken** is the number of tokens contained in the green bucket.
- **yellowToken** is the number of tokens contained in the yellow bucket.

(b) Double bucket setting

For double buckets, the green bucket ('Committed' or 'C' bucket) and the yellow bucket ('Excess' or 'E' bucket) needs to be set. For detail explanations concerning coupling flag, color mode and bucket utilization, refer to MEF standard [MEF10.3]. Equation (6) shows how to set information rates in **FWPMTRCIRCi.CIRi** and **FWPMTREIRCi.EIRi**. **FWPMTRCBSci.CBSi** and **FWPMTREBSci.EBSi** should be respectively set to the maximum excepted burst size for green and yellow frame in byte.

$$(6) \text{InformationRate[byte/cycle]} = \text{MaximumThroughput[bps]} / (8 * \text{clk_freq[Hz]})$$

Where:

- *InformationRate* is the value to set to **FWPMTRCIRCi.CIRi** or **FWPMTREIRCi.EIRi** register.
- *MaximumThroughput[bps]* is the expected maximum throughput.
- *clk_freq* is the clock clk frequency. R-Car/S4 clk = 320MHz, RA8M2 clk = 150MHz

[Example]

If the meter is to be programmed for information rate of 200Mbps and system clock of 100MHz :

$$\text{InformationRate} = ((200 * 1000000) / (8 * 100 * 1000000)) * 2^{16}$$

$$\text{CIR}[15:0] \text{ or EIR}[15:0] = (\underline{0.25}) * 2^{16} = 16384 (0x4000)$$

$$\text{CIR}[19:16] \text{ or EIR}[19:16] = 0 \text{ (Underlined integer)}$$

(CIR x 2⁻¹⁶) is added to the committed token bucket every system clock.

If the meter is to be programmed for information rate of 200Mbps and system clock of 320MHz :

$$\text{InformationRate} = ((200 * 1000000) / (8 * 320 * 1000000)) * 2^{16}$$

$$\text{CIR}[15:0] \text{ or EIR}[15:0] = (\underline{0.078125}) * 2^{16} = 5120 (0x1400)$$

$$\text{CIR}[19:16] \text{ or EIR}[19:16] = 0 \text{ (Underlined integer)}$$

(CIR x 2⁻¹⁶) is added to the committed token bucket every system clock.

Restrictions:

- HW: DropOnYellow is not available in PSFP. To achieve drop on yellow function, the yellow bucket *InformationRate* **FWPMTREIRCi.EIRi** and **FWPMTREBSci.EBSi** should be set to 0. As a result, all yellow frames will be marked as red and dropped.

(2) Single bucket meters

Single bucket meters aim at giving a color to a frame. Meters from meter number PSFP_DMTR_N to meter number PSFP_MTR_N-1 are Single bucket meters.

(a) Single bucket color assignment

Single bucker meter i color assignment flow is described in Fig 5.69.

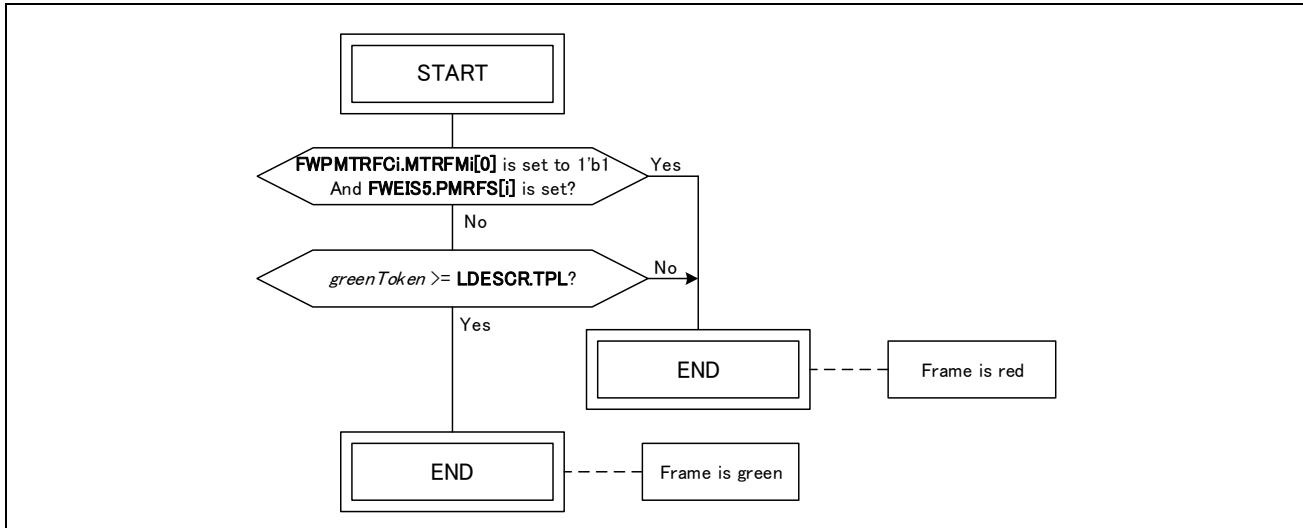


Fig 5.69: Single bucker meter i color assignment flow

In Fig 5.69:

- *greenToken* is the number of tokens contained in the green bucket.

(b) Single bucket setting

The single bucket should be set as the double bucket green bucket, refer to section 5.3.1.3(1)(b).

5.3.2 FRER

FRER functions is divided in three functions that happen independently (they can be used simultaneously):

- Replication
- Sequence number generation
- Elimination

Restrictions:

- SW: Latent error detection is not implemented in HW and should be implemented in SW using **FWFRPPCNi** and **FWFRDPCNi** counters.

5.3.2.1 Replication

FRER replication function is used to send a same frame to different ports with different streams. To do so, Layer 3 forwarding/routing/filtering (section 5.2.5) should be used along with Layer2/Layer3 Update function (section 5.2.8).

Layer 3 forwarding/routing/filtering is used to multicast the incoming FRER stream to several ports and to map the FRER stream to a routing number. Table 5-74 shows an example where Layer 3 table is used to multicast a frame coming from port 2 to port 0 and port 1 and to map the corresponding stream to routing number 5.

Table 5-74: Layer 3 table setting for replication

Field name L3.	Values	Explanation
SLV	'b100	Not mandatory, ensure that the corresponding stream only comes from port 2.
DV	'b011	Send the frame to port 0 and port 1
RV	1'b1	Enable routing
RN	'd5	Map the stream to Layer2/Layer3 Update rule number 5

Layer2/Layer3 rule remapping is used to remap Routing number **L3.RN** for one of the ports to send the frame with different stream IDs and allow to learn the rules and the new fields for stream update. Table 5-75 shows an example where port 1 Layer2/Layer3 Update rule number is remapped to rule number 8 with 8.2.8.5Routing number remapping rule number 4. Table 5-76 shown an example for Layer2/Layer3 Update rule setting for FRER.

Table 5-75: Layer2/Layer3 Update rule number remapping

Register name	Values	Explanation
FWL23URMC4.RME4	1'b1	Enable rule number remapping
FWL23URMC4.RMRNI4	'd5	Remap rule number 5
FWL23URMC4.RMSPN4	'd1	Remap when routing access comes from port 1
FWL23URMC4.RMNRN4	'd8	Remap rule to rule number 8

Table 5-76: Layer2/Layer3 Update rule settings

Field name L23U.	Values for rule 5	Values for rule 8	Explanation
RPV	'b001	'b001	Each rule is used for its corresponding port
TTLU	1'b0	1'b0	Do not update TimeToLive (user define)

Field name L23U.	Values for rule 5	Values for rule 8	Explanation
MDAU	1'b1	1'b1	Update destination MAC address (user define)
MSAU	1'b0	1'b0	Do not update source MAC address (user define)
CVIDU	1'b1	1'b1	Update C-TAG (user define)
CPCPU	1'b1	1'b1	Update C-TAG (user define)
CDEIU	1'b1	1'b1	Update C-TAG (user define)
SVIDU	1'b0	1'b0	Do not update S-TAG (user define)
SPCPU	1'b0	1'b0	Do not update S-TAG (user define)
SDEIU	1'b0	1'b0	Do not update S-TAG (user define)
RTU	2'b00 or 2'b01	2'b00 or 2'b01	Set to 2'b00 if the replicated stream contains a R-TAG at ingress Set to 2'b01 if the replicated stream does not contain R-TAG at ingress (section 5.3.2.2)
MDA	MAC0	MAC1	Set the new MAC address per each rule (user define)
CVID	VLAN0	VLAN1	Set the new VLAN ID per each rule (user define)
CPCP	PCP0	PCP1	Set the new PCP per each rule (user define)
CDEI	DEI0	DEI1	Set the new DEI per each rule (user define)
SVID	12'b0	12'b0	Do not update S-TAG (user define)
SPCP	3'b0	3'b0	Do not update S-TAG (user define)
SDEI	1'b0	1'b0	Do not update S-TAG (user define)

5.3.2.2 Sequence number generation

FRER sequence number generation is used during replication to generate a sequential sequence number to insert in stream corresponding frames (refer to section 5.3.2.1 for replication) using **FWSEQNGCi** and **FWSEQNRC** and can be monitored using **FWSEQNGMi**.

Functions:

- **FWSEQNGCi** register is used to enable sequence generation. While enabled, any frame forwarded with **FWSEQNGCi.SEQNGRNi** as routing number will see its sequence number (**FDESCR.SEQN**) set to **FWSEQNGMi.SEQNi**.
- **FWSEQNGMi** register is used to monitor the next sequence number to be used by sequence number generation rule i.
- **FWSEQNRC.SEQNR[i]** is used to reset to 16'b0 the next sequence number to be used by sequence number generation rule i.

Restrictions:

- SW: Sequence number generation shouldn't be used along with elimination.

Note:

- A frame rejected by PSFP will not see its sequence number updated by sequence number generation.

5.3.2.3 Elimination

FRER elimination aims at identifying the FRER streams (Layer 3 forwarding/routing/filtering, section 5.2.5), verifying the integrity of a stream (FRER individual recovery, section 5.3.2.3(2)(e)), at eliminating duplicated frames (FRER sequence recovery, 5.3.2.3(2)(f)), at recovering the stream stream ID (Layer2/Layer3 Update function (section 5.2.8)) and at checking that either the individual recovery or sequence recovery algorithm are stuck (Timeout function, section 5.3.2.3(3)). FRER elimination uses **FWFTL0/1/R**, **FWFTOC** and **FWFTOPC** registers and can be monitored using **FWFTIM** and **FWFTR/RR0/RR1/RR2** registers and **FWEIS60/61/62/63**, **FWEIS70/71/72/73** and **FWEIS80/81/82/83** interrupt registers.

Functions:

- **FWFTL0/1/R** registers are used to set/reset an entry in FRER table.
- **FWFTOC** and **FWFTOPC** registers are used to set timeout function.
- **FWFTIM** register is used to reset the FRER table before utilization. (Only one time, please refer 8.3.2.3 (2) (b) SW Learning for reconfiguration.)
- **FWFTR/RR0/RR1/RR2** registers are used to monitor FRER entries in FRER table.
- **FWEIS60/61/62/63**, **FWEIS70/71/72/73** and **FWEIS80/81/82/83** interrupt registers notify that an error happened during FRER elimination.

Restriction:

- SW: Sequence number generation shouldn't be used along with elimination.

(1) Stream identification, FRER recovery, initial stream recovery

In this section, example will be given to explain the different function dependencies and settings. In this example two streams, 0 and 1, are respectively entering the switch from port 0 and 1 that separately should pass through individual recovery algorithm for integrity check and through the same sequence recovery algorithm for duplicate elimination. The eliminated stream should see its stream ID updated to new one and should be forwarded to port 2

Stream identification is done by Layer 3 forwarding/routing/filtering function, refer to section 5.2.5. L3 table is used to map each stream to its corresponding FRER individual recovery individual recovery algorithm and also used to map stream to a Layer2/3 update rule for stream ID recovery. In Table 5-77 example, stream 0 and stream 1 are respectively mapped to FRER entry number 15 and 23 for individual recovery and both streams are mapped to routing rule number 5 for stream ID recovery.

Table 5-77: Layer 3 table setting for elimination

Field name L3.	Values for stream 0	Values for stream 1	Explanation
SLV	'b001	'b010	Not mandatory, ensure that each stream comes from its corresponding source port.
DV	'b100	'b100	All streams for the same sequence recovery algorithm are targeting the port
FRERV	1'b1	1'b1	FRER individual recovery
FRERN	'd15	'd23	All streams are targeting a different individual recovery algorithm
RV	1'b1	1'b1	Enable routing
RN	'd5	'd5	All streams for the same sequence recovery algorithm are targeting the same Layer2/Layer3 update rule for stream ID recovery

FRER table is then used to map stream 0 and 1 individual recovery algorithms to a sequence recovery algorithm and used to set all the recovery algorithms. Table 5-78 shows an example where individual recovery algorithm are mapped to FRER entry number 67 for sequence recovery.

Table 5-78: FRER table setting for sequence recovery

Field name FRER.	Values for FRER entry number 15	Values for FRER entry number 23	Values for FRER entry number 67	Explanation
SRPV	1'b1	1'b1	1'b0	Enable sequence recovery for an individual recovery algorithm
SRP	'd67	'd67	All0	Sequence recovery entry number

Layer2/Layer3 Update functions is used to recover the output stream ID in the frame. Table 5-79 shown an example for Layer2/Layer3 Update rule setting for FRER.

Table 5-79: Layer2/Layer3 Update rule settings

Field name L23U.	Values for rule 5	Explanation
RPV	'b100	Set to the target port
TTLU	1'b0	Do not update TimeToLive (user define)
MDAU	1'b1	Update destination MAC address (user define)
MSAU	1'b0	Do not update source MAC address (user define)
CVIDU	1'b1	Update C-TAG (user define)
CPCPU	1'b1	Update C-TAG (user define)
CDEIU	1'b1	Update C-TAG (user define)
SVIDU	1'b0	Do not update S-TAG (user define)
SPCPU	1'b0	Do not update S-TAG (user define)
SDEIU	1'b0	Do not update S-TAG (user define)
RTU	2'b00 or 2'b01	Set to 2'b00 if the output stream should contain the ingress R-TAG Set to 2'b10 if the output stream should be sent without R-TAG
MDA	MAC0	Set the new MAC address per each rule (user define)
CVID	VLAN0	Set the new VLAN ID per each rule (user define)
CPCP	PCP0	Set the new PCP per each rule (user define)
CDEI	DEI0	Set the new DEI per each rule (user define)
SVID	12'b0	Do not update S-TAG (user define)
SPCP	3'b0	Do not update S-TAG (user define)
SDEI	1'b0	Do not update S-TAG (user define)

In this section only an example has been developed, by using the same kind of settings it is possible to:

- Have only one ingress stream and one output stream with the same stream ID and only apply individual recovery.
- Have more than 2 input streams for elimination.
- Have more than 1 output stream after elimination (by applying FRER replication, section 5.3.2.1)

(2) FRER table

FRER table is used to store setting and information used for recovery algorithms.

FRER table is divided in the following items:

- Rule format: Determines what information will be stored in the FRER table
- SW Learning: Function to set an FRER entry in the FRER table.
- SW Reading: Function to read an FRER entry in the FRER table.

(a) Rule format

The FRER table is used to store FRER entries. A FRER entry contains information recovery algorithms. All the fields in this table, if quoted, will be written **FRER.{Field name}**. Table 5-80 describes fields contained in a FRER entry.

Table 5-80: FRER entry format

Field name	Field size (bit)	Field Explanation
SHL	FRER_HIST_LEN_W	Sequence History Length Values: - 0: Recovery match algorithm - i different than 0: Recovery vector algorithm with history length of i+1
SH	FRER_HIST_LEN1	Sequence History: Functions: - Used to save sequence history for recovery algorithms
RSN	16	Recovery Sequence Number Functions: - Used to save last highest sequence number (modulo 2^{16}) for recovery algorithms
TNS	1	Take No Sequence Values: - 1'b0: Frames received without R-TAG (LDESCR.RTGI [GWCA] not set) are rejected - 1'b1: Frames received without R-TAG (LDESCR.RTGI [GWCA] not set) are forwarded
SRPV	1	Sequence Recovery Pointer Valid Values: - 1'b0: After using this entry for individual recovery, sequence recovery will not happen - 1'b1: After using this entry for individual recovery, sequence recovery will happen using FRER entry number FRER.SRP
SRP	FRER_RECE_W	Sequence Recovery Pointer Functions: - Set the number of the FRER entry that should be used for sequence recovery Restrictions: - Any entry used for sequence recovery cannot be used for individual recovery. As a result, when a Recovery number is set in FRER.SRP when FRER.SRPV is set, the same number cannot be set in L3.FRERN when L3.FRERV is set.
SRRT	10	Set Recovery Remaining Tick Functions: - Time in tick (one tick is FWFTOC.TOCE) before timeout. - Setting this register to All0 disable timeout function for the corresponding entry

Field name	Field size (bit)	Field Explanation
RRT	10	Recovery Remaining Tick Functions: - Used by timeout function to detect timeout error.

(b) SW Learning

Learning is used to set/reset an entry in the FRER table. Table 5-81 describes register used to learn an entry in the FRER table. Table 5-82 describes the learn results. To reset an entry, software should re-learn the same entry again.

Table 5-81: FRER entry learn registers

Register name	Field name/corresponding field in I23u table	Field explanation
FWFTL0.FEAL	Entry Learn address	Corresponding the entry number that should be learnt in FRER table
FWFTL1.FSHLL	FRER.SHL	Refer to section 5.3.2.3(2)(a)
No register Set to All0 While learning (TakeAny)	FRER.SH	Refer to section 5.3.2.3(2)(a)
No register Set to All1 While learning	FRER.RSN	Refer to section 5.3.2.3(2)(a)
FWFTL1.FTNSL	FRER.TNS	Refer to section 5.3.2.3(2)(a)
FWFTL1.FSRPVL	FRER.SRPV	Refer to section 5.3.2.3(2)(a)
FWFTL0.FSRPL	FRER.SRP	Refer to section 5.3.2.3(2)(a)
FWFTL1.FSRRTL	FRER.SRRT	Refer to section 5.3.2.3(2)(a)
No register Set to All0 While learning	FRER.RRT	Refer to section 5.3.2.3(2)(a)

Table 5-82: FRER entry learn result

Register name	Field name/corresponding field in FRER table	Field explanation
FWFTLR.FLF	Learning fail	Learning fail with happen in one of the following conditions: - The FRER table is not ready (FWFTIM.FTR is not set)
FWFTLR.FLSF	Learning security fail	Security fail with happen in one of the following conditions: - The learn action is done by the unsecure APB and the learn entry is secure (corresponding FWSCR44/45/46/47.FRERRSL[i] is not set) - The learn action is done by the unsecure APB, learnt Sequence Recovery Pointer is valid (FWFTL1.FSRPVL set while learning) and Sequence Recovery Pointer points to a secure entry (corresponding FWSCR44/45/46/47.FRERRSL[i] is not set)

(c) SW Reading

Learning is used to read an entry in the FRER table. Table 5-83 describes register used to read an entry in the FRER table. Table 5-84 describes the read results.

Table 5-83: FRER entry read registers

Register name	Field name/corresponding field in I23u table	Field explanation
FWFTR.FEAR	Entry Read address	Corresponding the entry number that should be read from FRER table

Table 5-84: FRER entry learn result

Register name	Field name/corresponding field in I23u table	Field explanation
FWFTRR0	Read ECC fail	Reading failed because of an ECC error.
FWFTRR0.FSHLR	FRER.SHL	Refer to section 5.3.2.3(2)(a)
FWFTRR1.FSHR	FRER.SH	Refer to section 5.3.2.3(2)(a)
FWFTRR2.FRSNR	FRER.RSN	Refer to section 5.3.2.3(2)(a)
FWFTRR0.FTNSR	FRER.TNS	Refer to section 5.3.2.3(2)(a)
FWFTRR0.FSRPVR	FRER.SRPV	Refer to section 5.3.2.3(2)(a)
FWFTRR0.FSRPR	FRER.SRP	Refer to section 5.3.2.3(2)(a)
FWFTRR0.FSRRTR	FRER.SRRT	Refer to section 5.3.2.3(2)(a)
FWFTRR2.FRRTR	FRER.RRT	Refer to section 5.3.2.3(2)(a)

(d) Recovery algorithms

Individual recovery or sequence recovery algorithm can both be performed using either a match recovery algorithm or a vector recovery algorithm. For an entry, match recovery algorithm can be selected by setting All0 to its corresponding **FRER.SHL** field. If any other value is set vector recovery algorithm will be selected.

Match recovery algorithm is only used to detect if a stream is stuck (two frames are received consecutively with the same sequence number).

Vector recovery algorithm is used to check a stream sequence by accepting all packets within a given range (\pm **FRER.SHL**) from the last accepted highest sequence recovery number. This algorithm also ensures than within this range no sequence number is received more than on time.

(e) Individual recovery algorithms

Individual recovery match algorithm and vector algorithm are respectively described in Fig 5.70 and Fig 5.71. The variable *Delta* present in these figures is the distance from the ingress frame sequence number to **FRER.RSN** (This number should be considering overflow and should be contained in [-32767:32768] range).

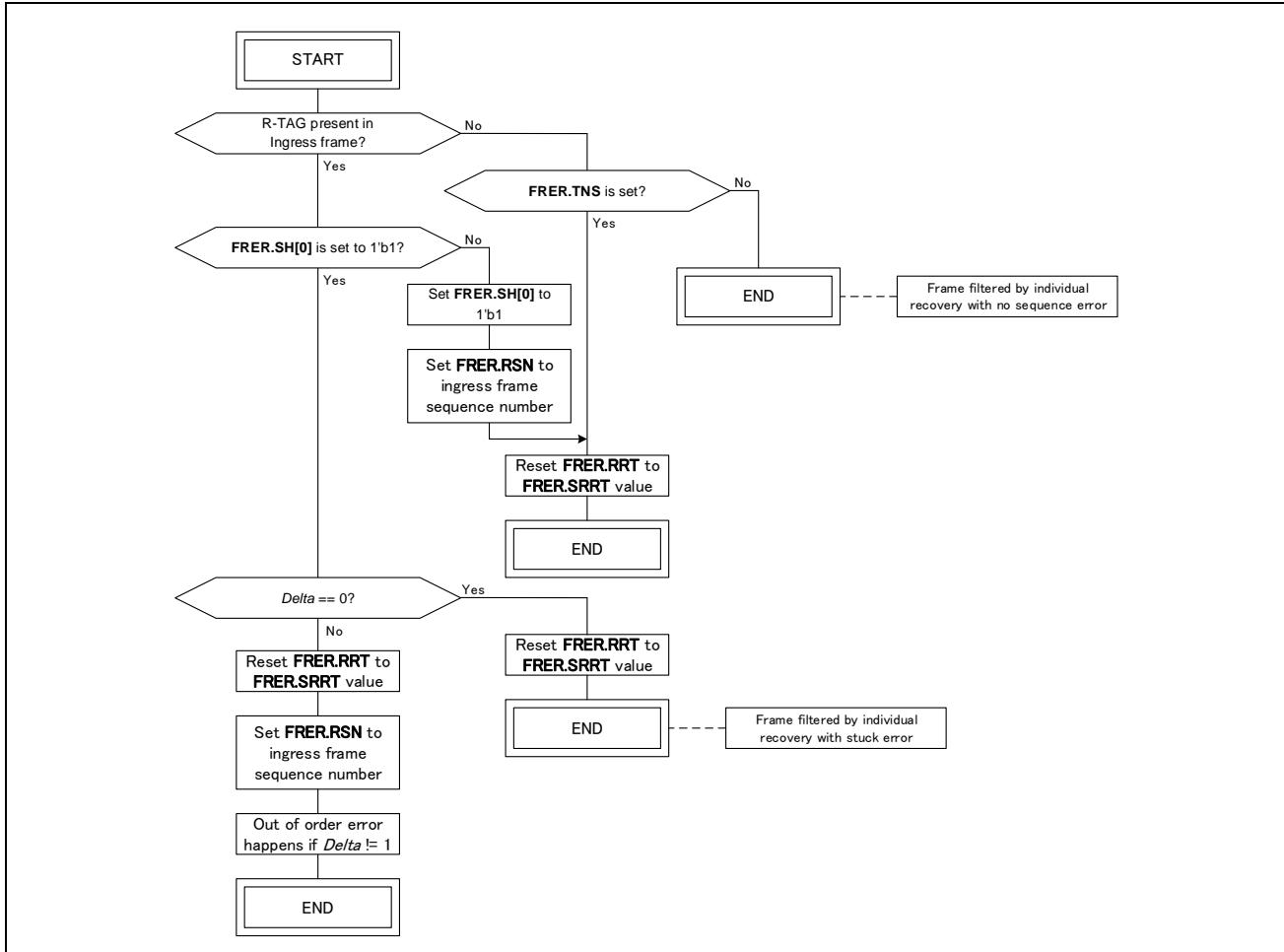


Fig 5.70: Individual recovery match algorithm

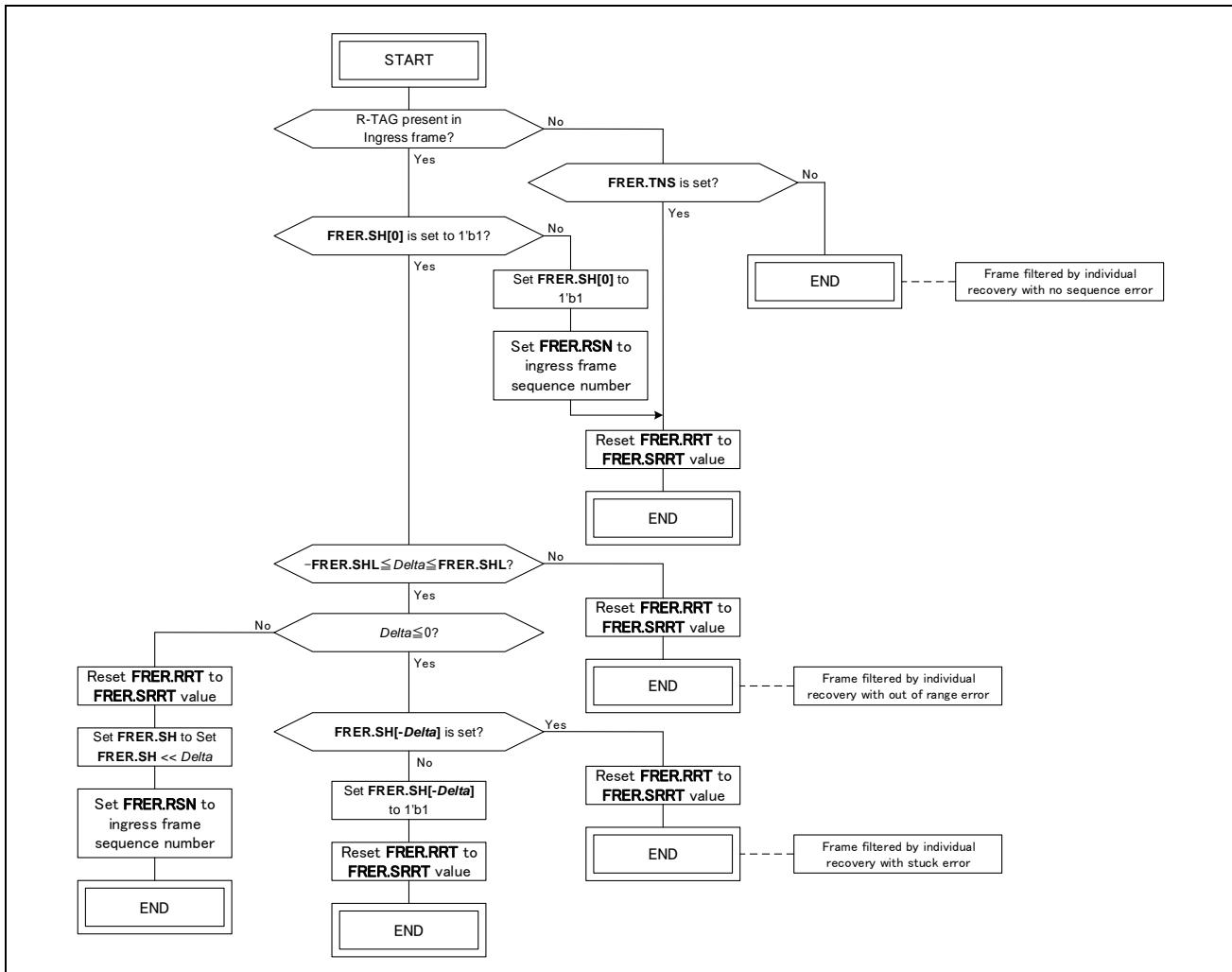


Fig 5.71: Individual recovery vector algorithm

Note:

- Even if the recovery length is smaller than FRER_HIST_LEN, the sequence history saved in the FRER table will contain the history until FRER_HIST_LEN. Vector recovery algorithm will ignore the useless bits.

(f) Sequence recovery algorithms

Sequence recovery match algorithm and vector algorithm are respectively described in Fig 5.72 and Fig 5.73. The variable *Delta* present in these figures is the distance from the ingress frame sequence number to **FRER.RSN** (This number should be considering overflow and should be contained in [-32767:32768] range).

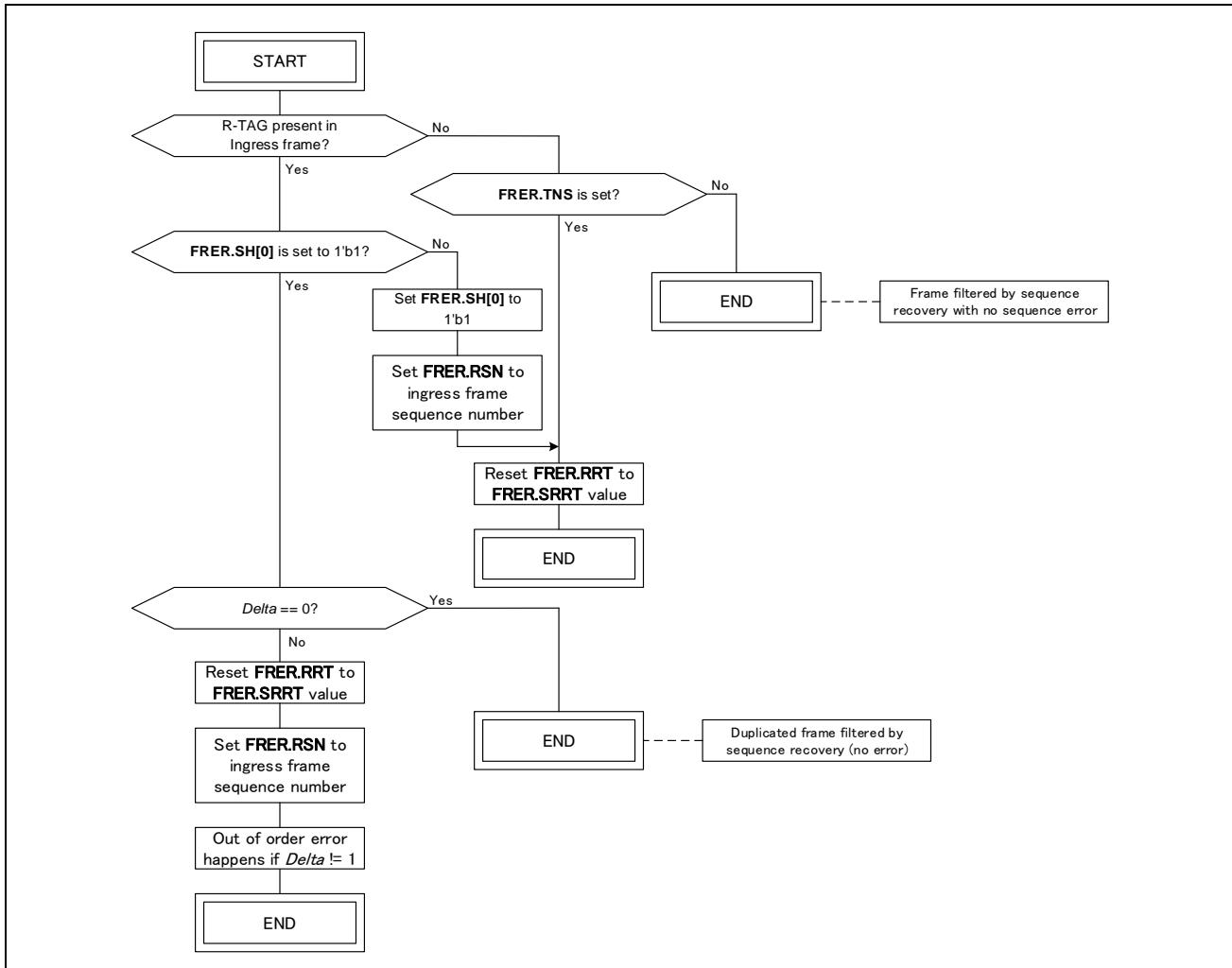


Fig 5.72: Sequence recovery match algorithm

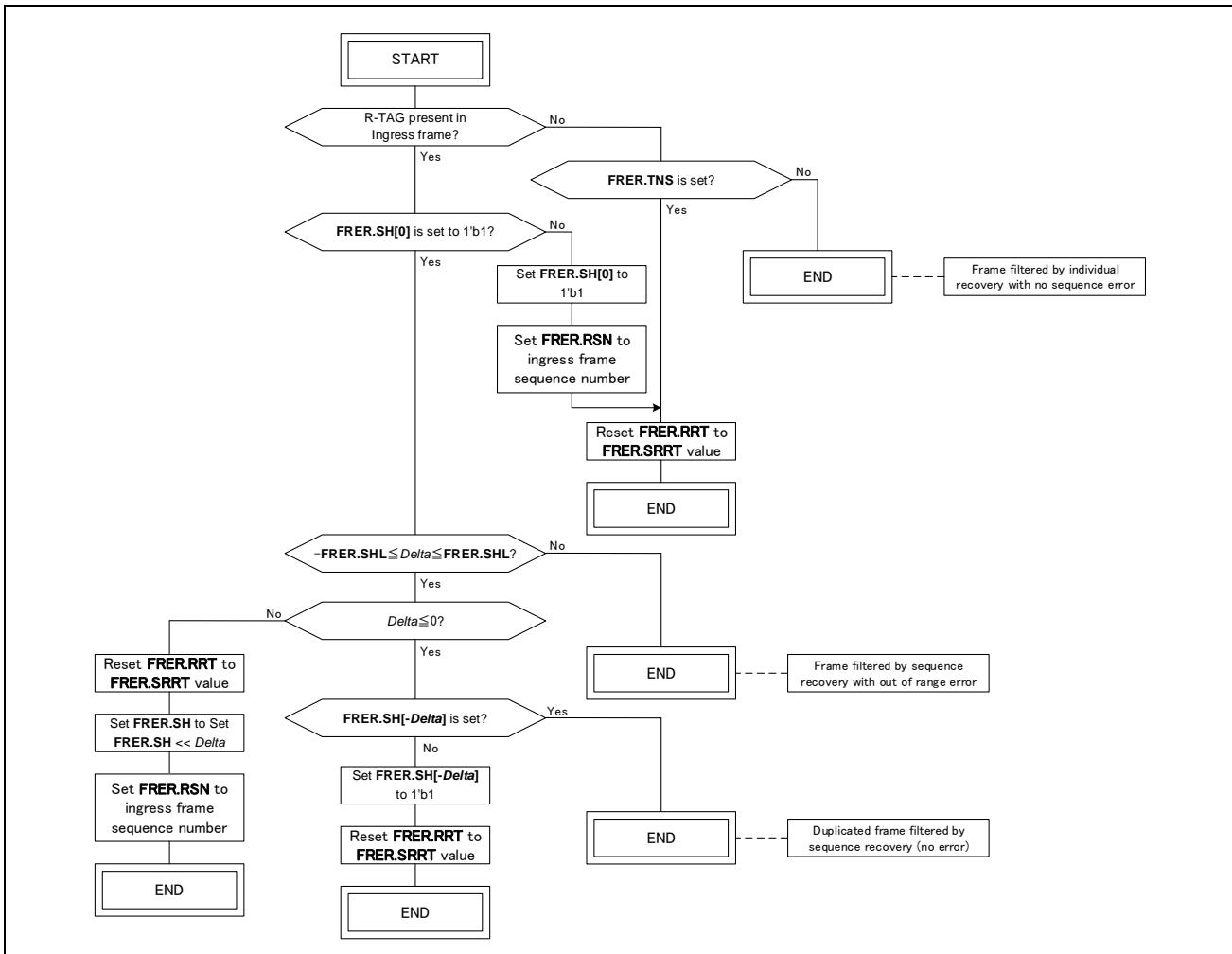


Fig 5.73: Sequence recovery vector algorithm

Note:

- Even if the recovery length is smaller than FRER_HIST_LEN, the sequence history saved in the FRER table will contain the history until FRER_HIST_LEN. Vector recovery algorithm will ignore the useless bits.

(3) Timeout

The timeout function aims at detecting when a recovery algorithm had no passing frame since a certain time and should be reset because it could be stuck. The timeout functional flow is described in for when timeout functions is enabled (**FWFTOC.TOCE** set to 1'b1). This flow happens for all the FRER entries.

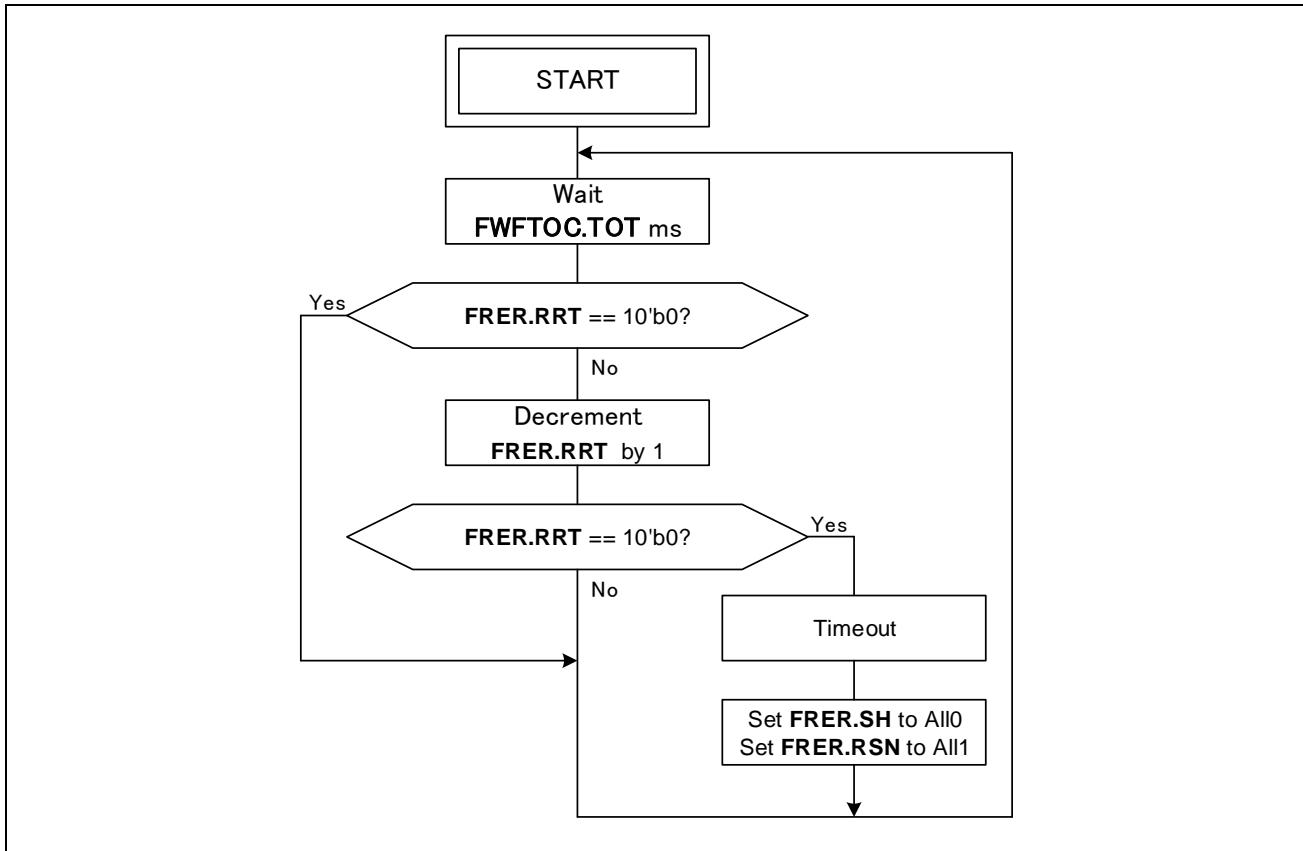


Fig 5.74: Timeout functional flow

6. Precautions

6.1 Precautions

NA.

6.2 Restrictions (Including known problems)

- Working sample version 1 devices have the following restrictions:
 - A) The read command is executed twice, and the second one is the valid result for 4.1.6.8 and 4.1.7.7.
 - B) Limited HW learning area to less than 256 entries (can be maximum entry number 0 to 255) for MACTHWLSA and MACTHWLEA.
 - C) The ECC error signal from TCAM is not connected, so 5.1.7 Self-recovery and ECC error detection cannot work.

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