User's Manual

R-Switch-3 GateWay

Outline specifications

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(2012.4)

General precautions for handling of product

The following notes are applicable to entire CBIC with CPU core. For detailed usage notes, refer to the relevant sections of the manual. If the description under General precautions and in the body of the manual differs from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flow internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Regarding Clock

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized. When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

Table of Contents

1. [R-Switch external] Overall specifications

This chapter defines the system specifications for the R-switch.

1.1 Overall block diagram

R-Switch-3's Ethernet (XGMII/GMII) interface 0-4 is directly connected to external port 0-4 (SerDes0-4).

R-Switch-3's Ethernet (XGMII/GMII) interface 5-7 can be connected to external ports 5-7 (SerDes5-7). OR

R-Switch-3's Ethernet (GMII) interface 5-7 can be connected to TSN-ES 0-2. Refer [RMAC] for connection selector.

R-Switch-3's Ethernet (GMII) interface 8-12 is directly connected to TSN-ES 3-7.

R-Switch-3 and gPTP(R-Switch-3) are connected one-to-one. gPTP(R-Switch-3) timer value will be used for CAN, PCI-E and UCI-E.

TSN-ES 0 and gPTPb(TSN-ES 0) are connected one-to-one.

TSN-ES 1-7 and gPTPa(TSN-ES 1-7) are connected one-to-one.

[Notes]

Restriction: The upper limit of the transfer bandwidth with the CPU is 2.5Gbps per TSNA and TSN-ES. As a result, one-to-one communication between external Ethernet (XGMII10Gbps) and internal Ethernet (GMII 2.5Gbps with TSN-ES) is not possible. Share the bandwidth with multiple TSN-ES.

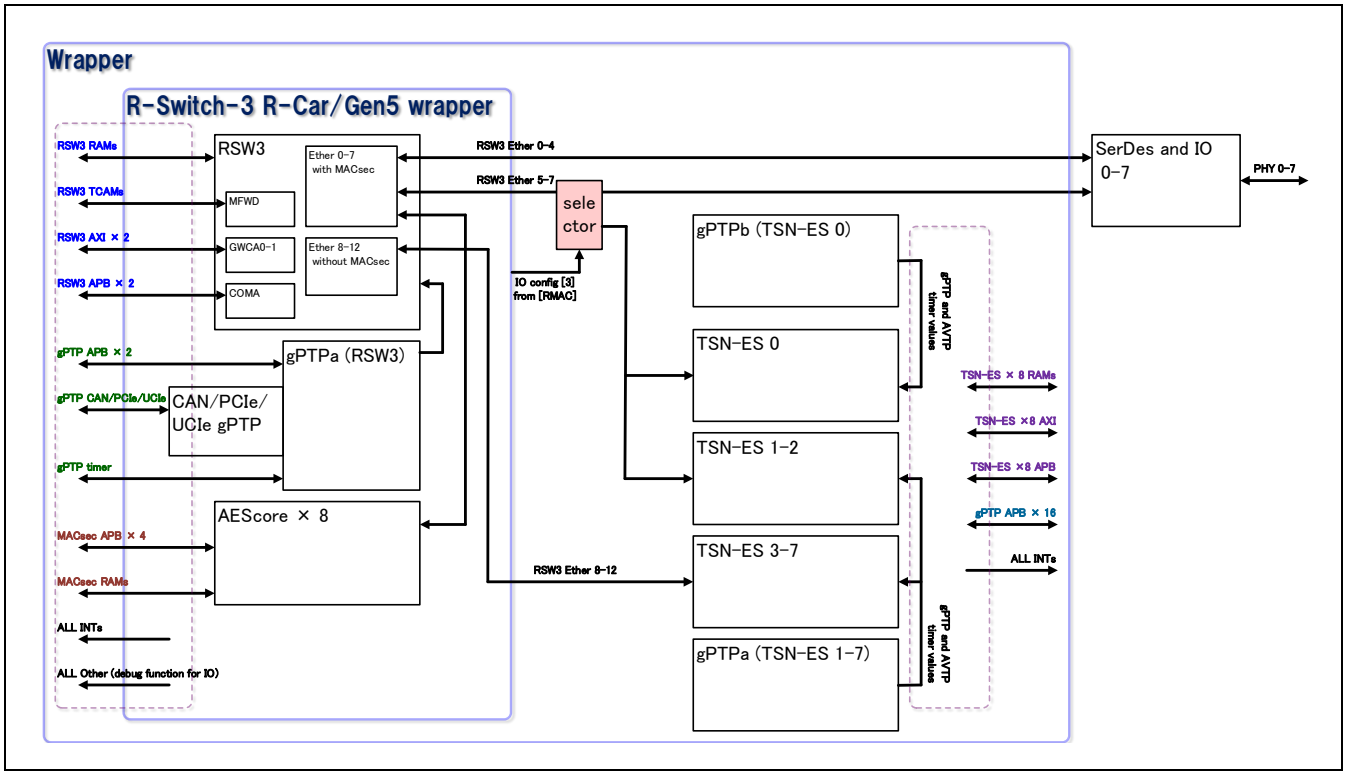


Fig 1.1: Wrapper connection diagram

1.2 Overall system

The above shows an example of system construction.

Example 1: 40Gbps total external 4 ports and 10Gbps total for internal 4 ports. This is the simplest configuration.

Example 2: 35Gbps total external 5 ports and 15Gbps total for internal 6 ports. Increased number of external ports and reduce total bandwidth. Therefore, it is possible to increase the number of internal ports.

Example 3: To enable all internal ports, it is necessary to control the internal port bandwidth using CBS or the like.

Example 4: TSNA5-7 can change from internal port to external port.

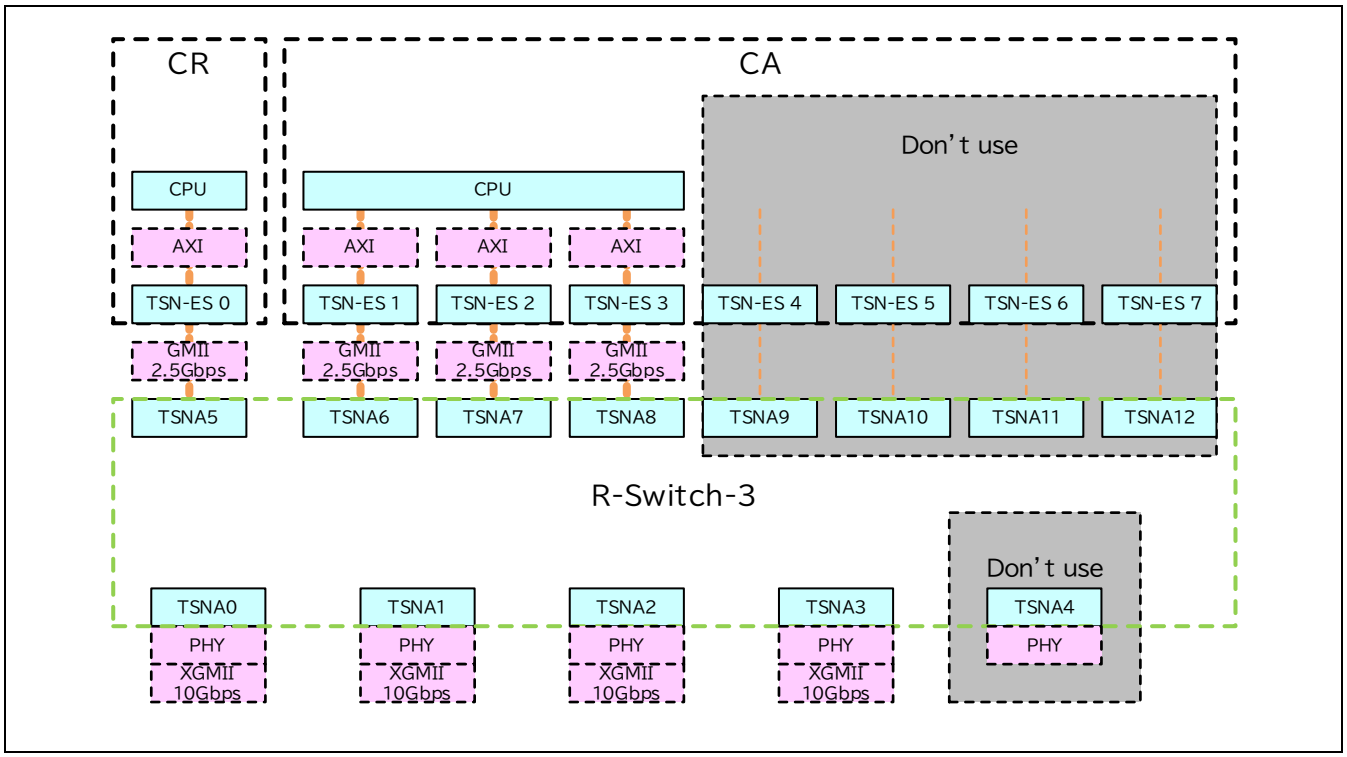


Fig 1.2: Overall system example 1

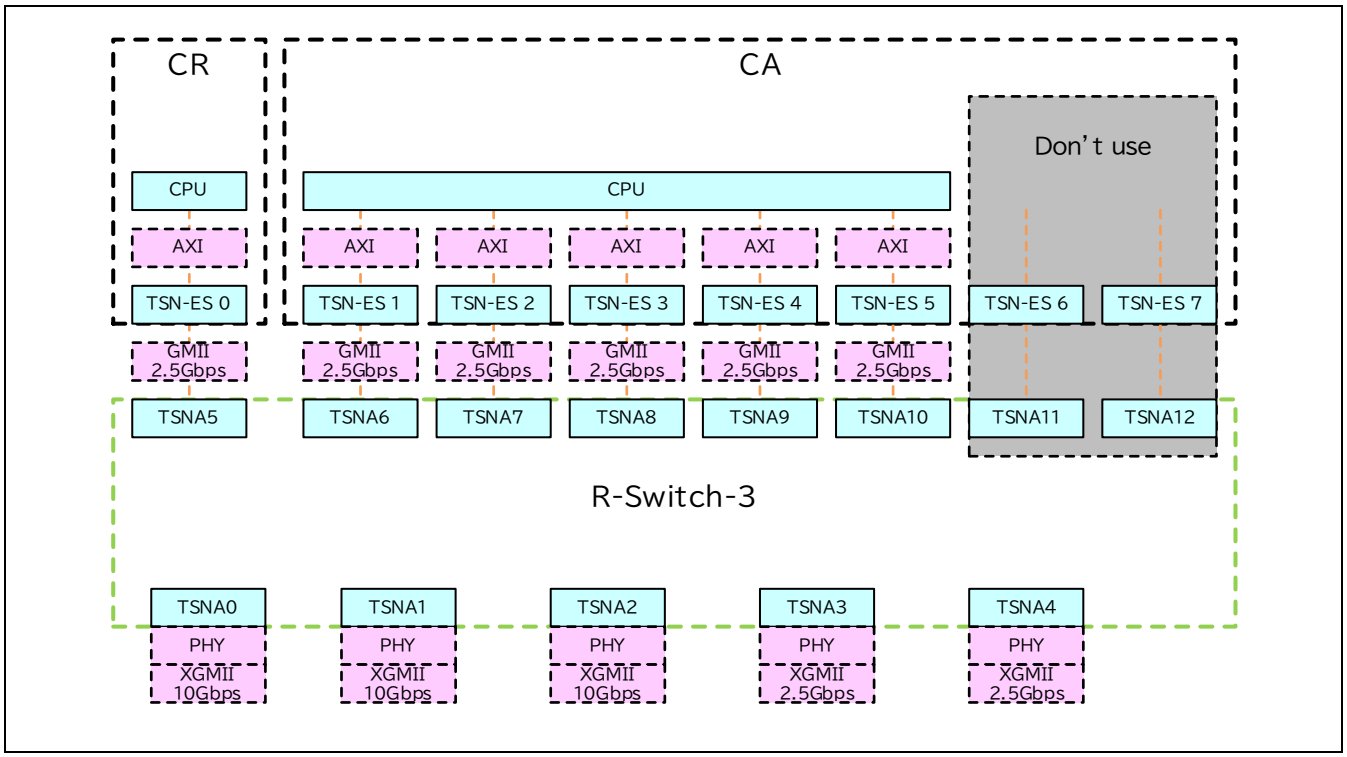


Fig 1.3: Overall system example 2

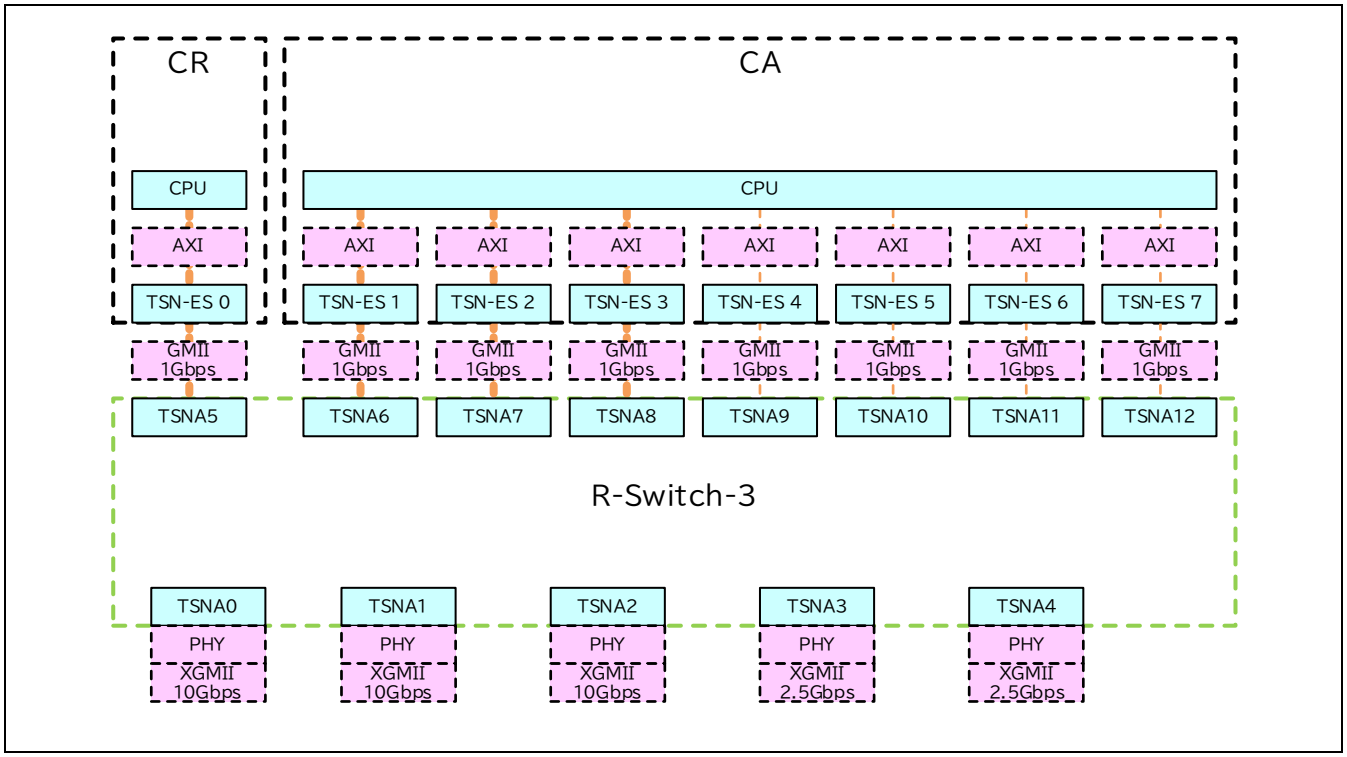


Fig 1.4: Overall system example 3

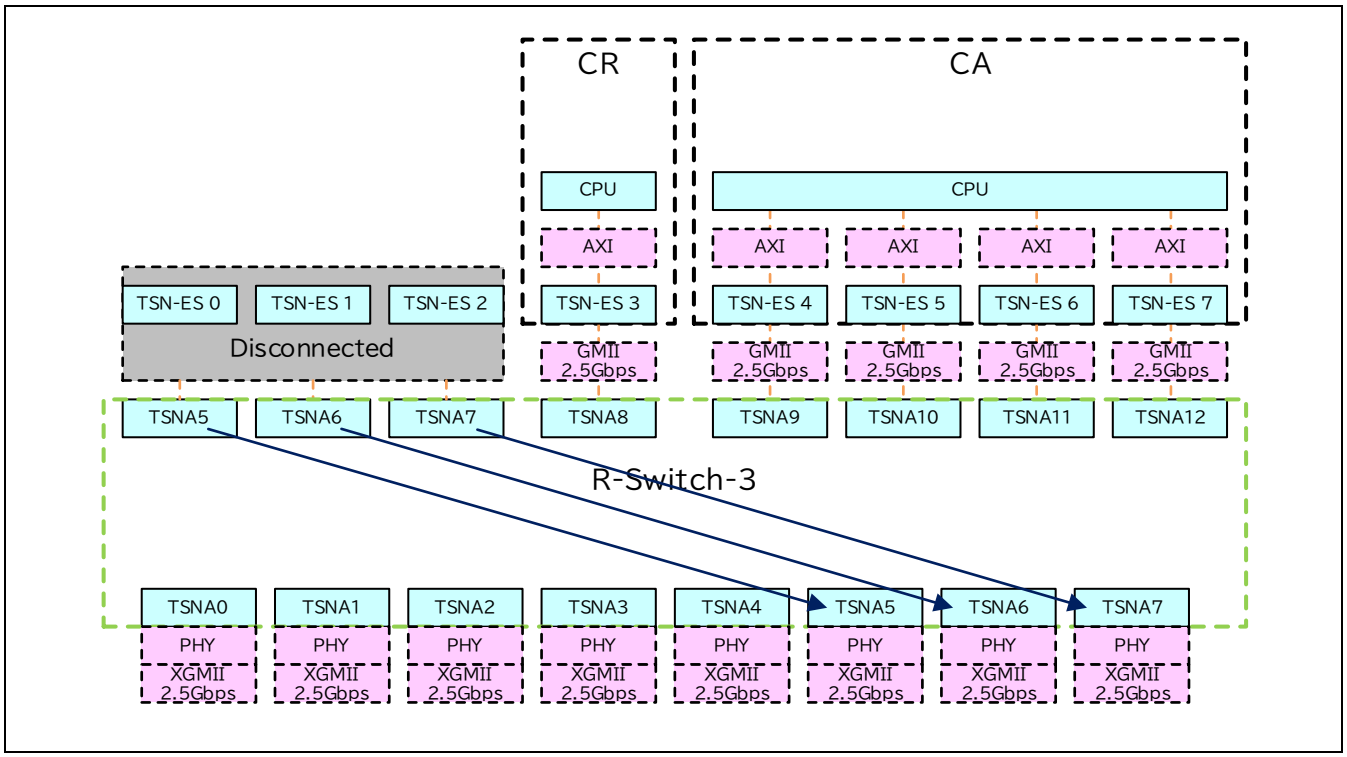


Fig 1.5: Overall system example 4

1.3 Interrupt mapping

Output signal name	Source	Clock	Init value
race_wrap_mfwd_int	race_mfwd_error_int, race_mfwd_status_int [MFWD] FWEIS(0-8), FWMIS0	clk	0
race_wrap_race_int	race_race_error_int (Fix to 0), race_race_status_int [TOP] RSSIS	clk	0
race_wrap_coma_int	race_coma_error_int, race_coma_status_int [COMA] CAEIS0, CAEIS1, CAMIS0, CAMIS1	clk	0
race_wrap_gwca(0-1)_int	race_gwca(0-1)_error_int, race_gwca(0-1)_status_int (Fix to 0) [GWCA(0-1)] GWEIS0(other TDFES), GWEIS1, GWEIS4, GWEIS5	clk	0
race_wrap_msc(0-7)_error_int	race_wrap_msc(0-7)_error_int [MACsec(0-7)] MSEIS0-2, MSAESEIS0-3, MSPNTIS, MSPNEIS	clk	0
race_wrap_aes_ecc1_error	OR [MACsec(0-7)] MSAESEIS4	clk	0
race_wrap_aes_ecc2_error	OR [MACsec(0-7)] MSAESEIS5	clk	0
race_wrap_etha(0-12)_int	race_etha(0-12)_error_int, race_etha(0-12)_status_int, race_rmac(0-12)_error_int, race_rmac(0-12)_status_int (Fix to 0), race_rmac(0-12)_mdio_int, race_rmac(0-12)_mp_int, race_rmac(0-12)_phy_int [TSNA(0-12)] EAEIS0, EAEIS1, EAEIS2 [RMAC(0-12)] MEIS, MMIS0, MMIS1, MMIS2	clk	0
race_wrap_gwca(0-1)_gwdis_int[7:0]	race_gwca(0-1)_core_int[7:0] Please refer [TOP] 7.4.1.1 Interrupt mapping function registers for details. [GWCA(0-1)] GWDIS, GWEIS2, GWEIS3, and other	clk	0
race_wrap_gwca(0-1)_gwtsdis_int[1:0]	race_gwca(0-1)_timer_int[1:0] Please refer [TOP] 7.4.1.1 Interrupt mapping function registers for details. [GWCA(0-1)] GWTSDIS, GWEIS0.TDFES	clk	0
race_wrap_gptp_int	[GPTPa] PTPIS0, PTPIS1	clk	0
tes(0-7)_status_int *1	tes(0-7)_int_n, tes(0-7)_rx_fil_int_n, tes(0-7)_stream_fil_int_n, tes(0-7)_srst_int_n, tes(0-7)_lpi_start_int_n, tes(0-7)_lpi_stop_int_n, tes(0-7)_mode_int_n, tes(0-7)_mp_int_n, tes(0-7)_mdio_int_n	ACLK_tes(0-7)	0
tes(0-7)_tx_int *1	tes(0-7)_tds_int_n[TX_CHAIN_N:0]	ACLK_tes(0-7)	0

tes(0-7)_rx_int *1	tes(0-7)_rds_int_n[RX_CHAIN_N:0]	ACLK_tes(0-7)	0
tes(0-7)_ts_int *1	tes(0-7)_ts_int_n[TS_CHAIN_N:0]	ACLK_tes(0-7)	0
tes(0-7)_error_int *1	tes(0-7)_tces_int_n[TX_CHAIN_N:0], tes(0-7)_rfses_int_n[RX_CHAIN_N:0], tes(0-7)_rfes_int_n[RX_CHAIN_N:0], tes(0-7)_rces_int_n[RX_CHAIN_N:0], tes(0-7)_ridaoes_int_n[RX_INC_CHAIN_N:0], tes(0-7)_tsfes_int_n[TS_CHAIN_N:0], tes(0-7)_tsces_int_n[TS_CHAIN_N:0]	ACLK_tes(0-7)	0
tes(0-7)_gptp_int	[GPTPb] PTPIS0, PTPIS1, PTPIS2 of tes0 [GPTPa] PTPIS0, PTPIS1 of tes(1-7)	ACLK_tes(0-7)	0

*1 : Please refer to “3.14 Interrupt” of 100a_RSW30_RTSNES_TOP_IPSpec_UM.

1.4 IO mapping

Signal name	Input/Output	Description
race_wrap_gptp[0-1]_capture	Input	Refer to MEDIA_IN[0-1] (007a_RSW30_gPTPa_IPspec_UM_0.40) of R-Switch-3
race_wrap_gptp[0-1]_match	Output	Refer to MEDIA_OUT[0-1] (007a_RSW30_gPTPa_IPspec_UM_0.40) of R-Switch-3
race_wrap_gptp[0-1]_pps	Output	Refer to PPS[0-1] (007a_RSW30_gPTPa_IPspec_UM_0.40) of R-Switch-3
tes0_gptp[0-1]_capture	Input	Refer to MEDIA_IN[0-1] (007b_RSW30_gPTPb_IPspec_UM_0.40) of TSN-ES-0
tes0_gptp[0-1]_match	Output	Refer to MEDIA_OUT[0-1] (007b_RSW30_gPTPb_IPspec_UM_0.40) of TSN-ES-0
tes0_gptp[0-1]_pps	Output	Refer to PPS[0-1] (007b_RSW30_gPTPb_IPspec_UM_0.40) of TSN-ES-0
tes0_gptp[2-16]_capture	Input	Refer to MEDIA_IN[2-16] (007b_RSW30_gPTPb_IPspec_UM_0.40) of TSN-ES-0
tes1_gptp[0-1]_capture	Input	Refer to MEDIA_IN[0-1] (007a_RSW30_gPTPa_IPspec_UM_0.40) of TSN-ES-1
tes1_gptp[0-1]_match	Output	Refer to MEDIA_OUT[0-1] (007a_RSW30_gPTPa_IPspec_UM_0.40) of TSN-ES-1
tes1_gptp[0-1]_pps	Output	Refer to PPS[0-1] (007a_RSW30_gPTPa_IPspec_UM_0.40) of TSN-ES-1
tes2_gptp[0-1]_capture	Input	Refer to MEDIA_IN[0-1] (007a_RSW30_gPTPa_IPspec_UM_0.40) of TSN-ES-2
tes2_gptp[0-1]_match	Output	Refer to MEDIA_OUT[0-1] (007a_RSW30_gPTPa_IPspec_UM_0.40) of TSN-ES-2
tes2_gptp[0-1]_pps	Output	Refer to PPS[0-1] (007a_RSW30_gPTPa_IPspec_UM_0.40) of TSN-ES-2
tes3_gptp[0-1]_capture	Input	Refer to MEDIA_IN[0-1] (007a_RSW30_gPTPa_IPspec_UM_0.40) of TSN-ES-3
tes3_gptp[0-1]_match	Output	Refer to MEDIA_OUT[0-1] (007a_RSW30_gPTPa_IPspec_UM_0.40) of TSN-ES-3
tes3_gptp[0-1]_pps	Output	Refer to PPS[0-1] (007a_RSW30_gPTPa_IPspec_UM_0.40) of TSN-ES-3
tes4_gptp[0-1]_capture	Input	Refer to MEDIA_IN[0-1] (007a_RSW30_gPTPa_IPspec_UM_0.40) of TSN-ES-4
tes4_gptp[0-1]_match	Output	Refer to MEDIA_OUT[0-1] (007a_RSW30_gPTPa_IPspec_UM_0.40) of TSN-ES-4
tes4_gptp[0-1]_pps	Output	Refer to PPS[0-1] (007a_RSW30_gPTPa_IPspec_UM_0.40) of TSN-ES-4
tes5_gptp[0-1]_capture	Input	Refer to MEDIA_IN[0-1] (007a_RSW30_gPTPa_IPspec_UM_0.40) of TSN-ES-5
tes5_gptp[0-1]_match	Output	Refer to MEDIA_OUT[0-1] (007a_RSW30_gPTPa_IPspec_UM_0.40) of TSN-ES-5
tes6_gptp[0-1]_pps	Output	Refer to PPS[0-1] (007a_RSW30_gPTPa_IPspec_UM_0.40) of TSN-ES-5
tes6_gptp[0-1]_capture	Input	Refer to MEDIA_IN[0-1] (007a_RSW30_gPTPa_IPspec_UM_0.40) of TSN-ES-6
tes6_gptp[0-1]_match	Output	Refer to MEDIA_OUT[0-1] (007a_RSW30_gPTPa_IPspec_UM_0.40) of TSN-ES-6
tes6_gptp[0-1]_pps	Output	Refer to PPS[0-1] (007a_RSW30_gPTPa_IPspec_UM_0.40) of TSN-ES-6
tes7_gptp[0-1]_capture	Input	Refer to MEDIA_IN[0-1] (007a_RSW30_gPTPa_IPspec_UM_0.40) of TSN-ES-7
tes7_gptp[0-1]_match	Output	Refer to MEDIA_OUT[0-1] (007a_RSW30_gPTPa_IPspec_UM_0.40) of TSN-ES-7
tes7_gptp[0-1]_pps	Output	Refer to PPS[0-1] (007a_RSW30_gPTPa_IPspec_UM_0.40) of TSN-ES-7

2. Overview

The R-Switch 3 system consists on an ethernet switch with higher level routing capability and multi-protocol interface support. It allows autonomous frame routing within same and between different network interfaces protocols (for now only Ethernet) for optimized gateway applications.

An AMBA APB 3.0 [APB] slave allows configuration and an AMBA AXI3 [AXI] bus master DMA handles the data transfers.

The R-Switch 3 system has also a three line interrupt signal for data transfer, monitoring and error handling.

2.1 Features

R-Switch 3 Features are described [MFWD] [GWCA] [TSNA] [RMAC].

2.2 Performance

Refer to the list below for details.

Overall bandwidth of the R-Switch fabric (Switching capacity)	Ethernet & CPU Total bandwidth (Ethernet & CPU capacity)	Latency *
Max 364.032 Gbps Restrictions: None. Min 101.92 Gbps Restrictions: Reception&Transmission Smallest frames From&To all ports.	Max total 50 Gbps Details: Total bandwidth of Ether and CPU ports used for transmission and reception. (Example : “Ether 10 Gbps 4 port” and “CPU 2.5 Gbps 4 port" *) * : GWCA can achieve specifications of up to 50Gbps using the AXI. However, this is the instantaneous maximum value due to ACLK* GWCA[i]_AXI_DW. The worst spec is 12.5Gbps due to factors such as frame interval and descriptor control.	MII 10Mbps : 40,000 ~ 80,000 ns MII 100Mbps : 4,000 ~ 8,000 ns GMII 1Gbps : 830 ~ 1,630 ns GMII 2.5Gbps or XGMII 10Gbps : 348 ~ 668 ns XGMII 2.5Gbps : 1,308 ~ 2,588 ns XGMII 5Gbps : 668 ~ 1,308 ns * : This is the value without MACsec. If using MACsec, to add Delay_RX_MAC [MACsec] and Delay_TX_MAC [MACsec]

[notes] : “Smallest frame” = DMAC(6), SMAC(6), Type(2), Data(46), FCS(4) = 64 byte (without MACsec)

Latency measurement conditions:

- From frame end (forwarding source port) to frame start (forwarding destination port)
- The forwarding (destination port) is not busy.
- L2 Forwarding unicast (1: 1 forwarding)

(Note 1) At the frame end (forwarding source port) -frame start (forwarding destination port). When measuring, there is no dependency on the payload length of the frame.

(Note 2) The frame start (forwarding destination port) is up to the point where the preamble starts to be output.

(Note 3) MAC sampling -> Local RAM 50~100 PHY clock cycle & Forwarding 20 R-Switch-3 clock cycle & Local RAM -> MAC transmitting 50~100 PHY clock cycle.

Restriction:

- MACsec has higher performance (lower latency) on RX(Decrypting) than TX(Encrypting). Therefore, when “Ethernet to Ethernet forwarding” using MACsec on “TX only” or “both TX and RX”, wire rate transfer is not possible because RX has higher throughput. For example (MII or GMII), The IFG supported by RX is 12 bytes, but the IFG inserted by TX is 64-128 bytes.

2.3 Block diagram

Fig 2.1 shows R-Switch 3 block diagram.

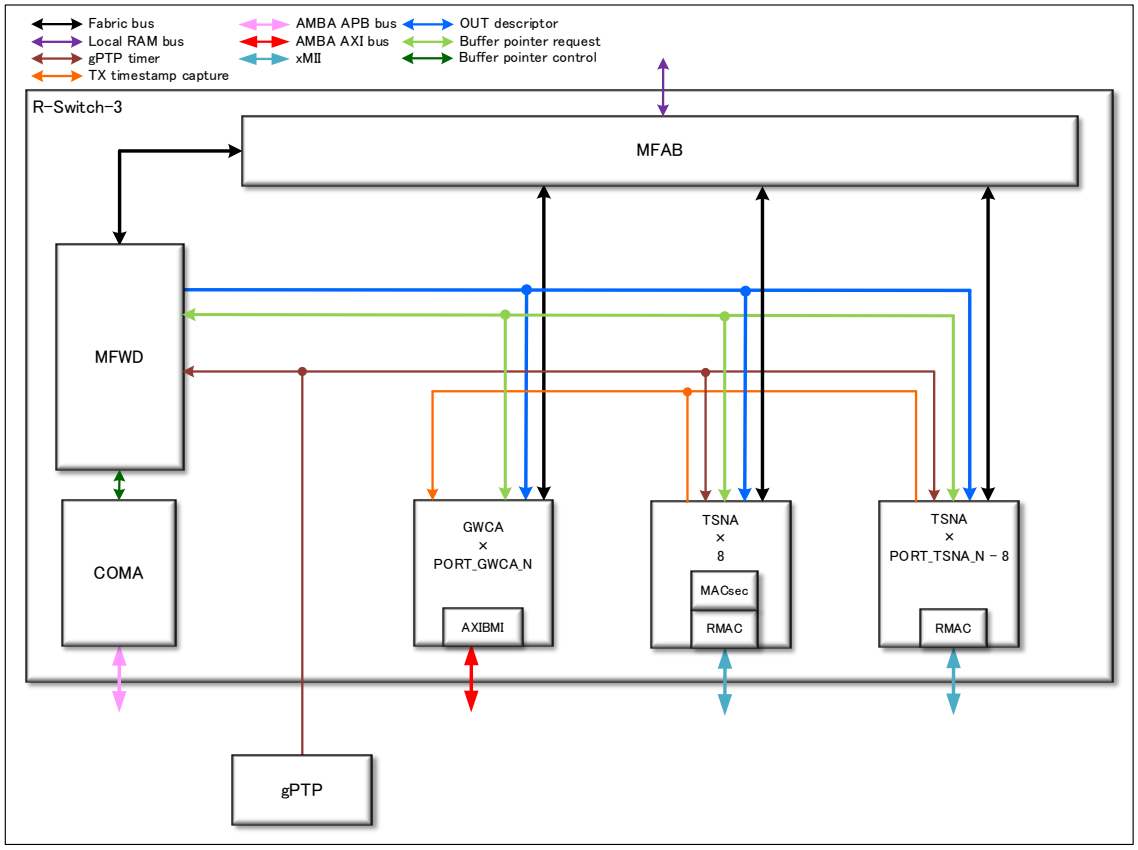


Fig 2.1: R-Switch 3 Block diagram

Table 2-1 R-Switch 3 Functional Blocks

Block name	Function
R-Switch 3	TOP
MFWD	Forwarding engine This module receives descriptor from different interface and aims at forwarding these descriptors to other interfaces based on MAC destination address and VLAN. This module also handles the R-ACE local memory pointers and PSFP [PSFP] ingress port filtering.
MFAB	Fabric It is a bus system connecting MFWD, Agents and local RAM.
ETHA	Ethernet TSN Agent The Ethernet Agent includes an Ethernet controller (MAC) conformed to the definition of MAC (Media Access Control) layer for Ethernet in the IEEE 802.3 standard. When connected with a physical-layer LSI chip (PHY-LSI) that complies with the standard, MAC is able to transmit and receive Ethernet (IEEE 802.3) frames. MAC has a single MAC layer interface.
GWCA	Gateway CPU Agent

	The GWCA consists of, a CPU sub-system executing the SW controlling R-ACE and, an agent interface module to allow communication within the R-ACE system. It handles the data exchange between the Rswitch (R-ACE GW engine) and the GWCPU subsystem.
COMA	Common Agent The COMA consists of, APB IF and Buffer pointer control for reject path and error descriptor.
gPTP	gPTP timer module External IP “uciapgptp030”

3. Parameter list

R-switch 3 global parameter list is shown in Table 3-1.

R-switch 3 local parameter list is shown in Table 3-2.

GWCA specific parameters are described in section 3.1.

TSNA specific parameters are described in section 3.2.

Table 3-1 Global parameter list

Parameter Name	R-Switch-3.0 Values	Explanation
SFRs		
RACE_PADDR_NBR_FWD	**110592/4**	Number of addresses used by Forwarding Engine SFRs [FWD] divided by 4 (bytes)
RACE_PADDR_NBR_FAB	4096/4	Number of addresses used by Fabric SFRs [FAB] divided by 4 (bytes)
RACE_PADDR_NBR_COMA	4096/4	Number of addresses used by Common Agent SFRs [COMA] divided by 4 (bytes)
RACE_PADDR_NBR_TSNA	8192/4	Number of addresses used by TSNA SFRs [TSNA] divided by 4 (bytes)
RACE_PADDR_NBR_GWCA	8192/4	Number of addresses used by GWCA SFRs [GWCA] divided by 4 (bytes)
RACE_PADDR_NBR_ACPA	8192/4	Number of addresses used by ACPA SFRs [ACPA] divided by 4 (bytes)
AXI master		
RACE_AXI_CHAIN_N	128	AXI Descriptor Chain number per GWCA [GWCA]
Port Number		
RACE_PORT_TSNA_N	**13**	TSN Agent Number [TSNA] Because of product rule restrictions, this parameter does not work. Changing this parameter will require RTL modification.
RACE_PORT_GWCA_N	**2**	CPU Agent Number [GWCA] Because of product rule restrictions, this parameter does not work. Changing this parameter will require RTL modification.
Local RAM		
RACE_LCL_RAM_SZ	**1024**	Local RAM size in Kbytes
RACE_LCL_RAM_BSZ	128	Local RAM block size (A pointer will always link to a LOCAL_RAM_BSZ byte block size in the local RAM)
RACE_LCL_RAM_DW	512	Local RAM data bit size
RACE_LCL_RAM_ECCR_N	8	Local RAM ECC error recovery number. Number of ECC error losing pointer allowed in the Buffer pool.
Frame		
RACE_FRM_TPL_W	16	Frame TPL (Total payload length) Width
RACE_FRM_VCTRL_W	3	Frame VLAN control width
Layer 3 forwarding/routing		
RACE_LTH_STREAM_N	1024	L3 stream number
RACE_LTH_RRULE_N	**2048**	L3 rule number (routing rule)
RACE_LTH_REMAP_N	32	L3 rule remapping number
RACE_LTH_SEQGN_N	32	L3 sequence generation rule number
RACE_LTH_RSLICE_WR_N	0	L3 hash write register slice number

Parameter Name	R-Switch-3.0 Values	Explanation
RACE_LTH_RSLICE_RD_N	1	L3 hash read register slice number
gPTP timer		
RACE_PTP_TN	2	gPTP timer number connected to the switch
Cut-through		
RACE_CT_CRULE_N	8	Cut-through rule number
Perfect filter		
RACE_PFL_TWBF_N	**512**	Two-byte filter number
RACE_PFL_THBF_N	**128**	Three-byte filter number
RACE_PFL_FOBF_N	**512**	Four-byte filter number
RACE_PFL_RAGF_N	**128**	Range-byte filter number
RACE_PFL_CADF_N	**512**	Cascade filter number
RACE_PFL_CFMF_N	7	Cascade filter mapped filter number
RACE_PFL_SID_W	7 + 128	Cascade filter stream ID width
PSFP[802.1Qci]		
RACE_PSFP_MSDU_N	16	PSFP MSDU filer number
RACE_PSFP_GATE_N	8	PSFP gate number
RACE_PSFP_DMTR_N	**104**	PSFP double bucket meter number
RACE_PSFP_SMTR_N	**1**	PSFP single bucket meter number
ATS[802.1Qcr]		
RACE_ATS_DESCR_N	16	Descriptor queue depth per meter in ATS table
FRER[802.1CB]		
RACE_FRER_RECE_N	128	FRER recovery entry number
RACE_FRER_HIST_LEN	14	FRER history length
RACE_FRER_RSLICE_WR_N	0	FRER write register slice number
RACE_FRER_RSLICE_RD_N	1	FRER read register slice number
Layer 2 forwarding		
RACE_MAC_ENTRY_N	2048	MAC table entry number
RACE_MAC_RSLICE_WR_N	0	MAC hash write register slice number
RACE_MAC_RSLICE_RD_N	1	MAC hash read register slice number
RACE_MAC_HW_LRN_N	8	MAC hardware leaning number (Number of MAC addresses that can be stored for HW learning before failing)
RACE_VLAN_RSLICE_WR_N	0	VLAN table write register slice number
RACE_VLAN_RSLICE_RD_N	1	VLAN table read register slice number
Counter		
RACE_COUNT_LOW_W	**32**	Low size Counter width
RACE_COUNT_MED_W	32	Medium size Counter width
RACE_COUNT_HIGH_W	64	High size Counter width
Pause frame		
RACE_PAS_LVL_N	2	Pause level number
Gate filter [802.1Qci]		
RACE_GATE_RAM_DP	256	PSFP gate filter RAM depth
CPU core		
RACE_CPU_CORE_N	8	CPU core number (defines the number of interrupt line)

Parameter Name	R-Switch-3.0 Values	Explanation
TCAM/CAM		
MFWD_FRM_PRIO_N	8	MFWD frame priority
MFWD_INTG_ETYPE_N	8	MFWD integrity check ether-type number
MFWD_INTG_FILT_SIPA_N	1	MFWD integrity check Source IP number
RACE_TCAM_DATA_W	135	L3 table TCAM data wisth
RACE_CAM_DATA_W	48	MAC table CAM data wisth

Table 3-2 Local parameter list

Parameter Name	R-Switch-3.0	Equation/Value	Explanation
SFRs			
RACE_PADDR_NBR_FWD_W	**15**	= $clog2(PADDR_NBR_FWD)	Number of addresses used by Forwarding Engine SFRs bus width[FWD]
RACE_PADDR_NBR_FAB_W	10	= $clog2(PADDR_NBR_FAB)	Number of addresses used by Fabric SFRs bus width[FAB]
RACE_PADDR_NBR_COMA_W	10	= $clog2(PADDR_NBR_COMA)	Number of addresses used by Common Agent SFRs bus width
RACE_PADDR_NBR_GWCA_W	11	= $clog2(PADDR_NBR_GWCA)	Number of addresses used by GWCA SFRs bus width[GWCA]
RACE_PADDR_NBR_TSNA_W	11	= $clog2(PADDR_NBR_TSNA)	Number of addresses used by TSN Agent SFRs bus width[TSN]
RACE_PADDR_AW	**16**	= $clog2(PADDR_NBR_FWD + PORT_TSNA_N*PADDR_NBR_TSNA+ PORT_ACPA_N*PADDR_NBR_ACPA+ PORT_GWCA_N*PADDR_NBR_GWCA+PADDR_NBR_COMA+ PADDR_NBR_FAB)	APB address bus width (the two APB unused bits are not taken in account)
AXI master			
RACE_AXI_CHAIN_W	**7**	= $clog2 (RACE_AXI_CHAIN_N)	AXI descriptor chain width
Port Number			

Parameter Name	R-Switch-3.0	Equation/Value	Explanation
RACE_PORT_N	**15**	= RACE_PORT_TSNA_N + RACE_PORT_GWCA_N	Port number on the switch
RACE_PORT_W	4	= $clog2 (RACE_PORT_N)	Port number on the switch bus width
RACE_PORT_W1	5	= $clog2 (RACE_PORT_N+1)	Port number on the switch +1 bus width
RACE_PORT_TIME_N	**13**	= RACE_PORT_TSNA_N	Number of time critical ports on the switch (plugged to the Fabric time arbiter [FAB])
RACE_PORT_TIME_W	**4**	= $clog2 (RACE_PORT_TIME_N)	Time critical port number on the switch bus width
RACE_PORT_SLOW_N	3	= RACE_PORT_GWCA_N + RACE_PORT_ACOP_N	Number of non-time critical ports on the switch (plugged to the Fabric LRU arbiter [FAB])
RACE_PORT_SLOW_W	2	= $clog2 (RACE_PORT_SLOW_N)	Non-time critical port number on the switch bus width
RACE_PORT_SLOW_2W	3	= $clog2 (2* RACE_PORT_SLOW_N)	Non-time critical port number *2 on the switch bus width
RACE_PORT_TSNA_W	4	= $clog2 (RACE_PORT_TSNA_N)	Number of ether TSN ports on the switch bus width
RACE_PORT_GWCA_W	1	= $clog2 (RACE_PORT_GWCA_N)	Number of GWCA ports on the switch bus width
RACE_PORT_FSRC_N	29	= RACE_PORT_N+ RACE_PORT_TIME_N	Forwarding source number
RACE_PORT_FSRC_W	5	= $clog2 (RACE_PORT_FSRC_N)	Forwarding source number bus width
RACE_PORT_FTSRC_N	26	= 2* RACE_PORT_TIME_N	Forwarding time-critical source number
RACE_PORT_FTSRC_W	5	= $clog2(RACE_PORT_FTSRC_N)	Forwarding time-critical source number bus width
Local RAM			
RACE_LCL_PTR_N	8192	= RACE_LCL_RAM_SZ * 1024 / RACE_LCL_RAM_BSZ	Pointer number to address local RAM
RACE_LCL_PTR_W	13	= $clog2(RACE_LCL_PTR_N)	Pointer width
RACE_LCL_PTR_W1	14	= $clog2(RACE_LCL_PTR_N+1)	Pointer+1 width
RACE_LCL_RAM_ECCR_W	3	= $clog2(RACE_LCL_RAM_ECCR_N)	Local RAM ECC error recovery bus width

Parameter Name	R-Switch-3.0	Equation/Value	Explanation
RACE_LCL_RAM_ECCR_W1	4	= $clog2(RACE_LCL_RAM_ECCR_N+1)	Local RAM ECC error recovery +1 bus width
Frame			
RACE_FRM_MTN_W	5	= $clog2(RACE_PORT_N+5)	Port number on the switch bus width
RACE_FRM_TIME_W	26	= $clog2((2**RACE_FRM_TPL_W)*8*100)	Frame time in ns bus width
Layer 3 forwarding/routing			
RACE_LTH_STREAM_W	10	= $clog2(RACE_LTH_STREAM_N)	L3 stream number bus width
RACE_LTH_RRULE_W	11	= $clog2(RACE_LTH_RRULE_N)	L3 rule number (routing rule) bus width
gPTP timer			
RACE_PTP_TN_W	1	= $clog2(RACE_PTP_TN)	gPTP timer number connected to the switch bus width
Cut-through			
RACE_CT_CRULE_W	3	= $clog2(RACE_CT_CRULE_N)	Cut-through rule number bus width
RACE_CT_MTN_N	18	= RACE_PORT_N+1+1	Cut-through multicast number
RACE_CT_MTN_W	5	= $clog2(RACE_CT_MTN_N)	Cut-through multicast number bus width
Perfect filter			
RACE_PFL_CADF_W	9	= $clog2(RACE_PFL_CADF_N)	Cascade filter number bus width
RACE_PFL_TFIL_N	2560	= 2*(RACE_PFL_TWBF_N+ RACE_PFL_THBF_N+ RACE_PFL_FOBF_N+ RACE_PFL_RAGF_N)	Total filter number
RACE_PFL_TFIL_W	12	= $clog2(RACE_PFL_TFIL_N)	Total filter number bus width
PSFP[802.1Qci]			
RACE_PSFP_MSDU_W	4	= $clog2(RACE_PSFP_MSDU_N)	PSFP MSDU filer number bus width

Parameter Name	R-Switch-3.0	Equation/Value	Explanation
RACE_PSFP_GATE_W	3	= $clog2(RACE_PSFP_GATE_N)	PSFP gate number bus width
RACE_PSFP_MTR_N	105	= RACE_PSFP_DMTR_N+ RACE_PSFP_SMTR_N	PSFP meter number
RACE_PSFP_MTR_W	7	= $clog2(RACE_PSFP_MTR_N)	PSFP meter number bus width
RACE_PSFP_GENTRY_N	16	= RACE_GATE_RAM_DP/ RACE_PSFP_GATE_N/2	Maximum entry number for a gate for a running schedule
RACE_PSFP_GENTRY_W	4	= $clog2(RACE_PSFP_GENTRY_N)	Maximum entry number for a gate for a running schedule bus width
RACE_PSFP_GENTRY_W1	5	= $clog2(RACE_PSFP_GENTRY_N+1)	Maximum entry number for a gate for a running schedule +1 bus width
ATS[802.1Qcr]			
RACE_ATS_DESCR_W	4	= $clog2(RACE_ATS_DESCR_N)	Descriptor queue depth per meter in ATS table bus width
RACE_ATS_DESCR_W1	5	= $clog2(RACE_ATS_DESCR_N+1)	Descriptor queue depth per meter in ATS table +1 bus width
FRER[802.1CB]			
RACE_FRER_RECE_W	7	= $clog2(RACE_FRER_RECE_N)	FRER recovery entry number bus width
RACE_FRER_HIST_LEN1	15	= RACE_FRER_HIST_LEN+1	FRER history length + 1
RACE_FRER_HIST_LEN_W	4	= $clog2(RACE_FRER_HIST_LEN)	FRER history length bus width
RACE_FRER_HIST_LEN_W1	4	= $clog2(RACE_FRER_HIST_LEN+1)	FRER history length + 1 bus width
RAMs			
RACE_LCL_RAM_DW	512	128-512	Local RAM data bus width
RACE_LCL_RAM_AW	14	$clog2(RACE_LCL_RAM_SZ*1024/RACE_LCL_RAM_DW*8)	Local RAM address bus width

Parameter Name	R-Switch-3.0	Equation/Value	Explanation
RACE_LCL_DATA_SIZE	6	$clog2(RACE_LCL_RAM_DW/8)	Local RAM data size width
RACE_BPR_RAM_DW	16	RACE_FRM_MTN_W+ RACE_LCL_PTR_W	Buffer pool RAM data bus width
RACE_RJT_RAM_DW	43	RACE_PORT_W+RACE_FRM_TPL_W+RACE_LCL_PTR_W+RACE_FRM_MTN_W+RACE_FRM_MTN_W	Reject RAM data bus width
RACE_LTH_META_INFO_W	74	0+0+1+1+RACE_PSFP_MSDU_W+1+RACE_PSFP_GATE_W+ 1+RACE_PSFP_MTR_W+1 +RACE_FRER_RECE_W+1 +RACE_LTH_RRULE_W+0 + RACE_PORT_N+RACE_PORT_GWCA_N*RACE_AXI_CHAIN_W+1+1+1+3	Layer 3 meta info data width
RACE_LTH_RAM_DW	97	RACE_PORT_N+RACE_LTH_META_INFO_W+4+4+1+ 0+0+0+0,	Layer 3 RAM data width
RACE_ATS_RAM_DW	199	3+1+RACE_AXI_CHAIN_W* RACE_PORT_GWCA_N+RACE_PORT_W+RACE_LCL_PTR_W+RACE_PORT_N+ 1+1+1+1+1+1+24+24+24+1 +RACE_FRER_RECE_W+1 +RACE_LTH_RRULE_W+RACE_FRM_VCTRL_W+1+1 6+1+1+1+RACE_FRM_MTN_W+1+RACE_FRM_MTN_W+RACE_FRM_TPL_W	ATS RAM data width
RACE_ATS_RAM_AW	11	$clog2(RACE_ATS_DESCR_N*RACE_PSFP_MTR_N)	ATS RAM address width
RACE_FRER_RAM_DW	8	RACE_FRER_HIST_LEN_W+RACE_FRER_HIST_LEN1+16+1+1+RACE_FRER_RECE_W+10+10	FRER RAM data width
RACE_GATE_RAM_AW	6	$clog2(RACE_GATE_RAM_DP)	PSFP gate filter RAM address width
Layer 2 forwarding			

Parameter Name	R-Switch-3.0	Equation/Value	Explanation
RACE_MAC_ENTRY_W	11	= $clog2(RACE_MAC_ENTRY_N)	MAC table entry number bus width
RACE_MAC_META_INFO_W	78	0+0+1+1+RACE_PSFP_MSDU_W+1+RACE_PSFP_GATE_W+1+RACE_PSFP_MTR_W+1+RACE_FRER_RECE_W+0+0+RACE_PORT_N+RACE_PORT_N+RACE_PORT_GWCA_N*RACE_AXI_CHAIN_W+1+1+1+3,	MAC meta info width
RACE_VLAN_META_INFO_W	90	RACE_PORT_N+0+1+1+RACE_PSFP_MSDU_W+1+RACE_PSFP_GATE_W+1+RACE_PSFP_MTR_W+1+RACE_FRER_RECE_W+1+RACE_LTH_RRULE_W+0+RACE_PORT_N+RACE_PORT_GWCA_N*RACE_AXI_CHAIN_W+1+1+1+3,	VLAN meta info width
RACE_MAC_RAM_DW	106	= 1 + 1 + 1 + RACE_MAC_ENTRY_W + 48 + 1 + 1 + 1 + 1 + RACE_PORT_N + RACE_PORT_N + RACE_PORT_N + RACE_PORT_GWCA_N* RACE_AXI_CHAIN_W + 1 + 1 + 1 + 3	MAC table data width
RACE_VLAN_RAM_DW	117	= 1 + 1 + PORT_N + 1 + PORT_N + PORT_GWCA_N*AXI_CHAIN_W + 1 + 1 + 1 + 3	VLAN table data width
RACE_L23U_RAM_DW	110	RACE_PORT_N+1+1+1+1+1+1+1+1+1+3+2+48+12+3+1+12+3+1,	L23U data width
RACE_CPU_CORE_W	3	$clog2(RACE_CPU_CORE_N)	CPU core number width

Parameter Name	R-Switch-3.0	Equation/Value	Explanation
RACE_PFL_META_INFO_W	90	1+1+RACE_PSFP_MSDU_W+1+RACE_PSFP_GATE_W+1+RACE_PSFP_MTR_W+1+RACE_FRER_RECE_W+1+RACE_LTH_RRULE_W+RACE_PORT_N+RACE_PORT_GWCA_N*RACE_AXI_CHAIN_W+1+1+1+3,	
RACE_PFL_RAM_DW	116	RACE_PORT_N+RACE_PFL_META_INFO_W+4+4+1+0+0+1	

3.1 GWCA i parameter (i=0..RACE_PORT_GWCA_N)

GWCA i global parameter list is shown in Table **3-3**.

GWCA i local parameter list is shown in Table **3-4**.

Table 3-3: GWCA i global parameter list

Parameter Name	R-Switch-3.0 Values	Explanation
My port number		
GWCA[i]_MY_PORT_N	RACE_PORT_TSNA_N+i	My port number Refer to Fabric specification to know an agent port number [FAB].
AXI master		
GWCA[i]_AXI_RINC_N	8	RX incremental descriptor Chain number.
GWCA[i]_AXI_TLIM_N	32	TX rate limiter number.
GWCA[i]_AXI_DW	128	AXI bus Data width
GWCA[i]_AXI_AW	40	AXI bus address width
GWCA[i]_AXI_BST_SZ	256	AXI burst size. Restrictions: - AXI_BST_SZ maximum value is AXI_DW*2.
GWCA[i]_AXI_RD_OUT_N	16	AXI read outstanding number Also equal to the number of read IDs.
GWCA[i]_AXI_WR_OUT_N	16	AXI write outstanding number. Also equal to the number of write IDs.
GWCA[i]_AXI_RD_BUF_DP	128	Read data bus buffer depth
GWCA[i]_AXI_WR_BUF_DP	128	Write data bus buffer depth
GWCA[i]_AXI_RX_DESCR_PRE_N	4	RX descriptor prefetch number
GWCA[i]_AXI_TX_DESCR_PRE_N	4	TX descriptor prefetch number
Frame		
GWCA[i]_FRM_PRIO_N	8	Priority number handled by GWCA
Descriptor RAM		
GWCA[i]_DES_RAM_DP	**2048**	Descriptor RAM depth
Timestamp RAM		
GWCA[i]_TS_RAM_DP	**256**	Timestamp RAM depth

Table 3-4: GWCA i local parameter list

Parameter Name	R-Switch-3.0	Explanation
AXI master		
GWCA[i]_AXI_RINC_W	3	AXI RX incremental chain width
GWCA[i]_AXI_STRB_W	16	AXI strobe width
GWCA[i]_AXI_STRB_WW	4	AXI strobe width width
GWCA[i]_AXI_RD_OUT_W	4	AXI read outstanding number width
GWCA[i]_AXI_RD_OUT_W1	5	AXI read outstanding number +1 width
GWCA[i]_AXI_WR_OUT_W	4	AXI write outstanding number width
GWCA[i]_AXI_WR_OUT_W1	5	AXI write outstanding number +1 width
GWCA[i]_AXI_BST_SZ_W	8	AXI burst size width
Frame		
GWCA[i]_FRM_PRIO_W	3	Priority width
Descriptor RAM		
GWCA[i]_DES_RAM_AW	11	Descriptor RAM address width
GWCA[i]_DES_RAM_AW1	12	Descriptor RAM address width
GWCA[i]_DES_RAM_DW	104	Descriptor RAM Data Width
Multicast RAM		
GWCA[i]_RMS_RAM_DW	22	RX multicast RAM Data Width
Timestamp RAM		
GWCA[i]_TS_RAM_DW	79	Timestamp RAM data width
GWCA[i]_TS_RAM_AW	8	Timestamp RAM address width
GWCA[i]_TS_RAM_AW1	9	Timestamp RAM address + 1 width

3.2 TSNA i parameter (i=0..RACE_PORT_TSNA_N)

TSN agent i global parameter list is shown in **Table 3-5**.

TSN agent i local parameter list is shown in **Table 3-6**.

Table 3-5 TSNA i global parameter list

Parameter Name	R-Switch-3.0 Values	Explanation
My port number		
ETHA[i]_MY_PORT_N	i	My port number Refer to Fabric specification to know an agent port number [FAB].
Frame		
ETHA[i]_FRM_PRIO_N	8	Priority number handled by TSNA
Cut-through		
ETHA[i]_CT_DESCR_N	8	Cut-through descriptor number
Descriptor RAM		
ETHA[i]_DES_RAM_DP	**2048**	Descriptor RAM depth
TAS RAM		
ETHA[i]_TAS_RAM_DP	256	TAS RAM depth

Table 3-6 TSNA i local parameter list

Parameter Name	R-Switch-3.0	Explanation
Frame		
ETHA[i]_FRM_PRIO_W	3	Priority width
ETHA[i]_FRM_TPRIO_N	9	Number of priorities including cut-through
ETHA[i]_FRM_TPRIO_W	4	Number of priorities including cut-through bus width
Cut-through		
ETHA[i]_CT_DESCR_W1	4	Cut-through descriptor number +1 bus width
Descriptor RAM		
ETHA[i]_DES_RAM_AW	11	Descriptor RAM address width
ETHA[i]_DES_RAM_AW1	12	Descriptor RAM address width
ETHA[i]_DES_RAM_DW	**72**	Descriptor RAM Data Width
TAS RAM		
ETHA[i]_TAS_RAM_AW	8	Timestamp RAM address width

4. Register

4.1 Register mapping

The R-Switch 3 register map is described in Table 4-1. This table is only an example of address mapping based on the switch default parameters. For the parameter dependant mapping, refer to common agent specification [COMA].

Access Mode:

- Any: Register can be accessed in any mode.

Note:

- All registers can be read in any mode.
- “Clear conditions” is having the higher priority than “Set conditions”.

Table 4-1: R-Switch 3 register map

Address range	Offset while reding specification documents	Register name
0_0000H-1_AFFFH	FWRO offset	[MFWD] registers
1_B000H-1_BFFFH	TPRO offset	[MFAB] registers In this version, fabric register address range is used for interrupt controller registers described in this document because fabric has no registers.
1_C000H-1_CFFFH	CARO offset	[COMA] registers
1_D000H-1_EFFFH	TARO offset of TSNA0, RMRO offset RMAC0 (TSNA have 1000H, RMAC have 1000H)	[ETHA] registers (port 0), [RMAC] registers (port 0)
1_F000H-2_0FFFH	TARO offset of TSNA1, RMRO offset RMAC1	[ETHA] registers (port 1), [RMAC] registers (port 1)
2_1000H-2_2FFFH	TARO offset of TSNA2, RMRO offset RMAC2	[ETHA] registers (port 2), [RMAC] registers (port 2)
2_3000H-2_4FFFH	TARO offset of TSNA3, RMRO offset RMAC3	[ETHA] registers (port 3), [RMAC] registers (port 3)
2_5000H-2_6FFFH	TARO offset of TSNA4, RMRO offset RMAC4	[ETHA] registers (port 4), [RMAC] registers (port 4)
2_7000H-2_8FFFH	TARO offset of TSNA5, RMRO offset RMAC5	[ETHA] registers (port 5), [RMAC] registers (port 5)
2_9000H-2_AFFFH	TARO offset of TSNA6, RMRO offset RMAC6	[ETHA] registers (port 6), [RMAC] registers (port 6)
2_B000H-2_CFFFH	TARO offset of TSNA7, RMRO offset RMAC7	[ETHA] registers (port 7), [RMAC] registers (port 7)
2_D000H-2_EFFFH	TARO offset of TSNA8, RMRO offset RMAC8	[ETHA] registers (port 8), [RMAC] registers (port 8)
2_F000H-3_0FFFH	TARO offset of TSNA9, RMRO offset RMAC9	[ETHA] registers (port 9), [RMAC] registers (port 9)
3_1000H-3_2FFFH	TARO offset of TSNA10, RMRO offset RMAC10	[ETHA] registers (port 10), [RMAC] registers (port 10)
3_3000H-3_4FFFH	TARO offset of TSNA11, RMRO offset RMAC11	[ETHA] registers (port 11), [RMAC] registers (port 11)
3_5000H-3_6FFFH	TARO offset of TSNA12, RMRO offset RMAC12	[ETHA] registers (port 12), [RMAC] registers (port 12)
3_7000H-3_8FFFH	GWRO offset of GWCA0	[GWCA] registers (port 13)
3_9000H-3_AFFFH	GWRO offset of GWCA1	[GWCA] registers (port 14)

4.2 Register attributes

The register attribute defines what kind of access a register supports. Per one register, there are always two attributes, a register access attribute which define what kind of accesses a register supports and, a register security attribute which define what accesses can perform the unsecure APB [APB] in the register access attribute depending on the security setting in security registers.

“Representation of register access attributes “ describes register access attributes and “Representation of register security attributes” describes register security attributes. Attributes are given to a register field in Register detailed explanation section by specifying the attribute symbols in the R/W-P column.

Table 4-2: Register access attributes

Symbol	Meaning	Impact on accesses	
		Write access	Read access
RW	Read write	Write value is written	Written value is read
R!=W	Read different than write	Write access happens	Read value differs from written value
R	Read only	Write value is ignored	Read access happens
R0	Only Read 0	Write value is ignored	Always read '0'
R1	Only Read 1	Write value is ignored	Always read '1'
R0W	Read 0 write	Write access happens	Always read as '0'
R1W	Read 1 write	Write access happens	Always read as '1'
RC	Read clear	Write value is ignored	Read access happens Read access clears the register

Table 4-3: Register security attributes

Symbol	Meaning	Impact on accesses	
		Write access	Read access
U	Unprotected	Write access happens for unsecure APB	Read access happens for unsecure APB
P	Protected	A security register should be set to authorize write access by the unsecure APB	A security register should be set to authorize read access by the unsecure APB
RU	Read-Unprotected	Write value ignored for unsecure APB	Read access happens for unsecure APB
RP	Read protected	Write value ignored for unsecure APB	A security register should be set to authorize read access by the unsecure APB
D	Duplicated	Write access happens for unsecure APB to a duplicated and independent register	Read access happens for unsecure APB to a duplicated and independent register
F	Forbidden	Write value ignored for unsecure APB	Read value ignored for unsecure APB
S	Switch	A security register should be set to authorize write access by the unsecure APB. A security register should be set to unauthorize write access by the secure APB.	A security register should be set to authorize read access by the unsecure APB

4.3 Register list

The TOP module register list is described in Table 4-1. TPRO (TOP Register Offset) indicates base address of address space allocated to TOP module by the system. All registers representations are done with the default values of the section 3. If the TOP module is not use with default parameters, it should be taken in account by the user while reading the SFR representation.

Notes:

- A register can have two addresses. The address preceded by “E:” correspond to an emulation address which allows to read a register without modifying its content.

Table 4-4: List of TOP module registers

Offset/Address	Register name	Abbreviation
TPRO + 0000H	TOP module Error and Monitoring Interrupt Mapping Configuration 0	TPEMIMC0
TPRO + 0004H	TOP module Error and Monitoring Interrupt Mapping Configuration 1	TPEMIMC1
TPRO + 0010H + 4*t	TOP module GWCA Error and Monitoring Interrupt Mapping Configuration t (t=0..RACE_PORT_GWCA_N-1)	TPGEMIMCt
TPRO + 0050H + 4*t	TOP module ETHA Error and Monitoring Interrupt Mapping Configuration t (t=0..RACE_PORT_TSNA_N-1)	TPEEMIMCt
TPRO + 0090H + 4*t	TOP module GWCA Timestamp Error and Monitoring Interrupt Mapping Configuration t (t=0.. RACE_PTP_TN-1)	TPTEMIMCt
TPRO + 0100H + 4*t	TOP module GWCA Data Error and Monitoring Interrupt Mapping Configuration t (t=0..RACE_AXI_CHAIN_N-1)	TPDEMIMCt
TPRO + 0900H	TOP module Switch Interrupt Mirroring	TSIM
TPRO + 0904H	TOP module Agent Interrupt Mirroring	TAIM
TPRO + 0908H	TOP module Forwarding engine Interrupt Mirroring	TFIM
TPRO + 090CH	TOP module COMA Interrupt Mirroring	TCIM
TPRO + 0910H + 4*t	TOP module GWCA Interrupt Mirroring t (t=0..RACE_PORT_GWCA_N-1)	TGIMt
TPRO + 0950H + 4*t	TOP module ETHA Interrupt Mirroring t (t=0..RACE_PORT_TSNA_N-1)	TEIMt

4.4 Register detailed explanation

This section describes SFR details.

4.4.1 TOP Function registers

4.4.1.1 Interrupt mapping function registers

(1) TPEMIMC0

TOP module Error and Monitoring Interrupt Mapping Configuration 0

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SSICM1 [RACE_CPU_CORE_W-1:0]				RSV / SSIGM1 [RACE_PORT_GWCA_W-1:0]			SSIM1	SSICM0 [RACE_CPU_CORE_W-1:0]				RSV / SSIGM0 [RACE_PORT_GWCA_W-1:0]			SSIM0
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV															

Bits	Bit name	RW-P	Initial value	Function description
RACE_CPU_CORE_W+27:28	SSICM1	RW-F	0H	Switch Status Interrupt Core Mapping 1 Functions: - Used to decide to which pin Switch Status Interrupt 1 are mapped when mapped to a GWCA.
27:RACE_PORT_GWCA_W+25	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
RACE_PORT_GWCA_W+24:25	SSIGM1	RW-F	0H	Switch Status Interrupt GWCA Mapping 1 Values: When **TPEMIMC0.SSIM1** is set to 1'b1, Switch Status Interrupt 1 are mapped to following pins. - 0: mapped to race_gwca0_core_int[**TPEMIMC0.SSICM1**] - 1: mapped to race_gwca1_core_int[**TPEMIMC0.SSICM1**]
24	SSIM1	RW-F	0H	Switch Status Interrupt Mapping 1 Values: - 1'b0: Switch Status Interrupt 1 are mapped to race_race_status_int - 1'b1: Switch Status Interrupt 1 are mapped to a specific core depending on **TPEMIMC0.SSIGM1** register Switch Status Interrupt 1 contain the following interrupts: - **RSSIS.NSSSISi** (i=0..7) [COMA].
RACE_CPU_CORE_W+19:20	SSICM0	RW-F	0H	Switch Status Interrupt Core Mapping 0 Functions: - Used to decide to which pin Switch Status Interrupt 0 are mapped when mapped to a GWCA.
19:RACE_PORT_GWCA_W+17	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.

RACE_PORT_GWCA_W+16 :17	SSIGM0	RW-F	0H	Switch Status Interrupt GWCA Mapping 0 Values: When **TPEMIMC0.SSIM0** is set to 1'b1, Switch Status Interrupt 0 are mapped to following pins. - 0: mapped to race_gwca0_core_int[**TPEMIMC0.SSICM0**] - 1: mapped to race_gwca1_core_int[**TPEMIMC0.SSICM0**]
16	SSIM0	RW-F	0H	Switch Status Interrupt Mapping 0 Values: - 1'b0: Switch Status Interrupt 0 are mapped to race_race_status_int - 1'b1: Switch Status Interrupt 0 are mapped to a specific core depending on **TPEMIMC0.SSIGM0** register Switch Status Interrupt 0 contain the following interrupts: - **RSSIS.SNSSISi** (i=0..7) [COMA].
15:0	RSV	R0-U	0H	- Reserved area. On read, 0 will be returned.

(2) TPEMIMC1

TOP module Error and Monitoring Interrupt Mapping Configuration 1

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CSICM [RACE_CPU_CORE_W-1:0]				RSV / CSIGM [RACE_PORT_GWCA_W -1:0]			CSIM	CEICM [RACE_CPU_CORE_W-1:0]				RSV / CEIGM [RACE_PORT_GWCA_W -1:0]			CEIM
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FSICM [RACE_CPU_CORE_W-1:0]				RSV / FSIGM [RACE_PORT_GWCA_W -1:0]			FSIM	FEICM [RACE_CPU_CORE_W-1:0]				RSV / FEIGM [RACE_PORT_GWCA_W -1:0]			FEIM

Bits	Bit name	RW-P	Initial value	Function description
RACE_CPU_CORE_W+27 : 28	CSICM	RW-F	0H	Common Status Interrupt Core Mapping Functions: - Used to decide to which pin Common Status Interrupt are mapped when mapped to a GWCA. - Refer to **TPEMIMC1.CSIGM**
27:RACE_PORT_GWCA_W+25	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
RACE_PORT_GWCA_W+ 24:25	CSIGM	RW-F	0H	Common Status Interrupt GWCA Mapping Values: When **TPEMIMC1.CSIM** is set to 1'b1, Common Status Interrupt are mapped to following pins. - 0: mapped to race_gwca0_core_int[**TPEMIMC1.CSICM**] - 1: mapped to race_gwca1_core_int[**TPEMIMC1.CSICM**]
24	CSIM	RW-F	0H	Common Status Interrupt Mapping Values: - 1'b0: Common Status Interrupt are mapped to race_coma_status_int - 1'b1: Common Status Interrupt are mapped to a specific core depending on **TPEMIMC1.CSIGM** register Common Status Interrupt contain the following interrupts: - **CAMIS0** [COMA] - **CAMIS1** [COMA]
RACE_CPU_CORE_W+19 : 20	CEICM	RW-F	0H	Common Error Interrupt Core Mapping Functions: - Used to decide to which pin Common Error Interrupt are mapped when mapped to a GWCA.
19:RACE_PORT_GWCA_W+17	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
RACE_PORT_GWCA_W+ 16:17	CEIGM	RW-F	0H	Common Error Interrupt GWCA Mapping Values: When **TPEMIMC1.CEIM** is set to 1'b1, Common Error Interrupt are mapped to following pins. - 0: mapped to race_gwca0_core_int[**TPEMIMC1.CEICM**] - 1: mapped to race_gwca1_core_int[**TPEMIMC1.CEICM**]

16	CEIM	RW-F	0H	Common Error Interrupt Mapping Values: - 1'b0: Common Error Interrupt are mapped to race_coma_error_int - 1'b1: Common Error Interrupt are mapped to a specific core depending on **TPEMIMC1.CEIGM** register Common Error Interrupt contain the following interrupts: - **CAEIS0** [COMA] - **CAEIS1** [COMA]
RACE_CPU_CORE_W+11 : 12	FSICM	RW-F	0H	Forwarding Status Interrupt Core Mapping Functions: - Used to decide to which pin Forwarding Status Interrupt are mapped when mapped to a GWCA.
11:RACE_PORT_GWCA_W+9	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
RACE_PORT_GWCA_W+ 8:9	FSIGM	RW-F	0H	Forwarding Status Interrupt GWCA Mapping Values: When **TPEMIMC1.FSIM** is set to 1'b1, Forwarding Status Interrupt are mapped to following pins. - 0: mapped to race_gwca0_core_int[**TPEMIMC1.FSICM**] - 1: mapped to race_gwca1_core_int[**TPEMIMC1.FSICM**]
8	FSIM	RW-F	0H	Forwarding Status Interrupt Mapping Values: - 1'b0: Forwarding Status Interrupt are mapped to race_mfwd_status_int - 1'b1: Forwarding Status Interrupt are mapped to a specific core depending on **TPEMIMC1.FSIGM** register Forwarding Status Interrupt contain the following interrupts: - **FWMIS0** [FWD]
RACE_CPU_CORE_W+3: 4	FEICM	RW-F	0H	Forwarding Error Interrupt Core Mapping Functions: - Used to decide to which pin Forwarding Error Interrupt are mapped when mapped to a GWCA.
3:RACE_PORT_GWCA_W+1	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
RACE_PORT_GWCA_W:1	FEIGM	RW-F	0H	Forwarding Error Interrupt GWCA Mapping Values: When **TPEMIMC1.FEIM** is set to 1'b1, Forwarding Error Interrupt are mapped to following pins. - 0: mapped to race_gwca0_core_int[**TPEMIMC1.FEICM**] - 1: mapped to race_gwca1_core_int[**TPEMIMC1.FEICM**]

0	FEIM	RW-F	0H	Forwarding Error Interrupt Mapping Values: - 1'b0: Forwarding Error Interrupt are mapped to race_mfwd_error_int - 1'b1: Forwarding Error Interrupt are mapped to a specific core depending on **TPEMIMC1.FEIGM** register Forwarding Error Interrupt contain the following interrupts: - **FWEIS0** [FWD] - **FWEIS1** [FWD] - **FWEIS2** [FWD] - **FWEIS3** [FWD] - **FWEIS4** [FWD] - **FWEIS5** [FWD] - **FWEIS6** [FWD] - **FWEIS7** [FWD] - **FWEIS8** [FWD]

(3) TPGEMIMCt (t=0..RACE_PORT_GWCA_N-1)

TOP module GWCA Error and Monitoring Interrupt Mapping Configuration t

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV								GEICMt [RACE_CPU_CORE_W-1:0]				RSV / GEIGMt [RACE_PORT_GWCA_W -1:0]			GEIMt

Bits	Bit name	RW-P	Initial value	Function description
31:18	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
RACE_CPU_CORE_W+3:4	GEICMt	RW-F	0H	GWCAt Error Interrupt Core Mapping Functions: - Used to decide to which pin GWCAt Error Interrupt are mapped when mapped to a GWCA.
3:RACE_PORT_GWCA_W+1	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
RACE_PORT_GWCA_W:1	GEIGMt	RW-F	0H	GWCAt Error Interrupt GWCA Mapping Values: When **TPGEMIMCt.GEIMt** is set to 1'b1, GWCAt Error Interrupt are mapped to following pins. - 0: mapped to race_gwca0_core_int[**TPGEMIMCt.GEICMt**] - 1: mapped to race_gwca1_core_int[**TPGEMIMCt.GEICMt**]
0	GEIMt	RW-F	0H	GWCAt Error Interrupt Mapping Values: - 1'b0: GWCAt Error Interrupt are mapped to race_ gwca[t]_error_int - 1'b1: GWCAt Error Interrupt are mapped to a specific core depending on **TPGEMIMCt.GEIGMt** register GWCAt Error Interrupt contain the following interrupts: - **GWEIS0** except **GWEIS0.TDFES** for GWCAt [GWCA] - **GWEIS1** for GWCAt [GWCA] - **GWEIS4** for GWCAt [GWCA] - **GWEIS5** for GWCAt [GWCA]

(4) TPEEMIMCt (t=0..RACE_PORT_TSNA_N-1)

TOP module ETHA Error and Monitoring Interrupt Mapping Configuration t

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EMSEICMt [RACE_CPU_CORE_W-1:0]				RSV / EMSEIGMt [RACE_PORT_GWCA_W -1:0]			EMSEIMt	RSV							
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ESICMt [RACE_CPU_CORE_W-1:0]				RSV / ESIGMt [RACE_PORT_GWCA_W -1:0]			ESIMt	EEICMt [RACE_CPU_CORE_W-1:0]				RSV / EEIGMt [RACE_PORT_GWCA_W -1:0]			EEIMt

Bits	Bit name	RW-P	Initial value	Function description
RACE_CPU_CORE_W+27:28	EMSEICMt	RW-F	0H	ETHAt MSEC Error Interrupt Core Mapping Functions: Used to decide to which pin ETHAt MSEC Error Interrupt are mapped when mapped to a GWCA. This register valid only t = 0-7.
27:RACE_PORT_GWCA_W+25	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
RACE_PORT_GWCA_W+24:25	EMSEIGMt	RW-F	0H	ETHAt MSEC Error Interrupt GWCA Mapping Values: When **TPEEMIMCt.EMSEIMt** is set to 1'b1, ETHAt MSEC Error Interrupt are mapped to following pins. - 0: mapped to race_gwca0_core_int[**TPEEMIMCt.EMSEICMt**] - 1: mapped to race_gwca1_core_int[**TPEEMIMCt.EMSEICMt**] This register valid only t = 0-7.
24	EMSIMt	RW-F	0H	ETHAt MSEC Error Interrupt Mapping Values: - 1'b0: ETHAt MSEC Error Interrupt are mapped to race_msc[t]_error_int - 1'b1: ETHAt MSEC Error Interrupt are mapped to a specific core depending on **TPEEMIMCt.EMSEIGMt** register ETHA0 MSEC Error Interrupt contain the following interrupts: - **MSEIS0-2** for ETHAt [MSEC] - **MSAESEIS0-3** for ETHAt [MSEC] - **MSPNTIS** for ETHAt [MSEC] - **MSPNEIS** for ETHAt [MSEC] This register valid only t = 0-7.
23:16	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
RACE_CPU_CORE_W+11:12	ESICMt	RW-F	0H	ETHAt Status Interrupt Core Mapping Functions: - Used to decide to which pin ETHAt Status Interrupt are mapped when mapped to a GWCA.
11:RACE_PORT_GWCA_W+9	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.

RACE_PORT_GWCA_W+8:9	ESIGMt	RW-F	0H	ETHAt Status Interrupt GWCA Mapping Values: When **TPEEMIMCt.ESIMt** is set to 1'b1, ETHAt Status Interrupt are mapped to following pins. - 0: mapped to race_gwca0_core_int[**TPEEMIMCt.ESICMt**] - 1: mapped to race_gwca1_core_int[**TPEEMIMCt.ESICMt**]
8	ESIMt	RW-F	0H	ETHAt Status Interrupt Mapping Values: - 1'b0: ETHAt Status Interrupt are mapped to race_etha[t]_status_int - 1'b1: ETHAt Status Interrupt are mapped to a specific core depending on **TPEEMIMCt.ESIGMt** register ETHA1 Status Interrupt contain the following interrupts: - **MMIS0** for RMACt [RMAC]
RACE_CPU_CORE_W+3:4	EEICMt	RW-F	0H	ETHAt Error Interrupt Core Mapping Functions: - Used to decide to which pin ETHAt Error Interrupt are mapped when mapped to a GWCA.
3:RACE_PORT_GWCA_W+1	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
RACE_PORT_GWCA_W:1	EEIGMt	RW-F	0H	ETHAt Error Interrupt GWCA Mapping Values: When **TPEEMIMCt.EEIMt** is set to 1'b1, ETHAt Error Interrupt are mapped to following pins. - 0: mapped to race_gwca0_core_int[**TPEEMIMCt.EEICMt**] - 1: mapped to race_gwca1_core_int[**TPEEMIMCt.EEICMt**]
0	EEIMt	RW-F	0H	ETHAt Error Interrupt Mapping Values: - 1'b0: ETHAt Error Interrupt are mapped to race_etha[t]_error_int - 1'b1: ETHAt Error Interrupt are mapped to a specific core depending on **TPEEMIMCt.EEIGMt** register ETHA0 Error Interrupt contain the following interrupts: - **EAEIS0** for ETHAt [TSNA] - **EAEIS1** for ETHAt [TSNA] - **EAEIS2** for ETHAt [TSNA] - **MEIS** for RMACt [RMAC]

(5) TPTEMIMCt (t=0..RACE_PTP_TN-1)

TOP module GWCA Timestamp Error and Monitoring Interrupt Mapping Configuration t

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV			GTSICM1t [RACE_CPU_CORE_W-1]				GTSIM1t	RSV			GTSICM0t [RACE_CPU_CORE_W-1]				GTSIM0t

Bits	Bit name	RW-P	Initial value	Function description
31:9+RACE_CPU_CORE_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
RACE_CPU_CORE_W+8:9	GTSICM1t	RW-F	0H	GWCA1 TimeStamp Interrupt Core Mapping timer t Functions: - Map GWCA1 TimeStamp Interrupts t to Race_gwca1_core_int[**TPTEMIMCt.GTSICM1t**] when **TPTEMIMCt.GTSIM1t** is set.
8	GTSIM1t	RW-F	0H	GWCA1 TimeStamp Interrupt Mapping timer t Values: - 1'b0: GWCA1 TimeStamp Interrupt t are mapped to race_gwca1_timer_int[t] - 1'b1: GWCA1 TimeStamp Interrupt t are mapped to race_gwca1_core_int depending on **TPTEMIMCt.GTSICM1t** setting GWCA1 TimeStamp Interrupt contain the following interrupts: - **GWTDIS.TSDIS[t]** for GWCA1 [GWCA] - **GWEIS0.TDFES[t]** for GWCA1 [GWCA]
7:1+RACE_CPU_CORE_W	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
RACE_CPU_CORE_W:1	GTSICM0t	RW-F	0H	GWCA0 TimeStamp Interrupt Core Mapping timer t Functions: - Map GWCA0 TimeStamp Interrupts t to race_gwca0_core_int[**TPTEMIMCt.GTSICM0t**] when **TPTEMIMCt.GTSIM0t** is set.
0	GTSIM0t	RW-F	0H	GWCA0 TimeStamp Interrupt Mapping timer t Values: - 1'b0: GWCA0 TimeStamp Interrupt t are mapped to race_gwca0_timer_int[t] - 1'b1: GWCA0 TimeStamp Interrupt t are mapped to race_gwca0_core_int depending on **TPTEMIMCt.GTSICM0t** setting GWCA0 TimeStamp Interrupt contain the following interrupts: - **GWTDIS.TSDIS[t]** for GWCA0 [GWCA] - **GWEIS0.TDFES[t]** for GWCA0 [GWCA]

(6) TPDEMIMCt (t=0..RACE_AXI_CHAIN_N-1)

TOP module GWCA Data Error and Monitoring Interrupt Mapping Configuration t

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV								GDICM1t [RACE_CPU_CORE_W-1]				GDICM0t [RACE_CPU_CORE_W-1]			

Bits	Bit name	RW-P	Initial value	Function description
31:8	RSV	R0-U	0H	- Reserved area. On read, 0 will be returned.
RACE_CPU_CORE_W+3:4	GDICM1t	RW-F	0H	GWCA1 Data Interrupt Core Mapping t Functions: - Map GWCA1 Data Interrupts t to race_gwca1_core_int[**TPDEMIMCt. GDICM1t**] GWCA1 Data Interrupt contain the following interrupts: - **GWDISi.DISt** for GWCA1 [GWCA] - **GWEIS2i.DFESt** for GWCA1 [GWCA] - **GWEIS3.IAOES[t]** for t=0.. RACE_AXI_RINC_N for GWCA1 [GWCA]
RACE_CPU_CORE_W-1:0	GDICM0t	RW-F	0H	GWCA0 Data Interrupt Core Mapping t Functions: - Map GWCA0 Data Interrupts t to race_gwca0_core_int[**TPDEMIMCt. GDICM0t**] GWCA0 Data Interrupt contain the following interrupts: - **GWDISi.DISt** for GWCA0 [GWCA] - **GWEIS2i.DFESt** for GWCA0 [GWCA] - **GWEIS3.IAOES[t]** for t=0.. RACE_AXI_RINC_N for GWCA0 [GWCA]

4.4.1.2 Interrupt mirroring registers

(1) TSIM

TOP module Switch Interrupt Mirroring

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV														CIM	FIM

Bits	Bit name	RW-P	Initial value	Function description
31:2	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
1	CIM	R-U	0H	Common Interrupt Mirroring Values: - 1'b0: No interrupt is set in common agent - 1'b1: An interrupt is set in common agent CAMIS* or CAEIS* or RSSIS*
0	FWM	R-U	0H	Forwarding engine Interrupt Mirroring Values: - 1'b0: No interrupt is set in forwarding engine - 1'b1: An interrupt is set in forwarding engine FWMIS* or FWEIS*

(2) TAIM

TOP module Agent Interrupt Mirroring

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV / GIM[RACE_PORT_GWCA_N-1:0]															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV / EIM[RACE_PORT_TSNA_N-1:0]															

Bits	Bit name	RW-P	Initial value	Function description
RACE_PORT_GWCA_N+15:16	GIM	R-U	0H	GWCAt Interrupt Monitoring Values: - Bit [t] 1'b0: No interrupt is set in GWCAt - Bit [t] 1'b1: An interrupt is set in GWCAt GWEIS* or GWTSDIS or GWDIS
RACE_PORT_TSNA_N-1:0	EIM	R-U	0H	ETHAt Interrupt Monitoring Values: - Bit [t] 1'b0: No interrupt is set in ETHAt - Bit [t] 1'b1: An interrupt is set in That MMIS or MEIS or EAEIS* or MSEIS0-2 or MSAESEIS0-3 or MSPNTIS or MSPNEIS

(3) TFIM

TOP module Forwarding engine Interrupt Mirroring

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV						FWMISIM0	FWEISIM8	FWEISIM7	FWEISIM6	FWEISIM5	FWEISIM4	FWEISIM3	FWEISIM2	FWEISIM1	FWEISIM0

Bits	Bit name	RW-P	Initial value	Function description
31:10	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
9	FWMISIM0	R-U	0H	FWMIS0 Interrupt Mirroring Values: - 1'b0: No interrupt is set in forwarding engine **FWMIS0** register - 1'b1: An interrupt is set in forwarding engine **FWMIS0** register
8	FWEISIM8	R-U	0H	FWEIS8 Interrupt Mirroring Values: - 1'b0: No interrupt is set in forwarding engine **FWEIS8** register - 1'b1: An interrupt is set in forwarding engine **FWEIS8** register
7	FWEISIM7	R-U	0H	FWEIS7 Interrupt Mirroring Values: - 1'b0: No interrupt is set in forwarding engine **FWEIS7** register - 1'b1: An interrupt is set in forwarding engine **FWEIS7** register
6	FWEISIM6	R-U	0H	FWEIS6 Interrupt Mirroring Values: - 1'b0: No interrupt is set in forwarding engine **FWEIS6** register - 1'b1: An interrupt is set in forwarding engine **FWEIS6** register
5	FWEISIM5	R-U	0H	FWEIS5 Interrupt Mirroring Values: - 1'b0: No interrupt is set in forwarding engine **FWEIS5** register - 1'b1: An interrupt is set in forwarding engine **FWEIS5** register
4	FWEISIM4	R-U	0H	FWEIS4 Interrupt Mirroring Values: - 1'b0: No interrupt is set in forwarding engine **FWEIS4** register - 1'b1: An interrupt is set in forwarding engine **FWEIS4** register
3	FWEISIM3	R-U	0H	FWEIS3 Interrupt Mirroring Values: - 1'b0: No interrupt is set in forwarding engine **FWEIS3** register - 1'b1: An interrupt is set in forwarding engine **FWEIS3** register
2	FWEISIM2	R-U	0H	FWEIS2 Interrupt Mirroring Values: - 1'b0: No interrupt is set in forwarding engine **FWEIS2** register - 1'b1: An interrupt is set in forwarding engine **FWEIS2** register

1	FWEISIM1	R-U	0H	FWEIS1 Interrupt Mirroring Values: - 1'b0: No interrupt is set in forwarding engine **FWEIS1** register - 1'b1: An interrupt is set in forwarding engine **FWEIS1** register
0	FWEISIM0	R-U	0H	FWEIS0 Interrupt Mirroring Values: - 1'b0: No interrupt is set in forwarding engine **FWEIS0** register - 1'b1: An interrupt is set in forwarding engine **FWEIS0** register

(4) TCIM

TOP module COMA Interrupt Mirroring

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV											CAMISIM1	CAMISIM0	CAEISIM1	CAEISIM0	RSSISIM

Bits	Bit name	RW-P	Initial value	Function description
31:5	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
4	CAMISIM1	R-U	0H	CAMIS1 Interrupt Mirroring Values: - 1'b0: No interrupt is set in Common agent **CAMIS1** register - 1'b1: An interrupt is set in Common agent **CAMIS1** register
3	CAMISIM0	R-U	0H	CAMIS0 Interrupt Mirroring Values: - 1'b0: No interrupt is set in Common agent **CAMIS0** register - 1'b1: An interrupt is set in Common agent **CAMIS0** register
2	CAEISIM1	R-U	0H	CAEIS1 Interrupt Mirroring Values: - 1'b0: No interrupt is set in Common agent **CAEIS1** register - 1'b1: An interrupt is set in Common agent **CAEIS1** register
1	CAEISIM0	R-U	0H	CAEIS0 Interrupt Mirroring Values: - 1'b0: No interrupt is set in Common agent **CAEIS0** register - 1'b1: An interrupt is set in Common agent **CAEIS0** register
0	RSSISIM	R-U	0H	RSSIS Interrupt Mirroring Values: - 1'b0: No interrupt is set in Common agent **RSSIS** register - 1'b1: An interrupt is set in Common agent **RSSIS** register

(5) TGIMt (t=0..RACE_PORT_GWCA_N-1)

TOP module GWCA Interrupt Mirroring t

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV								GWEISIM5	GWEISIM4	GWEISIM3	GWEISIM2	GWEISIM1	GWEISIM0	GWTSDISIM	GWDISIM

Bits	Bit name	RW-P	Initial value	Function description
31:8	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
7	GWEISIM5	R-U	0H	GWEIS5 Interrupt Mirroring Values: - 1'b0: No interrupt is set in GWCAt **GWEIS5** register - 1'b1: An interrupt is set in GWCAt **GWEIS5** register
6	GWEISIM4	R-U	0H	GWEIS4 Interrupt Mirroring Values: - 1'b0: No interrupt is set in GWCAt **GWEIS4** register - 1'b1: An interrupt is set in GWCAt **GWEIS4** register
5	GWEISIM3	R-U	0H	GWEIS3 Interrupt Mirroring Values: - 1'b0: No interrupt is set in GWCAt **GWEIS3** register - 1'b1: An interrupt is set in GWCAt **GWEIS3** register
4	GWEISIM2	R-U	0H	GWEIS2 Interrupt Mirroring Values: - 1'b0: No interrupt is set in GWCAt **GWEIS2** register - 1'b1: An interrupt is set in GWCAt **GWEIS2** register
3	GWEISIM1	R-U	0H	GWEIS1 Interrupt Mirroring Values: - 1'b0: No interrupt is set in GWCAt **GWEIS1** register - 1'b1: An interrupt is set in GWCAt **GWEIS1** register
2	GWEISIM0	R-U	0H	GWEIS0 Interrupt Mirroring Values: - 1'b0: No interrupt is set in GWCAt **GWEIS0** register - 1'b1: An interrupt is set in GWCAt **GWEIS0** register
1	GWTSDISIM	R-U	0H	GWTSDIS Interrupt Mirroring Values: - 1'b0: No interrupt is set in GWCAt **GWTSDIS** register - 1'b1: An interrupt is set in GWCAt **GWTSDIS** register
0	GWDISIM	R-U	0H	GWDIS Interrupt Mirroring Values: - 1'b0: No interrupt is set in GWCAt **GWDIS** register - 1'b1: An interrupt is set in GWCAt **GWDIS** register

(6) TEIMt (t=0..RACE_PORT_TSNA_N-1)

TOP module ETHA Interrupt Mirroring t

B31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV		MSPNEISIM	MSPNTISIM	MSAESEISIM3	MSAESEISIM2	MSAESEISIM1	MSAESEISIM0	MSEISIM2	MSEISIM1	MSEISIM0	MMISIM	MEISIM	EAEISIM2	EAEISIM1	EAEISIM0

Bits	Bit name	RW-P	Initial value	Function description
31:14	RSV	R0-U	0H	Reserved area. On read, 0 will be returned.
13	MSPNEISIM	R-U	0H	MSPNEIS Interrupt Mirroring Values: - 1'b0: No interrupt is set in ETHAt MSEC **MSPNEIS** register - 1'b1: An interrupt is set in ETHAt MSEC **MSPNEIS** register This register exist only t = 0-7.
12	MSPNTISIM	R-U	0H	MSPNTIS Interrupt Mirroring Values: - 1'b0: No interrupt is set in ETHAt MSEC **MSPNTIS** register - 1'b1: An interrupt is set in ETHAt MSEC **MSPNTIS** register This register exist only t = 0-7.
11	MSAESEISIM3	R-U	0H	MSAESEIS3 Interrupt Mirroring Values: - 1'b0: No interrupt is set in ETHAt MSEC **MSAESEIS3** register - 1'b1: An interrupt is set in ETHAt MSEC **MSAESEIS3** register This register exist only t = 0-7.
10	MSAESEISIM2	R-U	0H	MSAESEIS2 Interrupt Mirroring Values: - 1'b0: No interrupt is set in ETHAt MSEC **MSAESEIS2** register - 1'b1: An interrupt is set in ETHAt MSEC **MSAESEIS2** register This register exist only t = 0-7.
9	MSAESEISIM1	R-U	0H	MSAESEIS1 Interrupt Mirroring Values: - 1'b0: No interrupt is set in ETHAt MSEC **MSAESEIS1** register - 1'b1: An interrupt is set in ETHAt MSEC **MSAESEIS1** register This register exist only t = 0-7.
8	MSAESEISIM0	R-U	0H	MSAESEIS0 Interrupt Mirroring Values: - 1'b0: No interrupt is set in ETHAt MSEC **MSAESEIS0** register - 1'b1: An interrupt is set in ETHAt MSEC **MSAESEIS0** register This register exist only t = 0-7.
7	MSEISIM2	R-U	0H	MSEIS2 Interrupt Mirroring Values: - 1'b0: No interrupt is set in ETHAt MSEC **MSEIS2** register - 1'b1: An interrupt is set in ETHAt MSEC **MSEIS2** register This register exist only t = 0-7.

6	MSEISIM1	R-U	0H	MSEIS1 Interrupt Mirroring Values: - 1'b0: No interrupt is set in ETHAt MSEC **MSEIS1** register - 1'b1: An interrupt is set in ETHAt MSEC **MSEIS1** register This register exist only t = 0-7.
5	MSEISIM0	R-U	0H	MSEIS0 Interrupt Mirroring Values: - 1'b0: No interrupt is set in ETHAt MSEC **MSEIS0** register - 1'b1: An interrupt is set in ETHAt MSEC **MSEIS0** register This register exist only t = 0-7.
4	MMISIM	R-U	0H	MMIS0 Interrupt Mirroring Values: - 1'b0: No interrupt is set in ETHAt RMAC **MMIS0** register - 1'b1: An interrupt is set in ETHAt RMAC **MMIS0** register
3	MEISIM	R-U	0H	MEIS Interrupt Mirroring Values: - 1'b0: No interrupt is set in ETHAt RMAC **MEIS** register - 1'b1: An interrupt is set in ETHAt RMAC **MEIS** register
2	EAEISIM2	R-U	0H	EAEIS2 Interrupt Mirroring Values: - 1'b0: No interrupt is set in ETHAt **EAEIS2** register - 1'b1: An interrupt is set in ETHAt **EAEIS2** register
1	EAEISIM1	R-U	0H	EAEIS1 Interrupt Mirroring Values: - 1'b0: No interrupt is set in ETHAt **EAEIS1** register - 1'b1: An interrupt is set in ETHAt **EAEIS1** register
0	EAEISIM0	R-U	0H	EAEIS0 Interrupt Mirroring Values: - 1'b0: No interrupt is set in ETHAt **EAEIS0** register - 1'b1: An interrupt is set in ETHAt **EAEIS0** register

5. Register utilization

5.1 Software flows

Restrictions:

SW: Please follow to the flow in this section.

5.1.1 Software flow legend

Software flow legend is described in Fig 5.1.

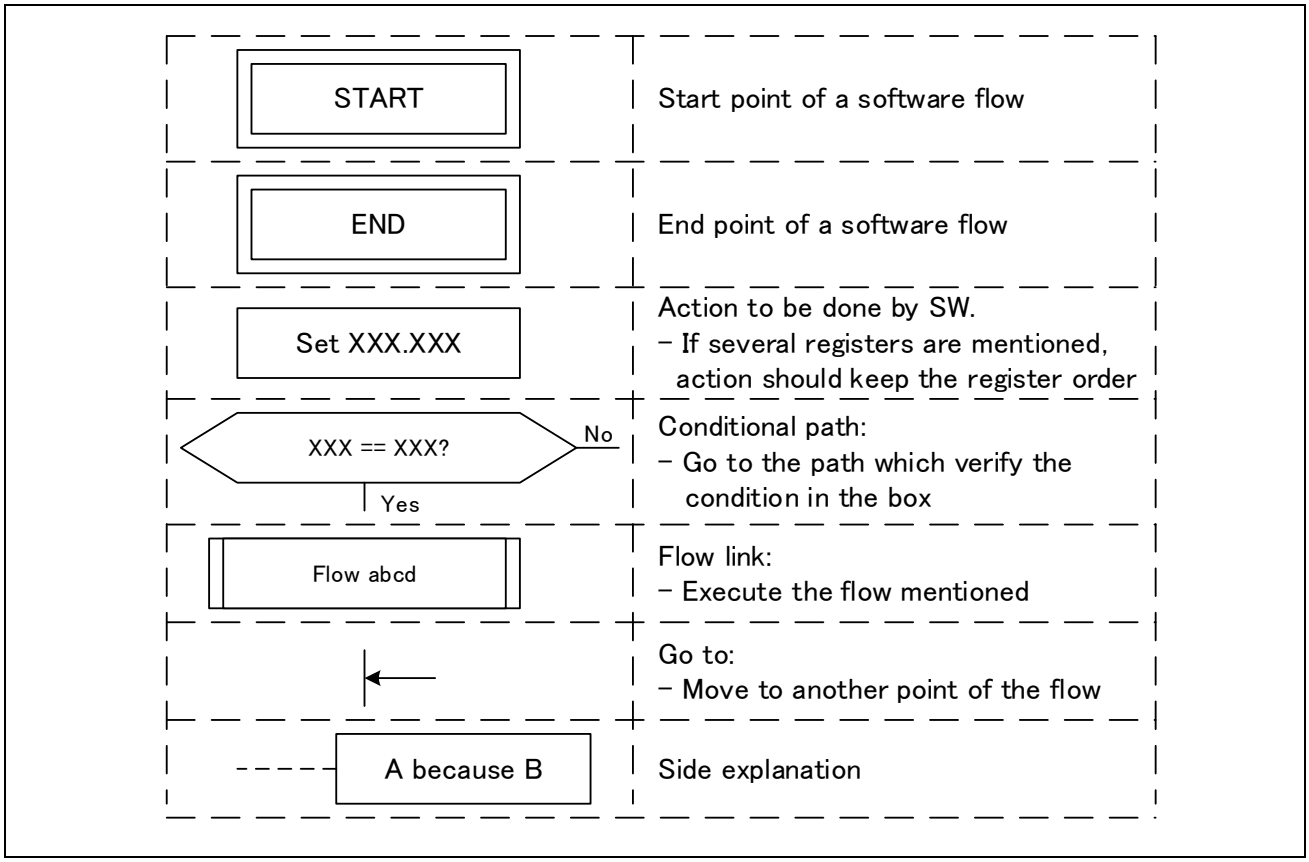


Fig 5.1: Software flow legend

5.1.2 Switch initialization flow

Switch initialization flow is described in Fig 5.2.

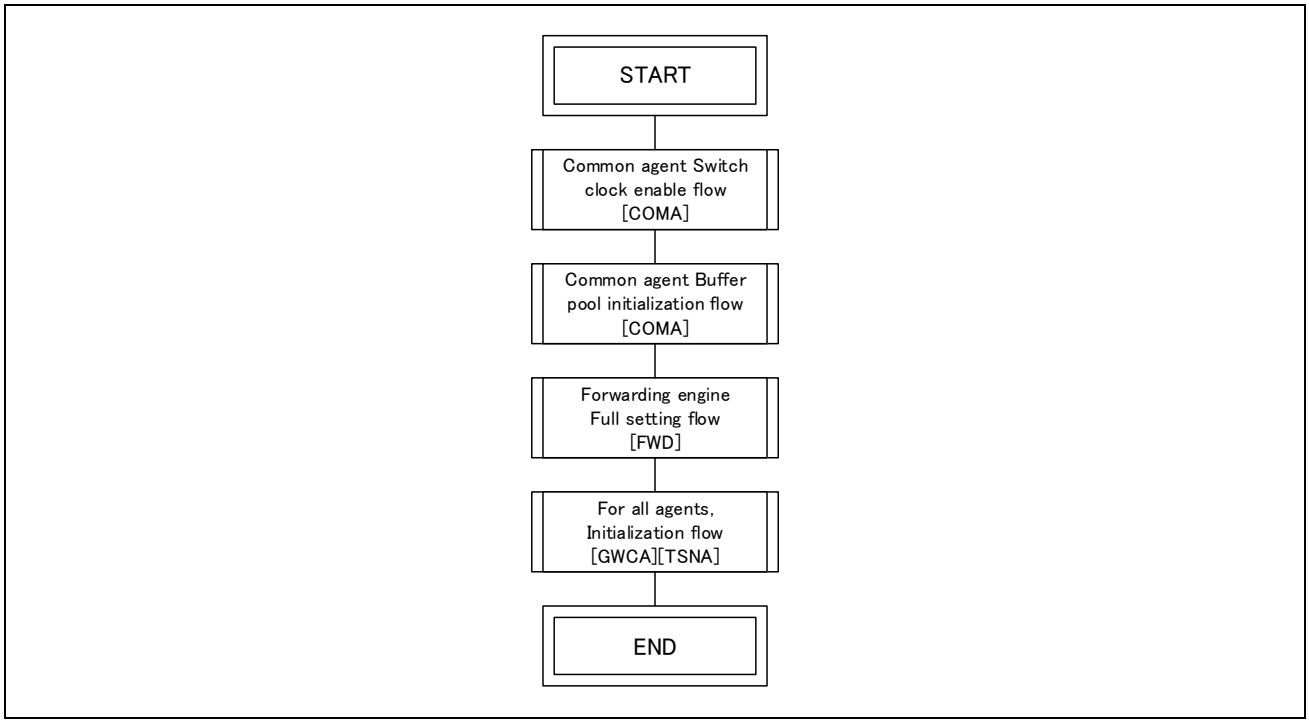


Fig 5.2: Switch initialization flow

5.1.3 Switch disable flow

Switch reset flow is described in Fig 5.3.

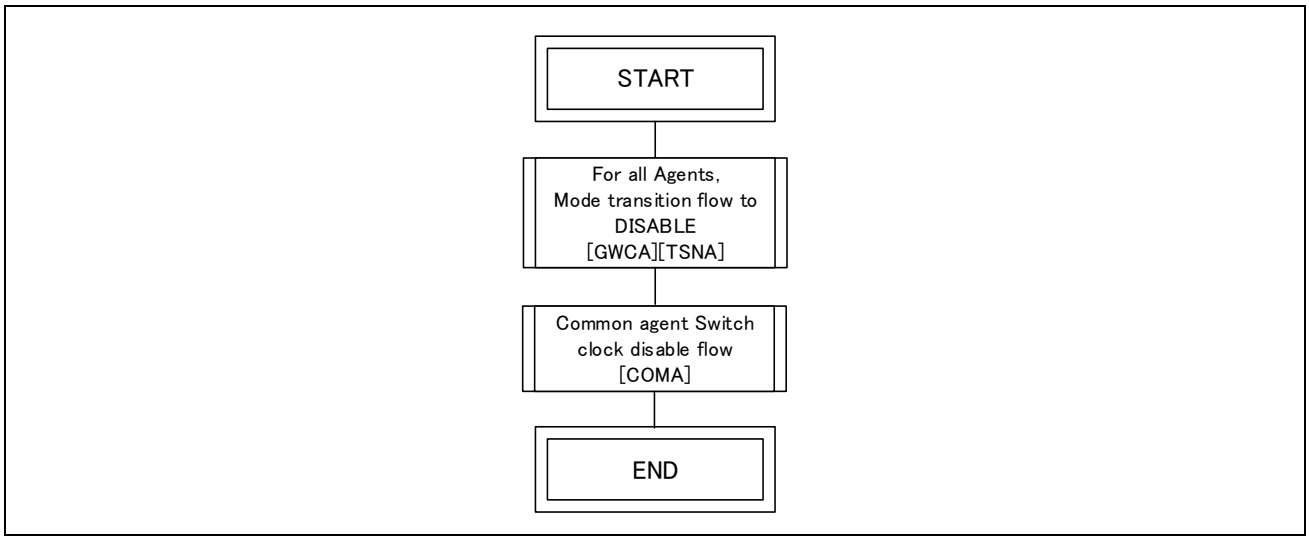


Fig 5.3: Switch disable flow

5.1.4 Switch reset flow

Switch reset flow is described in Fig 5.4.

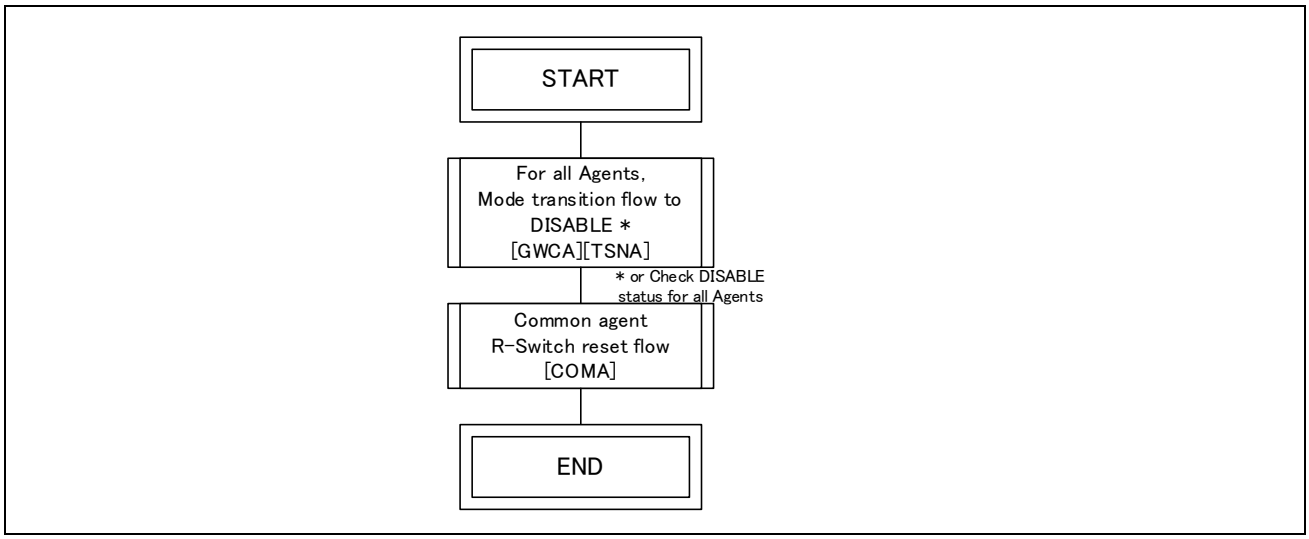


Fig 5.4: Switch reset flow

5.1.5 Switch emergency reset flow

Switch emergency reset flow is described in Fig 5.5.

This is used when [TSNA] locked.

For example, in the case of MII, if an error occurs in the PHY and the MII PHY TX clock stops, the Switch cannot send data and cannot release the pointer (locked on [TSNA] Operation mode). The state disappears when the MII PHY TX clock is restarted, but use emergency reset if required.

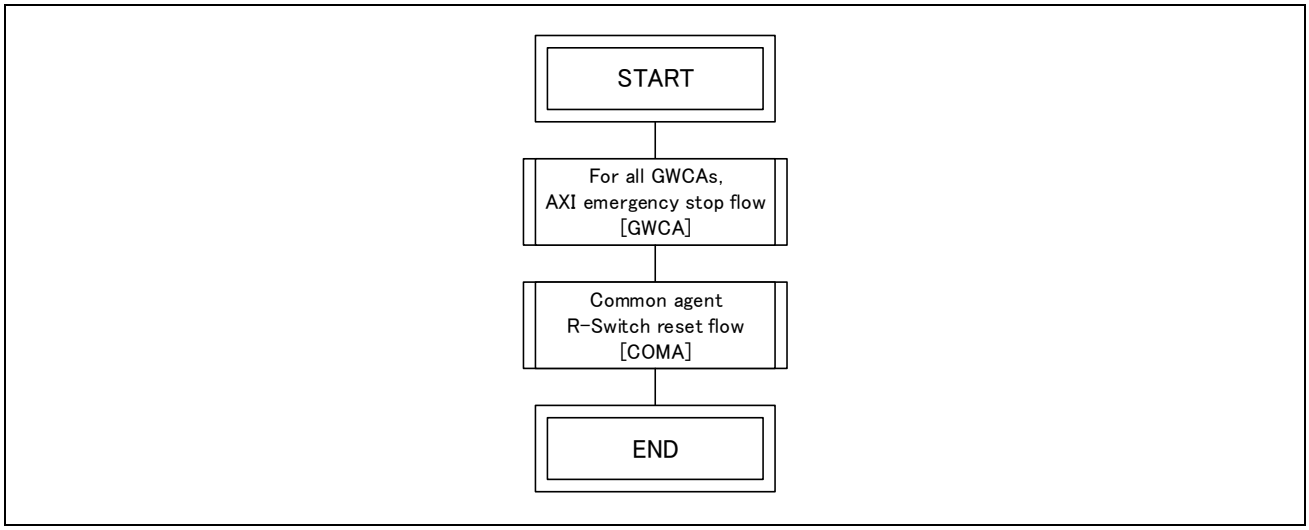


Fig 5.5: Switch emergency reset flow

5.1.6 Register writable without software flow

This section describes registers that have not been described so far. These registers can be changed dynamically. (However, it is necessary that the initial settings such as the clock enabling have been completed.)

6. Functional details

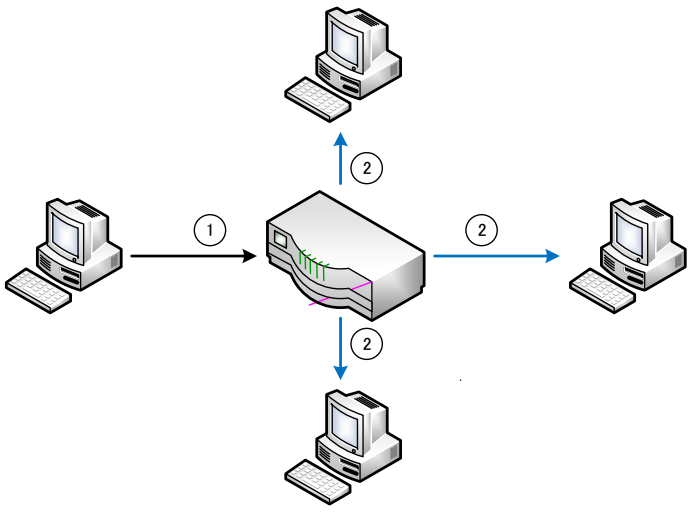
6.1 R-switch forwarding modes

6.1.1 Hub

6.1.1.1 Background

A Hub is an ethernet network interconnection system (OSI) which only works on Layer 1. It does not consider any kind of addressing and, consequently, is not aware of the kind of traffic which goes through it and can create security issues.

Hub operation is described in Fig 6.1.



1	The hub receives a packet from a port
2	The hub copies the packet to all ports except the ingress port

Fig 6.1: Hub operation

Notes:

- In hub mode, the internal port [GWCA] behaves like an ethernet port. In the following configuration, the internal port will receive all frames by AXI descriptor queue number 0 and transmit all frames by AXI descriptor queue number 1.

6.1.1.2 Settings

The setting required to set R-switch 3 in Hub mode are described in Table 6-1. This setting should be done by using the Switch initialization flow described in section 5.1.2. Any register not mentioned in the table should be kept to its initial value, so it does not need to be set. After using the Switch initialization flow, any used port should be moved to OPERATION mode when required.

Table 6-1 Hub settings

Register name	Setting value	Explanation
Forwarding engine [FWD]		
FWPBFC0i.DVi	All1 except for **FWPBFC0i.DVi[i]** which is set to 1'b0	All ports are set to send their incoming frames to all ports except themself
FWPBFC0i.PBSLi	All1	All ports are set to secure port for using.
Ethernet agent [TSNA]		
EAIRC	32'b0	All frames are directed to descriptor queue 0
EATDQDCq.DQDq	If q=0, set to DES_RAM_DP Else set to 0	There is no QoS, so all frames are stored in priority 0 queue. As a result, all the output descriptor queue memory is reserved for queue 0.
EAVCC.VEM	3'b011	Allows SC-Tagged frames and C-tagged frames to go through transparently.
EATTFC.UT	1'b0	Allows any TAG formats to go through even the unsupported ones.
RMAC [RMAC]		
MPIC.PIS	User defined	Set the PHY interface type
MPIC.LSC	User defined	Set the PHY speed
MRAFC	03C703C7H	Set MAC reception in promiscuous mode
GWCA [GWCA]		
GWIRC	32'b0	All frames are directed to descriptor queue 0
GWRDQDCq.DQDq	If q=0, set to DES_RAM_DP Else set to 0	There is no QoS, so all frames are stored in priority 0 queue. As a result, all the output descriptor queue memory is reserved for queue 0.
GWVCC.VEM	3'b011	Allows SC-Tagged frames and C-tagged frames to go through transparently.
GWTTFC.UT	1'b0	Allows any TAG formats to go through even the unsupported ones.
GWDCBAC0/1	User defined	Set the LINKFIX table base address
GWDCCi	For i = 1: - Set DQTi to 1'b1 - Set OSIDi to user defined. Else: - Set OSIDi to user defined.	Queue 0 is used for data reception and queue 1 is used for data transmission. All other queues are not used.

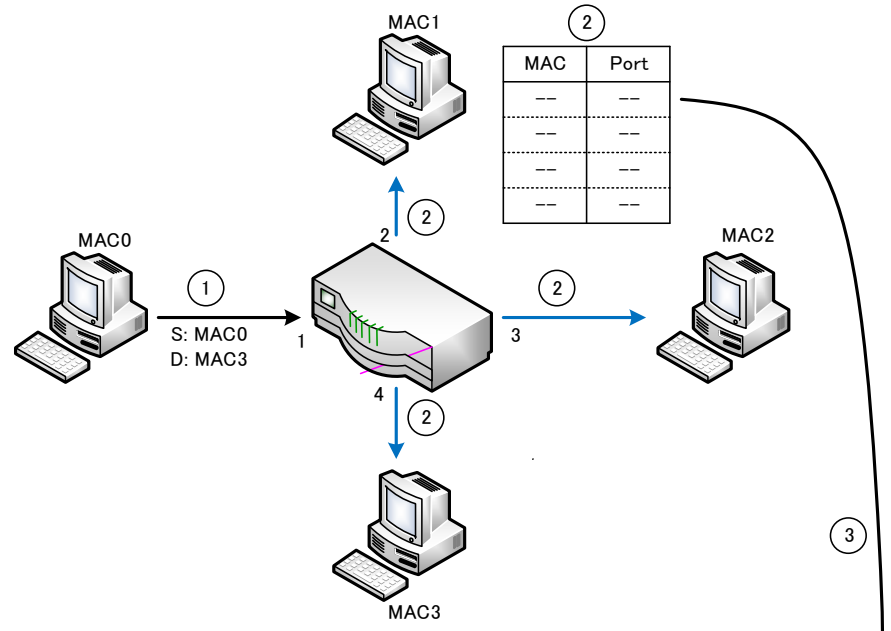
6.1.2 Layer 2 switch

6.1.2.1 Background

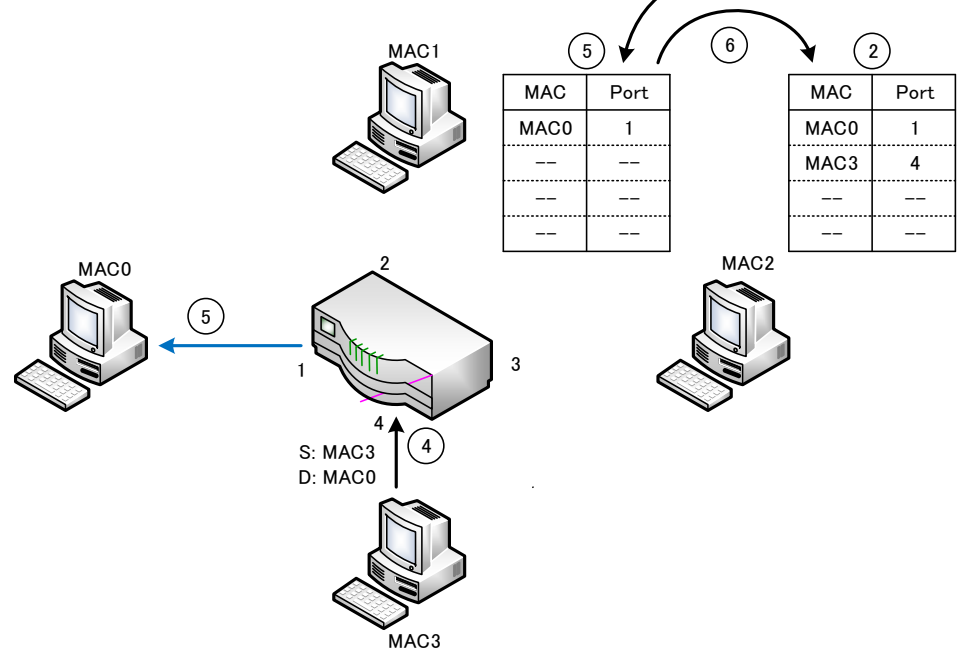
A Layer 2 switch is an ethernet network interconnection system (OSI) which only works on Layer 2 using MAC addresses. MAC addresses are used to filter and forward messages. A layer 2 switch has three main functions:

- Address learning: A switch can learn MAC addresses by looking at received frame source MAC addresses.
- Address aging: A switch can suppress a MAC address if a frame from the corresponding source has not been received since a given period (Usually 5 minutes).
- Frame forward/filter: A switch can decide to forward or filter a frame based on its destination MAC address.

Layer 2 switch operation is described in Fig 6.2.



1	The switch receives a packet from a port 1 with MAC0 as source MAC address and MAC3 as destination MAC address.
2	MAC3 is not present in the MAC table so the switch behaves like a Hub and copies the packet to all ports except the ingress port.
3	MAC0 is not present in the MAC table so it is learnt along with the frame source port.



4	The switch receives a packet from a port 4 with MAC3 as source MAC address and MAC0 as destination MAC address.
5	MAC0 is present in the MAC table along with port number 1 so the frame is only forwarded to port 1.
6	MAC3 is not present in the MAC table so it is learnt along with the frame source port.

Fig 6.2: Layer 2 switch operation

6.1.2.2 Settings

The setting required to set R-switch 3 in Layer 2 switch mode are described in Table 6-2. This setting should be done through using the Switch initialization flow described in section 5.1.2. Any register not mentioned in the table should be kept to its initial value, so it does not need to be set. After using the Switch initialization flow, any used port should be moved to OPERATION mode when required.

Table 6-2 Layer 2 switch settings

Register name	Setting value	Explanation
Forwarding engine [FWD]		
FWPBFC0i.DVi	All1 except for **FWPBFCi.DVi[i]** which is set to 1'b0	All ports are set to send their incoming frames to all ports except themself
FWPC0i.MACDSAi	1'b1	MAC destination search happens for all ports
FWPC0i.MACSAi	1'b1	MAC source search happens for all ports
FWPC0i.MACHLAi	1'b1	MAC source hardware learning is enabled for all ports
FWPC0i.MACHMAi	1'b1	MAC source hardware migration is enabled for all ports
FWCLPRC.USMACLF	User define	Unknown source MAC addresses can be sent to CPU for learning monitoring
FWCLPTC.LPCSD	2	Set the learning path queue number to 2
FWCLPTC.LPCS	User define	Select which CPU will be used for learning monitoring
FWMACTEC0.MACTUENC **FWMACHWLC***	User define	Set the dynamic entry upper limit with unsecure entry
Ethernet agent [TSNA]		
EAIRC	32'b0	All frames are directed to descriptor queue 0
EATDQDCq.DQDq	If q=0, set to DES_RAM_DP Else set to 0	There is no QoS, so all frames are stored in priority 0 queue. As a result, all the output descriptor queue memory is reserved for queue 0.
EAVCC.VEM	3'b011	Allows SC-Tagged frames and C-tagged frames to go through transparently.
EATTFC.UT	1'b0	Allows any TAG formats to go through even the unsupported ones.
RMAC [RMAC]		
MPIC.PIS	User defined	Set the PHY interface type
MPIC.LSC	User defined	Set the PHY speed
MRAFC	03C703C7H	Set MAC reception in promiscuous mode
GWCA [GWCA]		
GWIRC	32'b0	All frames are directed to descriptor queue 0
GWRDQDCq.DQDq	If q=0, set to DES_RAM_DP Else set to 0	There is no QoS, so all frames are stored in priority 0 queue. As a result, all the output descriptor queue memory is reserved for queue 0.
GWVCC.VEM	3'b011	Allows SC-Tagged frames and C-tagged frames to go through transparently.
GWTTFC.UT	1'b0	Allows any TAG formats to go through even the unsupported ones.
GWDCBAC0/1	User defined	Set the LINKFIX table base address

Register name	Setting value	Explanation
GWDCCi	For i = 1: - Set DQTi to 1'b1 - Set OSIDi to user defined. Else: - Set OSIDi to user defined.	Queue 0 is used for data reception, queue 1 is used for data transmission and queue 2 is used for learning monitoring. All other queues are not used. Notes: - For learning monitoring, extended descriptors should be used.

Notes:

- Any MAC address learnt by HW coming from an internal port [GWCA] will always be learnt along with AXI descriptor queue 0. As a result, AXI descriptor queue 0 should always be reserved for hardware learnt MAC addresses corresponding frames reception queue.

6.1.3 VLAN aware layer 2 switch

6.1.3.1 Background

A VLAN aware Layer 2 switch is an ethernet network interconnection system (OSI) which works on Layer 2 using MAC addresses and which can reduce its broadcast domains in sub-domains using VLAN IDs. A VLAN aware layer 2 switch has the same functions has a Layer 2 switch but is also able to handle VLANs.

VLAN aware layer 2 switch operation is described in Fig 6.2.

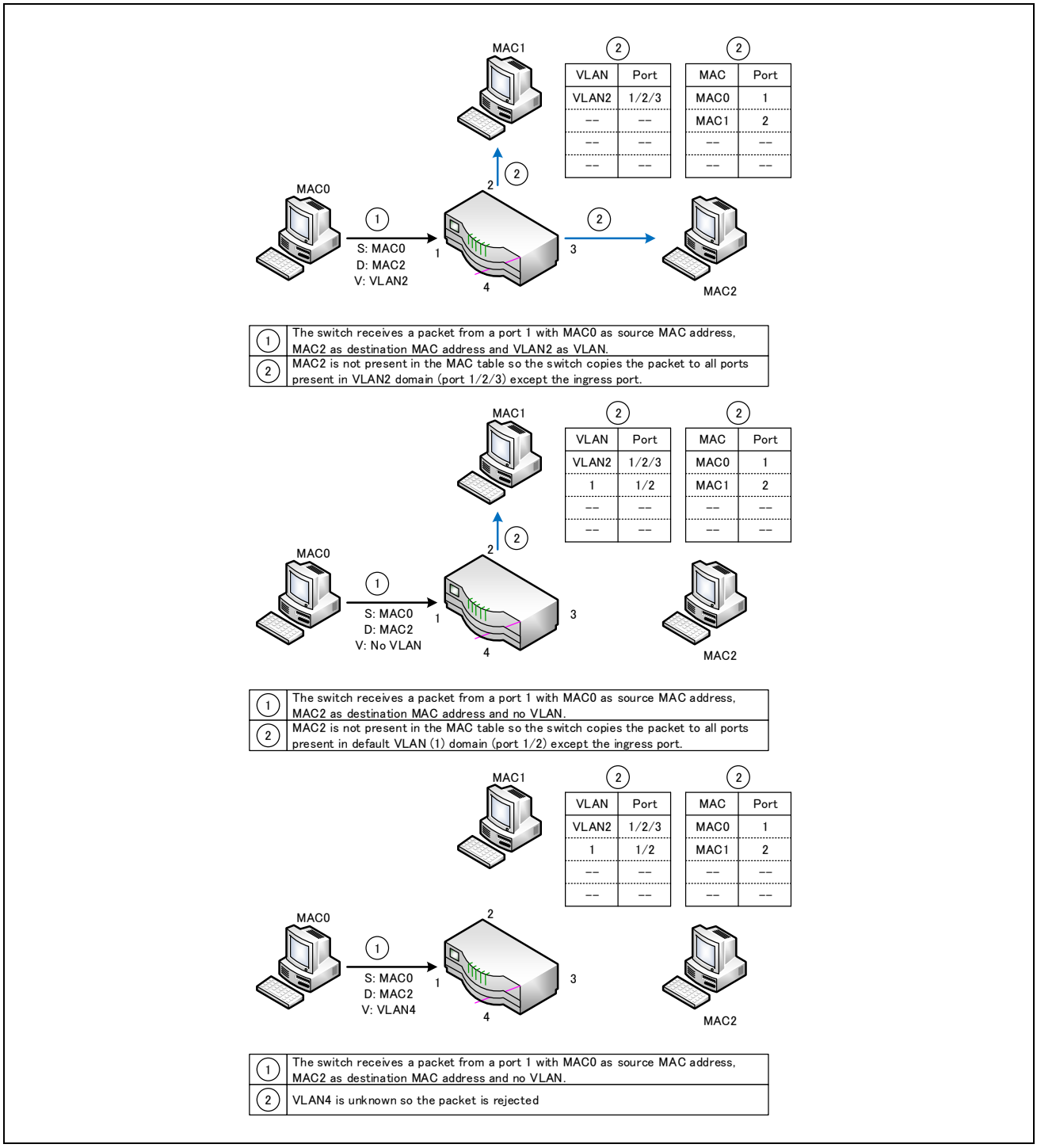


Fig 6.3: VLAN aware layer 2 switch operation

6.1.3.2 Settings

The setting required to set R-switch 3 in VLAN aware layer 2 switch mode are described in Table 6-3. This setting should be done through using the Switch initialization flow described in section 5.1.2. Any register not mentioned in the table should be kept to its initial value, so it does not need to be set. After using the Switch initialization flow, any used port should be moved to OPERATION mode when required.

Table 6-3 VLAN aware layer 2 switch settings

Register name	Setting value	Explanation
Forwarding engine [FWD]		
FWGC.SVM	2'b01	Set Rswitch in C-TAG mode
FWPBFC0i.DVi	All1 except for **FWPBFCi.DVi[i]** which is set to 1'b0	All ports are set to send their incoming frames to all ports except themself
FWPC0i.MACDSAi	1'b1	MAC destination search happens for all ports
FWPC0i.MACSAi	1'b1	MAC source search happens for all ports
FWPC0i.MACHLAi	1'b1	MAC source hardware learning is enabled for all ports
FWPC0i.MACHMAi	1'b1	MAC source hardware migration is enabled for all ports
FWPC0i.VLANSAi	1'b1	VLAN search happens for all ports
FWPC0i.VLANRUi	1'b1	Unknown VLANs are rejected.
FWCLPRC.USMACLF	User define	Unknown source MAC addresses can be sent to CPU for learning monitoring
FWCLPRC.UVLANLF	User define	Unknown VLANs can be sent to CPU for learning
FWCLPTC.LPCSD	2	Set the learning path queue number to 2
FWCLPTC.LPCS	User define	Select which CPU will be used for learning monitoring
FWVLANTL0-7	User define	New VLANs can be added to the VLAN table For details, refer to Table 6-4
Ethernet agent [TSNA]		
EATDQDCq.DQDq	User defines	The number of descriptors in descriptor queues can be set
EAVCC.VEM	3'b011	Allows SC-Tagged frames and C-tagged frames to go through transparently.
EAVTC.CTV	12'b1	Set the default VLAN value to 1
EATTFC.UT	1'b0	Allows any TAG formats to go through even the unsupported ones.
RMAC [RMAC]		
MPIC.PIS	User defined	Set the PHY interface type
MPIC.LSC	User defined	Set the PHY speed
MRAFC	03C703C7H	Set MAC reception in promiscuous mode
GWCA [GWCA]		
GWRDQDCq.DQDq	User defines	The number of descriptors in descriptor queues can be set
GWVCC.VEM	3'b011	Allows SC-Tagged frames and C-tagged frames to go through transparently.
GWVTC.CTV	12'b1	Set the default VLAN value to 1
GWTTFC.UT	1'b0	Allows any TAG formats to go through even the unsupported ones.
GWDCBAC0/1	User defined	Set the LINKFIX table base address

Register name	Setting value	Explanation
GWDCCi	For i = 1: - Set DQTi to 1'b1 - Set OSIDi to user defined. Else: - Set OSIDi to user defined.	Queue 0 is used for data reception, queue 1 is used for data transmission and queue 2 is used for learning monitoring. All other queues are not used. Notes: - For learning monitoring, extended descriptors should be used.

Table 6-4 VLAN learning in VLAN table

Field name VLAN.	Setting value	Explanation
SL	1'b0	No secure entry used
HLD	1'b0	Hardware learning for MAC addresses not disabled for any VLAN
SLV	Set to 1'b1 for ports included in VLAN	Only authorize to receive corresponding VLAN from ports included in this VLAN
DV	Set to 1'b1 for ports included in VLAN	Only authorize to send corresponding VLAN to ports included in this VLAN
CSD	0	Frames received by CPUs on sub-destination 0
CME	1'b0	No mirroring
EME	1'b0	No mirroring
IPU	1'b0	No frame priority update
IPV	3'b0	No frame priority update

Notes:

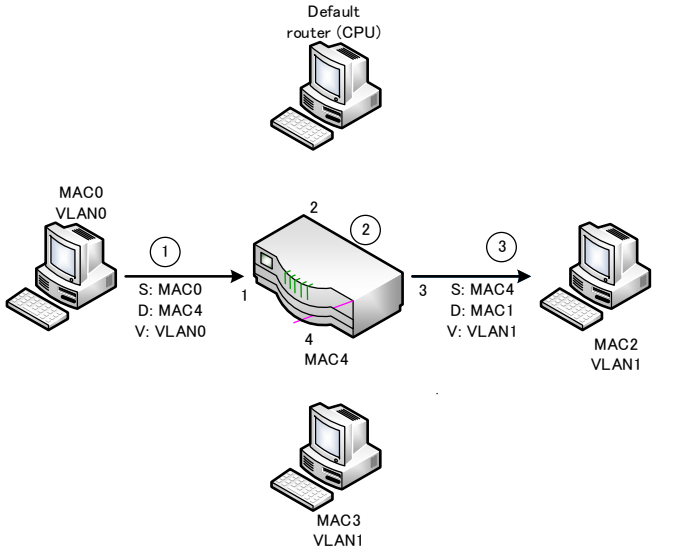
- When both VLAN and destination MAC addresses are found in forwarding tables and corresponding frame is forwarded to an internal port, the AXI descriptor queue (CPU sub-destination) chosen for forwarding is the one set in the MAC table. In this example, because both are set to 0, it raises no issue but, when AXI descriptor queue are used for virtualization it should be taken in account during system design.

6.1.4 L3 switch

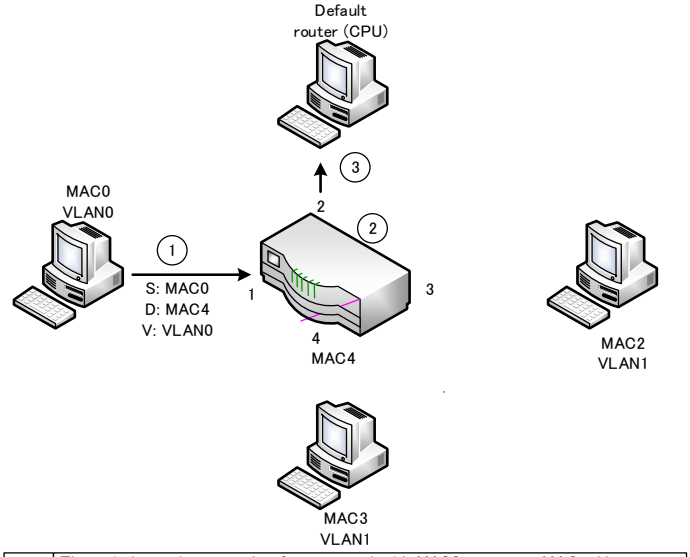
6.1.4.1 Background

A Layer 3 switch is an ethernet network interconnection system (OSI) which works on Layer 3 using IP addresses. Because R-switch 3 is only able to perform perfect matches by Stream forwarding, when developing a Layer3 switch, it is recommended to use perfect filters [FWD].

Layer 3 switch operation is described in Fig 6.2.



1	The switch receives a packet from a port 1 with MAC0 as source MAC address, MAC4 as destination MAC address and VLAN0 as VLAN.
2	The packet IP address matches the cascade filter and is should be routed to port 3.
3	The switch updates MAC destination to MAC1, MAC source to MAC4 and VLAN to VLAN1 and send the frame to port 3.



1	The switch receives a packet from a port 1 with MAC0 as source MAC address, MAC4 as destination MAC address and VLAN0 as VLAN.
2	The packet IP address is unknown so routing cannot happen.
3	The switch forwards the frame to the default router (CPU) without update for routing.

Fig 6.4: Layer 3 switch operation

6.1.4.2 Settings

The setting required to set R-switch 3 in Layer 3 switch mode are described in Table 6-3. This setting should be done through using the Switch initialization flow described in section 5.1.2. Any register not mentioned in the table should be kept to its initial value, so it does not need to be set. After using the Switch initialization flow, any used port should be moved to OPERATION mode when required.

Table 6-5 Layer 3 switch settings

Register name	Setting value	Explanation
Forwarding engine [FWD]		
FWGC.SVM	2'b01	Set Rswitch in C-TAG mode
FWPBFC0i.DVi	All1 except for FWPBFCi.Dvi[i] which is set to 1'b0	All ports are set to send their incoming frames to all ports except themselves
FWPC0i.MACDSAi	1'b1	MAC destination search happens for all ports
FWPC0i.MACSAi	1'b1	MAC source search happens for all ports
FWPC0i.MACHLAi	1'b1	MAC source hardware learning is enabled for all ports
FWPC0i.MACHMAi	1'b1	MAC source hardware migration is enabled for all ports
FWPC0i.VLANSAi	1'b1	VLAN search happens for all ports
FWCLPRC.USMACLF	User define	Unknown source MAC addresses can be sent to CPU for learning monitoring
FWCLPRC.UVLANLF	1'b1	Unknown VLANs are sent to CPU for learning
FWCLPTC.LPCSD	2	Set the learning path queue number to 2
FWCLPTC.LPCS	User define	Select which CPU will be used for learning monitoring
FWVLANTL0-7	User define	New VLANs can be added to the VLAN table For details, refer to Table 6-4
Ethernet agent [TSNA]		
EATDQDCq.DQDq	User defines	The number of descriptors in descriptor queues can be set
EAVCC.VEM	3'b011	Allows SC-Tagged frames and C-tagged frames to go through transparently.
EAVTC.CTV	12'b1	Set the default VLAN value to 1
EATTFC.UT	1'b0	Allows any TAG formats to go through even the unsupported ones.
RMAC [RMAC]		
MPIC.PIS	User defined	Set the PHY interface type
MPIC.LSC	User defined	Set the PHY speed
MRAFC	03C703C7H	Set MAC reception in promiscuous mode
GWCA [GWCA]		
GWRDQDCq.DQDq	User defines	The number of descriptors in descriptor queues can be set
GWVCC.VEM	3'b011	Allows SC-Tagged frames and C-tagged frames to go through transparently.
GWVTC.CTV	12'b1	Set the default VLAN value to 1
GWTTFC.UT	1'b0	Allows any TAG formats to go through even the unsupported ones.
GWDCBAC0/1	User defined	Set the LINKFIX table base address

Register name	Setting value	Explanation
GWDCCi	For i = 1: - Set DQTi to 1'b1 - Set OSIDi to user defined. Else: - Set OSIDi to user defined.	Queue 0 is used for data reception, queue 1 is used for data transmission and queue 2 is used for learning monitoring. All other queues are not used. Notes: - For learning monitoring, extended descriptors should be used.

Table 6-6 VLAN learning in VLAN table

Field name VLAN.	Setting value	Explanation
SL	1'b0	No secure entry used
HLD	1'b0	Hardware learning for MAC addresses not disabled for any VLAN
SLV	Set to 1'b1 for ports included in VLAN	Only authorize to receive corresponding VLAN from ports included in this VLAN
DV	Set to 1'b1 for ports included in VLAN	Only authorize to send corresponding VLAN to ports included in this VLAN
CSD	0	Frames received by CPUs on sub-destination 0
CME	1'b0	No mirroring
EME	1'b0	No mirroring
IPU	1'b0	No frame priority update
IPV	3'b0	No frame priority update

7. Precautions

7.1 Precautions

- R-Switch can support min [64 bytes] frame size (Example : DMAC 6 bytes + SMAC 6 bytes + EtherType 2 bytes + Payload 46 bytes + FCS 4 bytes).
- R-Switch can support max [“63488 bytes” or “(([Unused pointer number]*128) / RACE_PORT_N) bytes”] frame (supported maximum frame size). if try to transmit frames of size more than that, then Buffer overflow will happen. [Unused pointer number] = RACE_LCL_PTR_N – (Activated port number * 6).
  - Set to [RMAC] MRFSCE.EMXS or MRFSCP.PMXS smaller than maximum frame size for Ethernet ports.
  - Don’t transmit bigger than maximum frame size for CPU ports.
- When using Cut through, use it so as not to cause a buffer overflow. The following usage is recommended.
  - Only use from-one-to-one communication.
    (Example of prohibition : Multicast forwarding, To Ethernet Mirroring, Loopback forwarding)
  - Prohibition of the function to stop transmission. Please flow control on reception port.
    (Example of prohibition : TX queue pause, TAS)

7.2 Restrictions (Including known problems)

- "Do not select RSW3_PPS function before power on RSW3 domain" The debug test terminals (as PPS and GATE) will not work at "pseudo power off". (Outputs indefinite X.)

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