

CPE DDR Configuration

Application Note

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Chapter 1: DDR Configuration

1.1 Introduction

This document describes how to set up DDR parameters via an NVRAM.

DDR configuration parameters (size, clock, speed grade, memory chip data width, and so on) are stored in the NVRAM. The DDR configuration is a 32-bit board parameter ID, `bp_ulMemoryConfig` in the *boardparms.c* file for a particular board ID and is saved in NVRAM.

When a new board first boots up, the CFE ROM uses default safe mode DDR configuration to initialize the DDR and run CFE RAM. The CFE RAM then saves the configuration to NVRAM. The CFE RAM always compares the DDR configuration from the value set in *boardparms.c* to the NVRAM configuration. If they are different, it updates to the NVRAM configuration and reboots automatically. This allows the DDR configuration to be updated on a board automatically if a new software release changes the DDR configuration.

1.2 Supported Broadcom Devices

This document applies to all Broadcom devices that support NVRAM DDR configuration, the following is not an exhaustive list:

- BCM63138
- BCM63148
- BCM63158
- BCM62118
- BCM6858X
- BCM68360
- BCM68460
- BCM68560
- BCM4908

In some devices, the DDR configuration can be set by bootstraps. For more information regarding these devices, see the [DDR Strap Configuration](#) section.

1.3 Preventing Automatic DDR Config Update

To prevent the automatic update when setting the NVRAM configuration, set bit #31 (see [Changing DDR Configuration](#)). When CFE starts, and just before DDR Shmoo is running, the CFE prints out the current DDR configuration in NVRAM:

```
...
MAIN
DRAM
NVRAM memcMCB chksum 0xf51e43ef
DDR3-1600 CL11 128MBx2
...
```

The DDR configuration board parameter is defined in the following format in boardparms.c:

```
{bp_ulMemoryConfig, .u.ul = BP_DDR_SPEED_533_8_8_8 | BP_DDR_TOTAL_SIZE_128MB|
BP_DDR_DEVICE_WIDTH_16},
```

This means single x16 DDR chip of total size 128 MB running at DDR3 1066 data rate with CAS latency = 8.

```
{bp_ulMemoryConfig, .u.ul = BP_DDR_SPEED_1067_14_14_14 | BP_DDR_TOTAL_SIZE_1024MB|
BP_DDR_DEVICE_WIDTH_16 | BP_DDR_TOTAL_WIDTH_32BIT},
```

This means two x16 DDR chips of 512 MB each running at DDR3 2133 data rate with CAS latency = 14

NOTE: For production, it is required to store the DDR configuration data in the NVRAM, so DDR initialization in the first boot will be as required and not in safe mode.

1.4 DDR Settings Word Bit Mask

The complete parameter definitions of the word written to NVRAM are listed below (taken from boardparms.h):

```
#define BP_DDR_SPEED_MASK 0x1f
#define BP_DDR_SPEED_SHIFT 0
#define BP_DDR_SPEED_SAFE 0
#define BP_DDR_SPEED_400_6_6_6 1
#define BP_DDR_SPEED_533_7_7_7 2
#define BP_DDR_SPEED_533_8_8_8 3
#define BP_DDR_SPEED_667_9_9_9 4
#define BP_DDR_SPEED_667_10_10_10 5
#define BP_DDR_SPEED_800_10_10_10 6
#define BP_DDR_SPEED_800_11_11_11 7
#define BP_DDR_SPEED_1067_11_11_11 8
#define BP_DDR_SPEED_1067_12_12_12 9
#define BP_DDR_SPEED_1067_13_13_13 10
#define BP_DDR_SPEED_1067_14_14_14 11
#define BP_DDR_SPEED_933_10_10_10 12
#define BP_DDR_SPEED_933_11_11_11 13
#define BP_DDR_SPEED_933_12_12_12 14
#define BP_DDR_SPEED_933_13_13_13 15
#define BP_DDR_SPEED_CUSTOM_1 27
#define BP_DDR_SPEED_CUSTOM_2 28
#define BP_DDR_SPEED_CUSTOM_3 29
#define BP_DDR_SPEED_CUSTOM_4 30

#define BP_DDR_DEVICE_WIDTH_MASK 0xe0
#define BP_DDR_DEVICE_WIDTH_SHIFT 5
```

```

#define BP_DDR_DEVICE_WIDTH_8      (0 << BP_DDR_DEVICE_WIDTH_SHIFT)
#define BP_DDR_DEVICE_WIDTH_16    (1 << BP_DDR_DEVICE_WIDTH_SHIFT)
#define BP_DDR_DEVICE_WIDTH_32    (2 << BP_DDR_DEVICE_WIDTH_SHIFT)

#define BP_DDR_TOTAL_SIZE_MASK     0xf00
#define BP_DDR_TOTAL_SIZE_SHIFT    8
#define BP_DDR_TOTAL_SIZE_64MB    (1 << BP_DDR_TOTAL_SIZE_SHIFT)
#define BP_DDR_TOTAL_SIZE_128MB   (2 << BP_DDR_TOTAL_SIZE_SHIFT)
#define BP_DDR_TOTAL_SIZE_256MB   (3 << BP_DDR_TOTAL_SIZE_SHIFT)
#define BP_DDR_TOTAL_SIZE_512MB   (4 << BP_DDR_TOTAL_SIZE_SHIFT)
#define BP_DDR_TOTAL_SIZE_1024MB  (5 << BP_DDR_TOTAL_SIZE_SHIFT)
#define BP_DDR_TOTAL_SIZE_2048MB  (6 << BP_DDR_TOTAL_SIZE_SHIFT)
#define BP_DDR_TOTAL_SIZE_4096MB  (7 << BP_DDR_TOTAL_SIZE_SHIFT)

#define BP_DDR_SSC_CONFIG_MASK     0xf000
#define BP_DDR_SSC_CONFIG_SHIFT    12
#define BP_DDR_SSC_CONFIG_NONE    (0 << BP_DDR_SSC_CONFIG_SHIFT)
#define BP_DDR_SSC_CONFIG_1       (1 << BP_DDR_SSC_CONFIG_SHIFT) /*1% SSC*/
#define BP_DDR_SSC_CONFIG_2       (2 << BP_DDR_SSC_CONFIG_SHIFT) /*0.5% SSC*/
#define BP_DDR_SSC_CONFIG_CUSTOM  (3 << BP_DDR_SSC_CONFIG_SHIFT)

#define BP_DDR_TEMP_MASK           0x30000
#define BP_DDR_TEMP_SHIFT          16
#define BP_DDR_TEMP_NORMAL        (0 << BP_DDR_TEMP_SHIFT) /* Self-Refresh for Normal
Temperature */
#define BP_DDR_TEMP_EXTENDED_SRT   (1 << BP_DDR_TEMP_SHIFT) /* Self-Refresh for Extended
Temperature */
#define BP_DDR_TEMP_EXTENDED_ASR   (2 << BP_DDR_TEMP_SHIFT) /* Auto Self-Refresh Enabled for
Normal and Extended Temperature */

#define BP_DDR_TOTAL_WIDTH_MASK    0xc0000
#define BP_DDR_TOTAL_WIDTH_SHIFT   18
#define BP_DDR_TOTAL_WIDTH_16BIT   (0 << BP_DDR_TOTAL_WIDTH_SHIFT)
#define BP_DDR_TOTAL_WIDTH_32BIT   (1 << BP_DDR_TOTAL_WIDTH_SHIFT)

#define BP_DDR_CONFIG_MASK         (~ (BP_DDR_CONFIG_DEBUG|BP_DDR_CONFIG_OVERRIDE))
#define BP_DDR_CONFIG_DEBUG        (1 << 30)
#define BP_DDR_CONFIG_OVERRIDE     (1 << 31)

```

1.5 Changing DDR Configuration

When using a different DDR chip than the chip specified in the Broadcom reference design, create a new board ID with the correct `bp_ulMemoryConfig` setting. Loading the new code will automatically update the DDR configuration in the NVRAM.

CFE also supports a “ddr” command to manually change the DDR configuration from the CFE prompt without making any software change:

```
CFE> ddr
DDR Config OVERRIDE           : 0x307 0x80000303
Config Changed... REBOOT NEEDED
*** command status = 0
CFE>
```

The command writes the new configuration to NVRAM. In the example above, 0x307 is the old DDR configuration in the NVRAM and CFE board parameters. This command changes the DDR clock from 800 MHz to 533 MHz. It is also necessary to set bit 31. This bit is the NVRAM configuration overwrite bit that tells the CFE to not compare its built-in board parameter configuration 0x307 against NVRAM setting 0x303 and to update NVRAM. This ensures that CFE always uses the value entered from the command line.

1.6 Early Key Abort and DDR Safe Mode

CFE-ROM can be aborted before DDR initialization, this enables the user to set DDR configuration in runtime. In order to abort CFE-ROM:

1. Power off the device.
2. Hold down the 'a' key.
3. Power on the device. The following message will appear:

```
CFE-ROM WAS ABORTED
Please choose one of the following options:
c - continue
s - DDR safe mode
i - followed by 0 to boot to a previous fs image
0 - followed by hex numbers to select MCB; CR/NL to continue
```

- a. Press 's' for safe mode:

If a board failed to boot due to a DDR memory problem, the CFE has an option to run in DDR safe mode and allow the board to boot for further debugging or fixing with a new DDR configuration. The DDR safe mode runs with conservative DDR parameters.

To keep the board in safe mode without this special key abort, run the DDR command in CFE console and set the DDR configuration to 0x80000000 and reset the board:

```
CFE> ddr
DDR Config OVERRIDE           : 0x223 0x80000000
Config Changed... REBOOT NEEDED
*** command status = 0
```

- b. For Runtime selection: press '0' and Hex number

The number is according to the [DDR Settings Word Bit Mask](#) section.

1.7 DDR Strap Configuration

For the following devices, the DDR settings can be configured through NVRAM, as described in this document, or by straps: BCM6858XX, BCM5504X, BCM49508

- To take DDR parameters from NVRAM, the signal STRAP_SOFTWARE2 (GPIO_45) must be set to 0 at boot up. In this case, all other DDR straps will be ignored.
- To take DDR parameters from the straps, the signal STRAP_SOFTWARE2 (GPIO_45) must be set to 1. In this case the DDR clock will be 1067 MHz (CAS latency=14), and the DDR density will be set according to the following table:

STRAP_SW_1 (GPIO_44)	STRAP_DDR_DENSITY (GPIO_42)	STRAP_DDR_16BIT_ENABLE	
		1: 16 bit DDR	0: 32 bit DDR
1	1	= 2Gb x 1 = 256 MB	= 2Gb x 2 = 512 MB
0	1	= 8Gb x 1 = 1 GB	= 8Gb x 2 = 2 GB

For any configuration not listed in the table above, settings must be taken from NVRAM.

Chapter 2: Supported DDR Configurations

Each configuration has a corresponding MCB that is used by the DDR library during the initialization. CFE currently supports a limited number of common configurations and MCB due to the image size limitation.

The supported configuration is defined in `cfe/cfe/arch/arm/board/bcm63xx_rom/src/bcm63xx_impl1/2_ddr_mcb.c`.

The following tables list the currently supported configurations for the various devices. For the latest updates, see the software release notes.

2.1 BCM63138/BCM63148 DDR Configurations

Table 1: BCM63138/BCM63148 DDR Configurations Supported

Configuration	Value
DDR3-1066 CL8 Total 128 MB one 16-bit part	0x223
DDR3-1600 CL11 Total 128 MB One 16-bit part	0x227
DDR3-1066 CL8 Total 256 MB One 16-bit part	0x323
DDR3-1066 CL8 Total 256 MB two 8-bit parts	0x303
DDR3-1600 CL11 Total 256 MB One 16-bit part	0x327
DDR3-1600 CL11 Total 256 MB Two 8-bit parts	0x307
DDR3-1600 CL11 Total 256 MB One 16-bit part 0.5% SSC	0x2327
DDR3-1600 CL11 Total 256 MB One 16-bit part HT SRT	0x10327
DDR3-1600 CL11 Total 256 MB One 16-bit part HT ASR	0x20327
DDR3-800 CL6 Total 512 MB One 16-bit part	0x421 (safe mode)
DDR3-1066 CL8 Total 512 MB One 16-bit part	0x423
DDR3-1066 CL8 Total 512 MB two 8-bit parts	0x403
DDR3-1600 CL11 Total 512 MB one 16-bit part	0x427
DDR3-1600 CL11 Total 512 MB two 8-bit parts	0x407
DDR3-1600 CL11 Total 512 MB one 16-bit part 0.5% SSC	0x2427
DDR3-1600 CL11 Total 512 MB two 8-bit parts 0.5% SSC	0x2407
DDR3-1600 CL11 Total 512 MB one 16-bit part HT SRT	0x10427
DDR3-1600 CL11 Total 512 MB one 16-bit part HT ASR	0x20427
DDR3-1066 CL8 Total 1024 MB two 8-bit parts	0x503
DDR3-1600 CL11 Total 1024 MB two 8-bit parts	0x507
DDR3-1600 CL11 Total 1024 MB two 8-bit parts 0.5% SSC	0x2507

2.2 BCM62118 DDR Configurations

Table 2: BCM62118 DDR Configurations Supported

Configuration	Value
DDR3-1066 CL8 Total 256MB One 16-bits part %1 SSC	0x1323
DDR3-1066 CL8 Total 256MB Two 16-bits parts %1 SSC	0x41323
DDR3-1600 CL8 Total 256MB One 16-bits part %1 SSC	0x1327
DDR3-1600 CL8 Total 256MB Two 16-bits parts %1 SSC	0x41327
DDR3-1066 CL8 Total 512 MB one 16-bit part 1% SSC	0x1423
DDR3-1066 CL8 Total 512 MB Two 16-bit parts 1% SSC	0x41423
DDR3-1600 CL11 Total 512 MB one 16-bit part 1% SSC	0x1427
DDR3-1600 CL11 Total 512 MB Two 16-bit parts 1% SSC	0x41427
DDR3-1066 CL8 Total 1024 MB one 16-bit part	0x523 (safe mode)
DDR3-1066 CL8 Total 1024 MB one 16-bit part 1% SSC	0x1523
DDR3-1066 CL8 Total 1024 MB two 16-bit parts 1% SSC	0x41523
DDR3-1600 CL11 Total 1024 MB one 16-bit part 1% SSC	0x1527
DDR3-1600 CL11 Total 1024 MB two 16-bit parts 1% SSC	0x41527
DDR3-1600 CL11 Total 1024 MB two 16-bit parts 1% SSC HT SRT	0x51527
DDR3-1600 CL11 Total 1024 MB two 16-bit parts 1% SSC HT ASR	0x61527
DDR3-1066 CL8 Total 2048 MB two 16-bit parts 1% SSC	0x41623
DDR3-1600 CL11 Total 2048 MB two 16-bit parts 1% SSC	0x41627

2.3 BCM6858X DDR Configurations

The DDR configurations shown in [Table 3](#) are also valid for the following devices:

- BCM68580X/XV
- BCM55040
- BCM55045
- BCM49508
- BCM62119

Table 3: BCM6858X DDR Configurations Supported

Configuration	Value
DDR3-1600 CL11 Total 1024 MB one 16-bit part 1% SSC	0x1527 (safe mode)
DDR3-2133 CL14 Total 256 MB one 16-bit part 1% SSC	0x132B
DDR3-2133 CL14 Total 512 MB one 16-bit part 1% SSC	0x142B
DDR3-2133 CL14 Total 1024 MB one 16-bit part 1% SSC	0x152B
DDR3-2133 CL14 Total 512 MB two 16-bit parts 1% SSC	0x4142B
DDR3-2133 CL14 Total 1024 MB two 16-bit parts 1% SSC	0x4152B
DDR3-2133 CL14 Total 2048 MB two 16-bit parts 1% SSC	0x4162B

NOTE: There are many available options for BCM6858X. Due to image size restriction, only part of them are enabled. All available configurations can be seen in *bcm63xx_impl2_ddr_mcb.c*. In order to enable a configuration *bcm63xx_impl2_ddr_mcb.c* should be modified:

1. The appropriate .h file should be uncommented.
2. An appropriate entry should be added to the MCB[] array.

2.4 BCM68460 DDR Configurations

Table 4: BCM6846 DDR Configurations Supported

Configuration	Value
DDR3-1600 CL11 Total 1024 MB one 16-bit part 1% SSC	0x1527 (safe mode)
DDR3-1600 CL11 Total 512 MB one 16-bit part 1% SSC	0x1427
DDR3-1600 CL11 Total 256 MB one 16-bit part 1% SSC	0x1327
DDR3-2133 CL14 Total 1024 MB one 16-bit part 1% SSC	0x1527

2.5 BCM68360 DDR Configurations

Table 5: BCM68360 B0 DDR Configurations Supported

Configuration	Value
DDR3-1600 CL11 Total 1024 MB one 16-bit part 1% SSC	0x1527 (safe mode)
DDR3-1600 CL11 Total 512 MB one 16-bit part 1% SSC	0x1427
DDR3-1600 CL11 Total 256 MB one 16-bit part 1% SSC	0x1327
DDR3-2133 CL14 Total 1024 MB one 16-bit part 1% SSC	0x152B
DDR3-2133 CL14 Total 512 MB one 16-bit part 1% SSC	0x142B
DDR3-2133 CL14 Total 256 MB one 16-bit part 1% SSC	0x152B

2.6 BCM68560 DDR Configurations

Table 6: BCM68560 DDR Configurations Supported

Configuration	Value
DDR3-1600 CL11 Total 1024 MB one 16-bit part 1% SSC	0x1527 (safe mode)
DDR3-1600 CL11 Total 512 MB one 16-bit part 1% SSC	0x1427
DDR3-1600 CL11 Total 256 MB one 16-bit part 1% SSC	0x1327
DDR3-2133 CL14 Total 1024 MB one 16-bit part 1% SSC	0x152B
DDR3-2133 CL14 Total 512 MB one 16-bit part 1% SSC	0x142B
DDR3-2133 CL14 Total 256 MB one 16-bit part 1% SSC	0x152B
DDR3-1600 CL11 Total 512 MB two 16-bit parts 1% SSC	0x41427
DDR3-1600 CL11 Total 1024 MB two 16-bit parts 1% SSC	0x41427
DDR3-2133 CL14 Total 512 MB two 16-bit parts 1% SSC	0x4142B
DDR3-2133 CL14 Total 1024 MB two 16-bit parts 1% SSC	0x4152B

2.7 BCM63158 DDR Configurations

Table 7: BCM63158 DDR Configurations Supported

Configuration	Value
DDR3-1066 CL8 Total 1024 MB one 16-bit part	0x523 (safe mode)
DDR3-1600 CL11 Total 512 MB one 16-bit part 1% SSC	0x1427
DDR3-1600 CL11 Total 1024 MB one 16-bit part 1% SSC	0x1527
DDR3-1600 CL11 Total 512 MB two 16-bit parts 1% SSC	0x41427
DDR3-1600 CL11 Total 2048 MB four 8-bit parts 1% SSC	0x41607
DDR3-1600 CL11 Total 1024 MB two 16-bit parts 1% SSC	0x41527
DDR3-1600 CL11 Total 4096 MB four 8-bit parts 1% SSC	0x41707
DDR3-1600 CL11 Total 2048 MB two 16-bit parts 1% SSC	0x41627
DDR3-1866 CL13 Total 512 MB one 16-bit part 1% SSC	0x142F
DDR3-1866 CL13 Total 1024 MB one 16-bit part 1% SSC	0x152F
DDR3-1866 CL13 Total 512 MB two 16-bit parts 1% SSC	0x4142F
DDR3-1866 CL13 Total 2048 MB four 8-bit parts 1% SSC	0x4160F
DDR3-1866 CL13 Total 1024 MB two 16-bit parts 1% SSC	0x4152F
DDR3-1866 CL13 Total 4096 MB four 8-bit parts 1% SSC	0x4170F
DDR3-1866 CL13 Total 2048 MB two 16-bit parts 1% SSC	0x4162F
DDR3-2133 CL14 Total 512 MB one 16-bit part 1% SSC	0x142B
DDR3-2133 CL14 Total 1024 MB one 16-bit part 1% SSC	0x152B
DDR3-2133 CL14 Total 512 MB two 16-bit parts 1% SSC	0x4142B
DDR3-2133 CL14 Total 2048 MB four 8-bit parts 1% SSC	0x4160B
DDR3-2133 CL14 Total 1024 MB two 16-bit parts 1% SSC	0x4152B
DDR3-2133 CL14 Total 4096 MB four 8-bit parts 1% SSC	0x4170B
DDR3-2133 CL14 Total 2048 MB two 16-bit parts 1% SSC	0x4162B
DDR3-2133 CL14 Total 1024 MB two 16-bit parts 1% SSC HT SRT	0x5152B
DDR3-2133 CL14 Total 1024 MB two 16-bit parts 1% SSC HT ASR	0x6152B

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