
STM32
CubeMX

1. Description

1.1. Project

Project Name	AI_on_STM32
Board Name	custom
Generated with:	STM32CubeMX 6.3.0
Date	11/22/2021

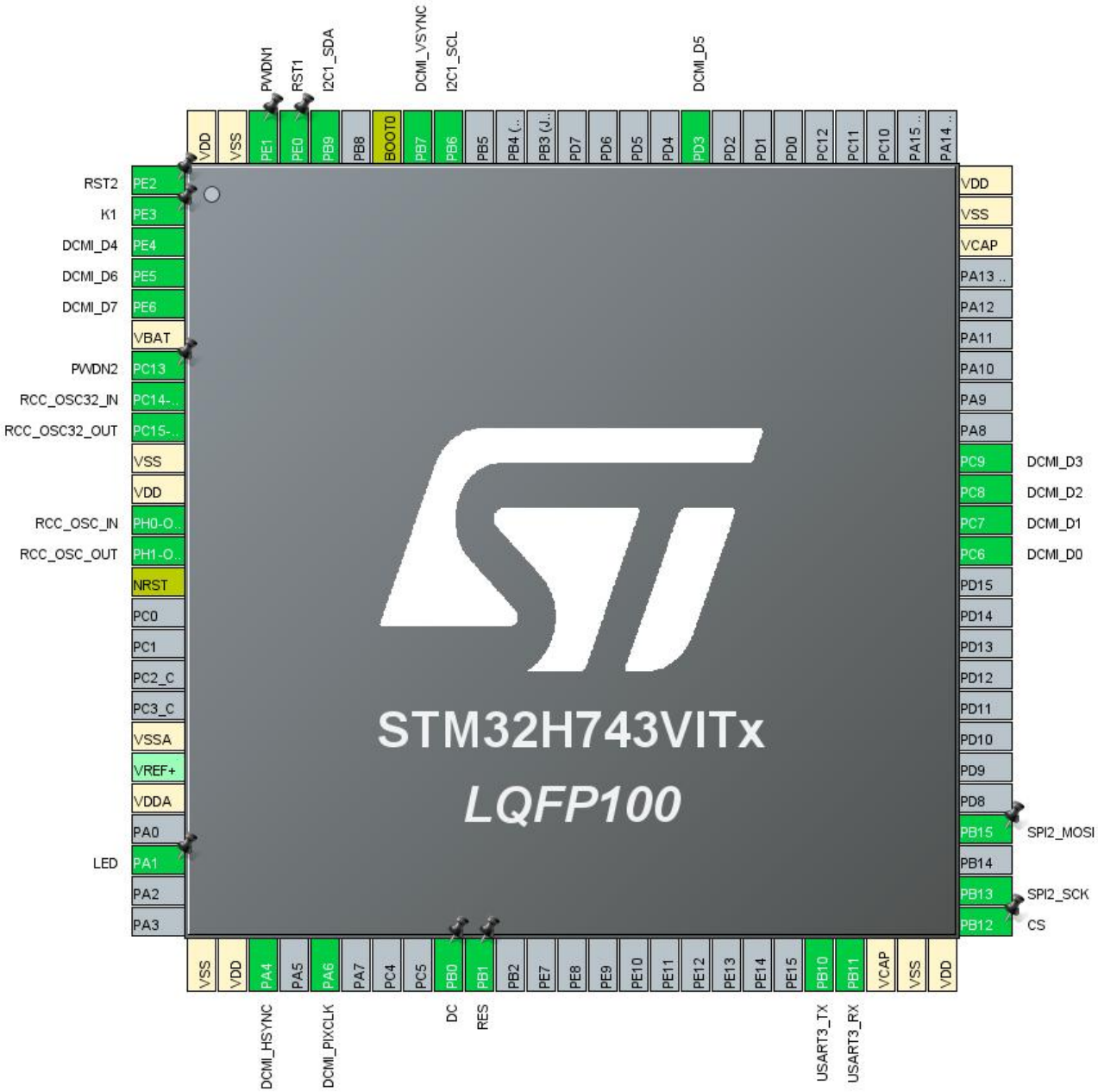
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H743/753
MCU name	STM32H743VITx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	ARM Cortex-M7

2. Pinout Configuration



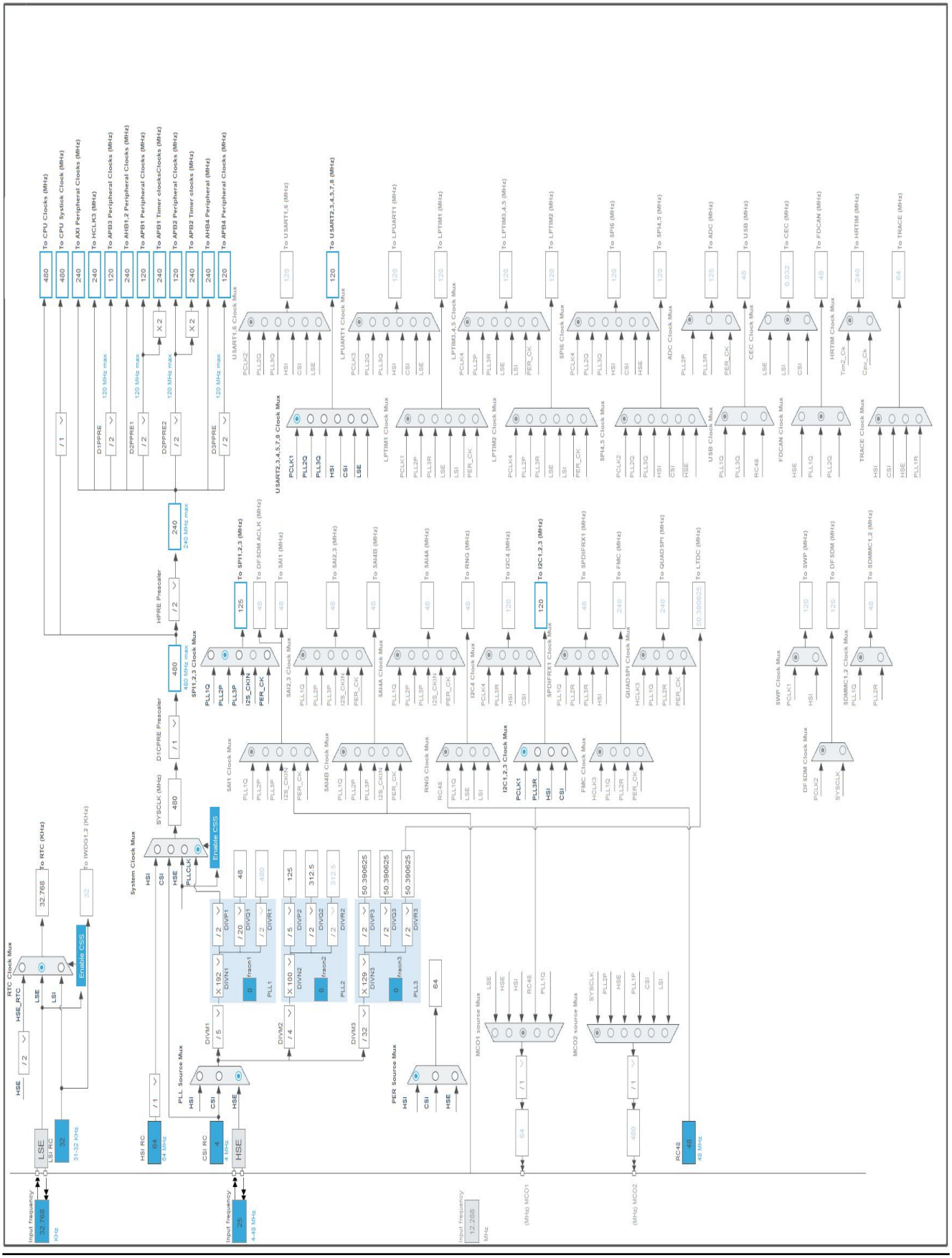
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	RST2
2	PE3 *	I/O	GPIO_Input	K1
3	PE4	I/O	DCMI_D4	
4	PE5	I/O	DCMI_D6	
5	PE6	I/O	DCMI_D7	
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Output	PWDN2
8	PC14-OSC32_IN (OSC32_IN)	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (OSC32_OUT)	I/O	RCC_OSC32_OUT	
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
14	NRST	Reset		
19	VSSA	Power		
21	VDDA	Power		
23	PA1 *	I/O	GPIO_Output	LED
26	VSS	Power		
27	VDD	Power		
28	PA4	I/O	DCMI_HSYNC	
30	PA6	I/O	DCMI_PIXCLK	
34	PB0 *	I/O	GPIO_Output	DC
35	PB1 *	I/O	GPIO_Output	RES
46	PB10	I/O	USART3_TX	
47	PB11	I/O	USART3_RX	
48	VCAP	Power		
49	VSS	Power		
50	VDD	Power		
51	PB12 *	I/O	GPIO_Output	CS
52	PB13	I/O	SPI2_SCK	
54	PB15	I/O	SPI2_MOSI	
63	PC6	I/O	DCMI_D0	
64	PC7	I/O	DCMI_D1	
65	PC8	I/O	DCMI_D2	

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
66	PC9	I/O	DCMI_D3	
73	VCAP	Power		
74	VSS	Power		
75	VDD	Power		
84	PD3	I/O	DCMI_D5	
92	PB6	I/O	I2C1_SCL	
93	PB7	I/O	DCMI_VSYNC	
94	BOOT0	Boot		
96	PB9	I/O	I2C1_SDA	
97	PE0 *	I/O	GPIO_Output	RST1
98	PE1 *	I/O	GPIO_Output	PWDN1
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	AI_on_STM32
Project Folder	E:\base\base_data\project\STM\AI_on_STM32
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.9.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x800
Minimum Stack Size	0x1000

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_DCMI_Init	DCMI
5	MX_I2C1_Init	I2C1
6	MX_USART3_UART_Init	USART3
7	MX_SPI2_Init	SPI2
8	MX_CRC_Init	CRC
9	MX_RTC_Init	RTC
10	MX_TIM6_Init	TIM6
12	MX_X_CUBE_AI_Init	STMicroelectronics.X-CUBE-AI.6.0.0

Rank	Function Name	Peripheral Instance Name
13	MX_X_CUBE_AI_Process	STMicroelectronics.X-CUBE-AI.6.0.0

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H743/753
MCU	STM32H743VITx
Datasheet	DS12110_Rev8

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

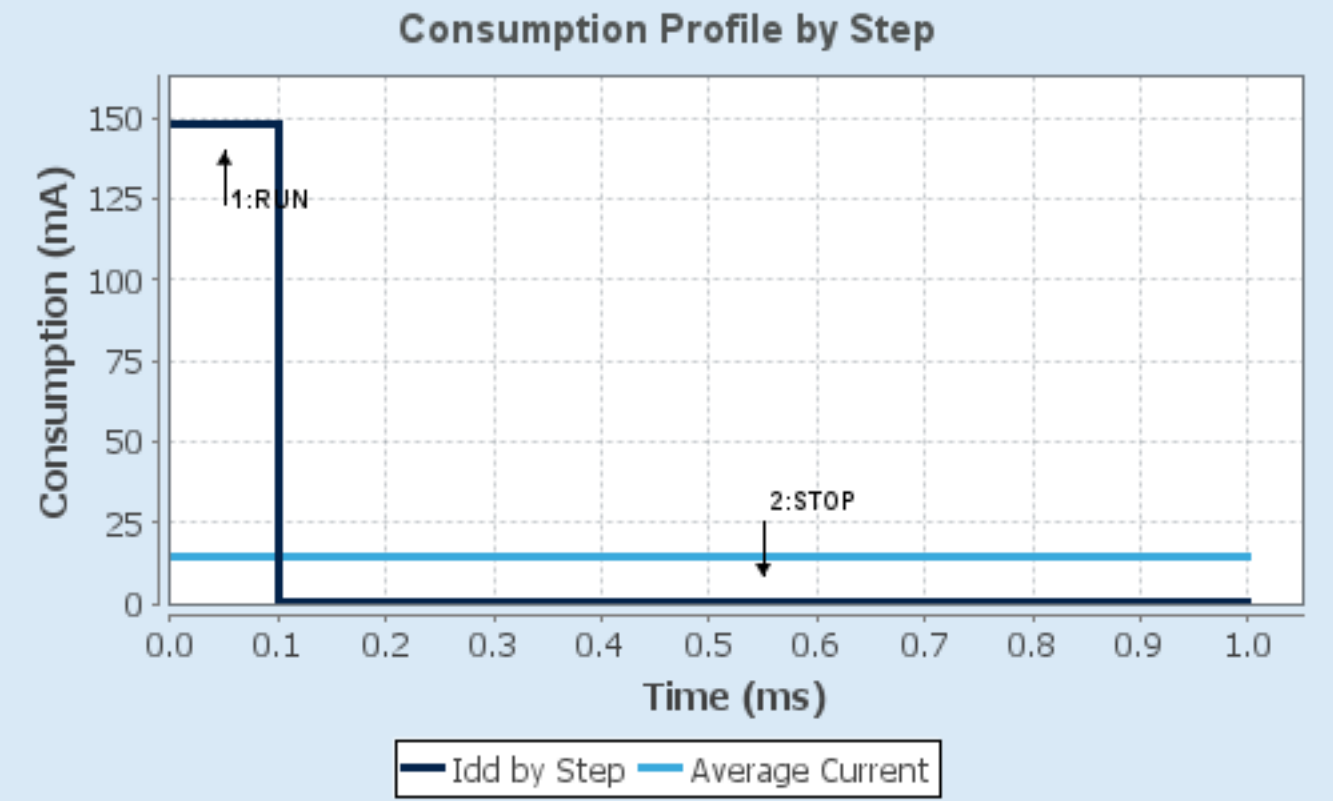
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0-High	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	ITCM	NA
CPU Frequency	480 MHz	0 Hz
Clock Configuration	HSE BYP PLL	Flash-OFF
Clock Source Frequency	24 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	148 mA	150 µA
Duration	0.1 ms	0.9 ms
DMIPS	1027.0	0.0
Ta Max	105.02	124.98
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	14.94 mA
Battery Life	1 day, 17 hours	Average DMIPS	1027.2001 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
150
125
100
75
50
25
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. CRC

mode: Activated

7.1.1. Parameter Settings:

Basic Parameters:

Default Polynomial State	Enable
Default Init Value State	Enable

Advanced Parameters:

Input Data Inversion Mode	None
Output Data Inversion Mode	Disable
Input Data Format	Bytes

7.2. DCMI

DCMI: Slave 8 bits External Synchro

7.2.1. Parameter Settings:

Mode Config:

Pixel clock polarity	**Active on Rising edge ***
Vertical synchronization polarity	Active Low
Horizontal synchronization polarity	Active Low
Frequency of frame capture	All frames are captured
JPEG mode	Disabled

Interface Capture Config:

Byte Select Mode	Interface captures all received bytes
Line Select Mode	Interface captures all received lines

7.3. I2C1

I2C: I2C

7.3.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	**300 ***

Fall Time (ns)	**300 ***
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x70843A4F ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.4.1. Parameter Settings:

Power Parameters:

SupplySource	PWR_LDO_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 0

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
LSE Drive Capability	LSE oscillator low drive capability
CSI Calibration Value	16
HSI Calibration Value	32

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	4 WS (5 CPU cycle)
Product revision	rev.Y

PLL range Parameters:

PLL1 clock Input range	Between 4 and 8 MHz
PLL2 input frequency range	Between 4 and 8 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	Wide VCO range

7.5. RTC

mode: Activate Clock Source

7.5.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

7.6. SPI2

Mode: Transmit Only Master

7.6.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**4 ***
Baud Rate	**31.25 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.7. SYS

Timebase Source: SysTick

7.8. TIM6

mode: Activated

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**48000 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**5000 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.9. USART3

Mode: Asynchronous

7.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable

Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.10. STMicroelectronics.X-CUBE-AI.6.0.0

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DCMI	PE4	DCMI_D4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE5	DCMI_D6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE6	DCMI_D7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA4	DCMI_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA6	DCMI_PIXCLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC6	DCMI_D0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	DCMI_D1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC8	DCMI_D2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC9	DCMI_D3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD3	DCMI_D5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB7	DCMI_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	**Pull-up ***	**Very High ***	
	PB9	I2C1_SDA	Alternate Function Open Drain	**Pull-up ***	**Very High ***	
RCC	PC14-OSC32_IN (OSC32_IN)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SPI2	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART3	PB10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RST2
	PE3	GPIO_Input	Input mode	**Pull-up ***	n/a	K1
	PC13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PWDN2
	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	DC
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	RES
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	CS
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RST1
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PWDN1

8.2. DMA configuration

DMA request	Stream	Direction	Priority
DCMI	DMA2_Stream1	Peripheral To Memory	**Very High ***
SPI2_TX	DMA1_Stream7	Memory To Peripheral	**High ***

DCMI: DMA2_Stream1 DMA request Settings:

Mode:	**Circular ***
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Byte ***
Peripheral Burst Size:	Single
Memory Burst Size:	Single

SPI2_TX: DMA1_Stream7 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. BDMA configuration

nothing configured in DMA service

8.4. MDMA configuration

nothing configured in DMA service

8.5. NVIC configuration

8.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
SPI2 global interrupt	true	0	0
DMA1 stream7 global interrupt	true	0	0
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	true	0	0
DMA2 stream1 global interrupt	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
USART3 global interrupt	unused		
DCMI global interrupt	unused		
FPU global interrupt	unused		
HSEM1 global interrupt	unused		

8.5.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
SPI2 global interrupt	false	true	true

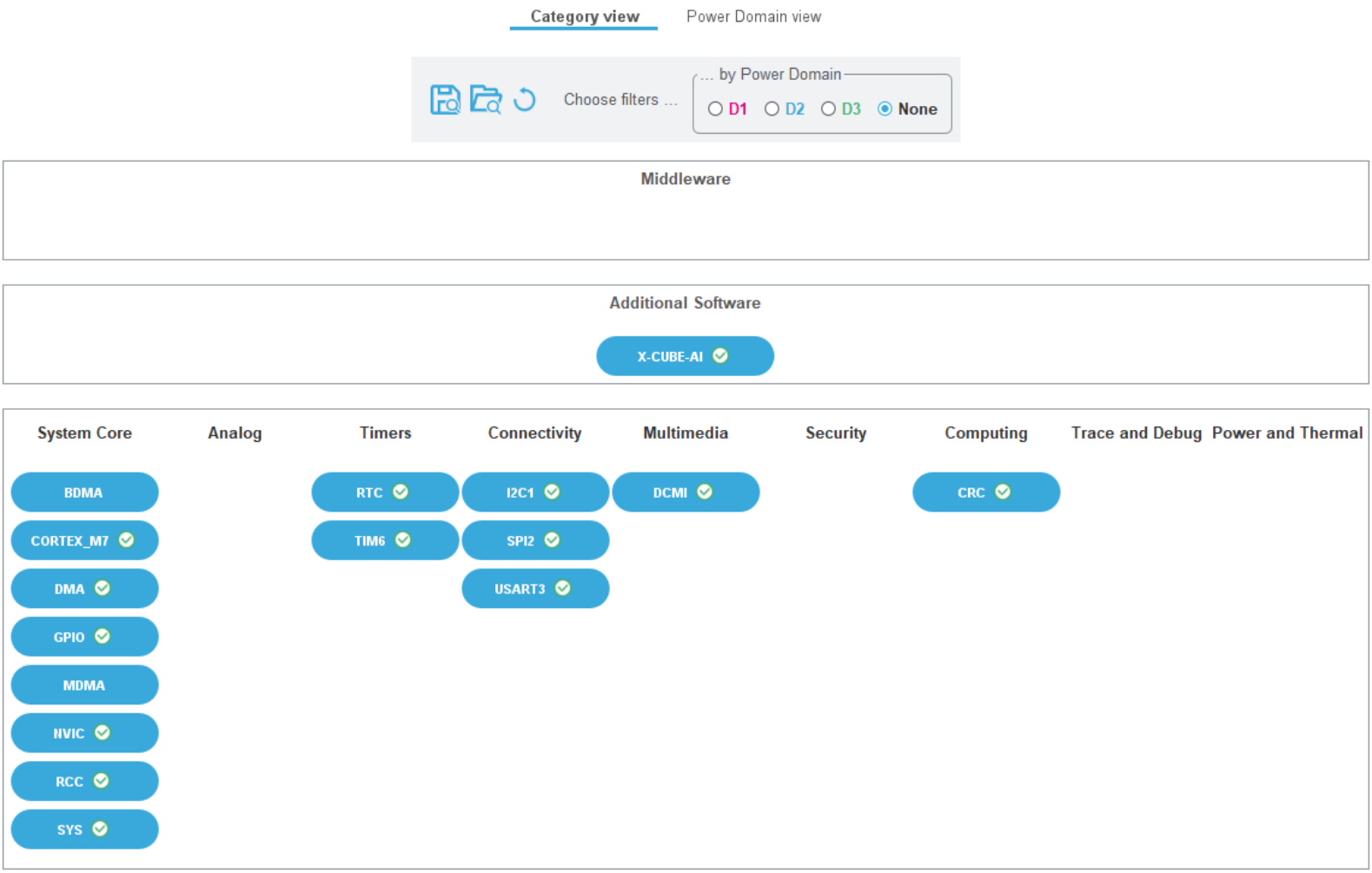
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
DMA1 stream7 global interrupt	false	true	true
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	false	true	true
DMA2 stream1 global interrupt	false	true	true

*** User modified value**

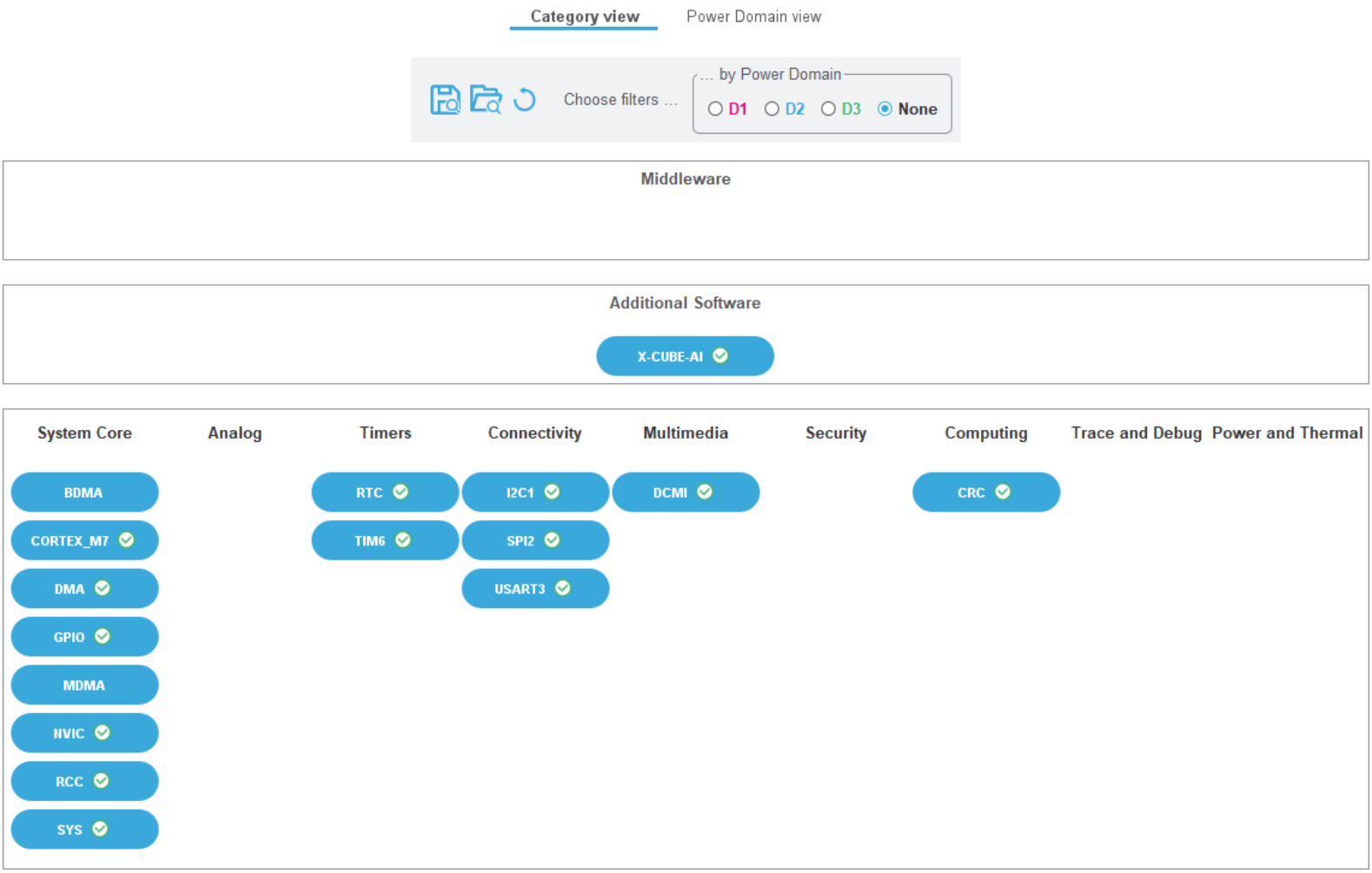
9. System Views

9.1. Category view

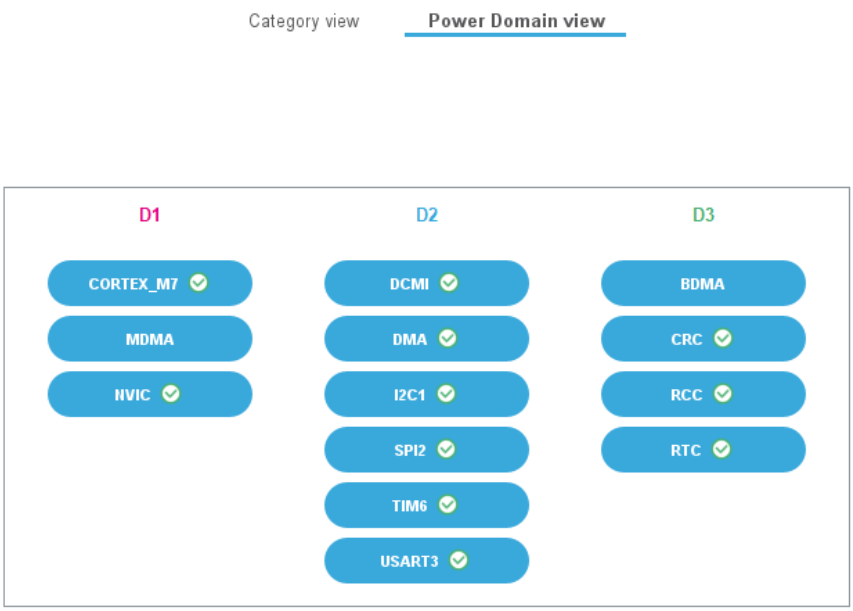
9.1.1. Current



9.1.2. Without filters



9.2. Power Domain view



10. Software Pack Report

10.1. Software Pack selected

Vendor	Name	Version	Component
STMicroelectronics	X-CUBE-AI	6.0.0	Class : Artificial Intelligence Group : Core Version : 6.0.0 Class : Device Group : Application Variant : ApplicationTemplate Version : 6.0.0

11. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00387108.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00314099.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00237416.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00368411.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00121475.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00151811.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00227538.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272913.pdf

Application note	http://www.st.com/resource/en/application_note/DM00287603.pdf
Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00337702.pdf
Application note	http://www.st.com/resource/en/application_note/DM00337873.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354333.pdf
Application note	http://www.st.com/resource/en/application_note/DM00356635.pdf
Application note	http://www.st.com/resource/en/application_note/DM00373474.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00393275.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00431633.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00525510.pdf
Application note	http://www.st.com/resource/en/application_note/DM00535045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00600614.pdf
Application note	http://www.st.com/resource/en/application_note/DM00609692.pdf
Application note	http://www.st.com/resource/en/application_note/DM00622045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00623136.pdf
Application note	http://www.st.com/resource/en/application_note/DM00625700.pdf
Application note	http://www.st.com/resource/en/application_note/DM00628458.pdf
Application note	http://www.st.com/resource/en/application_note/DM00660346.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf