# RAMAKRISHNA MISSION
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## B.Sc. End-Semester Examination

3. (a) $F = (X+Y*Z) / (Y \times Z)$

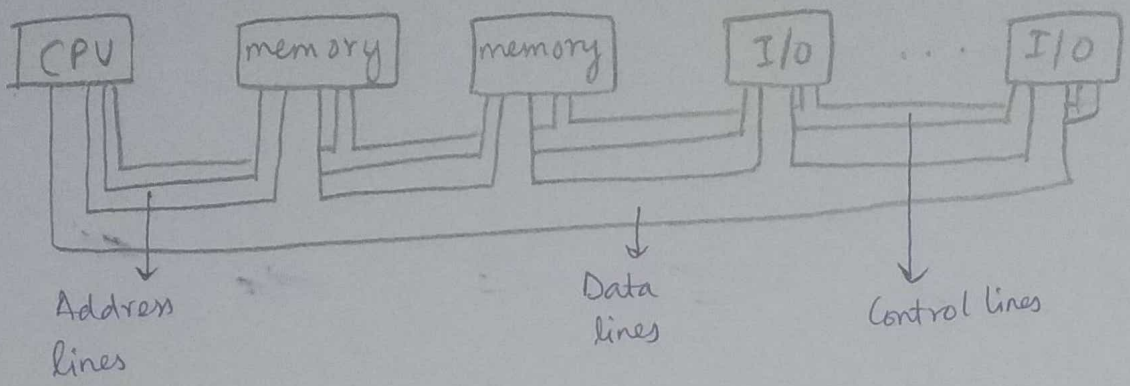
3 address instruction :

| | | |
|---|---|---|
| ADD | $R_1, X, Y$ | $R_1 \leftarrow X+Y$ |
| SUB | $R_1, R_1, Z$ | $R_1 \leftarrow R_1 - Z$ |
| MUL | $R_2, Y, Z$ | $R_2 \leftarrow Y \times Z$ |
| DIV | $F, R_1, R_2$ | $F \leftarrow R_1 / R_2$ |

2 address instruction :

| | | |
|---|---|---|
| MOV | $R_1, X$ | $R_1 \leftarrow X$ |
| ADD | $R_1, Y$ | $R_1 \leftarrow R_1 + Y$ |
| SUB | $R_1, Z$ | $R_1 \leftarrow R_1 - Z$ |
| MOV | $R_2, Y$ | $R_2 \leftarrow Y$ |
| MUL | $R_2, Z$ | $R_2 \leftarrow R_2 \times Z$ |
| DIV | $R_1, R_2$ | $R_1 \leftarrow R_1 / R_2$ |
| MOV | $F, R_1$ | $F \leftarrow R_1$ |

(b)




A system bus generally consists of 50 to 100 lines. Each line contains a particular function. There are many types of bus designs, but they contain lines of mainly three functional groups- data lines, control lines and address lines.

Data lines provide a path for moving data among system modules. Data lines are collectively called data bus. A data bus consists of 32, 64, 128 or more number of lines. The total number of lines is called the width of the data bus. The performance of the data bus depends on its width.

Control lines are used to operate the data and address lines, as they are used by all modules. Control lines transmit both command and timing information among the modules.

Address lines are used to designate the source or destination of the data in the data bus. That means if the processor needs to read a data of 8, 16 or 32 bits, it will put the address of the data on the address line. Address bus determines the maximum memory capacity of the system. Address lines are also used to address I/O ports.

1. (i) The characteristic of boolean algebra that states that one expression can be obtained from another expression by replacing every 1 with 0, every 0 with 1, every (+) with (.), every (.) with (+) is called principle of duality

(ii) $(10110.1111101)_2$

$= 1.0110111101 \times 2^{+4}$

Biased exponent = ~~$2^{k-1}-1+(+4)$~~ $2^{k-1}-1+(+4)$

Since it is 32 bit, here $K=8$

$\therefore$ Biased exponent $= 2^7 - 1 + (+4)$

$= 127 + (+4)$

$= 131$

$= 2^7 + 3$

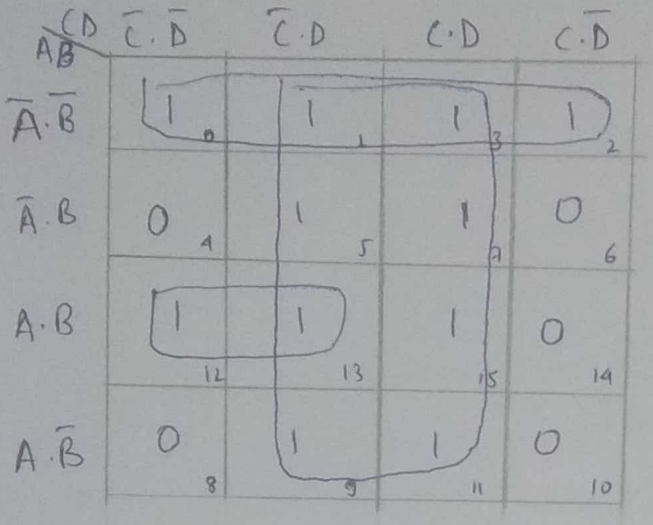
$= (10000000)_2 + (11)_2$

$= (10000011)_2$

$\therefore$ 32 bit IEEE 754 biased exponent format representation:

| 0 | 10000011 | 01101111010000000000000 |
|---|---|---|
| Sign bit (1 bit) | Biased exponent (8 bits) | Mantissa (23 bits) |

(iii) $F(A,B,C,D) = \Sigma m(0,1,2,3,5,7,9,11,12,13,15)$



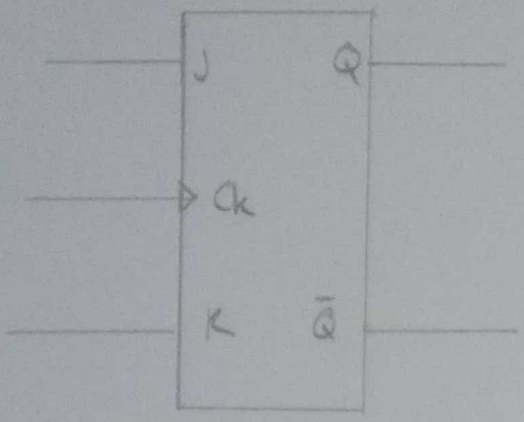

Octet = $m_1 m_3 m_5 m_7 m_{13} m_{15} m_9 m_{11} = D$

Quad = $m_0 m_1 m_3 m_2 = \bar{A}\cdot\bar{B}$

Pair = $m_{12} m_{13} = AB\bar{C}$

$\therefore F = D + \bar{A}\cdot\bar{B} + AB\bar{C}$

2. (a)




Graphic symbol of J-K flipflop

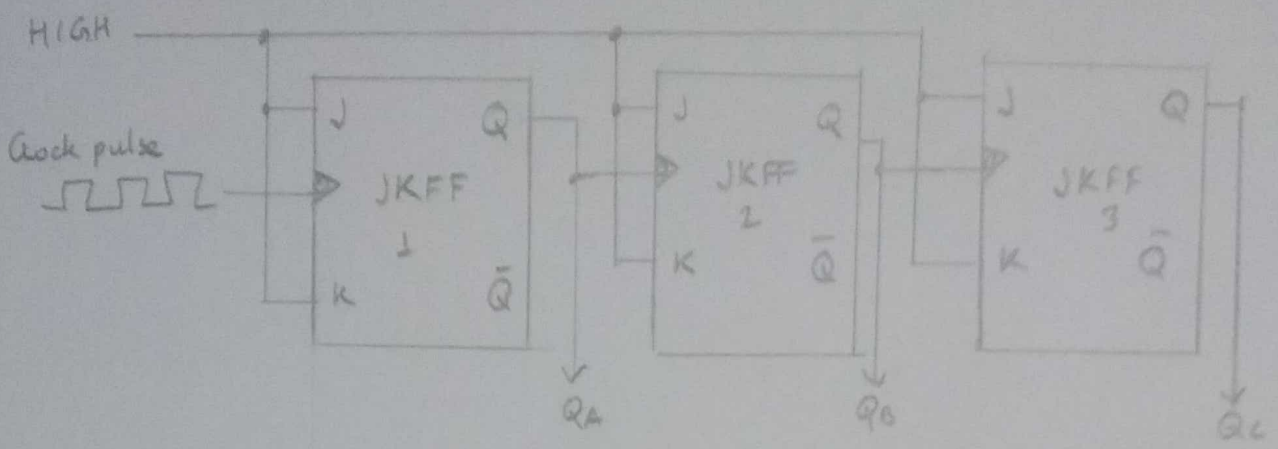
| J | K | $Q_{n+1}$ |
|---|---|---|
| 0 | 0 | $Q_n$ |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | $\bar{Q}_n$ |

Truth table of J-K flip flop

A J-K flip flop has two inputs, similar to the S-R flip flop. However, unlike the S-R flip flop, all possible combination of input values are valid in J-K flip flop.

With no input asserted, the output of J-K flip flop is stable.
If only the J input is asserted, the result is a set function, causing the output to be 1.
If only the K input is asserted, the result is a reset function, causing the output to be 0. When both J and K are 1, the function performed is referred to as the toggle function: the output is reversed. Thus, if Q is 1, and 1 is applied to J and K, then Q becomes 0.

(b)




Circuit diagram of ~~asynchronous~~ 3-bit asynchronous up counter

The ~~circuit~~ 3-bit asynchronous up counter uses ~~3 flip-flops~~ 3 T-flip flops.

The counter consists of $2^3 = 8$ count states (000, 001, 010, 011, 100, 101, 110, 111). The counter counts the incoming pulses starting from 0 to 7

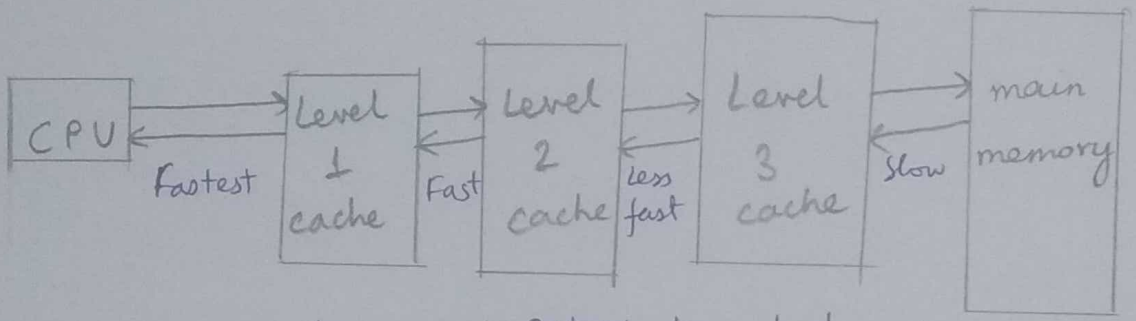
In the circuit digram, the clock pulse is given as clock input for JKFF1. For the other flip flops, the clock input is fed from the ~~output~~ output of other flip flops. The clock pulse count is noted at the output of each flip-flop ($Q_C Q_B Q_A$), where $Q_A$ is the LSB and $Q_C$ is the MSB

The operation of 3-bit asynchronous up counter is similar to that of the 2-bit asynchronous up counter. At the falling edge of each clock pulse, the output of ~~JKFF1~~ JKFF1 toggles. For each logic HIGH output ($Q_A = 1$) of JKFF1, at its falling edge, JKFF2 will toggle the output ($Q_B$). Similarly, for each logic HIGH output ($Q_B = 1$) of JKFF2, JKFF3 will toggle the output ($Q_C$).

5. (a) Microprogrammed control unit: The control unit which is used to generate complex instructions and control signals is called the microprogrammed control unit. It eases the task of designing and is used by CISC processors.

Control memory: A memory which is used to hold the control data in a microprogrammed processor is called control memory. The data stored here is used to control the operation of the data path in the processor.

(b)




Block diagram of three-level cache organization.

Cache memory is relatively faster memory. It holds frequently used data and instructions so that they can be used easily. Cache reduces the average access time of data from the main memory. When a processor needs to read or write a location in the main memory, it uses the cache first, before using the main memory.

7. (a)

| RISC | CISC |
|---|---|
| (i) RISC refers to Reduced Instruction Set Architecture | (i) CISC refers to Complex Instruction Set Architecture. |
| (ii) Simple instructions are used in RISC | (ii) Complex instructions are used in CISC. |
| (iii) Instructions are of size under 1 word. | (iii) Instructions are larger than 1 word in size. |
| (iv) It employs simple addressing modes. | (iv) It employs complex addressing modes. |
| (v) Number of data types used in RISC is fewer. | (v) CISC uses more datatypes. |
| (vi) More general purpose registers are used in RISC. | (vi) Less general purpose registers are used in CISC as operations are performed in the memory cell. |
| (vii) RISC uses only hardwired control unit | (vii) CISC uses both hardwired and microprogrammed control unit. |
| (viii) Each instruction is executed in a single clock cycle | (viii) Each instruction takes multiple clock cycles. |

(b) The tendency of a computer program to access instructions of nearby address is called locality of reference.

(c) The process by which the current bus accesses and then leaves the control of the bus and passes it to another bus requesting processor unit is called Bus arbitration.