AN13182

VR5510 Device Design Guidelines

Rev. 1 — 3 May 2021 Application note

Document information

Information	Content
Keywords	VR5510, Design Guidelines, Getting started, PMIC Configuration
Abstract	This application note provides design guidelines for VR5510 PMIC configuration and hardware development.

1 Overview

The VR5510 is an automotive, functionally-safe, multi-output power supply IC that focuses on Gateway, ADAS, Radio, and Infotainment applications. The device includes multiple switch modes and linear voltage regulators. It offers external frequency synchronization on inputs and outputs for optimized system EMC performance.

The VR5510 includes enhanced safety features with fail-safe outputs. The device covers ASIL B and ASIL D safety integrity levels and complies with the ISO 26262 standard. The VR55100 can be fully utilized in safety-oriented system partitioning.

The VR5510 is available in several versions that support a variety of safety applications and offer numerous choices with respect to the number of output rails, output voltage settings, operating frequencies, and power-up sequence.

2 VR5510 Features

- 60 V DC maximum input voltage
- VPRE synchronous buck controller with external MOSFETs, configurable output voltage, switching frequency, and current capability up to 10 A
- Low-voltage integrated synchronous BUCK1 and BUCK2 converters, dedicated to MCU core supply with SVS/DVS capability. Configurable output voltage and current capability up to 3.6 A peak. Dual-phase operation to extend the current capability up to 7.2 A peak
- Low-voltage integrated synchronous BUCK3 converter. Configurable output voltage and current capability up to 3.6 A peak
- BOOST converter with integrated low side switch. Configurable output voltage and current capability up to 2.25 A peak
- 3x linear voltage regulators (LDOx) for MCU IOs, DDR, and ADC supplies Configurable output voltage and current capability up to 400 mA DC
- High-voltage linear regulator (HVLDO) with current capability up to 10 mA in LDO mode and 100 mA in Switch mode
- EMC optimization techniques including SMPS frequency synchronization, spread spectrum, slew rate control, manual frequency tuning
- Low-power Standby mode with very low quiescent current (35 µA with VPRE and HVLDO ON)
- 2x input pins for wake-up detection and battery voltage sense
- Device control via I^2C interface with CRC (up to 3.4 MHz)
- Dual devices operation possible via dedicated synchronization pin
- Scalable portfolio from QM to ASIL B to ASIL D with Independent Monitoring Circuitry, dedicated interface for MCU monitoring, simple and challenger watchdog function, Power good, Reset and Interrupt, Built-in Self-Test, Fail-safe Output
- Configuration by OTP programming. Prototype enablement to support custom setting during project development in engineering mode

3 VR5510 Device Pinout

The VR5510 comes in a 56-pin QFN package.

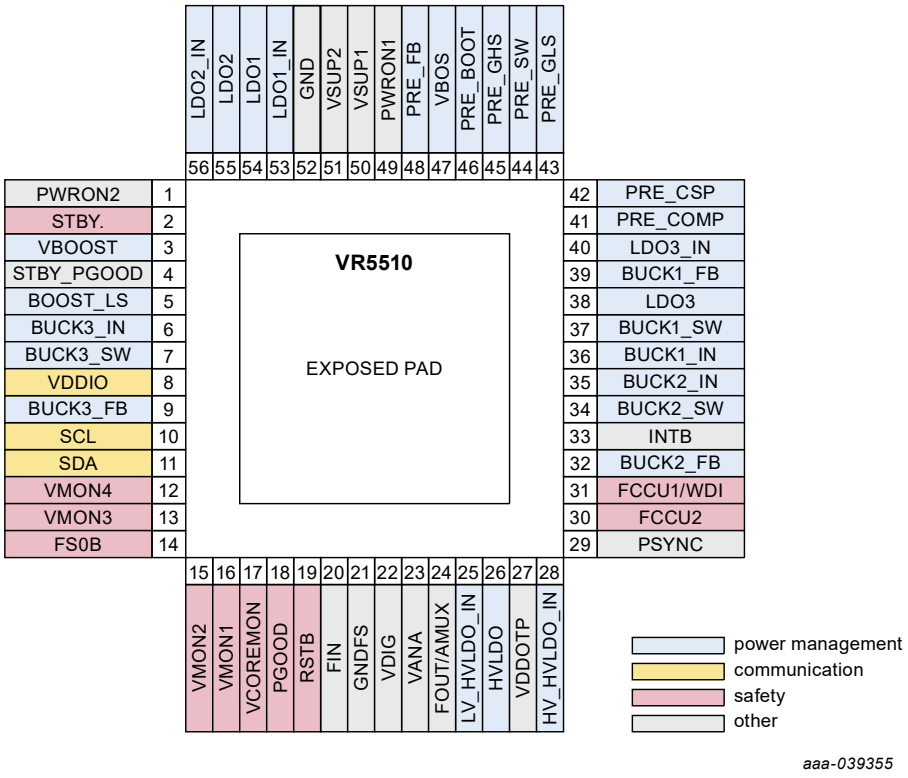

Figure 1. VR5510 device pinout

4 Simplified Application Diagram

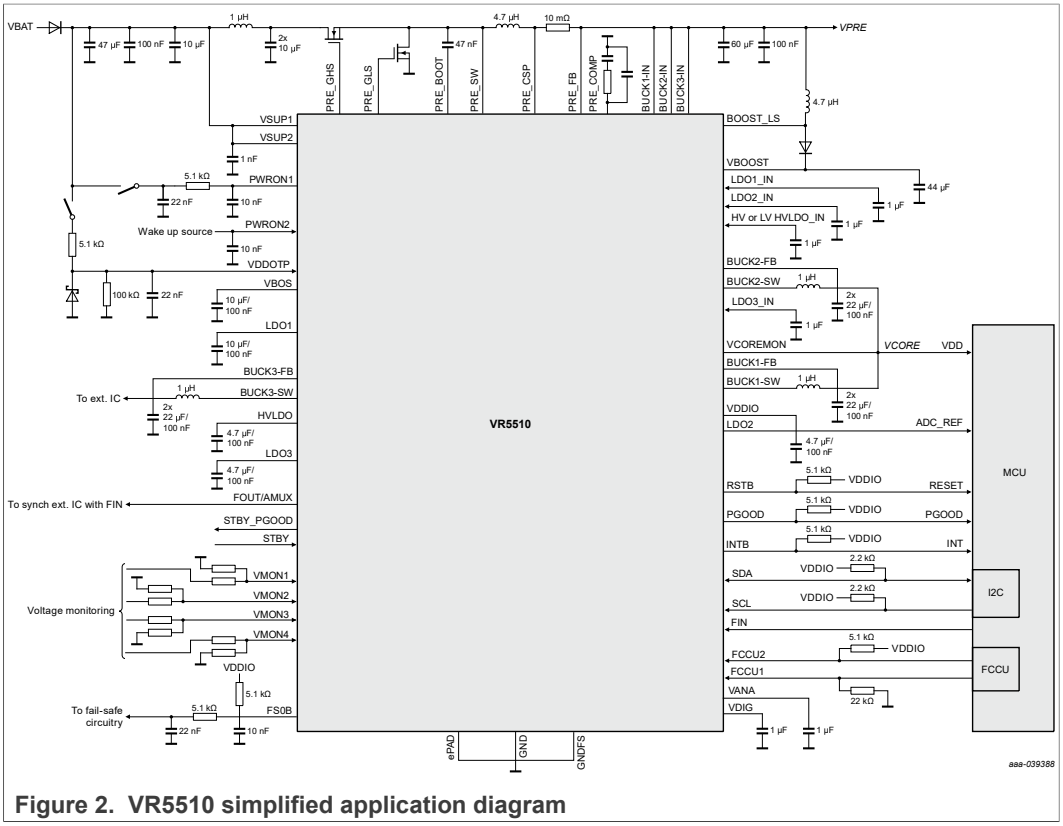

Figure 2. VR5510 simplified application diagram

5 Getting Started

5.1 Entering Debug mode/test mode

- Figure 3 shows the hardware sequence that must be followed to enter Debug mode. The VDDOTP and VSUP1/2 pins must come up first (together or separately). PWRON1 and/or PWRON2 must come up only after the VDDOTP and VSUP1/2 pins have gone high.

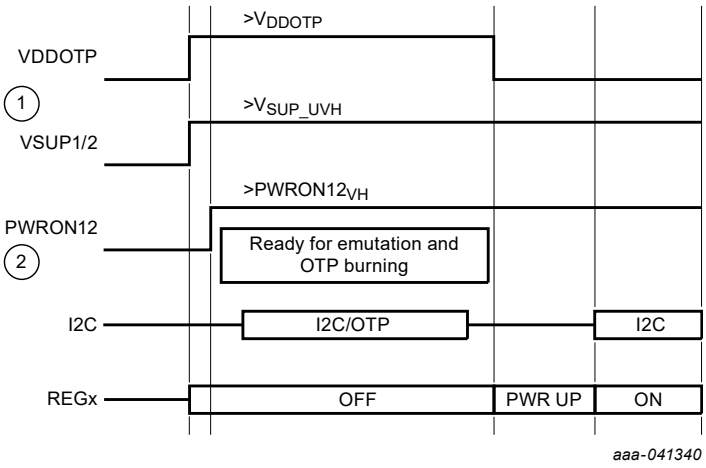

Figure 3. Debug entry startup sequence

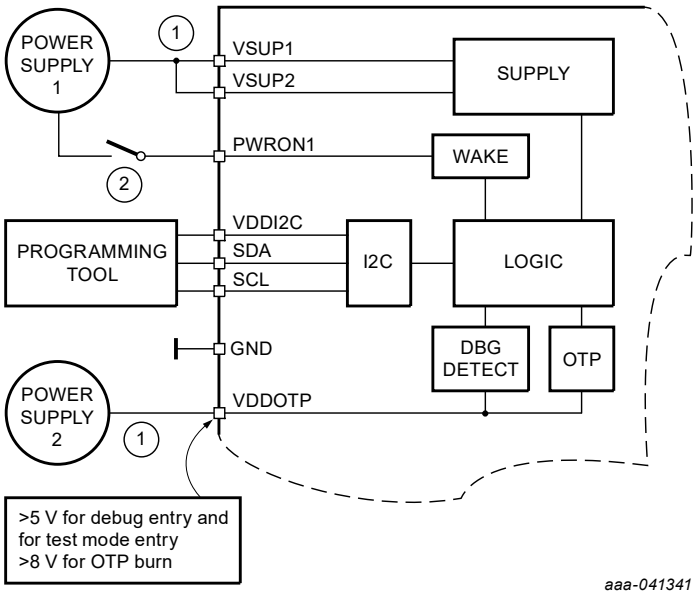

Figure 4. Debug mode startup sequence implemented on board

- The Debug entry startup sequence can be implemented on board by adding an external supply (shown in Figure 4).
- The part then starts up in Debug mode. In this mode, as long as the VDDOTP pin is held high (>5 V), the regulators will be OFF. Debug mode can be confirmed by reading the fail-safe register, FS_STATES(0x18h). If bit 14 is set to 1, then the Debug mode entry is successful.

Table 1. FS_STATES

Register Address	R/W	Bit 15 RO	Bit 14 W	Bit 13 RO	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
(0x18h)		1		1					
Bit name		TCM_ ACTIVE		DBG_ MODE					
Register Address	**R/W**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4 RO**	**Bit 3 RO**	**Bit 2 RO**	**Bit 1 RO**	**Bit 0 RO**
(0x18h)									
Bit Name					FSM_STATES[4:0]				

- After debug entry, a set of test mode keys must be sent through I^2C to enter test mode. This is required in order to access the OTP registers and modify them to the required setting. The VDDOTP pin must be high for test mode keys to be accepted
- The same set of test mode keys must be written to both the main and fail-safe test mode entry registers - M_TM_ENTRY (0x1Fh) and FS_TM_ENTRY (0x26h). Each of the keys below must be written in succession to each register
  - key1: 11010101_10100111
  - key2: 10111000_11101110
  - key3: 00001111_00110111
- After the test mode entry keys are successfully sent, read bit 6 of M_TM_STATUS1 (0x25h) and bit 15 of FS_STATES(0x18h) registers to verify the test mode status. If both the bits are set to 1, then test mode entry is successful

Table 2. M_TM_STATUS1

Register Address	R/W	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
[0x25h]									
Bit Name									
Register Address	**R/W**	**BIT 7**	**BIT 6 RO**	**BIT 5**	**BIT 4 RO**	**BIT 3 RO**	**BIT 2 RO**	**BIT 1 RO**	**BIT 0 RO**
[0x25h]			1						
Bit Name			M_TM_ACTIVE	M_FSM_CURR_STATE[5:0]					

- The VDDOTP pin can now be pulled low and the device turns on with the newly updated OTP settings. Regardless of the VDDOTP pin status, the OTP settings can be modified at this point.
- The new settings take effect immediately

5.2 Modifying a programmed OTP in Debug mode

- To modify the OTP or to read the existing OTP settings, the following procedure must be followed:
  - The part must be set in Debug mode and test mode as explained in Section 5.1 "Entering Debug mode/test mode"
  - VR5510 uses indirect referencing for accessing the OTP registers where the functional I^2C mirror registers in the main and fail-safe domain must be used.
  - Read only: The OTP address must be written first in the MIRRORCMD register and then the MIRRORDATA register must be used for reading the data. Bits 8-15 of MIRRORDATA must be used to read the data. The same procedure must be followed for each OTP register, one register at a time
  - Write: The OTP data must be written first in the MIRRORDATA register (bits 0–7) and then the address must be written in the MIRRORCMD register. Note that bit 8 of MIRRORCMD must be set to 1. The same procedure must be followed for each OTP register, one register at a time

Table 3. MIRRORCMD and MIRRORDATA registers for Main and FS

Registers (I^2C) Name	I^2C Section/Device Address	Register (I^2C) Address	Comments
FS_MIRRORCMD [8:0]	Failsafe, 0x21h	[0x19h]	Bits 0 to 7 must be used to program the OTP address of the required register. Bit 8 is set to 0 for read and 1 for the write operation
FS_MIRRORDATA [15:0]	Failsafe, 0x21h	[0x1Ah]	Bits 0 to 7 must be used to write the OTP data of the required register. Bits 8 to 15 must be used for read operation
M_MIRRORCMD [8:0]	Main, 0x20h	[0x12h]	Bits 0 to 7 must be used to program the OTP address of the required register. Bit 8 is set to 0 for read and 1 for the write operation
M_MIRRORDATA [15:0]	Main, 0x20h	[0x13h]	Bits 0 to 7 must be used to write the OTP data of the required register. Bits 8 to 15 must be used for read operation

- To modify the OTP settings like VPRE output voltage or BUCK12 output voltage, follow the above steps and write to the appropriate register address specified in the data sheet. For example: to change the VPRE output voltage from 3.3 V to 3.5 V (+6 %), write 0x11h to register M_MIRRORDATA, then write the register address 0x18h to M_MIRRORCMD [VPRE voltage OTP register = CFG_VPRE_1_OTP (0x18h)] in the main side state machine
- Proper attention must be paid to the fail-safe side settings as well when a change is being made to the main state machine. In the example above, if the VPRE voltage was monitored externally using one of the VMONs, then the threshold selection on the VMON must also be adjusted in order to prevent an overvoltage or undervoltage condition from disabling the system

- After making the required configuration changes, the DBG_EXIT bit (bit 14) can be set to 1 (in FS_STATES register) to exit Debug mode, which might be essential to test the system with the full functionality.

Table 4. FS_STATES Register

Register Address	R/W	BIT 15 RO	BIT 14 W	BIT 13 RO	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
[0x18h]		1	1	1					
Bit Name		TM_ ACTIVE	DBG_EXIT	DBG_MODE					
Register Address	**R/W**	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4 RO**	**BIT 3 RO**	**BIT 2 RO**	**BIT 1 RO**	**BIT 0 RO**
[0x18h]									
Bit Name					FSM_STATES[4:0]				

6 Interfacing between the PMIC and the MCU

- The VR5510 communicates with the MCU through I^2C
- I^2C specifications are according to the latest NXP I^2C specification UM10204 rev6
- The communication is secured by an 8-bit CRC for each Write and Read command
- Typical I^2C packet transactions between the host(MCU) and the PMIC are below:

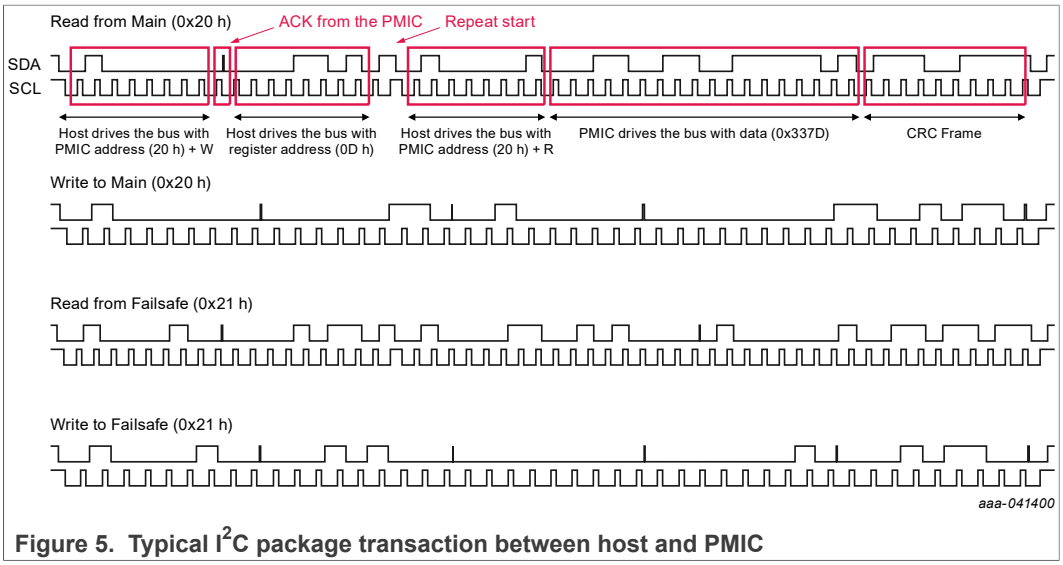

Figure 5. Typical I^2C package transaction between host and PMIC

7 Configuring the PMIC

7.1 Configuring the OTP

- Follow steps in Section 5 "Getting Started" to understand the OTP programming procedure. Most devices come with pre-programmed OTP settings, so the device starts functioning immediately upon powering up.
- Refer to **Section 27** in the VR5510 data sheet for additional information about all the OTP registers.
- The following functions should be used as a guideline on how to implement a software routine for the drivers. Examples of software routines are mentioned in the following sections as PMIC_xxx (). Depending on each MCU, the contents of these functions might vary. Therefore, the following sections define a generic set of registers to configure in each function.

7.2 Initializing the PMIC (safety applications – ASILB to ASILD)

- After initial power-up, the device reaches the initialization stage **(INIT_FS)** of the state machine and releases the RSTB pin as an indication. The MCU can be programmed to send initialization commands to the PMIC during this phase to modify the default functions or read the status.
- The following is applicable for initial power-up, wake up from the standby state or from a reset condition
- The **(INIT_FS)** has a configurable window of 256 ms to 67 s during which all the initialization commands must be set by the MCU. After this phase, these registers become **read only**
- The MCU must follow the procedure below to write to the INIT_FS registers. This is to secure the write process
  - Write the desired data in the FS_I_Register_N (DATA)
  - Write the opposite in the FS_I_NOT_Register_N (DATA_NOT)
- After writing to all the registers, the MCU must close the INIT_FS window by sending a good watchdog refresh before the window period expires. Refer to the VR5510 data sheet for more information
- The MCU can also request to go to this INIT_FS state by writing to the bit “GO_TO_INITFS” (bit 2) in FS_SAFE_IOs (0x15h) register in address 0x21h
- The MCU can use the default I^2C device address: **0x20h for Main and 0x21h for Failsafe (FS)** registers. These addresses are also configurable in the OTP using DEVICEID_OTP (main) and I2CDEVID_OTP (fail-safe). Refer to the VR5510 data sheet for more information

Table 5. Prerequisites in OTP

	Register Address	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
						0	0	0	0
Bit Name (Main)	[0x31h]					DEVICEID_OTP [3:0]			
Bit Name (Failsafe)	[0x17h]					I2CDEVID_OTP [3:0]			

- See **Sections 23, 24, 25, and 26** in the data sheet for detailed description regarding the I^2C configurations, data frame to use, and list of registers,
- The following registers are required for the PMIC to release the safety pin FS0B after the MCU sets the right initialization values, issues a valid watchdog refresh, and sends a release FS0B command.
- **PMIC_Init ()** – to configure initial register configuration

Table 6. List of INIT_FS registers

Registers (I^2C) Name	I^2C Section/Address	Registers (I^2C) Address	Comments
FS_I_OVUV_SAFE_REACTION1	Fail-safe, 0x21h	[0x01h]	To configure the OV, UV impact reaction of monitors
FS_I_NOT_OVUV_SAFE_REACTION1	Fail-safe, 0x21h	[0x02h]	Write opposite data of 0x01h
FS_I_OVUV_SAFE_REACTION2	Fail-safe, 0x21h	[0x03h]	To configure the OV, UV impact reaction of monitors
FS_I_NOT_OVUV_SAFE_REACTION2	Fail-safe, 0x21h	[0x04h]	Write opposite data of 0x03h
FS_I_ABIST2_CTRL	Fail-safe, 0x21h	[0x05h]	To configure the ABIST2 assignments of VMONs
FS_I_NOT_ABIST2_CTRL	Fail-safe, 0x21h	[0x06h]	Write opposite data of 0x05h
FS_I_WD_CFG	Fail-safe, 0x21h	[0x07h]	Configure the WD error and refresh settings
FS_I_NOT_WD_CFG	Fail-safe, 0x21h	[0x08h]	Write opposite data of 0x07h
FS_I_SAFE_INPUTS	Fail-safe, 0x21h	[0x09h]	Configure the FCCU settings and reaction
FS_I_NOT_SAFE_INPUTS	Fail-safe, 0x21h	[0x0Ah]	Write opposite data of 0x09h
FS_I_FSSM	Fail-safe, 0x21h	[0x0Bh]	Configure the fault error impact and count settings
FS_I_NOT_FSSM	Fail-safe, 0x21h	[0x0Ch]	Write opposite data of 0x0Bh
FS_I_SVS	Fail-safe, 0x21h	[0x0Dh]	Configure the SVS settings
FS_I_NOT_SVS	Fail-safe, 0x21h	[0x0Eh]	Write opposite data of 0x0Dh

7.3 Disabling Watchdog and FCCU monitoring

The ASIL B and ASIL D versions of the device have a windowed watchdog with different watchdog types. Simple watchdog for ASILB and challenger type (Q&A) for ASILD devices. The watchdog can only be disabled in the INIT_FS state.

To disable the watchdog, modify the watchdog window period configuration bits of the FS_WD_WINDOW register.

Table 7. WD_WINDOW setting

WD_WINDOW[3:0]	Watchdog Window Period
0000	DISABLE (during INIT_FS only)
0001	1.0 ms
0010	2.0 ms
0011 (default)	3.0 ms

Table 7. WD_WINDOW setting*...continued*

WD_WINDOW[3:0]	Watchdog Window Period
0100	4.0 ms
0101	6.0 ms
0110	8.0 ms
0111	12 ms
1000	16 ms
1001	24 ms
1010	32 ms
1011	64 ms
1100	128 ms
1101	256 ms
1110	512 ms
1111	1024 ms
Reset condition	POR

Table 8. FS_WD_WINDOW register

	Register Address	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Bit Name	0x0Fh	WD_WINDOW[3:0]				Reserved	WDW_DC[2:0]		
	Register Address	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit Name	0x0Fh	Reserved	Reserved	Reserved	Reserved	WDW_RECOVERY[3:0]			

Write

FS_WD_WINDOW=0x20B //Disable watchdog

FS_NOT_WD_WINDOW=0xF504

When the device exits INIT_FS state, FCCU monitoring starts. In order to avoid a fault coming from the FCCU, pins should be put in the correct state, or FCCU should be disabled. FCCU monitoring can be disabled with the FCCU_CFG[1:0] bits of the FS_I_SAFE_INPUTS register.

Table 9. FCCU configuration

FCCU_CFG[1:0]	FCCU pins configuration
00	No monitoring
01 (default)	**FCCU1 and FCCU2 monitoring by pair (bi-stable protocol)**
10	FCCU1 or FCCU2 input monitoring
11	FCCU1 input monitoring only
Reset condition	POR

Table 10. FS_I_SAFE_INPUTS register

	Register Address	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Bit Name	0x09h	FCCU_CFG[1:0]		0	FCCU12_ FLT_POL	FCCU1_ FLT_POL	FCCU2_ FLT_POL	Reserved	FCCU12_ FS_ IMPACT
	Register Address	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit Name	0x09h	FCCU1_ FS_ IMPACT	FCCU2_ FS_ IMPACT	Reserved	Reserved	TIMING_WINDOW_STBY[3:0]			

Write

FS_I_SAFE_INPUTS=0x01CA

FS_I_NOT_SAFE_INPUTS=0xFE35

A good watchdog refresh is required to exit the INIT_FS state. The good answer should be written in FS_WD_ANSWER register.

Table 11. FS_WD_ANSWER register

	Register Address	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Bit Name	0x12h	WD_ANSWER[15:0]							
	Register Address	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit Name	0x12h	WD_ANSWER[15:0]							

FS_WD_ANSWER= 0xA54D // Challenger watchdog refresh

FS_WD_ANSWER=0x5AB2 // Simple watchdog refresh

The command sequence is:

FS_WD_WINDOW=0x020B //Disable watchdog

FS_NOT_WD_WINDOW=0xFDF4

FS_I_SAFE_INPUTS=0x01CA //Disable FCCU monitoring

FS_I_NOT_SAFE_INPUTS=0xFE35

FS_WD_ANSWER= 0xA54D or FS_WD_ANSWER=0x5AB2 // Good watchdog (for Challenger or Simple) to exit INIT_FS

The watchdog refresh that enables exiting from the INIT_FS state should be written before the WD_INIT_TIMEOUT expires. The value of this timer is configurable by OTP with the WD_INIT_TIMEOUT_OTP[1:0] bits of the CFG_2_OTP register. For the S32G OTP, this timer is 1024 ms.

7.4 Configuring the low-power mode (STBY)

- **PMIC_SetMode ()** – to configure low-power Standby mode (STBY)

STBY is an input that can be connected in the application to the MCU. The standby input pin polarity can be programmed through STBY_POLARITY_OTP bit to either active high or active low in Standby mode.

The STBY function should be enabled via the STBY_EN_OTP bit. There are two possible paths for entering Standby mode (selected via the STBY_SAFE_DIS_OTP bit):

- Standard path using only the STBY pin transition,
- Safety path using an I^2C request (STBY_REQ bit) + STBY pin transition

Table 12. Prerequisites in OTP - Main (0x20h)

Register Address	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
[0x31h]	RW	1	0	0	1				
Bit Name		STBY_ PGOOD _EN_OTP	STBY_ POLARITY _OTP	STBY_DISCH _OTP	STBY_TIMER _EN_OTP				

Table 13. Prerequisites in OTP - Main (0x20h) (continued)

Register Address	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
[0x19h]	RW			1	0	0	1	0	
Bit Name				STBY_ WINDOW_EN_ OTP	STBY_ SAFE_DIS_ OTP	STBY_ POLARITY_ OTP	STBY_ EN_OTP	RSTB_DELAY _OTP	

Table 14. List of I^2C STANDBY mode registers

Registers (I^2C) Name	I^2C Section/Address	Registers (I^2C) Address	Comments
FS_SAFE_IOS [1]	Fail-safe, 0x21h	[0x15h]	STBY_REQ; Write 1 to this bit to make a standby request via I^2C by the MCU
FS_I_SAFE_INPUTS [3:0]	Fail-safe, 0x21h	[0x09h]	TIMING_WINDOW_STBY; Configure the standby window duration between I^2C request and pin transition settings by writing to these bits
M_MODE [0]	Main, 0x20h	[0x1h]	STBY_PGOOD_TEST_EN; Configure this bit to enable or disable the STBY_PGOOD test function
M_SM_CTRL1 [10]	Main, 0x20h	[0x2h]	STBY_TIMER_EN; Configure this bit to enable or disable the standby timer
M_SM_CTRL1 [15:12]	Main, 0x20h	[0x2h]	TIMER_STBY_WINDOW; Configure the duration of standby operation using these bits

7.5 Getting the status of regulators and IOs

- **PMIC_GetSystemEvents ()** – to read status of safety and non-safety related events

Table 15. Flags and IOs registers

Registers (I^2C) Name	I^2C Section/Address	Registers (I^2C) Address	Comments
FS_GRL_FLAGS	Fail-safe, 0x21h	[0x00h]	To read the status of the safety pins FCCU1 and FCCU2; Also, to read the flags related to WD, IOs or I^2C communication
FS_OVUVREG_STATUS	Fail-safe, 0x21h	[0x13h]	To read the status of all OV, UV flags related to the monitors
FS_DIAG_SAFETY	Fail-safe, 0x21h	[0x16h]	To read the status of the diagnostics checks like ABIST, LBIST. Also, to read the flags related to the safety pins, CRC, and low-power CLK
FS_SAFE_IOS [15:3]	Fail-safe, 0x21h	[0x15h]	To configure and read the status of all the safety IO pins like RSTB, PGOOD and FS0B
FS_STATES	Fail-safe, 0x21h	[0x18h]	To read the status of the fail-safe state machine and the integrity of fail-safe OTP and INIT_FS registers
M_FLAG	Main, 0x20h	[0x00h]	To read the status of all the events/ interrupts of the regulators
M_FLAG1	Main, 0x20h	[0x0Ch]	To read the status of OC and TSD flags of the regulators
M_FLAG2	Main, 0x20h	[0x0Dh]	To read the status of UV and OV flags of the regulators
M_FLAG3	Main, 0x20h	[0x0Eh]	To read the present status of all the regulators

7.6 Configuring the PMIC interrupts

- **PMIC_SetSystemReactions ()** – to configure the interrupt mask for several safety and non-safety related events. Safety related impact registers must be modified only during the INITS_FS state. Refer to Section 20.2 in the VR5510 data sheet for more information.

Table 16. Interrupts registers

Registers (I^2C) Name	I^2C Section/Address	Registers (I^2C) Address	Comments
FS_INTB_MASK	Fail-safe, 0x21h	[0x17h]	To mask the interrupt related to all the OV, UV faults of the monitors, WD and the FCCU pins
M_INT_MASK1	Main, 0x20h	[0x0Ah]	To mask the interrupts related to OC and TSD flags of all the regulator
M_INT_MASK2	Main, 0x20h	[0x0Bh]	To mask the interrupts related to UVL and *UVH* flags of all the regulator

7.7 Configuring the SVS settings

- **PMIC_ConfigureSvs ()** – to configure Static Voltage Scaling settings. Refer to Section 22.2.6 in the VR5510 data sheet for configuring the SVS settings related to offset and the sign.

Table 17. SVS setting registers

Registers (I^2C) Name	I^2C Section/Address	Registers (I^2C) Address	Comments
M_LVB1_SVS	Main, 0x20h	[0x10h]	Read only register to get the SVS offset value of Buck1 set in failsafe register FS_I_SVS
M_LVB1_STBY_DVS	Main, 0x20h	[0x11h]	Buck1 output voltage in standby

7.8 Configuring the Watchdog settings

- **PMIC_Watchdog ()** – Configure the watchdog settings, feed the watchdog, and get the watchdog status.

Refer to Section 7.3 "Disabling Watchdog and FCCU monitoring" in this document and Section 22.4 in the VR5510 data sheet for configuring the safety-related watchdog settings during the INIT_FS phase.

Table 18. List of OTP bits

Register Address	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
[0x16h]	RW	0	1						
Bit Name		WD_DIS_OTP	WD_SELECTION_OTP						

Table 19. List of I^2C Watchdog registers

Registers (I^2C) Name	I^2C Section/Address	Registers (I^2C) Address	Comments
FS_WD_WINDOW_DUR	Fail-safe, 0x21h	[0x0Fh]	To configure the window, duty cycle and recovery settings of WD
FS_NOT_WD_WINDOW_DUR	Fail-safe, 0x21h	[0x10h]	Write opposite data of 0x0Fh
FS_WD_SEED	Fail-safe, 0x21h	[0x11h]	To read the default seed from the PMIC or write a new seed
FS_WD_ANSWER	Fail-safe, 0x21h	[0x12h]	To write the seed value during the open WD window for a good WD refresh

7.9 Releasing the FS0B pin

- **PMIC_ReleaseFS0B ()**

The FS_RELEASE_FS0B register must be filled with the current WD_SEED to successfully release the FS0B pin. The FS_RELEASE_FS0B register must be filled with the ongoing WD_SEED bit field (FS_WD_SEED register) reversed and complemented.

In addition, the fault counters must be cleared and the LBIST, ABIST checks must have passed.

Refer to the data sheet for more information.

Table 20. FS0B I^2C bits

Registers (I^2C) Name	I^2C Section/Address	Registers (I^2C) Address	Comments
FS_RELEASE_FS0B	Failsafe, 0x21h	[0x14h]	To release the FS0B pin

8 VPRE Stability Measurement

8.1 High-voltage BUCK VPRE

VPRE is the high-voltage, synchronous, peak current mode buck controller that uses an external N-CH MOSFET for the high side and low side.

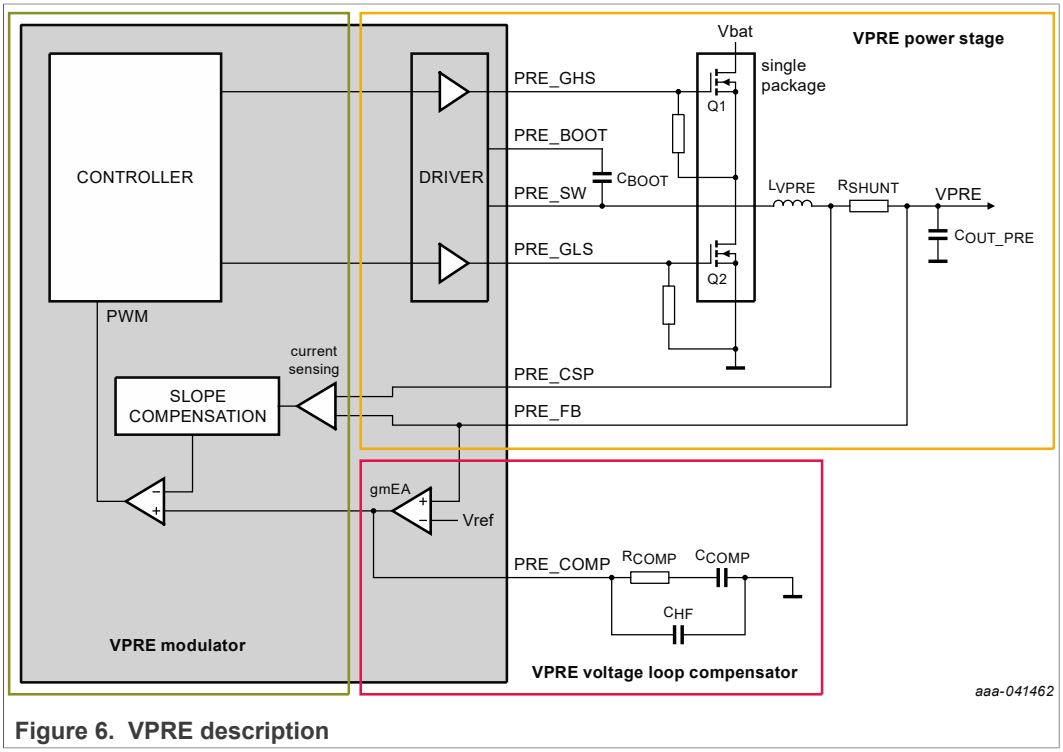

Figure 6. VPRE description

A current-mode regulation loop can be divided into three parts:

- The buck converter power stage includes the power stage of the buck converter
- The modulator creates the PWM using the current sense signal
- The voltage loop compensator ensures stability using the voltage feedback

8.2 Stability measurement method

The standard stability measurement method injects noise between the voltage feedback (PRE_FB) and the output voltage (VOUT) through a resistor. These measurements allow a Bode diagram to be traced in order to assess stability. Figure 7 shows the standard stability measurement setup.

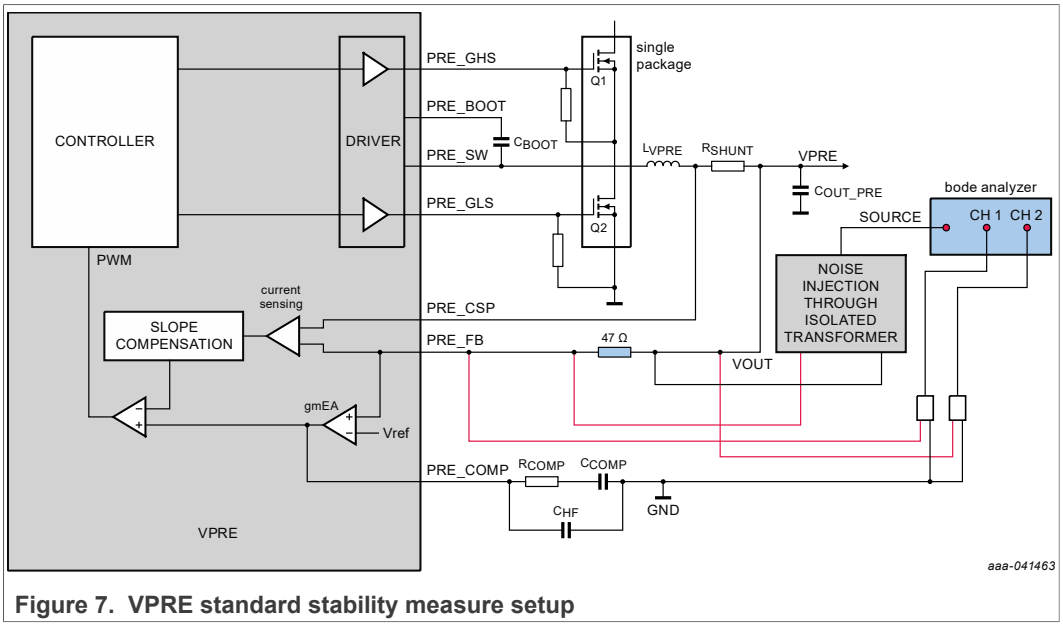

Figure 7. VPRE standard stability measure setup

Figure 8 shows the simulation results for the VPRE stability measurement.

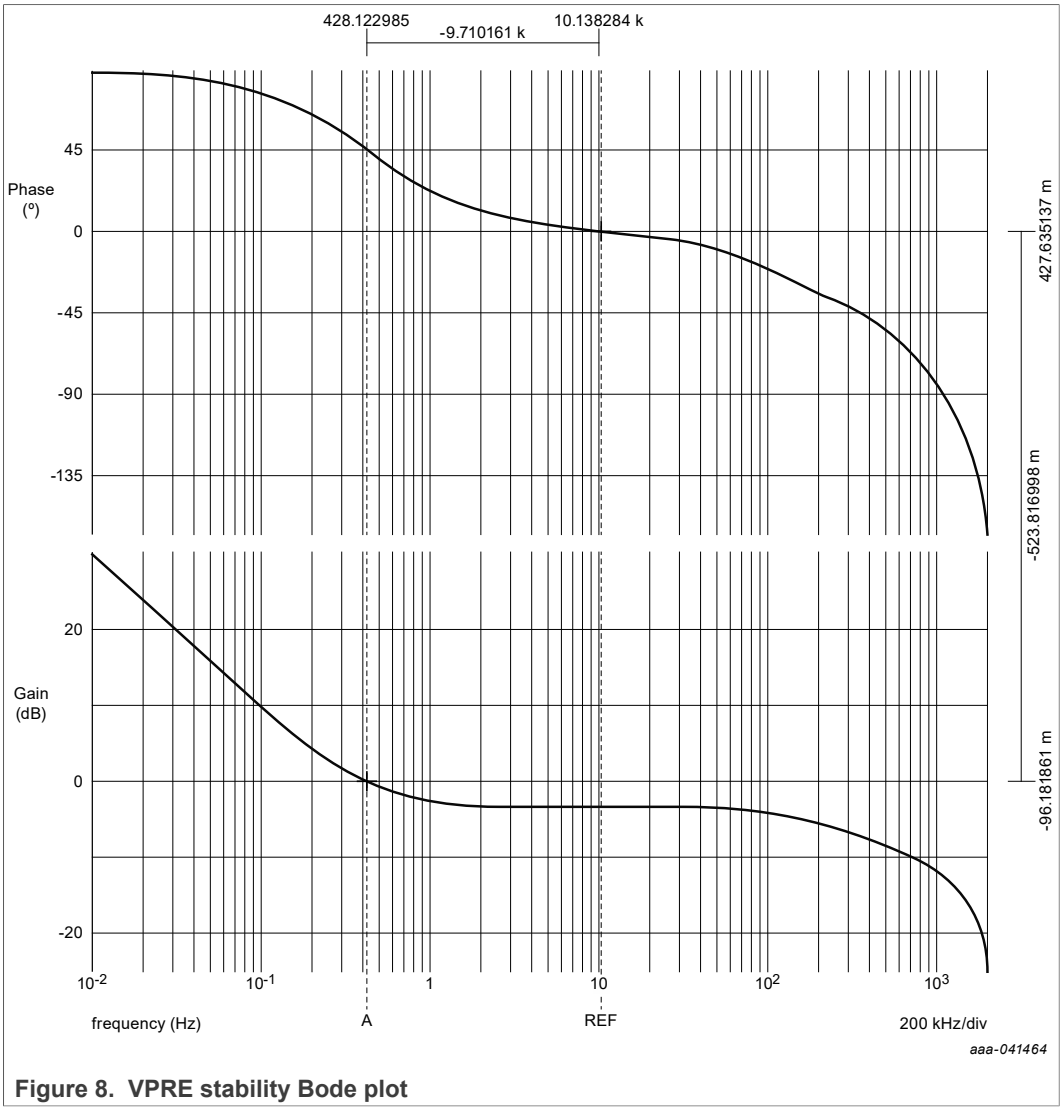

Figure 8. VPRE stability Bode plot

The standard stability measurement method does not work with the VR5510. During the integration of the HV BUCK controller in the VR5510 device, the feedback pin (PRE_FB) was merged with the negative current sense pin (PRE_CSN). Due to this integration, the noise injected in PRE_FB (voltage loop) is also injected into the current loop.

To overcome this limitation, split the measurements in two:

- Part 1 - The error amplifier measurement: injecting at PRE_FB and measuring at PRE_COM
- Part 2 - The power stage measurement: injecting at PRE_COMP and measuring at PRE_FB

The entire loop stability is obtained by adding both Bode plots.

8.2.1 Part 1 - Error amplifier part

The first measurement obtains the stability of the error amplifier part by injecting noise at PRE_FB and measuring at PRE_COMP (error amplifier output)

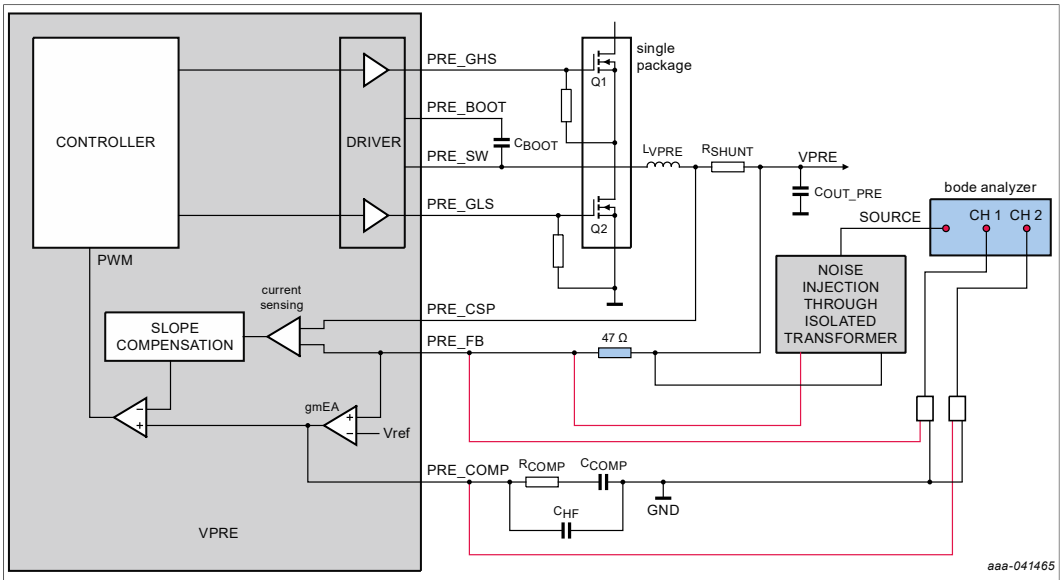

Figure 9. Error amplifier stability measurement setup

The noise is injected through a resistor at PRE_FB and the Bode analyzer monitors PRE_FB (input) and PRE_COMP (output).

The simulation result is shown in Figure 10.

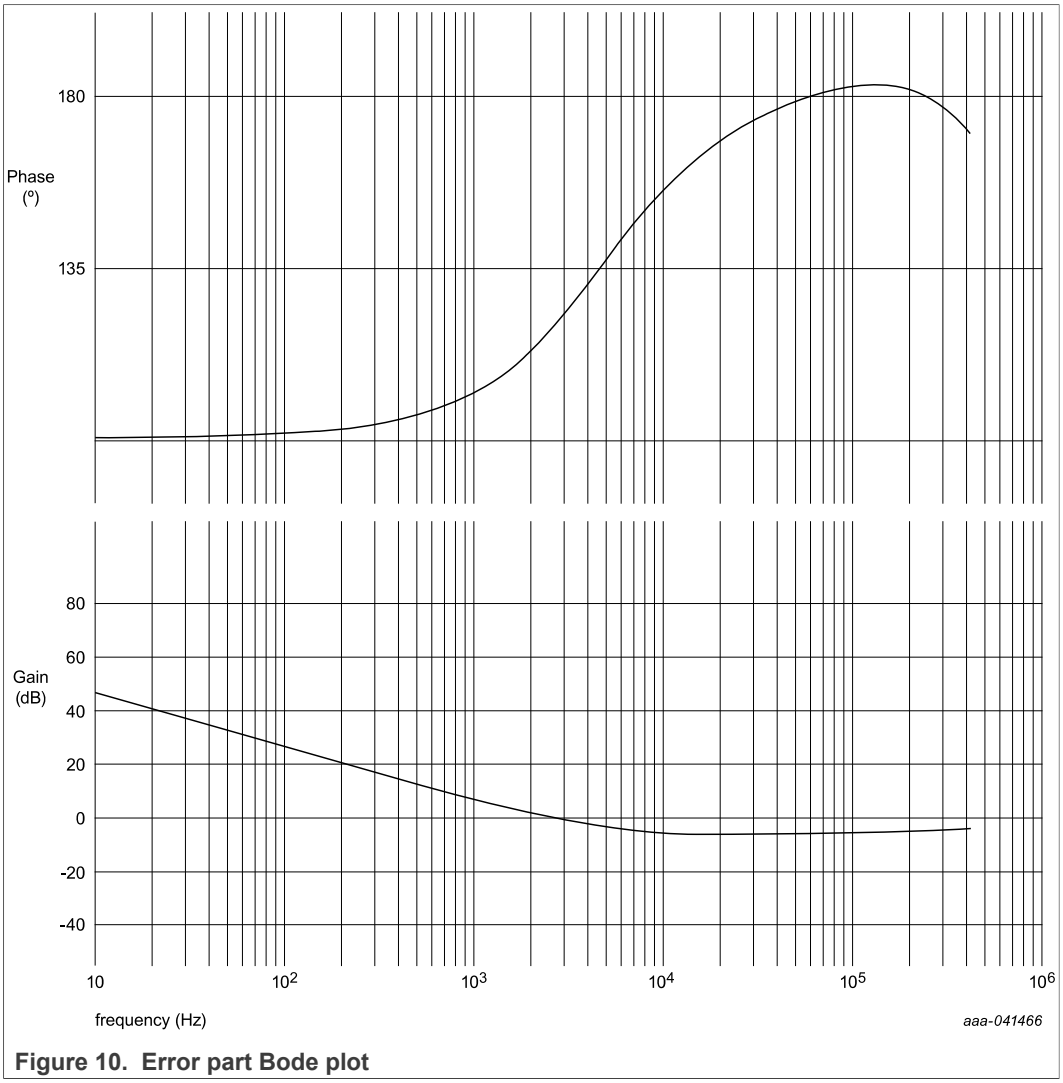

Figure 10. Error part Bode plot

8.2.2 Part 2 - Power stage part

The second measurement focuses on the power stage by injecting noise at PRE_COMP and measuring at PRE_FB.

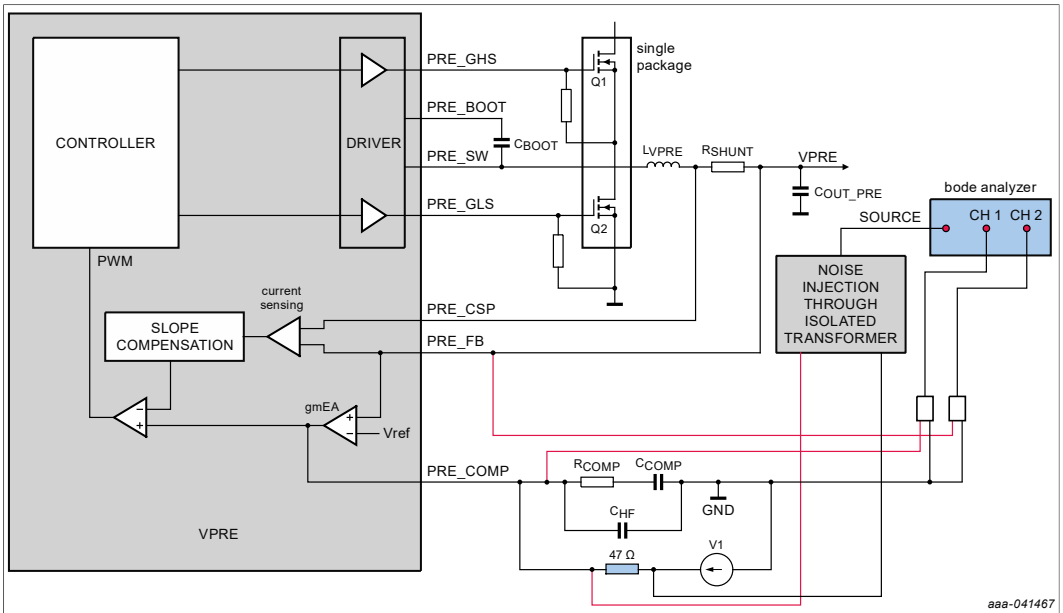

Figure 11. Power stage stability measurement setup

In this setup, the injection resistor cannot be placed in series with the compensation network. The voltage level of PRE_COMP must be maintained using a four-quadrant voltage source. Before creating the setup, PRE_COMP voltage must be measured as precisely as possible (no current leaving the supply). Then, the voltage source (V1=PRE_COMP) and the resistor must be placed in parallel. Try to have as little current as possible flowing in or out of PRE_COMP pin (<20 µA is a good target).

The simulation results are shown in Figure 12.

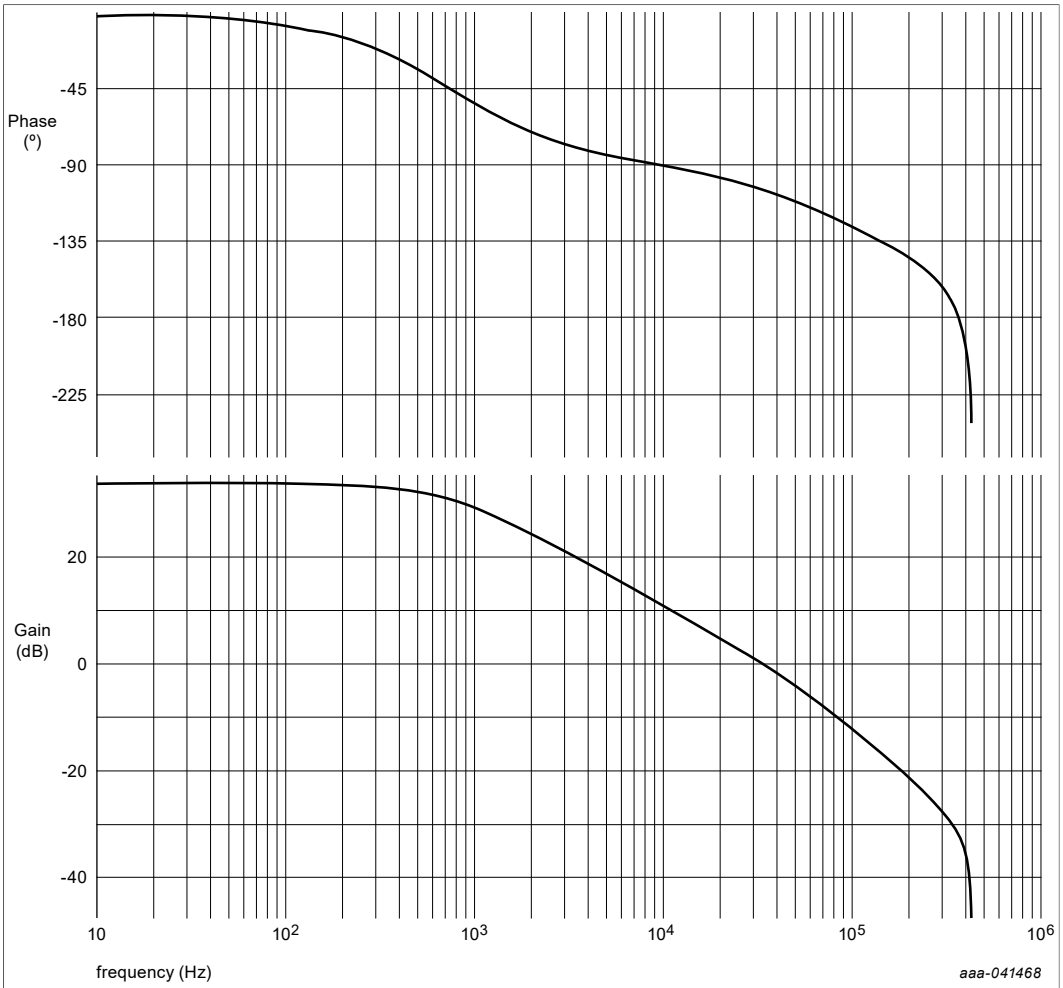

Figure 12. Power stage Bode plot

8.2.3 Part 3 – Complete VPRE stability

The entire loop bode plot is obtained adding the two Bode plots obtained from the error amplifier part and the power stage part. With the measurement tool, data can be exported to a spreadsheet (e.g. Excel), where the addition of gain and phase data can be done.

Gain = Gain-error + Gain-power

Phase = Phase-error + Phase-power

Figure 13 shows the curves of both stages and the two stages added together.

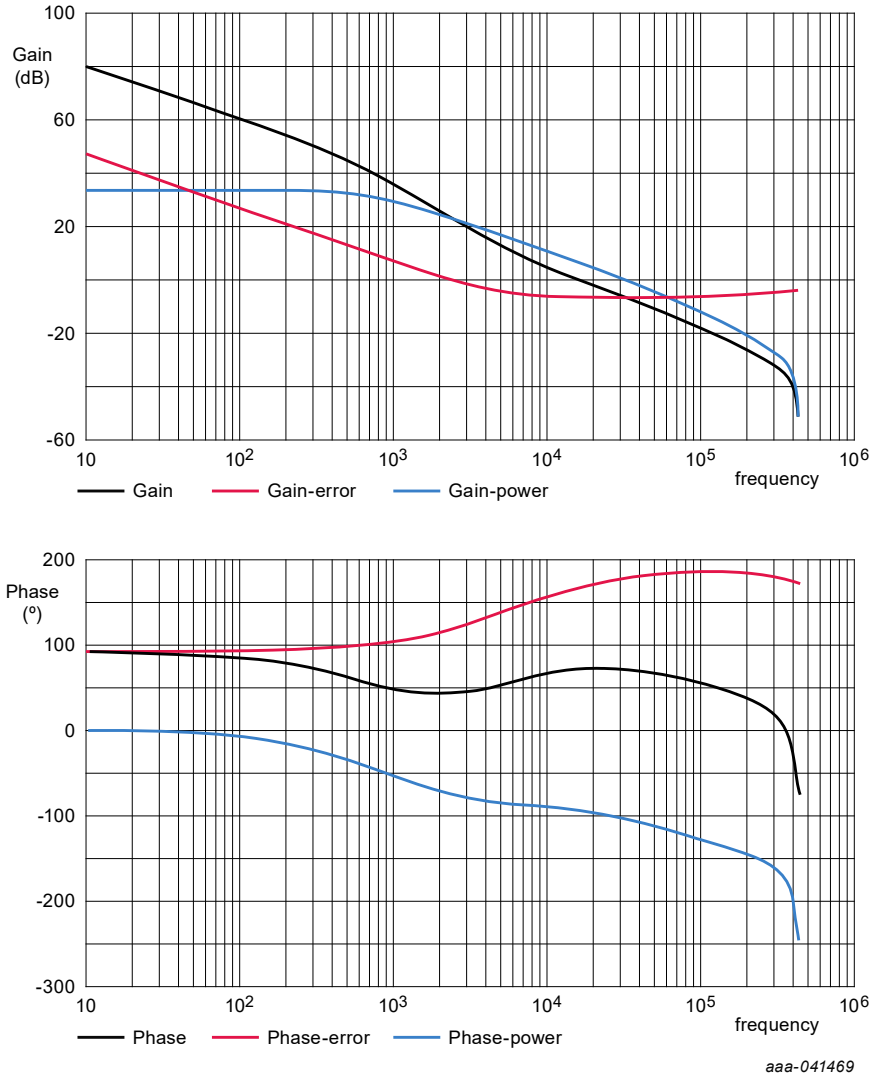

Figure 13. Addition of power stage and error stage Bode plots

The results of the addition of error and power part correlate with the VPRE stability Bode plot in simulation, separating the feedback pin (PRE_FB) and the negative current sense pin (PRE_CSN).

9 Hardware Design Guidelines

9.1 Schematic and BOM recommendations

9.1.1 High-voltage Buck VPRE

The high-voltage Buck VPRE requires several external elements. The VPRE recommended schematic is shown in Figure 14.

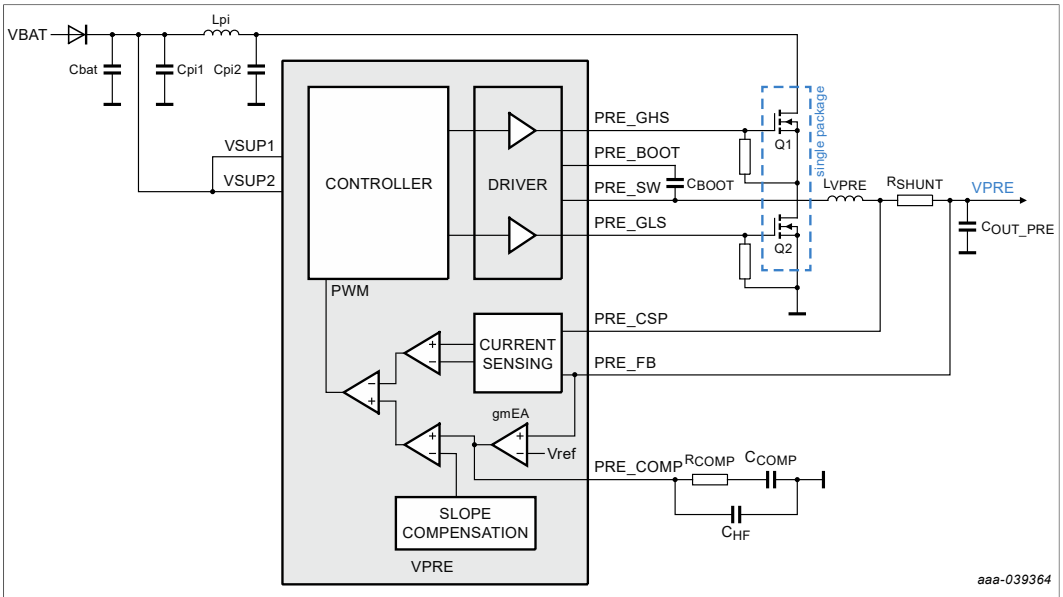

Figure 14. VPRE schematic

- The high-voltage Buck VPRE requires an external dual N-channel MOSFET. The selection of the MOSFET is based on the customer's application. Below there are some recommended external MOSFETS depending on the application parameters.
- the high-voltage Buck VPRE requires at least a typical value 47 µF, 50 V, 20% as input capacitance.
- The high-voltage Buck VPRE requires a typical effective output capacitor of 66 µF, 16 V, 20% X7R for 455 kHz switching frequency, and a typical effective value of 44 µF, 16 V, 20% X7R for 2.22 MHz switching frequency.
- The high-voltage Buck VPRE requires a typical inductor value of 4.7 µH for a switching frequency of 455 kHz and a typical inductor value of 1.5 µH for a switching frequency of 2.22 MHz.

Table 21. External MOSFET recommendations

Appli-cations	F_{PRE}	I_{PRE} < 2 A	I_{PRE} < 4 A	I_{PRE} < 6 A	I_{PRE} < 10 A
12 V	455 kHz	BUK9K25-40E BUCK9K18-40E	BUK9K25-40E BUCK9K18-40E	BUCK9K18-40E	BUCK9K18-40E NVTFS5C471NLWFTAG HS = BUK9M9R5-40H LS = BUK9M3R3-40H

Table 21. External MOSFET recommendations*...continued*

Appli-cations	F_{PRE}	I_{PRE} < 2 A	I_{PRE} < 4 A	I_{PRE} < 6 A	I_{PRE} < 10 A
	2.22 MHz	BUK9K25-40E BUK9Y29-40E	BUK9K25-40E BUK9Y29-40E	BUK9K25-40E BUK9Y29-40E	NA
24 V	455 kHz	BUK9K35-60E BUK9K52-60E	BUK9K35-60E BUK9K52-60E	BUK9K35-60E	BUK9K12-60E

Other MOSFETS can be used provided their performance is similar to that of the recommended parts.

- A bootstrap capacitor is required to supply the gate drive circuit of the high side NMOS. The bootstrap capacitor value should be >10 times the Gate Source capacitor, total Qg. Table 22 shows the calculated values for some of the recommended MOSFETs.

Table 22. Calculated values for recommended MOSFETs

MOSFET	C_{BOOT} (F) (Calculated)	C_{BOOT}min (F) (Recommended)	C_{BOOT}max (F) (Recommended)
BUK9K18-40E	3.33E-08	4.00E-08	6.67E-08
BUK9K25-40E	2.33E-08	2.80E-08	4.67E-08
BUK9K12-60E	8.00E-08	9.60E-08	1.60E-08
BUK9K35-60E	2.00E-08	2.40E-08	4.00E-08

- To guarantee a passive switching off of the transistors when a pin disconnection occurs, use gate-to-source resistors on Q1 and Q2, possibly in the 100 kΩ to 500 kΩ range.
- The output current is sensed via an external shunt in series with the inductor. The external shunt recommended value is 10 mΩ for 455 kHz and 20 mΩ for 2.2 MHz.
- A PI filter is required to filter the VPRE switching frequency on the Battery line. with $F_{RES} = 1 / [2\pi \times \sqrt{(LC)}]$ and calculated for F_{RES} < VPRE_FSW / 10
- An input capacitance of 300 pF is required on the battery line.
- The high-voltage Buck VPRE requires an external Type 2 compensation network with slope compensation to ensure stability.
- If VPRE is supplying regulators of external devices other than the VR5510, use a ferrite bead on the output line to limit the EMC perturbations.

9.1.2 Low-voltage BOOST

The low-voltage BOOST requires several external elements. The BOOST recommended schematic is shown in Figure 15.

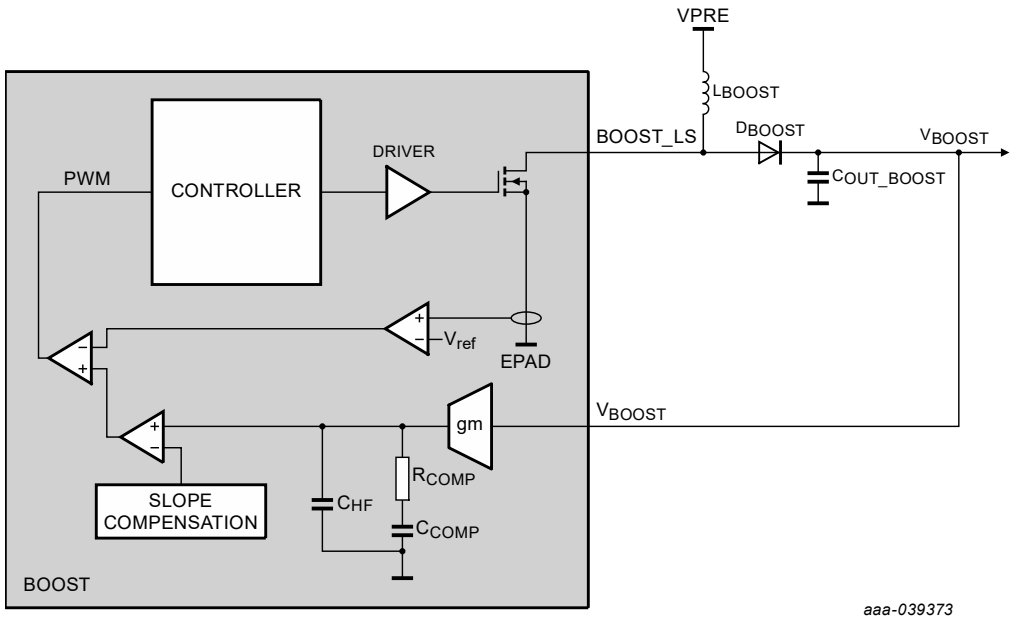

Figure 15. BOOST schematic

- Boost regulator requires a 4.7 µH@1 MHz, 2.2 A inductor to VPRE.
- Select a Schottky diode 2 A, 30 V for DBOOST to limit the impact on the SMPS efficiency.
- Boost regulator requires at least a typical value of 2 x 22 µF, 10 V, X6S as output capacitance connected to VBOOST pin.
- If BOOST is supplying regulators of external devices other than the VR5510, use a ferrite bead on the output line to limit the EMC perturbations.

9.1.3 LVBUCK

The low-voltage BUCK converters require several external elements. The BUCK recommended schematic is shown in Figure 16.

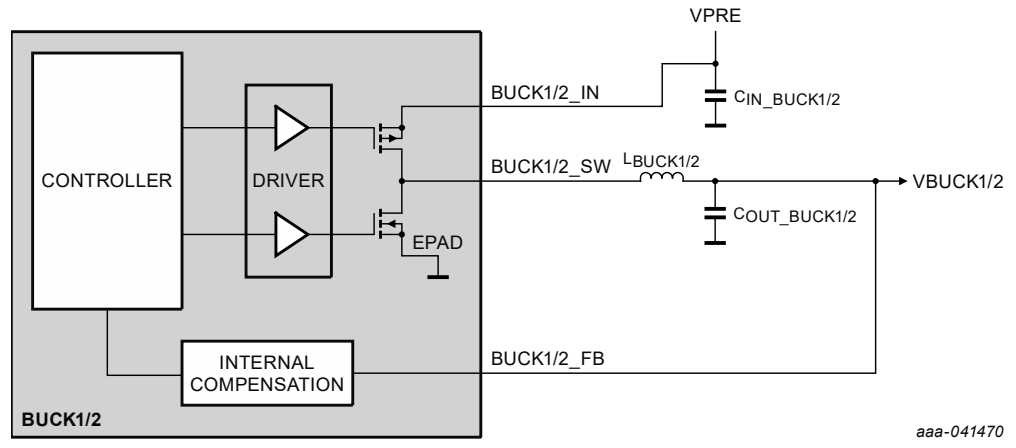

Figure 16. BUCK1/2 schematic

- Low voltage buck converters need an effective input capacitor of typical value 4.7 µF, 50 V, X7R (one each close to BUCKX_IN pin)

- The low voltage buck converters require at least 1 × 1 µH inductor per regulator at the SWxIN pin as input capacitance. The DC resistance (DCR) and the saturation current specification of the inductor can be optimized based on the application requirements.
- Low voltage buck converters require at least typical value 2 x 22 µF, 10 V, X6S capacitor per regulator as output capacitance connected to the inductor.
- In addition to the above capacitors, 1 × 0.1 µF typical value capacitor can be added as bypass capacitor at the input and output pins of the regulators. This capacitor is optional and can be added mainly to improve the noise and/or electromagnetic interference (EMI) performance.

9.1.4 LDO1 regulator

The medium voltage linear regulator LDO1 requires several external elements. The LDO1 recommended schematic is shown in Figure 17.

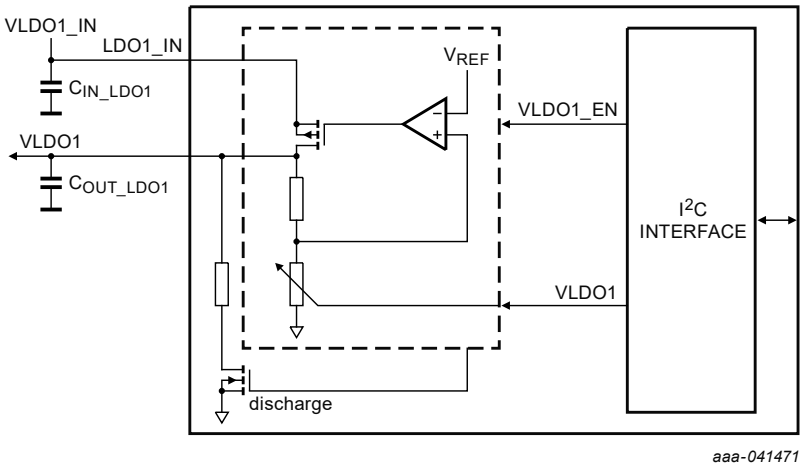

Figure 17. LDO1 schematic

- The low dropout (LDO) regulator requires at least typical value 1 × 1 µF, 16 V or 10 V, X7R capacitor at the LDO1IN pin as input capacitance. This capacitor should be connected next to the input pin.
- The LDO1 regulator requires a typical value 4.7 µF capacitor for 150 mA output current capability and 6.8 µF capacitor for 400 mA capability as output capacitance connected to the LDO1OUT pin.

9.1.5 LDO2,3 regulators

The linear voltage regulators LDO2 and LDO3 require several external elements. The LDO2/3 recommended schematic is shown in Figure 18.

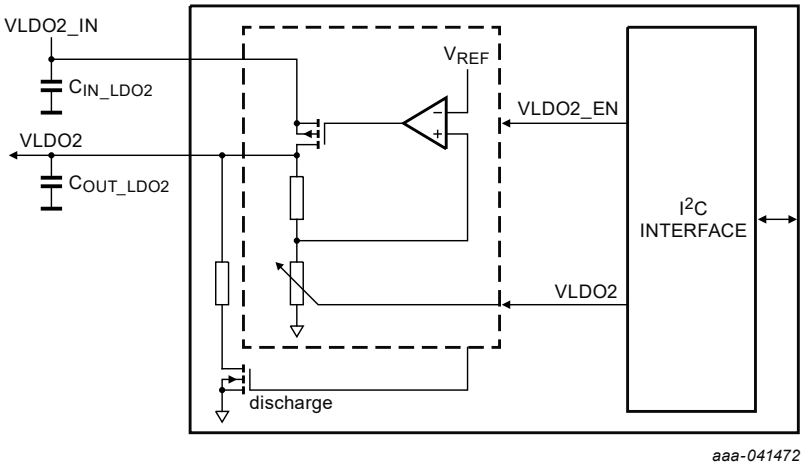

Figure 18. LDO2/3 schematic

- The low dropout (LDO) regulator requires at least typical value 1 × 1 µF, 16 V or 10 V, X7R capacitor at the LDO1IN pin as input capacitance.
- The LDO regulator requires at least typical value 1 × 4.7 µF, 10 V, X7R capacitor as output capacitance connected to the LDOXOUT pin.
- In addition to the above capacitors, 1 × 0.1 µF typical value capacitor can be added as bypass capacitor at the input and output pins of the regulators. This capacitor is optional and can be added mainly to improve the noise and/or electromagnetic interference (EMI) performance.

9.1.6 High-voltage LDO

The high-voltage, low-power, low drop-out linear regulator HVLDO requires several external elements. The HVLDO recommended schematic is shown in Figure 19.

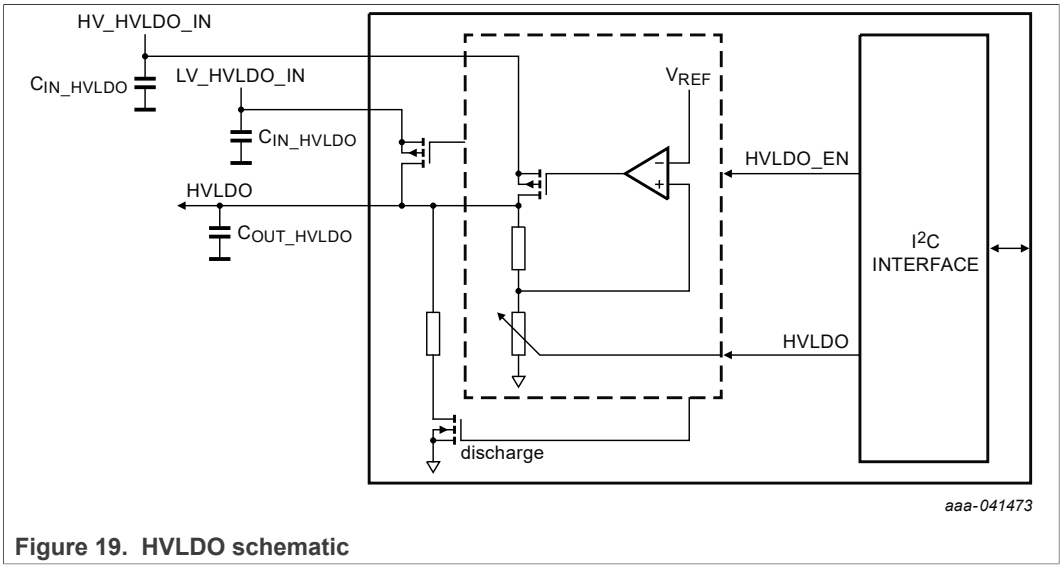

Figure 19. HVLDO schematic

- HV_HVLDO_IN must be connected to either VPRE or VBAT and LV_HVLDO_IN can be connected to either VBUCK1/2 or VPRE.
- Both input pins require a typical value 1µF, 50 V, X7R as input capacitance connected to HV_HVLDO_IN and LV_HVLDO_IN.

- HVLDO requires a typical value 4.7 µF, 16 V, X7R capacitor as output capacitance connected to the HVLDO pin.

9.1.7 VDIG, VANA, VDDIO

- Pins VDIG, VANA, VDDIO require at least typical value 1 x 1 µF, 16 V, X6S capacitor at each output.

9.1.8 Voltage monitors

- VCOREMON must be connected to S32G CORE supply (BUCK12 regulator). This pin should be connected next to the processor input supply to avoid a voltage drop.
- VDDIO must be connected to S32G IO supply (LDO3 regulator). The regulator connected to VDDIO must be at 1.8 V or 3.3 V.
- VMONx input pins can be connected to VPRE, LDO1, LDO2, LDO3, BUCK1, BUCK2, BUCK3, BOOST, or to an external regulator. An external resistor bridge is required to deliver a 0.8 V midpoint on the monitoring input pin. Use ± 0.1% or less resistor accuracy. For the S32G application:
  - VMON1 monitors LDO2 regulator
  - VMON2 is used to monitor BUCK3 regulator
  - VMON3 monitors VPRE regulator
  - VMON4 is used to monitor LDO1 regulator

Refer to AN13118- S32G VR5510 Safety Concept application note for more details about the monitoring connections.

9.2 PCB guidelines

9.2.1 LVBUCKs

- As a rule, all the components related to the switching regulators (SWx) must be placed close to the regulators and connected to the pins with short, wide traces wherever necessary.
- All input capacitors including the bypass capacitors can be placed either on the top side or bottom of the board. However, it is important that they are placed close to the PMIC between the SWxIN pin and either the EPAD or the closest GND plane on the board. This connection is important to ensure that the parasitic inductance in this input current path is minimized and the current loop is made shorter.
- All output capacitors must be placed close to the IC but also at an optimum location from the load. The output capacitors must be provided with sufficient thermal vias to the GND plane.
- SWxFB pins must be connected to thin traces that are taken from close to the output capacitors and must be routed on one of the inner signal layers to shield from outside noise. In a multiphase configuration, connect all the feedback pins together.
- In the S32G application SW12FB can be connected directly to the PMIC_SENSE input of the S32G processor.
- The trace that connects the SWxLX pin and the output inductor is a critical power trace which must always be routed as short and wide as possible to minimize the power loss.
- For multiphase configurations, make sure that all the recommendations are followed symmetrically between all the regulators.

- The inductor charging and discharging current loop must be designed as small as possible:

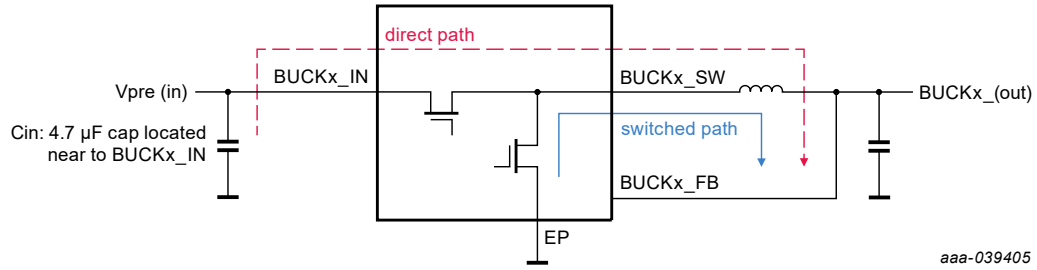

Figure 20. LVBUCKS PCB guidelines

9.2.2 VPRE

- The inductor charging and discharging current loop must be designed as small as possible.
- Input decoupling capacitors must be placed close to the high-side drain transistor pin.
- The boot strap capacitor must be placed close to the device pin using a wide and short track to connect to the external low-side drain transistor.
- PRE_GLS, PRE_GHS and PRE_SW tracks must be wide and short and should not cross any sensitive signals (current sensing, for example).
- PRE_FB used as voltage feedback AND current sense must be connected to RSHUNT and routed as a pair with CSP.

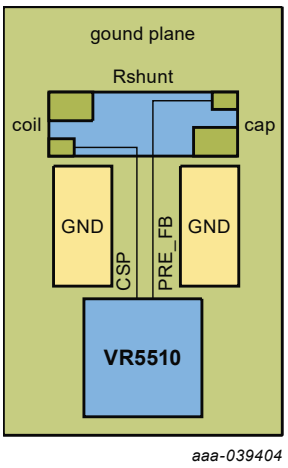

Figure 21. VPRE PCB guidelines

- The external transistor thermal shape should be in the range of 25 x 25 mm for optimum Rth.
- See LFPAK56 application note for more details: http://assets.nexperia.com/documents/application-note/AN10874.pdf

9.2.3 LDO regulators

- The LDO regulator does not have many external components except for the input and the output capacitor.
- Place these capacitors as close as possible to the PMIC.

9.2.4 LV BOOST

- Place the output capacitor as close as possible to the VBOOST pin.

10 Revision History

Table 23. Revision history

Revision	Date	Description
v.1	20210503	Initial Release
Modifications	NA	

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