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DesignWare OTP NVM IP

COMPONENT DESCRIPTION: DWC NVM OTP TSMC 180nm BCDG2 5.0V

COMPONENT NAME: dwc_nvm_ts18u71sxxxxpbnopxxxq

PRODUCT CODE: C959-0

ARCHITECTURE: SLP_B

CONFIGURATION: 256 x 16 OTP Core

CONFIGURATION METAL LAYERS: M4 is UTM

MACRO NAME: slp_b_tsmc180bcd50_256x16_cm16s_eb

PROCESS: TSMC 180nm BCD50 (1.8V Core, 5.0V I/O)

QUALIFIED FABS: 5,6,8

DATABOOK VERSION: D1.0B1.5T2.5

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The SLP macrocells are embedded non-volatile memory (NVM) IP cores providing one-time programmable (OTP) solutions in a standard high voltage 180nm CMOS process. These macrocells are intended for use in consumer products and similar applications.

Synopsys OTP products are compatible with a wide variety of 180nm processes and are portable down to 65nm and beyond.

Synopsys OTP solutions target area and power efficient electrical fuse replacement for secure key storage, medical, wireless or RFID applications, and provide a field programmable alternative for mask ROM and external flash memory devices. Please note custom logic operations are required, see the waiver document for details.

This databook describes the functionality and characteristics of the slp_b_tsmc180bcd50_256x16_cm16s_eb macro in TSMC 180nm BCD50 CMOS process addressing a wide range of embedded NVM needs.

SLP_B Family Features

- Standard CMOS Logic Process
- Densities up to 256Kbits per Macro
- I/O Widths up to 32bits per Macro
- Ultra Low Active and Stand-by Power
- Very Small Silicon Area Footprint
- Wide Storage Temperature Range
- Wide Operating Temperature Range
- Wide Supply Voltage Operating Range
- Built-in Differential and Redundant Read Modes
- Optional Integrated Power Supply with Charge Pump for Field Programming
- Exceeds 10 Years of Data Retention
- Highly Secure

Deliverables

- Databooks
- Design Models (Verilog, .LIB)
- Hard Macro Placement File in LEF format
- GDSII
- LVS netlist
- Design Integration and Application Notes available upon Request

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1. SLP_B Overview

The Synopsys SLP_B Low Power One-Time Programmable Memory design is based on a patented split-channel non-volatile antifuse memory cell and is optimized for very low power consumption. The CMOS-only design is internally architected such that a minimum of circuitry switches during each read cycle.

The design is made modular with row increments in multiples of 16 and column increments in multiples of 4. The maximum bit count is 256Kbits per macro and maximum word width is 128bits. The macrocell aspect ratio is controlled by a column multiplexer with allowed values of 4:1, 8:1 and 16:1. Multiple macrocells can be combined into larger memory modules. The built-in tri-state data outputs minimize multiplexing overhead.

Apart from the standard digital core supply (VDD), two additional voltage levels are required: a programming voltage (VPP) and a read supply voltage (VRR). These voltages can be supplied externally or generated with the optional Synopsys Integrated Power Supply macro.

Synopsys Low Power OTP designs macros are available in many configurations and process nodes. All SLP macrocells share the same basic functionality and access interface, but differ in internal memory organization, supply voltage level and manufacturing process details.

This document summarizes the key features and characteristics of the slp_b_tsmc180bcd50_256x16_cm16s_eb macrocell implemented in TSMC 180nm BCD50

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CONFIGURATION SUMMARY - SLP_B_TSMC180BCD50_256X16_CM16S_EB

Table 1-1. Configuration Summary					
Parameter	**Supply**	**Min[1]**	**Typ**	**Max[1]**	**Units**
General					
Process Node	TSMC 180nm BCD50 1.8/5.0 V				
Configuration Metal Layers	M4 is UTM				
Memory size	4k				
I/O Bus width (n)	16 bits				
Organization S x R x CM x bits	1 arrays x 16 rows x 16 Column Mux x 16 bits				
	256 words x 16 bits (Single Cell Mode)				
Number of Arrays	1				
Address Bus width	8				
Area	X = 352.49µm x Y = 92.18µm Area = 0.032mm^2				
Retention		10			Years
Power Supply	VDD	1.62	1.8	1.98	V
Current (Standby)	VDD		0.08	5.5	µA
Power Supply	VRR	2.7	3.0	3.3	V
Current (Standby)	VRR		0.01	0.4	µA
Program (Single Bit)					
Power Supply	VPP	7.9	8.15	8.4	V
Current[2]	VPP		250		µA
Time			100		µs/bit
Temperature Range		-40	+25	+125	°C
Read (Single ended, 16 Bits)					
Current (not including standby)	VDD	5.7	6.9	8.6	µA/MHz
Current (not including standby)	VRR	1.6	2.2	3	µA/MHz
Temperature Range		-40	+25	+150	°C
Storage					
Temperature Range		-55	+25	+150	°C

[1]: Across the conditions described in Corner Conditions on page 18.
[2]: One bit at a time programming.

2. Functional Description

Figure 2-1. SLP_B 180nm OTP Macrocell Block Diagram (shown with optional Synopsys Integrated Power Supply Block)

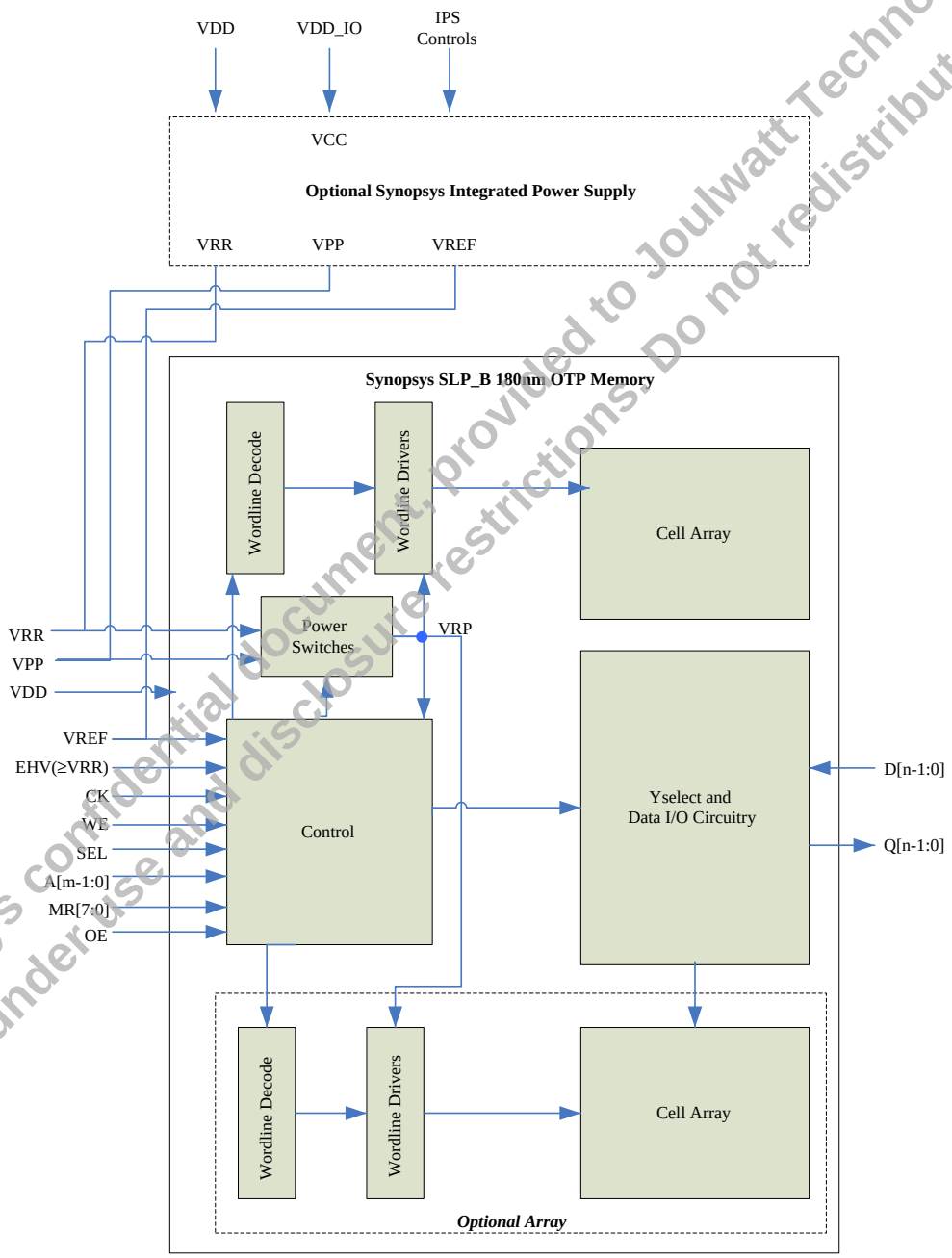

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Figure 2-1 on page 7 shows a block diagram for the SLP_B macro. Inputs and outputs are in the VDD voltage domain, except for EHV which should be generated in the VDD_IO domain. VRR (ReadV) and VPP (ProgV) are provided to a Power Switch Block within the macrocell. During standby and read cycles, VRR is switched onto an internal voltage supply, VRP. During program cycles, VPP is switched onto the internal VRP voltage supply. The internal VRP voltage supply is used in the wordline drivers and for some control circuitry.

The macro select (SEL), write enable (WE), data input (D[15:0]) and address (A[7:0]) signals are latched on the rising edge of CK. In a read cycle, the outputs (Q[15:0]) become valid on the falling edge of CK. Different read modes and other test modes can be selected via the mode select signals, MR[7:0]. Note that the The MR[7:0] pins are not latched - and so the proper values must always be supplied to the macrocell. The OE signal allows the data outputs to be tristated.

The SLP_B macrocell is available in single array or dual array configurations. The bottom circuitry shown in Figure 2-1 on page 7 is only included in dual array macrocells. Dual array configurations are required if differential read operationsare to be used.

The VRR and VPP voltages can be supplied from pins, from a user designed voltage generator or from a separate Synopsys supplied Integrated Power Supply macrocell.

3. Memory Operation

The memory has a simple dual clock edge interface where address, data inputs, write enable, and select lines are latched at the rising clock edge, and the output data become valid following the falling clock edge.

3-1. Read Cycle

A read cycle to the addressed word is initiated on the rising edge of the clock, CK, when the WE input is low and the memory select input, SEL is high. The address A[7:0], WE and SEL are latched at the rising edge of CK. The data outputs, Q[15:0], become valid following the subsequent falling edge of CK. If an output data bit does not change state during a read operation, there is no intermediate transition at the output during the access time. OE high activates the output buffers. All outputs remain tri-stated (high impedance) when OE is low.

The read supply voltage VRR sets the active wordline voltage level and is required for correct read operation. The programming voltage, VPP, is not needed during read operations and may be held at any level between 0V and chip IO supply.

In order to minimize idle and read power consumption, the amount of address and SEL switching should be minimized and the WE should be kept low at all times.

The memory array is organized in rows and columns where each DATA IO bit is assigned to 4, 8 or 16 columns. The memory array is further subdivided into sectors with local bit lines and row decoders. The sector size is optimized for power consumption and is fixed. The memory array can be built in increments of 16 rows and 8 columns.

Read Modes: Single-Ended and Redundant

By default, the OTP macrocells are read in single-ended mode utilizing one memory cell per logical bit of information.

In single-ended read mode, the memory cell is compared to a reference to determine its state. The read mode is controlled by the mode pins MR[7:0] and can be dynamically changed for different sections of the address space. Note that the MR[7:0] pins are not latched and the proper values must always be supplied to the macrocell. This memory configuration is addressed by A[7:0] in single-ended read mode.

One additional read mode is provided for enhanced margins and data security needed for highly reliable, field programmable systems: redundant read mode.

In redundant read mode (MR[4]=1), two memory cells are accessed in parallel and compared to a reference, which doubles the signal margin. In redundant read mode, the memory configuration is addressed by A[7:7,5:0]. Bit A[6] is ignored during read but is used during program and verify operations.

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3-2. Write (Programming) Cycle

All memory cells in the macro are initially manufactured as "0"s and their state may be changed from a "0" to a "1" using the write (program) operation. Once programmed, it is not possible to reverse a "1" to a "0".

Programming is done one cell at a time. If an attempt to program multiple cells at a time is made, the first cell to break will collapse the VPP voltage and result in insufficient voltage available to program the remaining cells.

During program operation the "1"s in the data input word, D[15:0], are "burned" into the addressed memory location. "0"s in the data input word mask programming in the corresponding bit locations. The bits already programmed should be masked by "0"s in the input word. Any attempt to program an already programmed bit increases VPP power consumption preventing other bits from being programmed. During a program operation, the data outputs Q[15:0] do not change state from their last value.

Memory cells are programmed by gate oxide breakdown while selectively exposed to the elevated programming voltage level on VPP. A write cycle begins by precharging the internal circuitry to the programming VPP level when both WE and SEL are brought high and the clock, CK, is low. The programming voltage VPP should be applied to the macro prior to WE and SEL activation and must be maintained for the duration of the programming pulse.

The VPP level should be maintained between VRR + 0.5V and VPPmax when WE and SEL are high. However, if the programming voltage is generated by an un-regulated charge pump, the charge pump should be started after the WE and SEL are activated and should be switched off before WE or SEL removed. This sequence assures a minimum load on the charge pump to prevent VPP from overshooting above VPPmax.

A programming pulse to the addressed memory location is initiated on the rising edge of CK, when the WE input is high and the memory select input, SEL is high. The address inputs A[7:0], data inputs D[15:0], WE and SEL are latched by the rising edge of CK. A high input level on a data input D[i] will cause that bit to be programmed in the selected word. A CK low transition ends the programming pulse.

During sequential programming of single bits in the selected address location, the WE and SEL signals should be kept high between the programming pulses to ensure the VPP voltage level is maintained in the internal circuitry, minimizing power dissipation and internal voltage switching. VPP should only be removed when CK and WE (and/or SEL) are low. VRR should be maintained at the default voltage level during the entire program cycle.

3-3. Deselected Cycle

To prevent a read or write operation from occurring in the presence of a continuously running clock, or to prevent power dissipation from the switching address bus, the select input SEL should be held low when the macro is not being accessed. When the macro is deselected, no read or write operations are performed and the address and data bus states are ignored. The programming voltage (VPP) and the read supply voltage (VRR) are also not required during these cycles. VPP can be held at any level between 0V and VRRMax.

3-4. Power Sequencing

The EHV pin allows some options for the power sequencing. When EHV is low (VSS), the internal VRR and VPP power switches are turned off, the SEL latch is forced to the unselected state and the macro is put in a low power state. To enable the macro, set EHV high (≥VRR). CK must be low for the value on the SEL pin to take effect. It is expected that the EHV input would normally be generated in the VDD_IO (chip IO voltage) domain where VDD_IO≥VRR. If EHV is not used it should be tied to VDD_IO.

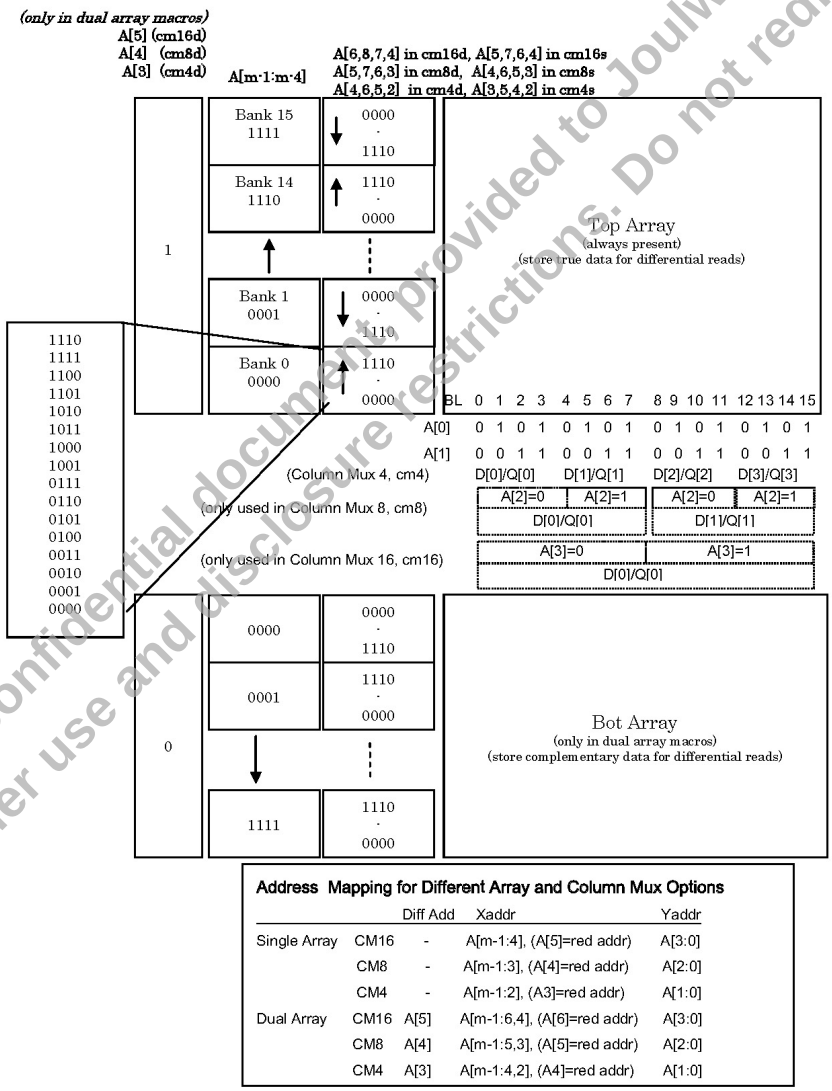
When EHV is low, there is no power sequence requirement between VDD and VRR. Set EHV high when VDD is stable. To power down, either set EHV low prior to removing supplies, or remove VDD and VRR simultaneously. If EHV is tied high, VRR must be applied after VDD and removed prior to, or simultaneously with, VDD.

VPP must be applied after VRR and removed prior to, or simultaneously with, VRR. VPP must not exceed VDD_IO when EHV=0. A delay of tVPPS is required after applying VPP before performing a program operation. An initial pause of tVRRS is required following the application of the VDD and VRR supplies before performing an operation. It is recommended that all other inputs be held at VSS during this period to block the clock and minimize activity associated with other signal inputs. The VPP delay is specified in Table 6-7 on page 19.

3-5. SLP_B Address Map

The address map for the SLP_B macro is shown in Figure 3-1 on page 11.

Figure 3-1. SLP_B Address Map



4. Functional Truth Tables

Table 4-1. Functional Truth Table - Memory and Data Register Access Commands

Function	Pin						
	CK	SEL	WE	D[15:0]	A[7:0]	OE	Q[15:0]
IDLE	X	L	X	X	X	L / H	Z / Vx
PROGRAM	L->H->L	H	H	V	V	L / H	Z / Vx
VPP PRECHARGE	L	H	H	X	X	L / H	Z / Vx
READ	L->H->L	H	L	X	V	L / H	Z/Vx->V

L = logic LOW H = logic HIGH V = Valid Z = Tri-state
Vx = Last Data Valid X = 'Don't Care'

5. SLP_B Power Supplies

In addition to digital core supply voltage (VDD), the SLP_B macros require two analog voltage supplies: read voltage VRR and program voltage VPP.

Synopsys offers an Integrated Power Supply macro specifically designed for operation with SLP_B macrocells. The Synopsys Integrated Power Supply is configurable and can contain various combinations of three components: a VPP Charge Pump module, VRR Voltage Regulator module and VDD Doubler module.

5-1. VPP Supply Voltage

A boosted VPP supply voltage is required for programming the macrocells. The VPP voltage can be supplied externally through a VPP pin or can be supplied by the Synopsys Integrated Power Supply macro containing a VPP Charge Pump module.

The Synopsys Integrated Power Supply allows the SLP_B macrocell to be programmed in the field using the standard IO supply (VDD_IO) after the chip has been packaged. The VPP Charge Pump module includes secondary ESD protection on the VPP port facilitating connection to the external VPP pad. The charge pump setup and activation is through the Synopsys Integrated Power Supply control pins.

5-2. VRR Supply Voltage

A regulated VRR voltage supply is required for read operations of the SLP_B macrocells. The read voltage VRR can be supplied externally through a VRR pin or can be supplied by the Synopsys Integrated Power Supply macro containing a VRR Voltage Regulator module.

The Synopsys Integrated Power Supply generates VRR from an external IO supply voltage (VDD_IO) through a step down regulation. The VRR Voltage Regulator module is adjustable through the Integrated Power Supply control pins. An additional VREF output is provided for read verify and sense margin tests.

5-3. VREF Supply Voltage

A regulated reference voltage supply (VREF) is available for characterization purposes. The VREF pin is internally pulled up to VDD. The internal pull-up can be disabled by MR[6]=1, which allows the VREF voltage level to be supplied externally.

6. OTP Macro Characteristics

Table 6-1. Macrocell Configuration	
Configuration	**Per Macrocell**
Memory size	4k
I/O Bus width (n)	16 bits
Organization S x R x CM x bits	1 sectors x 16 rows x 16 Column MUX x 16 bits
Organization	256 words x 16 bits (Single Cell Mode)
	128 words x 16 bits (Redundant Mode)
Number of Arrays	1
Address Bus width	8
Configuration Metal Layers	M4 is UTM

Process	**Standard Logic CMOS**
Name	TSMC 180nm BCD50 1.8/5.0 V
Process Metal Layers	4
VDD	1.8V ± 10%
VDD_IO	5.0V ± 10%

Physical Dimensions	
Actual	X = 352.49µm x Y = 92.18µm; Area = 0.032mm^2

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6-1. Pin Descriptions

(VSS to VDD level) are latched on the rising edge of CK and are held until CK is low. The MR pins are not latched and the proper value must always be supplied to the macrocell.

Table 6-2. Pin Descriptions

Pin	Usage	Direction	Default Level	Description
VDD	Power	Inout	VDD_CORE	Control logic and macro IO supply
VSS	Ground	Inout	0V	Ground / Substrate
VPP	Analog	Inout	Programming Voltage	ProgV (program supply voltage)
VRR	Analog	Inout	Read Voltage	ReadV (read supply voltage)
VREF	Analog	Inout	Analog Input	Test input for sense amp characterization (VSS < VREF < VDD)
EHV	Digital	Input	Active HIGH	Enable High Voltage Circuitry. A '1' indicates that VDD is in the specified voltage range. A logic '1' level for EHV can be any voltage between VRR and the chip IO voltage.
A[7:0]	Digital	Input		Program/Read Address inputs
D[15:0]	Digital	Input		Program Data inputs
MR[7:0]	Digital	Input	Active HIGH	Read and Test mode control pins (see Table 9-1 on page 29).
WE	Digital	Input	Active HIGH	Program command pin
SEL	Digital	Input	Active HIGH	Macro Select
CK	Digital	Input	Active HIGH	Address/Data/Command Strobe
OE	Digital	Input	Active HIGH	Output Enable. OE=1: data output; OE=0: data output HiZ
Q[15:0]	Digital	Output		Data outputs

Table 6-3. Absolute Maximum Ratings

VPP	-0.50V to 8.4V
VRR	-0.5V to VDDIO_MAX
VDD	-0.5V to VDD_COREMAX
DC Voltage on any other pin	-0.50V to VDD + 0.50 V
Storage Temperature	-55°C ≤ Tj ≤ +150°C

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6-2. Functional Truth Table

Table 6-4. Functional Truth Table - Memory and Data Register Access Commands

	Pin						
Function	**CK**	**SEL**	**WE**	**D[15:0]**	**A[7:0]**	**OE**	**Q[15:0]**
IDLE	X	L	X	X	X	L / H	Z / Vx
PROGRAM	L->H->L	H	H	V	V	L / H	Z / Vx
VPP PRECHARGE	L	H	H	X	X	L / H	Z / Vx
READ	L->H->L	H	L	X	V	L / H	Z/Vx->V

L = Logic low (0) H = Logic high (1) X = Don't care (0 or 1)
V = Valid Z = Tri-state Vx = Last Data Valid

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Table 6-5. Pin Capacitances

Pin	Input Pin Capacitance		Max Output Cap Load	Unit
	Read Operation	Write Operation		
VDD	10	7		pF
VRR	3	2		pF
VPP	1	2		pF
VREF (MR[6]=0)	38			fF
EHV	29.4			fF
OE	15			fF
CK	9.5			fF
WE	2.6			fF
SEL	8.4			fF
A	6.7			fF
D	2.1			fF
MR	18.5			fF
Q[15:0]			300	fF

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6-3. Corner Conditions

The table in this section describes the conditions used to determine the minimum, typical, and maximum parameter values. Any additional supply voltages not listed in the table were simulated at the edges of their range and the maximum value obtained for each parameter recorded in this Databook.

Table 6-6. Corner Conditions

Process	VDD [V]	VRR [V]	Temperature [°C]
TT	1.8	3	25
FF	1.98	3.3	150
FF	1.98	3.3	-40
SS	1.62	2.7	150
SS	1.62	2.7	-40

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6-4. AC Characteristics

Table 6-7. AC Characteristics: Program				
Description	**Symbol**	**Typ**	**Worst**	**Units**
PROGRAM Timing				
PGM Recovery time	tPR	100	100	ns
VPP Warm-up time	tVPPS	100.0	100.0	ns
WE Setup time	tWP	100.0	100.0	ns
SEL Setup time	tSP	100.0	100.0	ns
VPP Recovery time	tVPPH	20	20	ns

Table 6-8. AC Characteristics: Read				
Description	**Symbol**	**Typ**	**Worst**	**Units**
READ Timing				
READ pulse width (single-ended mode)	tRP	26	51	ns
READ pulse width (redundant mode)	tRPR	11	23	ns
READ recovery time	tRR	7	12	ns
READ access time	tRACC	2	3	ns
Output drive load factor (Q[15:0] pins)	tLOAD	1.68	3.09	ps/fF
VRR warmup time	tVRRS	3000	3000	ns
WE Setup time	tWS	11	16	ns
SEL Setup time	tSS	7	12	ns
Max Read Pulse width[1]	tRP_MAX	2000	2000	ns

Notes:

- tRP_MAX is the maximum clock high time for one read cycle.

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Table 6-9. AC Characteristics: Other				
Description	**Symbol**	**Typ**	**Worst**	**Units**
OE Timing				
OE Access time	tQACC	1	1	ns
OE Delay	tQH	1	1	ns
Common Timing				
Address Setup time	tAS	4	8	ns
Address Hold time	tAH	1	2	ns
Data Setup time	tDS	1	1	ns
Data Hold time	tDH	2	2	ns
WE Hold time	tWH	1	2	ns
SEL Hold time	tSH	1	1	ns
MR Setup time	tMRS	12	17	ns
MR Hold time	tMRH	6	10	ns
EHV Level Setup time	tES	3000	3000	ns
EHV Level Hold time	tEH	50	50	ns

Term definitions:

- **Setup:** Time between signal stable and positive CK edge.
- **Hold:** Time the signal remains stable after the positive or negative CK edge, depending on the signal.
- **Recovery:** Time between the end of a command and the beginning of another command.
- **Pulse:** Time between the positive and negative CK edge.

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6-5. DC Characteristics

Table 6-10. DC Characteristics: Program				
Description	**Symbol**	**Typ**	**Worst**	**Units**
Program				
VPP current during programming[1]	iVPPP	250		µA/bit

[1]: Single bit programming.

Table 6-11. DC Characteristics: Read				
Description	**Symbol**	**Typ**	**Worst**	**Units**
Read Single Ended[1]				
VRR current during READ	iVRRR	2.2	3	µA/ MHz
VDD current during READ	iVDDR	6.9	8.6	µA/ MHz
Read Redundant[1]				
VRR current during READ	iVRRRR	3.3	4.4	µA/ MHz
VDD current during READ	iVDDRR	7.1	8.9	µA/ MHz
Stand by				
VRR current during Stand-by	iVRRSB	0.01	0.4	µA
VDD current during Stand-by	iVDDSB	0.08	5.5	µA

[1]: Read currents are for 50% of cells programmed, 50% of outputs switching and no load on the outputs.

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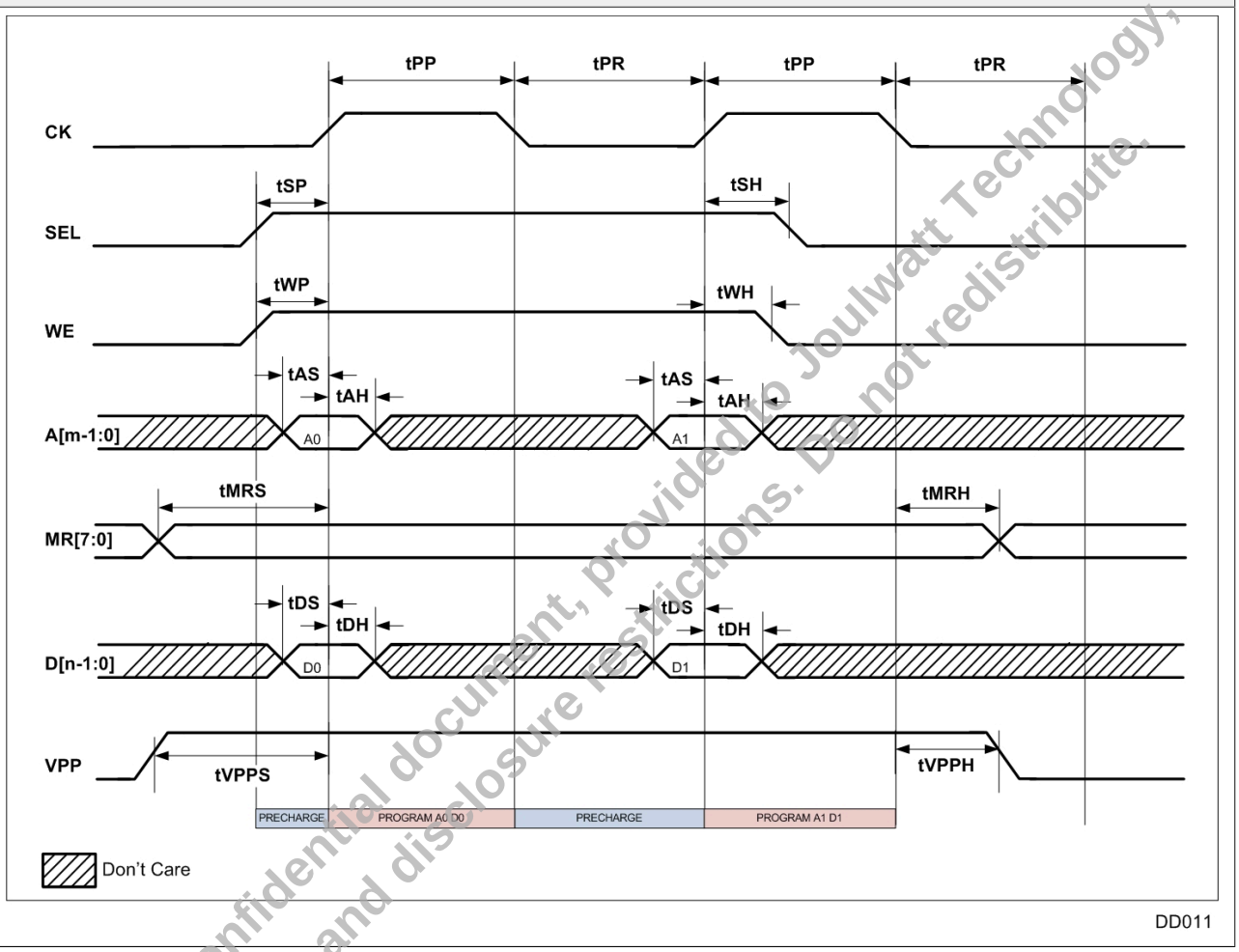
7-1. Timing Diagrams

Figure 7-1. Program Timing Diagram



Notes:

- tSP, tAS and tWP times do not start until CK=0 since these signals are latched while CK=1.

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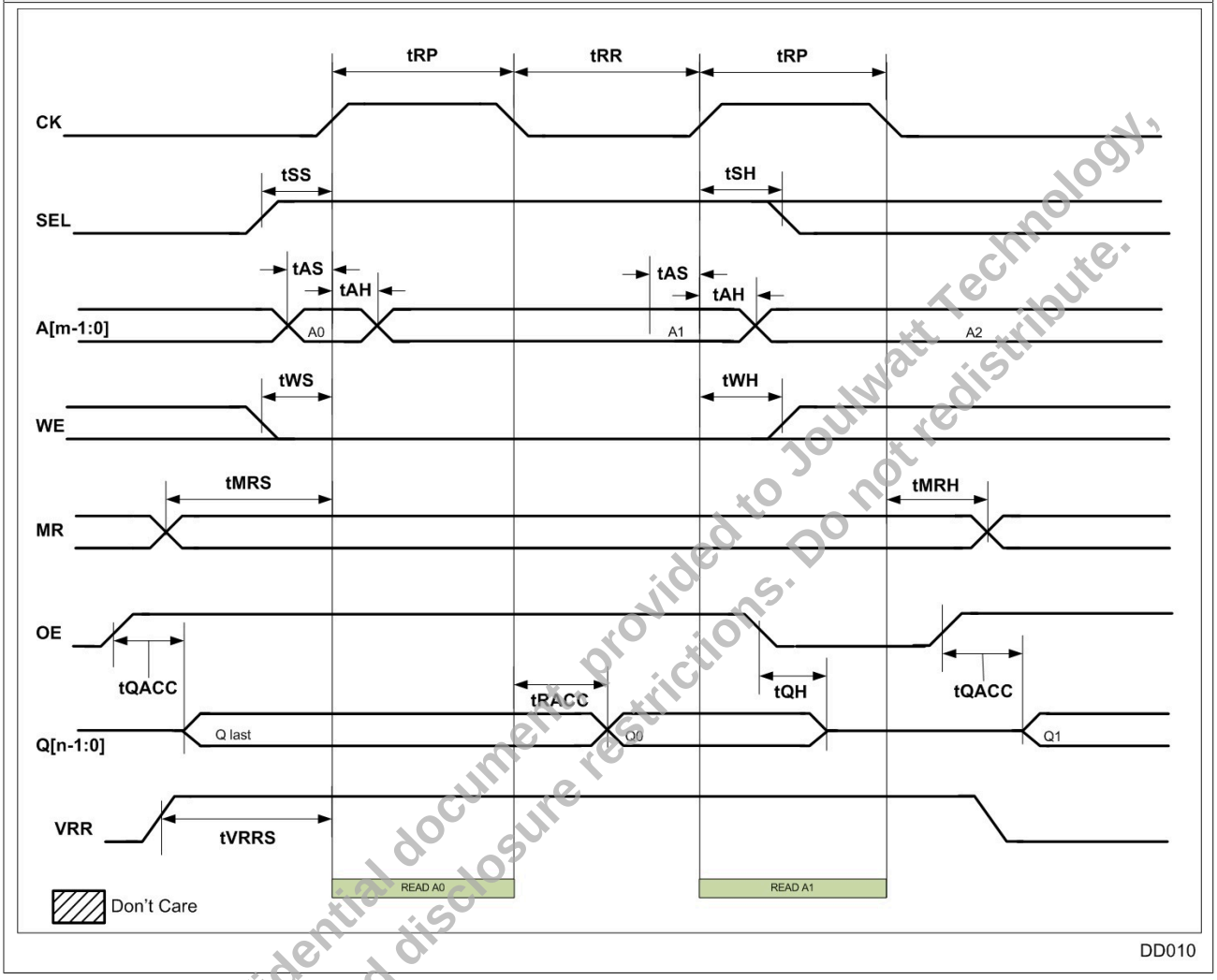
Figure 7-2. Read Timing Diagram



Notes:

- tSS, tAS and tWS times do not start until CK=0 since these signals are latched while CK=1.

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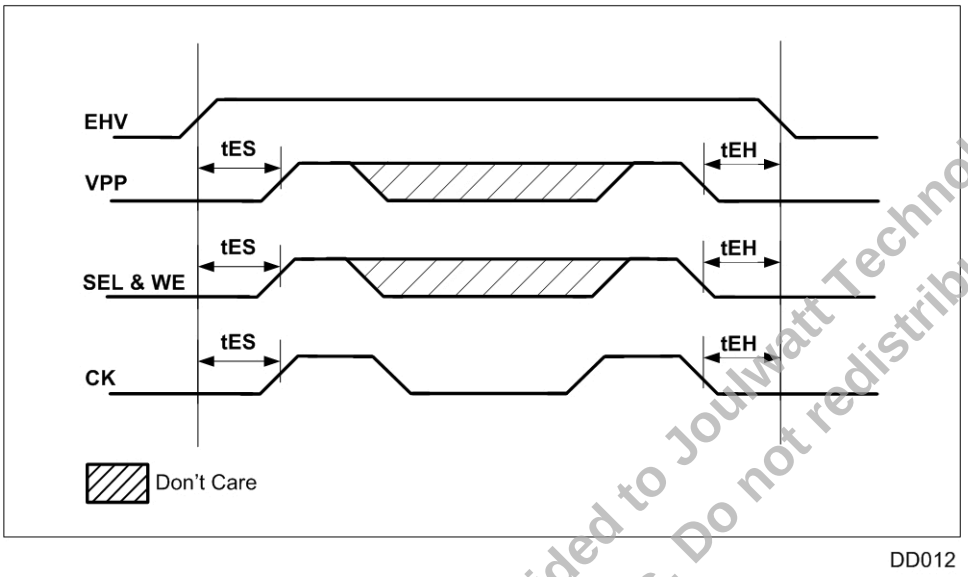
Figure 7-3. Power Enable Diagram



Notes:

1. EHV HIGH level must be ≥ VRR.
2. VPP LOW level is = VDD_IO MAX, VPP HIGH level is > VDD_IO MAX.
3. tES time starts when EHV=1 and CK=0 since CK=1 will latch the EHV=0 state.

8. Programming Algorithm

Figure 8-1. SLP_B Single Bit Programming Algorithm - Overview

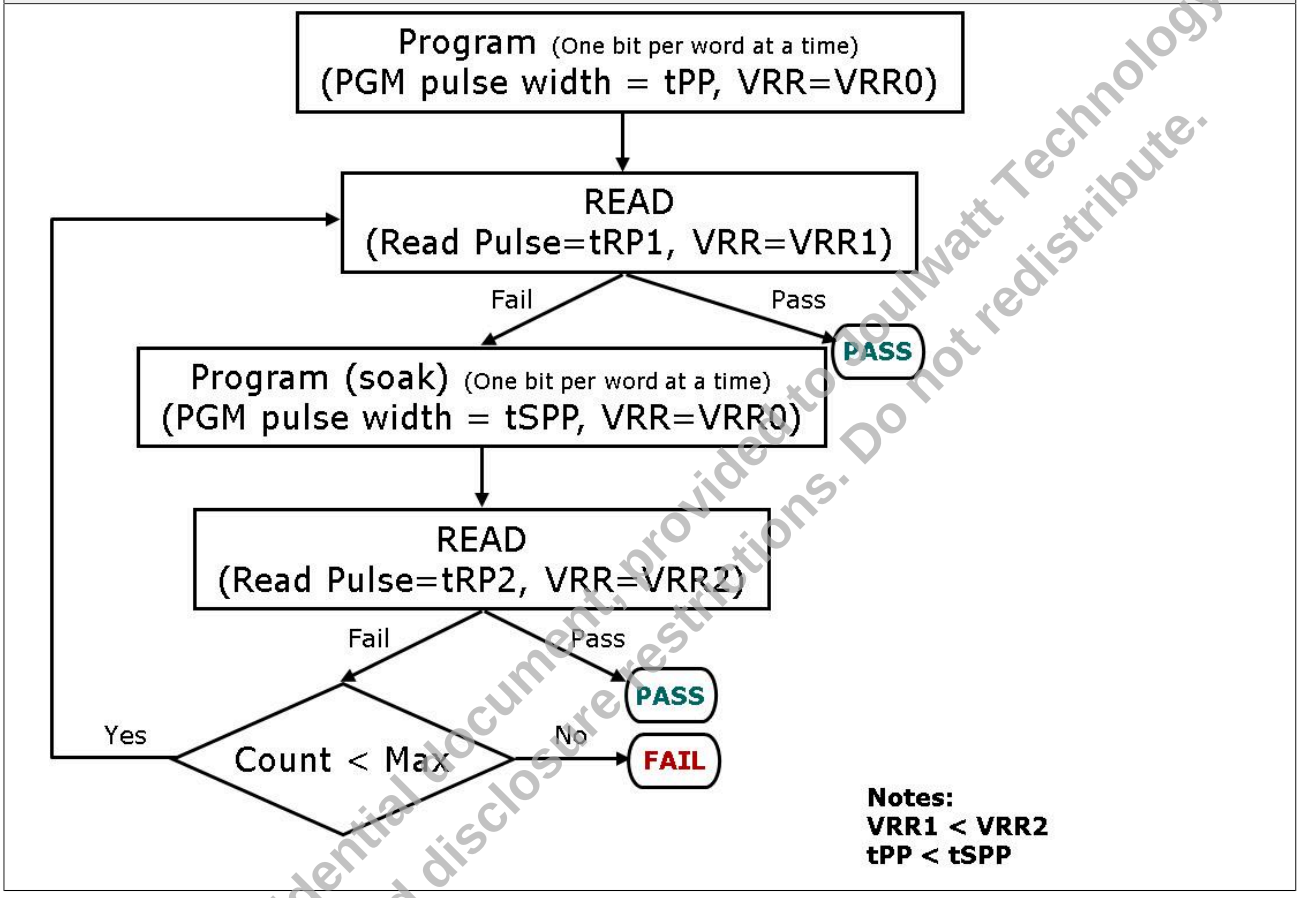


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Figure 8-2. SLP_B Single Bit Programming Flowchart

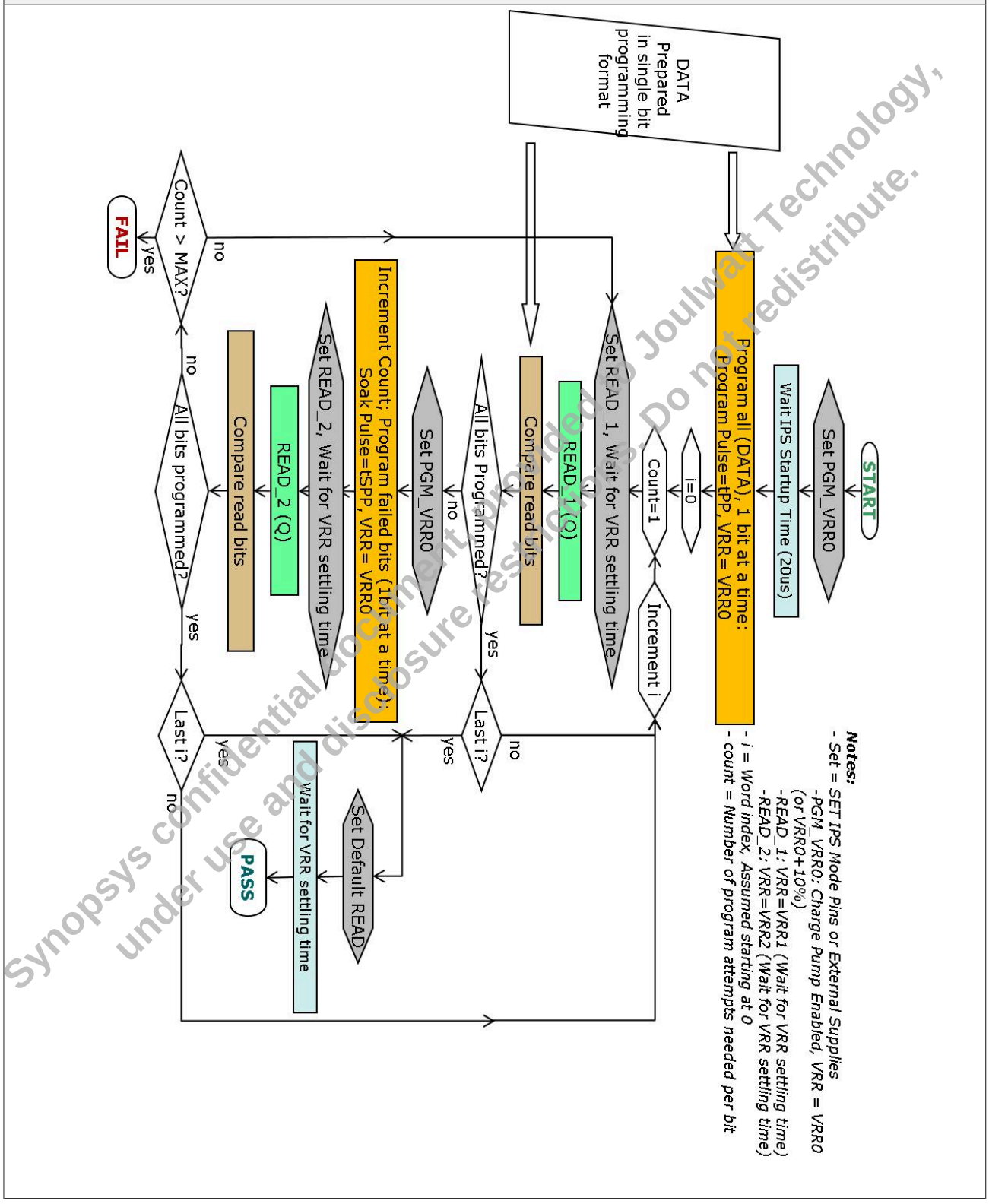

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Table 8-1. Programming/Verification Parameter Values			
Parameter	**Description**	**Value**	**Comments/IPS Mode Pin Setup**
tPP	Program Pulse	100µs	
tSPP	Soak Pulse	400µs	
tRP1	Read Pulse for READ_1	tRP_worst	Configuration dependent
tRP2	Read Pulse for READ_2	tRP_worst	Configuration dependent
VPP	Programming Voltage	7.900V to 8.400V	Charge Pump: VPPEN=1, MPP[7:4]=0000, MPP[3:0]=0000 External VPP: VPPEN=0
VRR1	Read Verify Voltage Level 1	1.80V	VRREN=1, MRR[15:4]=0x000, MRR[3:0]=1000
VRR2	Read Verify Voltage Level 2	2.20V	VRREN=1, MRR[15:4]=0x000, MRR[3:0]=1111
VRR0	Default Read Voltage Level	3.00V	VRREN=1, MRR[15:4]=0x000, MRR[3:0]=0100 (This VRR value should be used when writing (WE High))
MAX	Recommended maximum number of soaking pulses	10	

Notes:

- These parameters are for Standard SLP macrocell. If the macrocell is customized or the default read voltage level is different than VRR0 above, please contact support_center@synopsys.com.
- It is recommended that all mode pins are made accessible and/or programmable for increased testability and process portability.

IMPORTANT INFORMATION

The programming algorithm (and all parameter values) detailed in this section are critical factors in the performance of the OTP macro. It is necessary that these instructions are followed without deviation to ensure that the OTP macro performs to specification. The Synopsys support team (support_center@synopsys.com) is available for further clarification.

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SLP_B Programming Algorithm Description

1. Programming conditions:
   - If programming on a tester, maintain Max VDD, VDD_IO and VPP voltage levels for best program and verify performance.
   - Note that the un-programmed bit locations are not checked within this procedure and should be verified before and/or after the programming is completed.
2. Program all the bits in the target address space (array, row, word, byte, nibble or bit), one bit per word at a time, using a short programming pulse (tPP).
   - The data should be prepared in single bit programming format with only one bit selected in each word for programming in each data word.
   - VRR must be set to VRR0.
3. READ_1: Verify cell margins of each programmed bit by reading at low read voltage (VRR1) with a short read pulse (tRP1).
4. Re-Program (soak) all the bits failing READ_1 or READ_2 conditions (one bit at a time) using a long programming pulse (tSPP). VRR must be set to VRR0.
5. READ_2: Verify if all the programmed bits in the target address space can be read with sufficient timing margin (tRP2) at the minimum read voltage level (VRR2).
   - If any bit fails, repeat from step 3, until all the bits pass READ_2 condition or the MAX number of soaking pulses per bit is exceeded.
   - Note that the failed bits might still read correctly under nominal read conditions, but might become marginal at certain voltage, temperature or speed conditions.
6. Turn OFF VPP and set all the voltages to nominal read conditions.

Notes:

- When turning ON or changing voltage levels (VRR, VPP) when using IPS, a wait time in the order of 20µs for start-up and 1µs voltage level change should be observed. Refer to the IPS datasheet for the specifications of the wait times.

9. Mode Register Description

Table 9-1. Mode Register Pin Description				
REG Bits	**Description**	**"0"**	**"1"**	**Default**
MR[0]	Differential Read Mode (requires dual memory array arrangement, not available in this macro)	Single	Differential	0
MR[1]	WL Test Mode	Disabled	Enabled	0
MR[2]	BL Test Mode	Disabled	Enabled	0
MR[3]	SA Test Mode P	Disabled	Enabled	0
MR[4]	Redundant Read Mode	Disabled	Enabled	0
MR[5]	SA Test Mode N	Disabled	Enabled	0
MR[6]	External VREF	VREF=VDD	VREF External	0
MR[7]	Cell Current Test Mode	Disabled	Enabled	0

Table 9-2. Operating Mode Truth Table						
Description Reference	**MR[7:0]**	**VREF Value**	**Memory Array State**	**Q**	**Read (WE = 0)**	**Write (WE = 1)**
1	0000 0000	VDD	V	V	single-ended	allowed
2	X000 0001	VDD	V	V	differential	not allowed
3	X001 0000	VDD	V	V	redundant	not allowed
4	X001 0001	VDD	V	V	differential-redundant	not allowed
5	1000 0000	VDD	V	V	single-ended	TDDB or Cell current test through VRR
6	X000 0010	VDD	0	Q[15]=1	WL test	not allowed
7	X000 0100	VDD	0	1	BL test	not allowed
8	X000 0101	VDD	0	Q=A[5]	Differential BL test	not allowed
9	X000 1000	VDD	X	1	SA Test P	not allowed
10	X010 0000	VDD	0	0	SA Test N	not allowed
11	X10X 000X	Vext	V	V	read	not allowed
12	X100 1000	Vext > 0.25V	X	1	SA Offset Test P1	not allowed
13	X100 1000	Vext < 0.15V	X	0	SA Offset Test P0	not allowed
14	X100 1001	Vext > 0.05V	1	1	Diff SA Offset Test P1	not allowed
15	X100 1001	Vext < -0.05V	0	0	Diff SA Offset Test P0	not allowed
16	X110 0000	Vext > -0.1V	0	0	0 Margin Test	not allowed
17	X110 0000	Vext < 0.1V	1	1	1 Margin Test (Program-verify)	not allowed
18	OTHER		X	?	not allowed	not allowed

V = Valid X=any (0 or 1) ?=unknown VDD = internal pull up to VDD

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1 Default Single-ended Read Mode

The SLP_B is in single-ended read mode when MR[6:0]=0. In this read mode, unprogrammed bits are read as '0's.

2 Differential Read Mode (not available in this configuration)

Note that this mode requires dual memory array arrangement and is not available in single array macros.

3 Redundant Read Mode

MR[4]=1 enables 100% redundancy read mode in which A[6] is ignored and two memory cells are read in a wired-or fashion. For this mode to work, both memory bits selected by A[6] must be programmed using a single cell (non-redundant) mode. The redundant read mode is provided for the applications requiring increased margins when programmed in-field.

4 Differential-Redundant Read Mode (not available in this configuration)

Note that this mode requires dual memory array arrangement and is not available in single array macros.

5 Cell Current Test Mode

MR[7]=1 makes it possible to measure core cell current through the VRR pin. To set up the macro for cell current measurements, set SEL=1, WE=1, MR[7]=1, A[7:0] selected address, D[15:0]= "00100.." where "1" indicates the position of the bit to be measured, and measure the VRR supply current when CK=1.

6 Word Line (WL) Test Mode

MR[1]=1 couples a programmed ROM test bit line to the input of the last sense amp Q[15:0] in parallel to the normal bit line selected by A[7:0]. A read operation of an un-programmed array resulting in "1" on the highest Q bit verifies that the selected row decodes and reads correctly.

7 Bit Line (BL) Test Mode

MR[2]=1 turns on a precharge high circuit at the end of the local BL. Reading "1" on all bits in an un-programmed memory array in single-ended mode verifies BL continuity and correctness of the decoders at the selected column address.

8 Sense Amp Test Mode P

MR[3]=1 disables normal row access and sets the input of the sense amplifiers to VREF. If VREF=VDD (default value) the sense amplifiers will read as "1" (or programmed). This allows the sense amplifier operation to be verified. It also allows switching all memory outputs to the high state regardless of whether the array is programmed or not. This sense amp test read should be interleaved with normal read when verifying the native un-programmed state of the memory array (to ensure outputs switching in every cycle).

9 Sense Amp Test Mode N

MR[5]=1 connects VREF to the reference side of the sense amplifier. In this mode it is possible to modify the sense amplifier reference level by enabling MR[6] and forcing VREF level.

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10 External VREF

MR[6]=0 pulls VREF to VDD. When MR[6]=1, VREF is floating and can be forced externally. MR[6] does not affect read operation. In conjunction with other modes, it allows for the verification of read margins.

11 Sense Amp Reference

The Sense Amp Reference (or the effective offset) can be directly verified by applying analog voltage 0V to 0.5V to VREF pin and performing READ with MR[6]=1 and MR[3]=1.

12 Differential Sense Amp Test Mode P

MR[0]=1, MR[3]=1, MR[6]=1 allows testing of sense amp offset directly by applying an analog voltage +/-0.3V to VREF pin and performing READ operation.

13 Un-Programmed Cell Margin

Can be directly verified by applying a negative voltage 0 to -200mV on VREF while performing a read operation with MR[6]=1, MR[5]=1.

14 Program-verify

The programmed cell margin can be directly measured by applying a positive voltage 0 to 400mV on VREF while performing a read operation with MR[6]=1, MR[5]=1. Programmed cell margins can be checked (tested) in the following ways:

1. Lowering the VRR voltage level (VRRmin-10%) during a read operation
2. Applying an external reference voltage VREF=50mV with MR[6]=1, MR[5]=1
3. Shortening the read pulse length to 75% of the minimum pulse used by the application

15 Other Mode Pin Combinations

The Operating Mode Truth Table lists all the allowed mode pin combinations during read and program pulse. Performing a read operation in a not allowed state gives unpredictable results. Performing a write (program) operation in a not allowed state may result in data corruption.

10. Revision History

The footer of this document contains an identifier for this document revision:

D1.0B1.5T2.5

It is comprised of the following:

- D1.0: version of the macro-specific data (timing and power consumption values, area size, number of words, bits, mux, etc.)
- B1.5: version of the baseline-specific data (voltage and temperature ranges, process-related data, timing diagrams, mode register settings, etc.)
- T2.5: version of the template (document styles and structure, header and footer, generic definitions, spelling, grammar, etc.)

The tables below contain the revision history of the template, baseline and macro:

Table 10-1. Revision History - Databook Template (TSMC-180BCD50)

Revision	Date	Change Description
1.0	2011-02-10	Release
1.1	2011-06-17	Added new revision history. Added note to tRP_MAX (on page).
1.2	2011-11-02	Minor correction to address map (address setting clarified when using Column Mux 8 or 16).
1.3	2012-08-29	Additional changes to address mapping, affecting SLP_B revisions AB and later (AA not affected). Updated Differential, Redundant and Differential-Redundant Read Mode Register descriptions (Mode Register Description on page 29) to address new address mapping. Updates also reflected in Memory Operation on page 9.
1.4	2012-09-17	Modification to Table 9-2 on page 29 - correct value of the column 'memory array state' for rows 'sense amp differential offset tests' P0 and P1 have been corrected to read '0' and '1' respectively instead of 'X'.
1.5	2013-02-07	Adding optional text for macros with additional CKD block included. No other changes.
1.6	2013-02-25	Differentiating programming flowchart to be baseline-specific. No other changes.
1.7	2013-06-25	Updates on Single Bit Programming Flowchart.
1.8	2013-08-08	Updates on Timing Diagrams.
1.9	2013-10-16	Updates on Timing Diagrams, tSH changed back to clock rising edge.
1.10	2013-12-20	Updated AC and Power tables to populate three additional columns beside the worst column.
1.11	2014-04-10	Change VPP and VRR pin type to V.
1.12	2016-02-29	Minor updates on the block diagram; Added statement to programming algorithm specifying critical factors in the performance of the OTP macro. It is necessary that the programming algorithm is followed without deviation to ensure that the OTP macro performs to specification.
1.13	2016-06-22	Correcting figure 6-2, Read Timing Diagram. Previous version of template was pulling out-of-date diagram.
1.14	2016-12-09	Template revision that does not impact this baseline. No changes.

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Table 10-1. Revision History - Databook Template (TSMC-180BCD50)		
Revision	**Date**	**Change Description**
1.15	2017-02-14	Corrected figure 6-2, Read Timing Diagram. In previous version the SEL signal went low after the second read pulse.
1.16	2017-08-15	Updated datasheet values.
2.0	2018-09-10	Logos, diagrams, pictures, legal and contact information updated to match corresponding Synopsys information. Updated the storage temperature definition to 'no bias' from 'under bias'.
2.1	2019-11-21	Template integrated into DBGEN compiler.
2.2	2020-04-02	Changed references to VCC to VDD_IO for consistency, fixed other minor typos.
2.3	2020-10-19	Added read temperture range to Table 1-1.
2.4	2020-11-13	Updated template to include macro name in header. Updated to support G50 and BCD50 processes.
2.5	2020-11-20	Changed pin description column in Table 6-2 from Type to Usage and Description.

Table 10-2. Revision History - Baseline SLPB		
Revision	**Date**	**Change Description**
1.0	2012-08-29	Release
1.1	2012-09-14	Updating process to 2nd generation of BCD process. All timing and power values have been re-simulated with new process.
1.2	2013-11-22	Expanded VPP range to 8.4V Max. Minor revisions to programming algorithm values - MRR settings for VPP, VRR2, max. number of soak pulses.
1.3	2017-11-23	Updated program temperature range to -40 ≤ Tj ≤ +125 from -40 ≤ Tj ≤ +150.
1.4	2020-03-19	Corrected Typo in Table1-1 to change max read/program temperature to 150C
1.5	2020-11-23	Reverted Table 1-1 temperature range to -40 ≤ Tj ≤ +125 from -40 ≤ Tj ≤ +150.

Table 10-3. Revision History - Macro-specific slp_b_tsmc180bcd50_256x16_cm16s_eb		
Revision	**Date**	**Change Description**
1.0	2017-03-09	Release

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11. Web Resources

- DesignWare IP product information: http://www.designware.com
- Your custom DesignWare IP page: http://www.mydesignware.com (Synopsys password required)
- Documentation through SolvNet: https://solvnet.synopsys.com (Synopsys password required)
- Synopsys Common Licensing (SCL): http://www.synopsys.com/keys

12. Customer Support

To obtain support for your product, contact Support Center using one of the following methods:

- *For fastest response,* use the SolvNet website. If you fill in your information as explained below, your issue is automatically routed to a support engineer who is experienced with your product. The **Sub Product** entry is critical for correct routing.

  Go to https://solvnet.synopsys.com/support/open_case.action and click on the link to enter a call.

  Provide the requested information, including:

  a. **Product:** DesignWare NVM

  b. **Sub Product:** Select the OTP architecture (OTP SHF, OTP SLP, OTP SiPROM, or OTP Other).

  c. **Product Version:** See release notes.

  d. Platform and OS are not pertinent to DesignWare NVM.

  e. **Problem Title:** Provide a short summary of the issue or error message you have encountered.

  f. **Problem Description:** Specify the databook name (databook name) and a description of the issue. For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood.

- Or, send an e-mail message to support_center@synopsys.com (your e-mail will be queued and then, on a first-come, first-served basis, manually routed to the correct support engineer):

  a. Include the Product name, Sub Product name, process, and Tool Version number in your e mail (as identified above) so it can be routed correctly.

  b. For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood.

  c. Attach any debug files you created.

- Or, telephone your local support center:

  a. Call (800) 245-8005 from within the continental United States.

  b. Call (650) 584-4200 from Canada.

  c. Find other local support center telephone numbers at http://www.synopsys.com/Support/GlobalSupportCenters.