ememory

EO0128X8KB180BC01A

TSMC 0.18um Pure 5V BCD Process

128 x 8 bits One Time Programmable Device

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Document Update History

Ver.	Effective	Revised Content	Applicant
1.0	2018-01-17	Original version	Justin

[QM-201(01A)]

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128 x 8-bits One Time Programmable Fuse

eMemory's OTP HR (Neobit®) is adopted in TSMC 0.18µm Pure 5V design in 1.8V/5V/60V BCD Process. Programming is by hot electrons injection generated by avalanche impact ionization in eMemory's Neobit® bit cell. OTP HR required programming voltage 7.5V which is supplied from IP external through VPP pin. Cells are initialized by ultraviolet light through internal photoemission from the floating gate.

Features

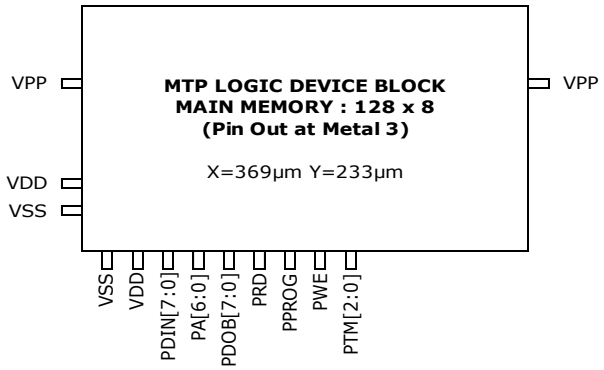
- TSMC 0.18um Pure 5V BCD Process
  - 1P3M IP design, Capable of using on 1P4M/1P5M/1P6M.
  - Metal-3 follows 40KA ultra-thick metal rule. Dummy Metal-4 ~ Metal-6 follow ultra-thick metal rule.
- VDD and VPP Power Supply
  - 2.0V~5.5V VDD for Read
  - 7.25V~7.75V VPP, 2.0V~5.5V VDD for Program
- Memory Organization 128 x 8 bits
- Byte Program Operation
- Junction Temperature T_J : -40°C ~ 150°C
- Data Retention: >10 Years @ 125°C
- Power Switch embedded
- **OTP Cell :** 5V device
- **IP Size :** 0.086 mm^2 (369um x 233um)
- **Access Time :** 200ns (max)
- **Byte Program Time :**
  - 100us (typ.)
- **Operating Current : (max)**
  - I_{VDD_R}: 1.2mA
  - I_{VPP_R}: 1uA
- **Standby Current : (max)**
  - I_{VDD_SB}: 3uA
  - I_{VPP_SB}: 1uA

General Description

EO0128X8KB180BC01A is a CMOS 128 x 8-bits One Time Programmable device. The main memory block is organized as a 128 by 8 bits output in read mode, and 256 by 8 bits input in program mode. The OTP cell design will provide a low cost logic process OTP approach compared with alternative approaches. The EO0128X8KB180BC01 programs with 5V power supply and 7.5V external VPP supply.

PGM is the abbreviation for program and $\mathbf{T_J}$ stands for junction temperature.

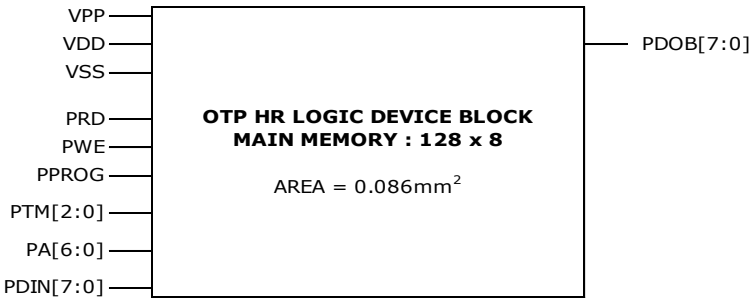
Pin Assignments



Power Connection Requirement

- Power/Ground bouncing beyond DC specifications is not allowed.
- PDIN/PDOB/PTM pins are randomly located at IP down side, please check phantom GDS for details.

Symbol



Pin Description

Pin Name	Direction	Description
PA [6:0]	I	Address input
PDIN [7:0]	I	Data input
PDOB [7:0]	O	Data output reversed
PTM [2:0]	I	Test mode enabling
PWE	I	Define program cycle
PPROG	I	Program mode enabling
PRD	I	Define read cycle
VDD	I	Power supply
VSS	I	Ground
VPP	I	High voltage power supply for programming

[8,940]

Notes

1. No glitch immunity on these signals. Users should provide the non-glitch signals to all pins.

Data Pin Connection Requirement

- PDOB to connect drain/source of NMOS/PMOS as Fig.(b) is not allowed. Gate electrode connection as Fig.(a) is strongly recommended.

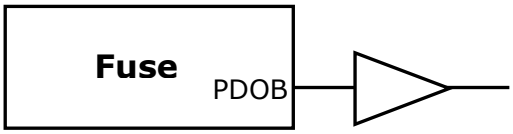


Fig.(a) Recommended PDOB Connection

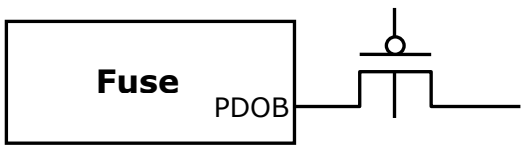


Fig.(b) Not allowed PDOB Connection

Truth Table

Operating Mode Truth Table

User Mode	PTM[2:0]	PPROG	PWE	PRD
Stand-by	L L L	L	L	L
Read Access	L L L	L	L	H
Program Entry	L L L	H	L	L
Program Access	L L L	H	H	L

Testing Mode	PTM[2:0]	PPROG	PWE	PRD
Margin-1 Read Mode	H H L	L	L	H
Margin-2 Read Mode	H H H	L	L	H
Off State Margin Read Mode	H L H	L	L	H
IPP Mode	L L L	H	H	L

Notes

1. H stands for logic High level. L stands for logic Low level.
2. PTM[2] = L, PTM[1] = L, PTM[0] = L is for User mode.
3. PTM[2] = H, PTM[1] = H and PTM[0] = L is for Margin-1 Read Mode. Margin Read Mode provides a critical read condition to filter out “weak programmed” bits during CP sort in the testing flow and only can be used at 25°C ~85°C. To cover all worse corners, customer should implement Margin-1 Read Mode during testing.
4. PTM[2] = H, PTM[1] = H and PTM[0] = H is for Margin-2 Read Mode. Margin-2 Read Mode setup another critical read condition to filter out “weak retention” bits during CP2 sort in the testing flow and only can be used at 25°C ~85°C.
5. PTM[2] = H, PTM[1] = L and PTM[0] = H is for Off state Margin read mode. Off State Margin read provides a stern read criterion to filter out high off state bits during CP sort in the testing flow and only can be used at 25°C ~85°C.
6. PTM[2] = L, PTM[1] = L and PTM[0] = L is for IPP Mode. IPP Mode is implemented for bit cell current measurement. Customer should design in IPP mode, which allow to measure OTP cell current. It's for debug purpose in case of malfunction happen in merged product.

Write/Read Truth Table

Cell State	PDIN Write	PDOB Read
Programmed	L	H
Un-programmed(Initial)	H	L

Notes

1. **For “Initial” (un-programmed) state or “Erased" state (UV erase), the read out data is "L".**

DC Specifications

DC Operating Conditions

Operating Mode	Power Pin	Min	Typ	Max	Unit
Read Mode	V_{DD}	2.0	5.0	5.5	V
	V_{PP}	VDD/VSS/Floating			
	V_{SS}	0			V
PGM Mode	V_{DD}	2.0	5	5.5	V
	V_{PP}	7.25	7.5	7.75	V
	V_{SS}	0			V

[8,940]

Notes

1. **Power/Ground supply voltage beyond DC operating range is not guaranteed.**
2. **Power/Ground bouncing beyond DC operating range might cause invalid data output and will not guaranteed by eMemory. Customers must take care of power stability on their own.**
3. **Normally, junction temperature is from -40°C to 150°C for normal operation, but from -20°C to 125°C for programming operation.**

DC Electrical Characteristics

Parameter	Power Pin	Typ	Max	Unit	Test Condition
Read Current at Tprd=200ns	I_{VDD_R}	0.8 (for 8 bits)	1.2 (for 8 bits)	mA	PA[7:0]=0/V_{DD}, PTM[2:0]=0, V_{DD}=V_{PP}=V_{DDMAX}, PDIN[7:0]=0, PRD=V_{DD}, PPROG=PWE=0
	I_{VPP_R}	1 (for 8 bits)	1 (for 8 bits)	µA	
Normal Program Current	I_{VDD_P}	1	1	µA	V_{PP} =V_{PPMAX}, PTM[2:0]=0, V_{DD}=V_{DDMAX}, PRD=0 PPROG=PWE=V_{DD}
	I_{VPP_P}	400 (for 1 bit)	800 (for 1 bit)	µA	
Standby Current	I_{VDD_SB}	<1	3	µA	PA[7:0]=0/V_{DD}, PTM[2:0]=0, V_{DD}=V_{PP}=V_{DDMAX}, PRD=PPROG=PWE=0
	I_{VPP_SB}	<1	1	µA	

[8,940]

Notes

1. **All electrical parameters listed above are based on SPICE (or equivalent) simulations and subject to changes after silicon verification.**
2. **Capacitive loading should be less than 1pf same as simulation conditions.**
3. **No active current at standby mode thus I_{SB} is dependent on device leakage current.**
4. **Normally, junction temperature is from -40°C to 150°C for normal operation, but from -20°C to 125°C for programming operation.**

Timing

Timing Parameters (C_{LOAD}=1pf)

Parameter	Symbol	Min	Max	Unit
Rising Time	T_r	-	1	ns
Falling Time	T_f	-	1	ns
Read Data Access Time	T_{aa}	-	200	ns
Read Pulse Width Time	T_{prd}	200	50000	ns
Read Pulse Interval Time	T_{prdi}	13	-	ns
Output Data Hold Time	T_{oh}	0	-	ns
Address Setup Time	T_{as}	4	-	ns
Address Hold Time	T_{ah}	9	-	ns
Data Setup Time	T_{ds}	4	-	ns
Data Hold Time	T_{dh}	9	-	ns
Program Mode Setup Time	T_{pps}	10	-	ns
Program Mode Recovery Time	T_{ppr}	10	-	ns
External VPP Setup Time	T_{vps}	10	-	ns
External VPP Hold Time	T_{vph}	10	-	ns
Program Pulse Width Time	T_{pw}	90	110	µs
Program Pulse Interval Time	T_{pwi}	2	-	µs
Program Recovery Time	T_{vr}	10	-	µs
Control Signal Enable Time	T_{rst}	20	-	ns
PTM Mode Setup Time	T_{ms}	10	-	ns
PTM Mode Hold Time	T_{mh}	10	-	ns

[8,940]

Notes

1. **All electrical and timing parameters listed above are based on SPICE (or equivalent) simulations and subject to changes after silicon verification.**
2. **Capacitive loading should be less than 1pf same as simulation conditions.**
3. **T_{pw} have maximum value limitation, which is reliability concern to avoid long HV stress time.**
4. **Normally, junction temperature is from -40°C to 150°C for normal operation, but from -20°C to 125°C for programming operation.**

Input Capacitance

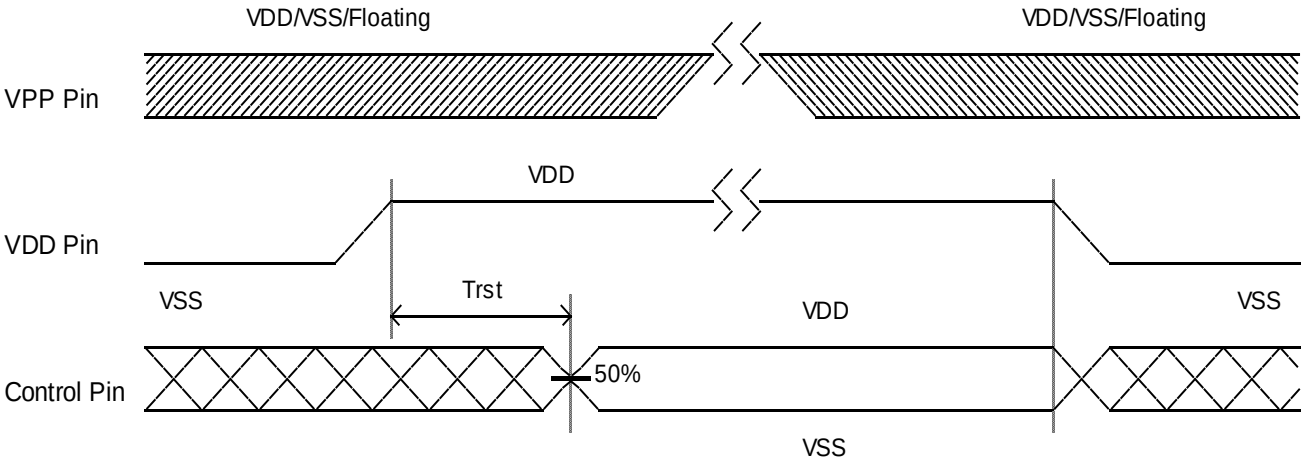
Parameter	Symbol	Min	Max	Unit	Test Condition
Control Input	C_{CON}	-	0.1	pF	VIN=0 at f=1 MHz
Address Input	C_{ADD}	-	0.1	pF	VIN=0 at f=1 MHz
Data Input	C_{DIN}	-	0.1	pF	VIN=0 at f=1 MHz
VPP input(from memory block)	C_{PP}	-	100	pF	VPP=0 at f=1 MHz

[8,940]

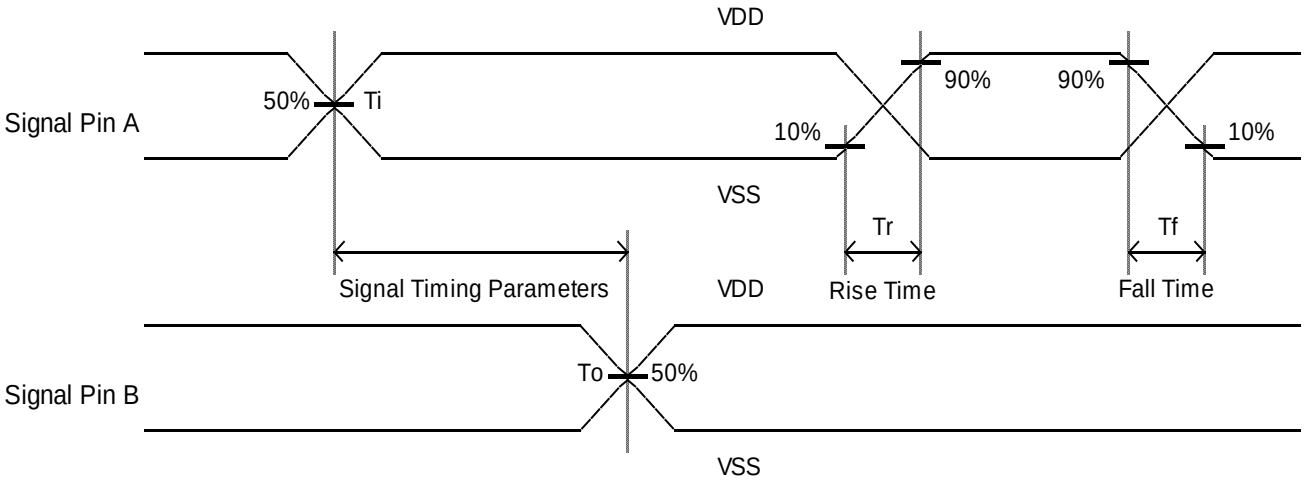
Timing Waveforms

Timing Definition

Power Up/Down Sequence



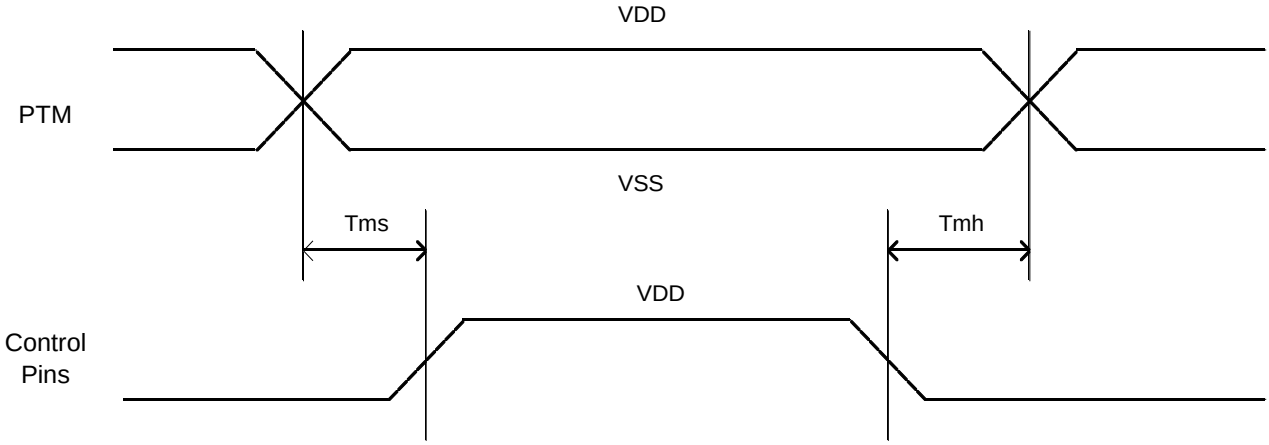
Signal Pin Timing Definition



- VDD/VPP/VSS level is specified in each timing waveform.
- Power up sequence timing is based on power measuring point while VDD/VPP is stable as waveform indicated.
- Signal to signal timing is measured from T_i to T_o of input/output signal at 50% VDD level based on VSS=0V.
- Signal rise time T_r (fall time T_f) is defined from 10% => 90% (10% <= 90%) of VDD level based on VSS=0V.

Timing Definition

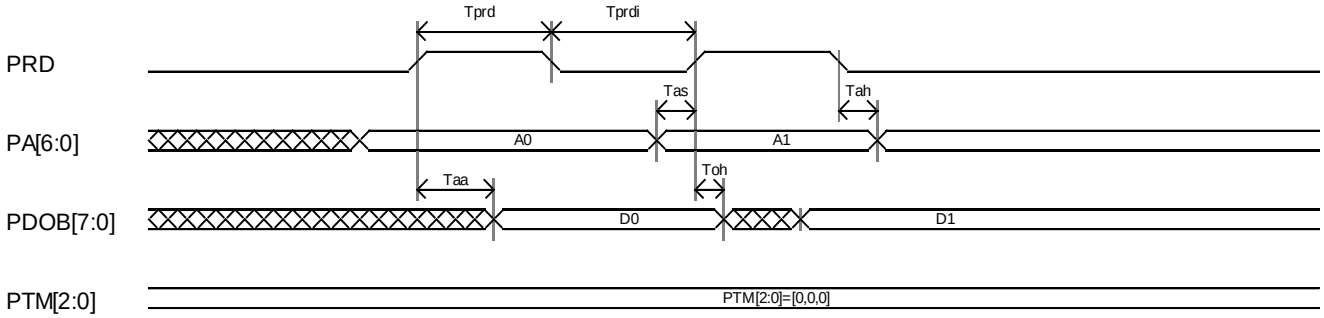
Control Pin Timing Definition



- Control pins are included PRD, PPROG, and PWE.
- Control pins have to be executed Tms later after PTM change.

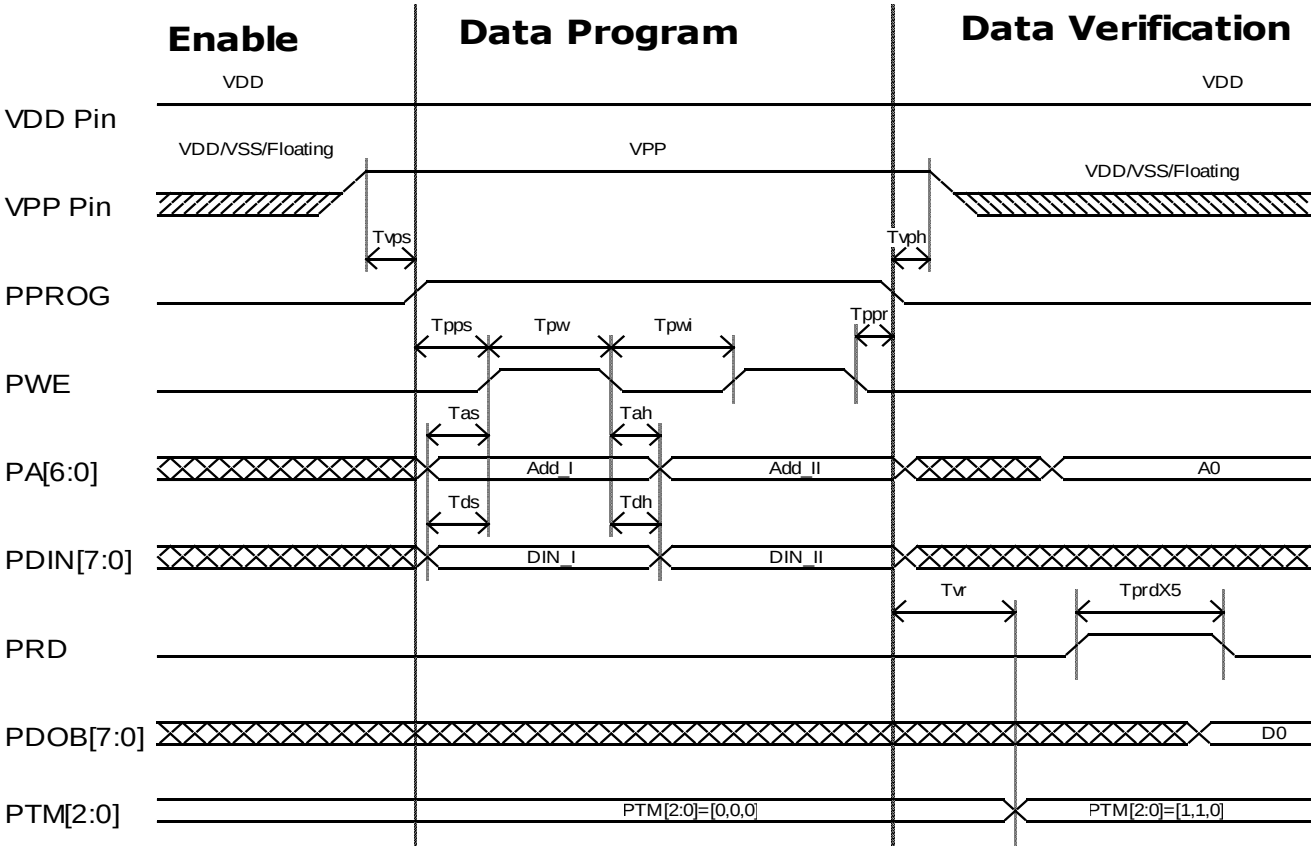
User Mode

Read Cycle



PPROG=PWE=0V, PDIN[7:0]=H/L, PA[1:0]= H/L, VDD=2.0V~5.5V, VPP=VDD/VSS/Floating, VSS=0V

Program Cycle



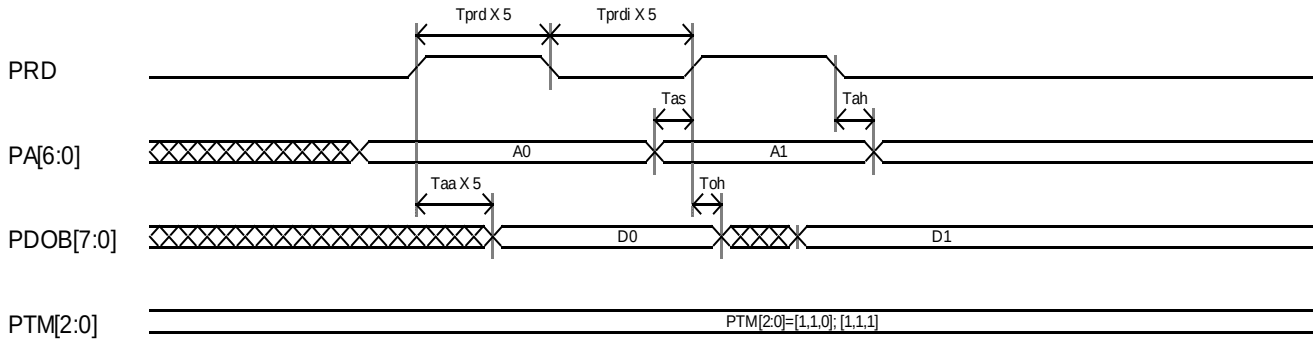
PTM[2:0]=[0,0,0], VDD=2.0V~5.5V, VPP=7.25V~7.75V, VSS=0V

Notes

1. **It is suggested using Margin Read Mode to do data verification. The details of Margin Read Mode are shown in the following page.**
2. **The next operation has to be executed Tvr later after PPROG falls to low.**

Testing Mode

Margin Read Cycle



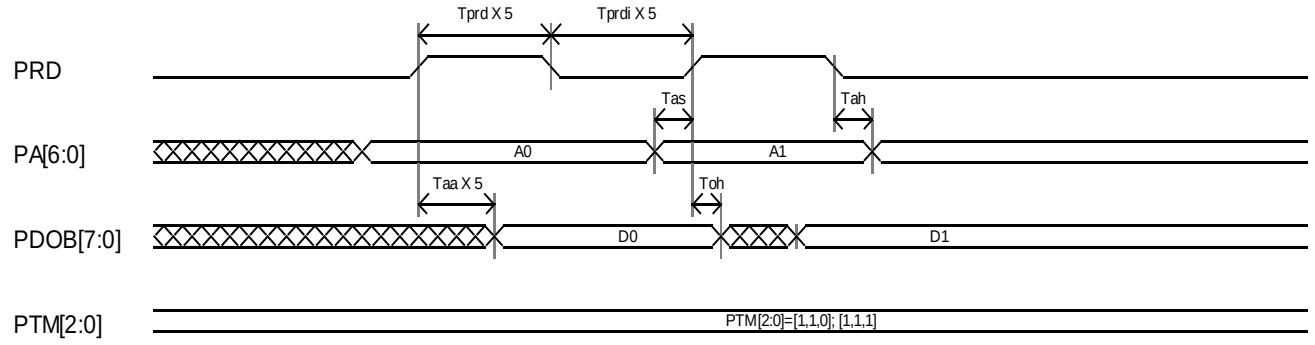
PPROG=PWE=0V, PDIN[7:0]=H/L, VDD=5V, VPP=VDD/VSS/Floating, VSS=0V

PTM[2:0]=[1,1,0] for Margin-1 Read Mode; PTM[2:0]=[1,1,1] for Margin-2 Read Mode

Notes

1. **VDD needs to use typical value 5V when doing Margin Read Mode.**
2. **Please relax the setting of Tprd to be 5 times of the typical one when doing Margin Read Mode, and Taa will be 5 times.**
3. **VDD needs to use typical value 5V when doing Margin Read Mode.**

Off Margin Read Cycle



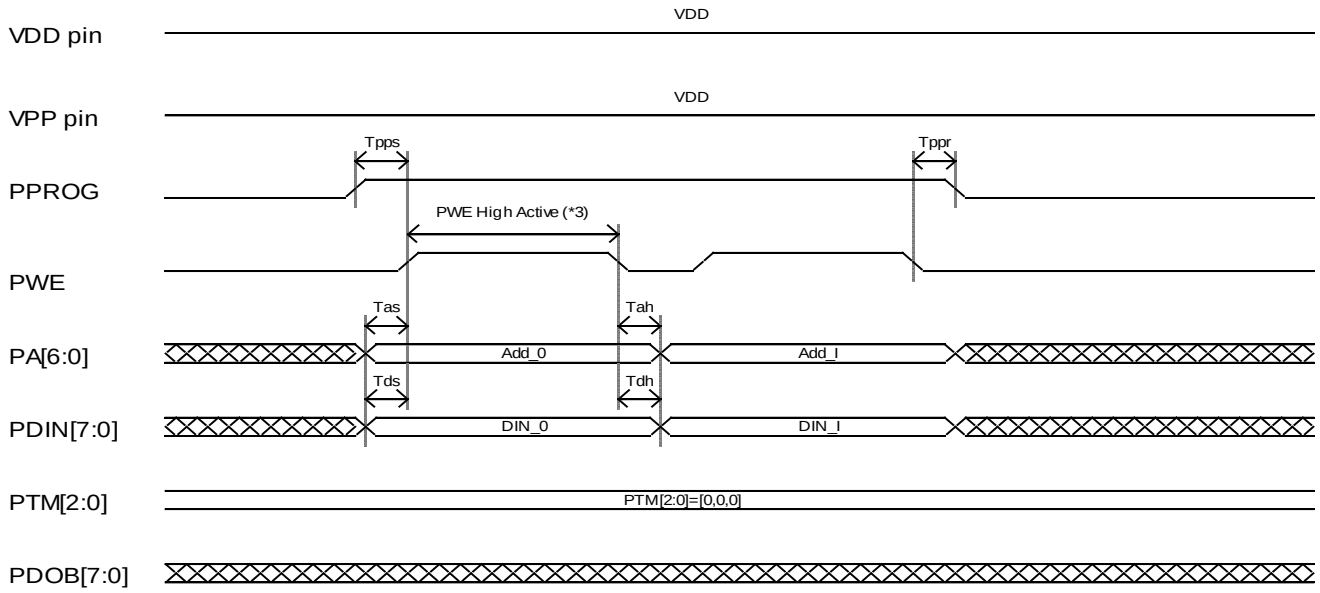
PPROG=PWE=0V, PDIN[7:0]=H/L, VDD=5V, VPP=VDD/VSS/Floating, VSS=0V

PTM[2:0]=[1,0,1] for Off Margin Read Mode

Notes

1. **VDD needs to use typical value 5V when doing Off Margin Read Mode.**
2. **Please relax the setting of Tprd to be 5 times of the typical one when doing Off Margin Read Mode, and Taa will be 5 times.**

IPP Mode



PRD=0V, VDD=VPP=2.0V, VSS=0V

Note:

1. **To measure one designate memory cell, PA is used to select byte and one PDIN[X] is forced as logic "L" with all other PDIN bus are logic "H".**
2. **Cell current is measured from VPP pin.**
3. **When dedicated PA and PDIN is selected, customer can measure Ipp during PWE high active period. PWE high active period depends on Parameter Measurement Unit of tester, and it's suggested to be over 30ms.**