UMA11LSCEP15BDRLLN_A
UMC 0.11um Al 1.5V
EE2PROM Low Leakage
Tapless Standard Cell Library
Application Note

Revision History

Version	Date	Description
A01	2016/08/17	Initial publication

Table of Contents

General Description

Use of IP described herein requires a license from UMC.
This application note provides information that assists the users of this standard cell library, UMA11LSCEP15BDRLLN_A, in achieving the following design goals:
• Correct placing and routing (P&R)
• Correct usage of UMA11LSCEP15BDRLLN_A Standard Cell Library

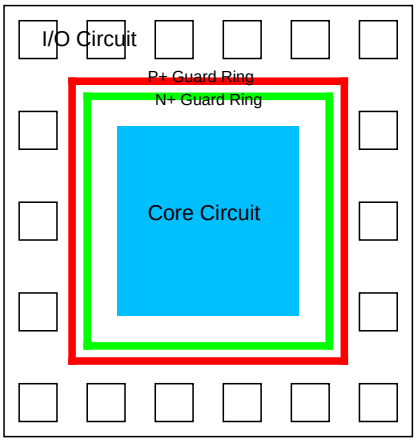
Logical Synthesis Notice

The cells with smallest driving strengths (M0HM, M1HM) of each type are set as "dont_touch" and "dont_use" cells by default in the liberty models of UMA11LSCEP15BDRLLN_A. This is for the consideration of the high-speed design application. With these smallest driving cells used in synthesis stage, the design may cause performance penalty in timing although theses cells have smaller leakage. Nevertheless, the users may decide to keep this setting or not upon their design`s timing or leakage concerned, relatively.

This library includes some special cell types. They are also set as "dont_touch" and "dont_use" by default in liberty models. Users must take care and understand the function usage when using in design.
They are listed as below,
BHDM1HM, TIE0HM, TIE1HM

Chip Implementation Notice

This is a tap-less library. The substrate/well contacts are added by placing a well-tap cell periodically. For effective latch-up prevention, it is suggested to add a guard ring between core and IO circuit. Please refer to latch-up rule of TLR for details. The following picture is an example.



Physical Information

The following definitions and layout rules are used for the design of standard cell library, UMA11LSCEP15BDRLLN_A. Please review them before start designing.

Bus Definitions

The definitions of power bus are described in Table 1 and illustrated in Figure 1.

Table 1. Definitions of Power Bus

Power Name	Description	Voltage
VDD	Core Cell Power	1.5 V
VSS	Core Cell Ground	0 V

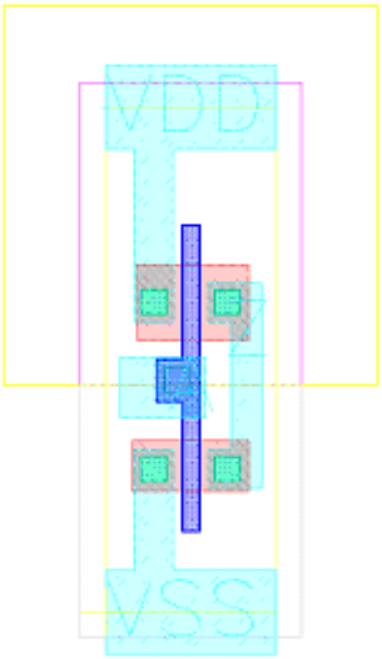


Figure 1. Architecture of Core Cell Power Ground

Specifications of Standard Cell Library

The specifications of standard cell library, UMA11LSCEP15BDRLLN_A, are listed in Table 2.

Table 2. Specifications of UMA11LSCEP15BDRLLN_A

Characteristics	Specifications
Cell Height	2.4 um
Drawn Gate Length	0.12 um
Layers of Metals	4, 5, 6, 7, 8
Layout Grid	0.001 um
Metal Layer Used In Cell Library Itself	Metal1, Metal2
Vertical Pin Grid	0.4 um
Horizontal Pin Grid	0.4 um
Power Rail Width	0.28 um

Filler Cells

The library includes filler cells to fill the empty spaces among standard cells. The filler cells connect disjointed N-wells, N+/P+, power and ground rails into a continuous and united area.

Table 3 lists all different sizes of filler cells with and without MOS capacitances in this standard cell library.

Table 3. Different Sizes of Filler Cells with/without MOS Capacitance

Filler Cells							
Cell Name	FIL1HM	FIL2HM	FIL4HM	FIL8HM	FIL16HM	FIL32HM	FIL64HM
Cell Width	0.4um	0.8um	1.6um	3.2um	6.4um	12.8um	25.6um

Filler Cells with P/N MOS Capacitance							
Cell Name	FILE3HM	FILE4HM	FILE8HM	FILE16HM	FILE32HM	FILE64HM	FILE128HM
Cell Width	1.2um	1.6um	3.2um	6.4um	12.8um	25.6um	51.2um
Cell Leakage	1.5462 pW	2.8562 pW	3.4614 pW	7.1209 pW	14.4882 pW	29.2586 pW	58.6416 pW

Note:
1. The cell leakage is characterized at the typical condition (1.5V, TT, 25C).
2. Filler cell insertion should be applied largest cell width first, then go down smaller ones in order.

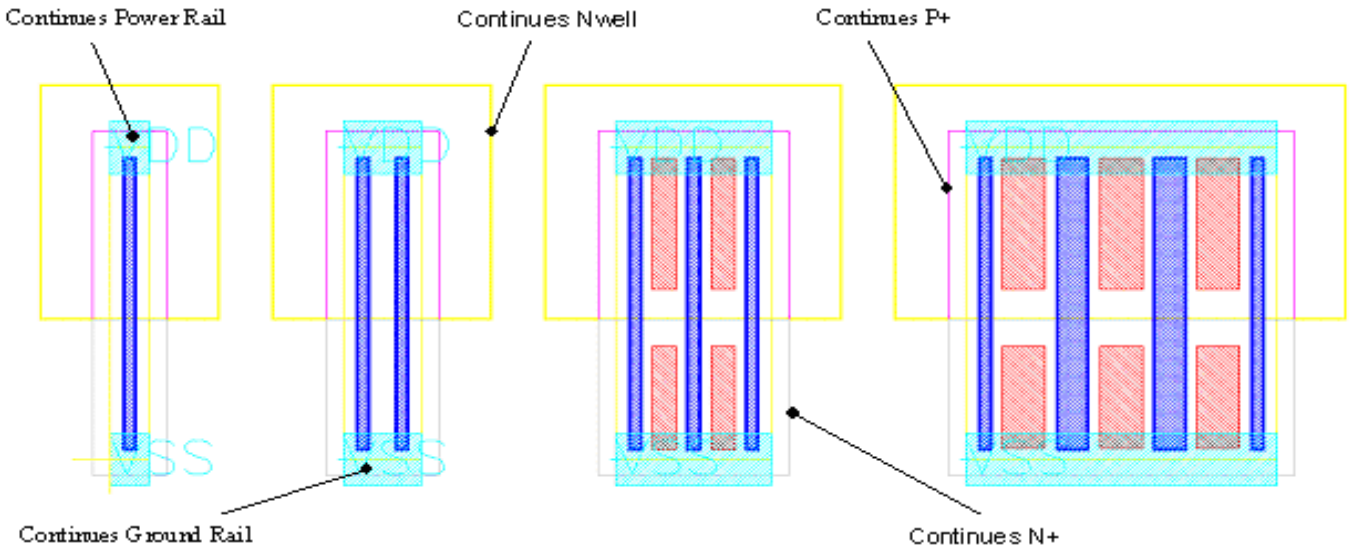


Figure 2. Filler Cells without MOS Capacitances

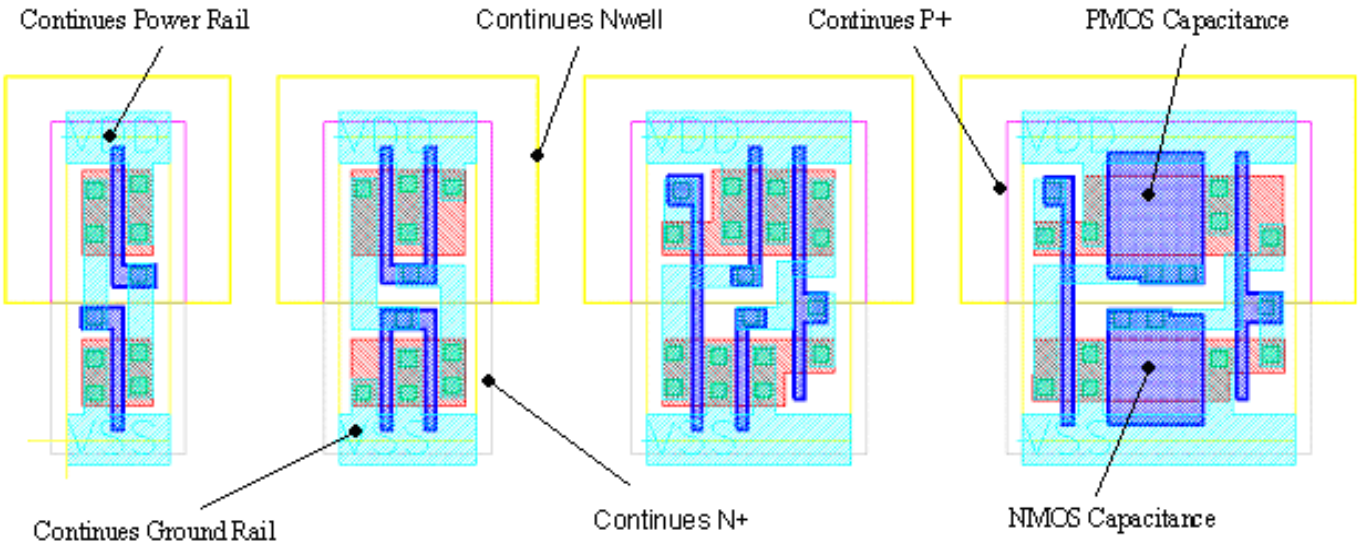


Figure 3. Filler Cells with P/N MOS Capacitances

Well-Tap Cells

The well-tap cell is used to tie NW to VDD and tie the substrate to VSS. Based on the corresponding UMC TLR, Well Tap cell should be pre-placed periodically every 30 um. This library provides four well-tap cells. Please refer to table 4 for the detail.

Table 4. Cell Description of Four Well-Tap Cells

Cell Name	Cell description	
WT2HM	Normal Well-Tap Cell	
WTBB2HM	This cell includes VBP & VBN pins that can be used to bias NWELL & PWELL	Well-Tap cells for special WELL bias
WTBP2HM	This cell includes VBP pin that can be used to bias NWELL	
WTBN2HM	This cell includes VBN pin that can be used to bias PWELL	

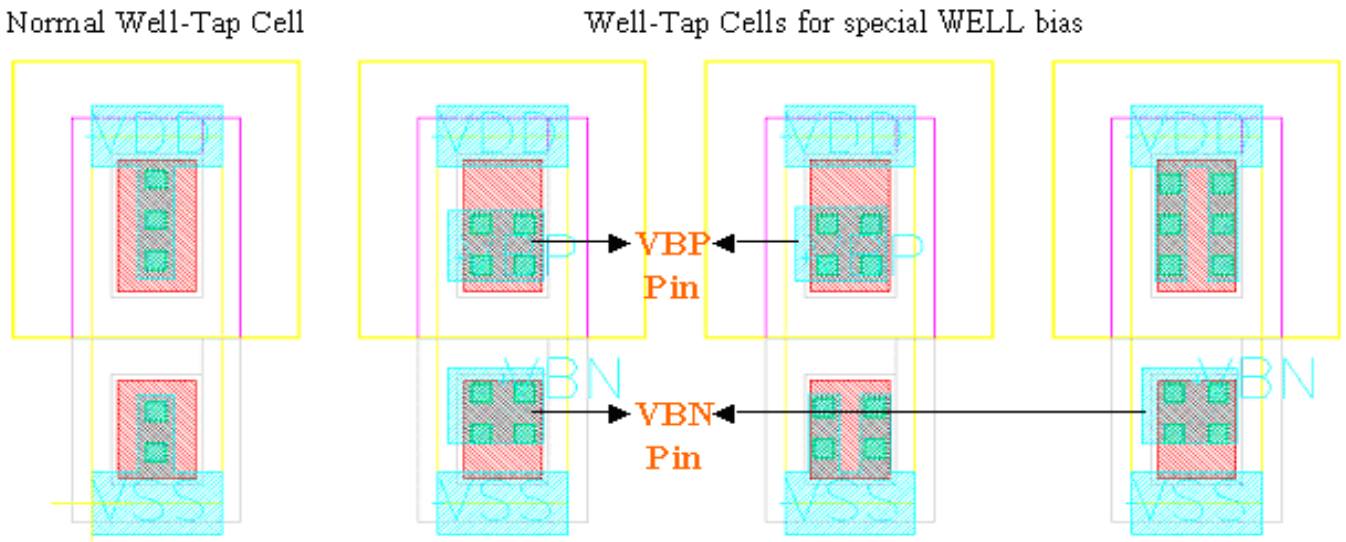


Figure 4. Layout Example of Well-Tap Cell

Well-Tap Cell Pre-placement Demonstration

The following section will guide users about the pre-placement of WT2HM cells. And the interval of the example between two WT2HM well-tap cells measures 50um.

Cadence SOC Encounter environment (v. 6.2)

Script command : addWellTap -cell WT2HM -maxGap 50 -checkboard

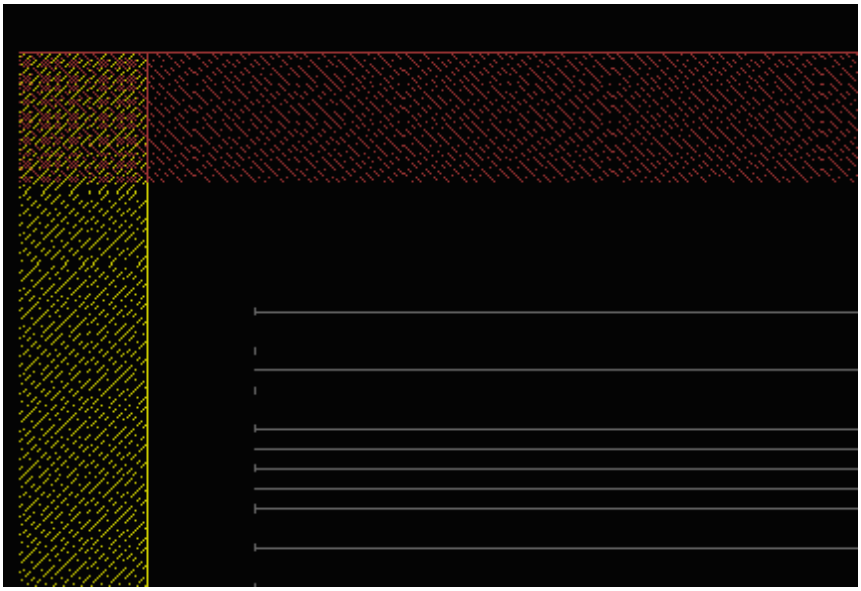


Figure 5. Before the addition of well-tap cells

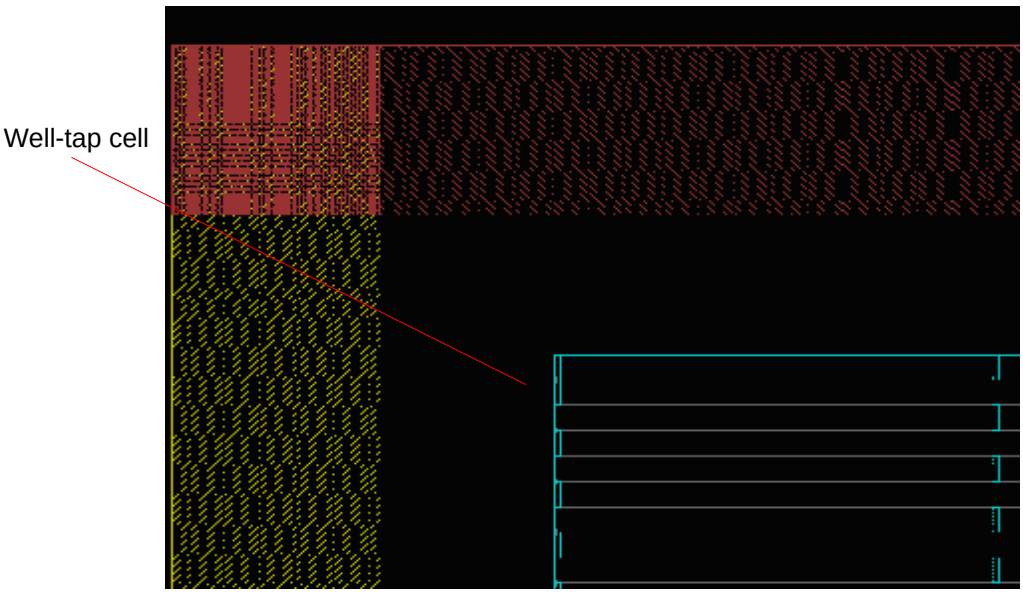


Figure 6. After the addition of well-tap cells

Synopsys Astro environment (v. 2005.09)

Script command:

```
axgArrayTapCell
setFormField "Array Tap Cell" "Tap Master Name" "WT2HM "
setFormField "Array Tap Cell" "Tap Cell Distance in Array" "50"
setFormField "Array Tap Cell" "Pattern" "Stagger Every Other Row"
formOK "Array Tap Cell"70
```

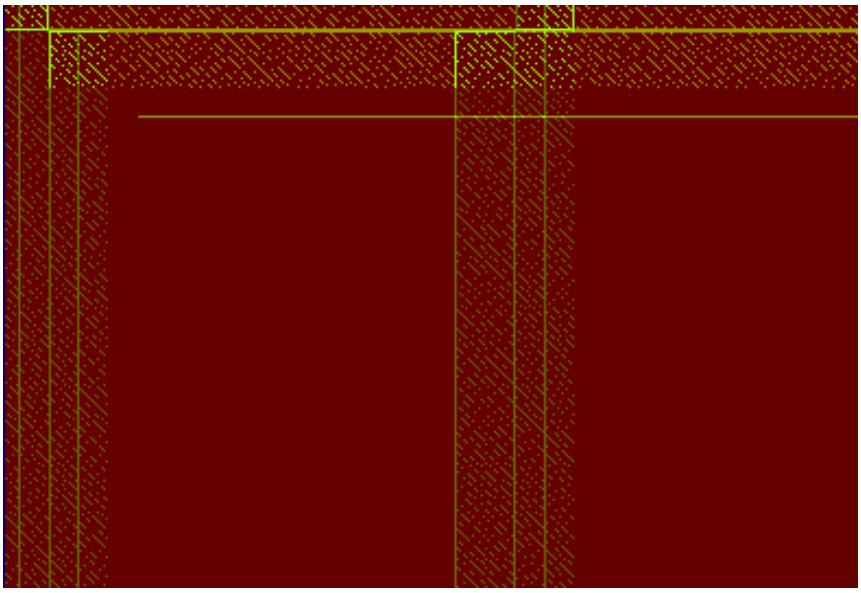


Figure 7. Before the addition of well-tap cells

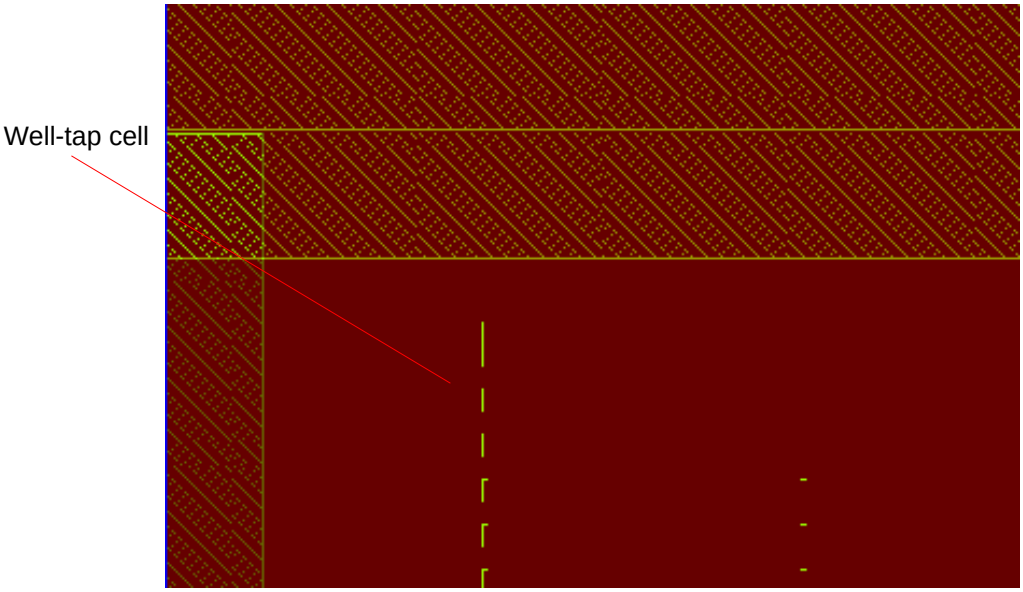


Figure 8. After the addition of well-tap cells