UMA11LSCEP15BDRLLN_A
UMC 0.11um Al 1.5V
EE2PROM Low Leakage
Tapless Standard Cell Library
Release Note

Revision History

Version	Date	Description
A01	2016/08/17	Initial publication

Table of Contents

General Description

This release note provides the technical information of Standard Cell Library "UMA11LSCEP15BDRLLN_A" which is implemented in UMC 0.11um Al 1.5V EE2PROM Low Leakage process. The specifications and operating conditions of library, cell numbers, cell types and EDA views are offered herein including the path of each EDA view in this library package for direct reference.

Please refer to the following content for a detailed description.

DSM Table

Item	Document No.	Version	Phase
DSM	G-01-EE2PROM11-2P8M-MMC/AL-DSM-8N	1.0	1
EDR	G-02-EE2PROM11-2P8M-MMC/AL-EDR-8N	0.2	1
TLR	G-03-EE2PROM11-2P8M-MMC/AL-TLR-8N	1.2	1
INTERCAP	G-04-EE2PROM11-2P8M-MMC/AL-INTERCAP-8N	0.4	1
SPICE	G-05-EE2PROM11-MMC/AL-SPICE-8N	1.0	1
LPE	G-DF-EE2PROM11-2P7M2T-MMC/AL/TOP_METAL12.85K/XRC-LPE-8N	0.4	1
DRC(CALIBRE)	G-DF-EE2PROM11-2P8M-MMC/AL/CALIBRE-DRC-8N	1.2	1
LVS(CALIBRE)	G-DF-EE2PROM11-2P8M-MMC/AL/CALIBRE-LVS-8N	0.2	3

Cell Types And Numbers

Cell Group	Cell Type	Cell Number
Combinational Cell	95	557
Sequential Cell	56	233
Arithmetic Cell	2	10
Special Cell	7	22
Total	**160**	**822**

EDA View Offering

Design Phase	Deliverable item
Schematic Capture	EDIF Symbols
	Composer Symbol Library
Synthesis	Synopsys Synthesis Model
	Synopsys Synthesis Symbol
Verilog Simulation	Verilog Simulation Model
Testability	Synopsys liberty Model for DFT Compiler
	Fastscan ATPG Model
Static Timing Analysis	Synopsys liberty Model for Primetime
AP&R	Astro CEL/FRAM Views
	Astro Technology Files for metal-options
	CLF Model
	LEF (5.5) Files for SOC Encounter
	SoC Encounter Technology Files
Post Layout Simulation	SPICE Netlist with Interconnect RC
Layout Verification	SPICE LVS Netlist
	Physical Library (GDSII)

EDA Tool

EDA Tools	Version
Cadence Abstract Generator	**5.10.41.500.5.110**
Cadence Composer	**ic_615-501**
Cadence Conformal LEC	**confrml_1510-120**
Cadence NC-Sim IUS	**ius_1510-008**
Cadence SoC Encounter	**edi_1413-000**
Mentor Calibre DRC	**calibre_20152-3627**
Mentor Calibre LPE	**calibre_20152-3627**
Mentor Calibre LVS	**calibre_20152-3627**
Mentor Fastscan ATPG	**dft_20084-10**
Mentor ModelSim	**modelsim_60b**
SiliconSmart	**siliconsmart_201206-sp2**
SpringSoft Laker	**laker_2014-06**
Synopsys Design Compiler	**synthesis_201409-sp3**
Synopsys HSPICE	**hspice_201409-sp2-3**
Synopsys ICCompiler	**iccompiler_201506-sp2**
Synopsys Milkyway	**milkyway_201409-sp5**
Synopsys PrimeTime	**primetime_201512-sp3**

Deliverable Content

File Name or Path	Description
doc	A directory containing the files of databook.pdf, application_note.pdf, release_note.pdf and cell list
cir	A directory containing the netlist file after RC extraction
lvs_netlist	A directory containing the netlist file for LVS
gds	A directory containing the GDSII file
synopsys	A directory containing the files of Synopsys NLDM liberty models and the files before and after compiling.[2]
symbol	A directory containing the Cadence composer symbol and EDIF symbol
verilog	A directory containing verilog model
fastscan	A directory containing ATPG model
celtic	A directory containing celtic model
lef	A directory containing lef macro files and technology files
milkyway	A directory containing ICC technology files and database

Note:

(1) Words in red represent the directory names.

(2) The Synopsys liberty models were characterized with state-dependent timing mode for combinational cells and state-dependent timing mode for sequential cells, and the setup/hold time was calculated by using degrade mode. (use 10% for sequential cells and 1% for clock-gating cells)

(3) It is strongly recommended that the user takes care of the design margin carefully due to the degradation mode has been used for timing constraints.

(4) Some cell with diode in the lvs_netlist is for LVS check usage only. For pre-simulation usage purpose, the user need to replace "DZ0 A B DIODE_NAME area='X*Y'p pj='2(X+Y)'u" to "XZ0 A B DIODE_NAME w='X'u l='Y'u".

(5) For pre-simulation usage purpose, please use the following option for spice netlist.

```
.option scale = 0.9
```

False Violation

•False Error of ERC

The following ERC violations that can be waived.

PATHCHK_GND
PATHCHK_PWR
WRONG_FLOATING_WEL
WRONG_FLOATING_NTAP
WRONG_FLOATING_PTAP
WRONG_FLOATING_PSUB
PATHCHK_NLABELED

•DRC Violation

The following DRC errors for a single cell are false violations that can be waived.

6A.1_DF.R
6A.8_PLY1.R1
6A.9.1_N_DF_P_PU.S7.PW
6A.10.1_P_DF_N_PU.S7.NW
6D.1_M1.R1.DEN
6D.1_M1.R2.DEN
6D.3_M2.R1.DEN
6D.3_M2.R2.DEN
6D.3_M3.R2.DEN
6D.3_M4.R2.DEN
6D.3_M5.R2.DEN
6D.3_M6.R2.DEN
6D.6_M7.R2.DEN
6D.7_M8.R2.DEN
8.B.2_DC.L2.ME1
8.B.2_DC.L2.ME2

Silicon Verification

FAB	Status
8N	In developing