jwq40260

发行版本 *0.0*

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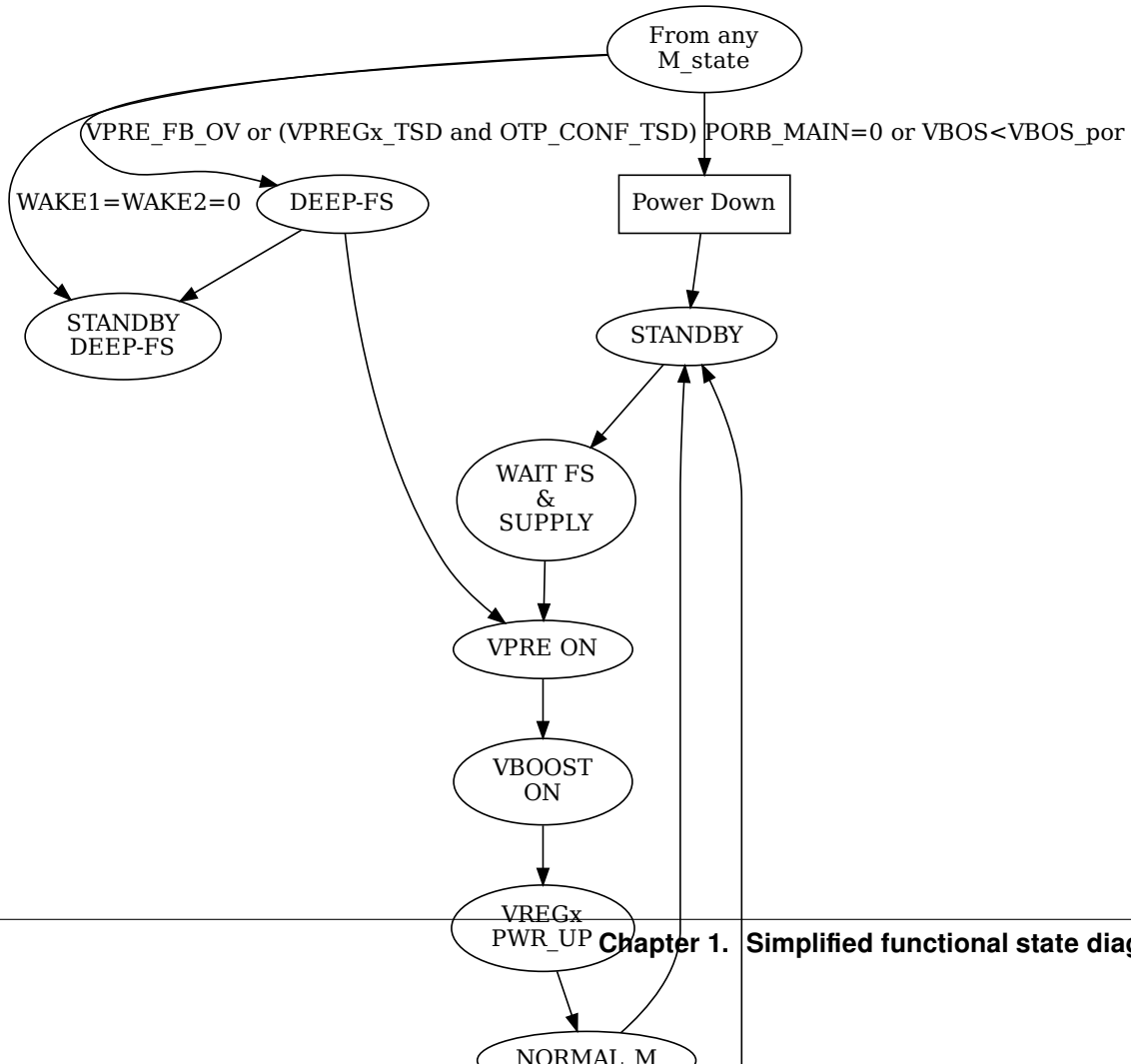
Contents:

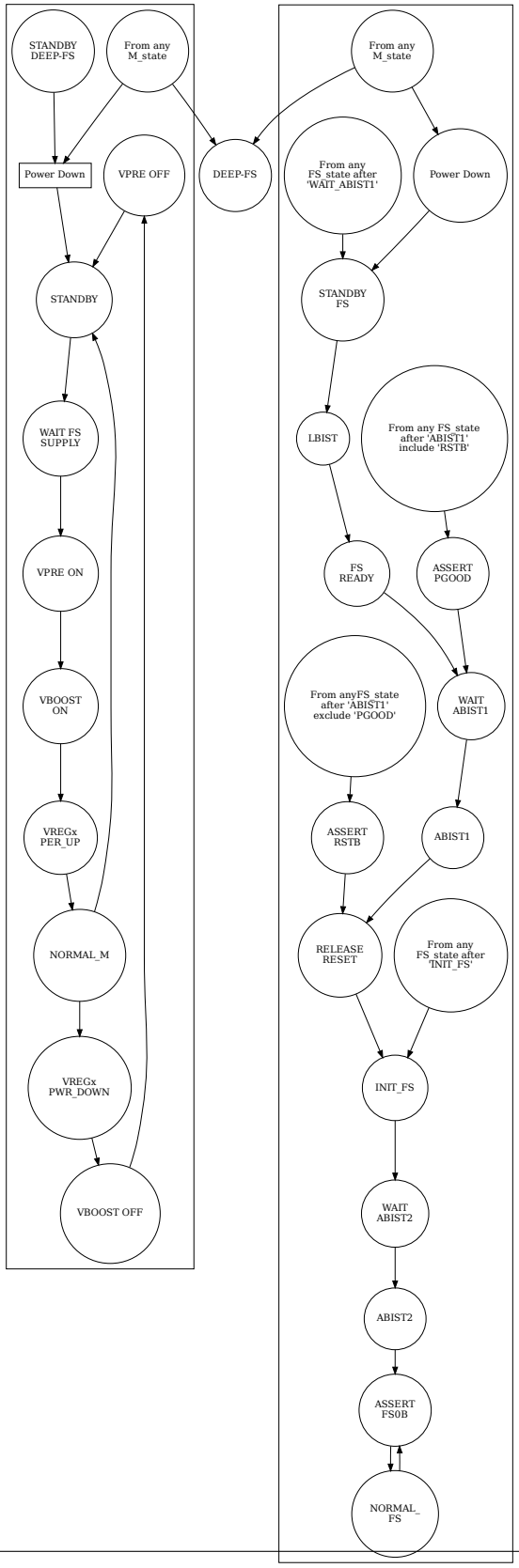
CHAPTER 1

Simplified functional state diagram

1.1 graphviz

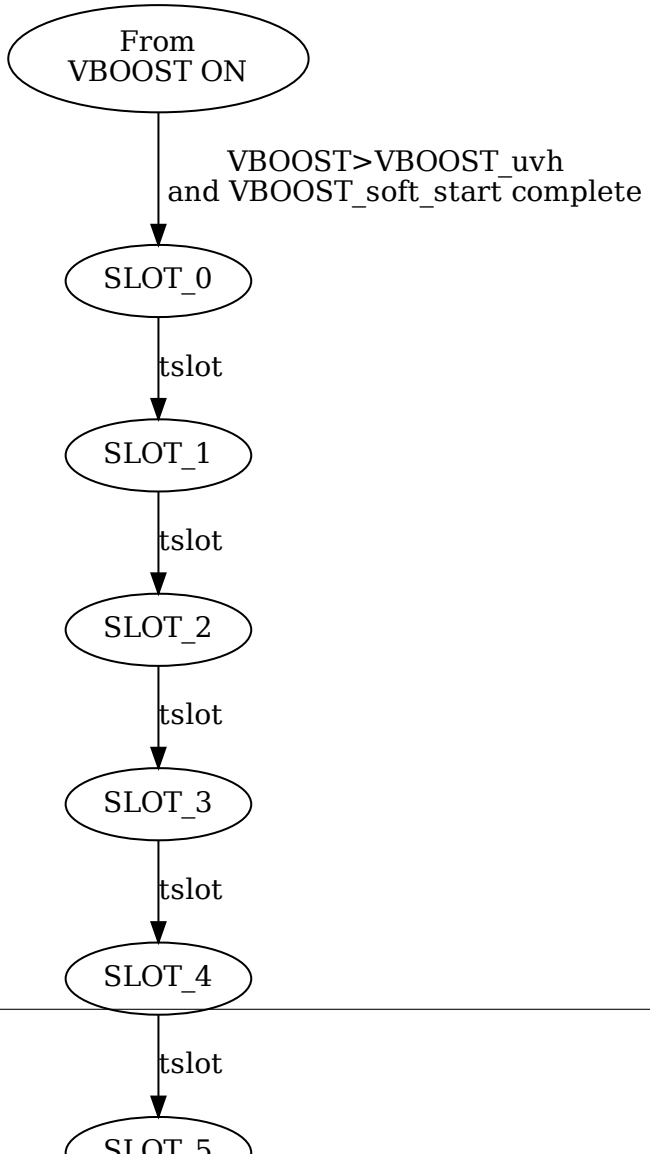


1.2 graphviz1



CHAPTER 2

Power sequencing



CHAPTER 3

Debug mode entry

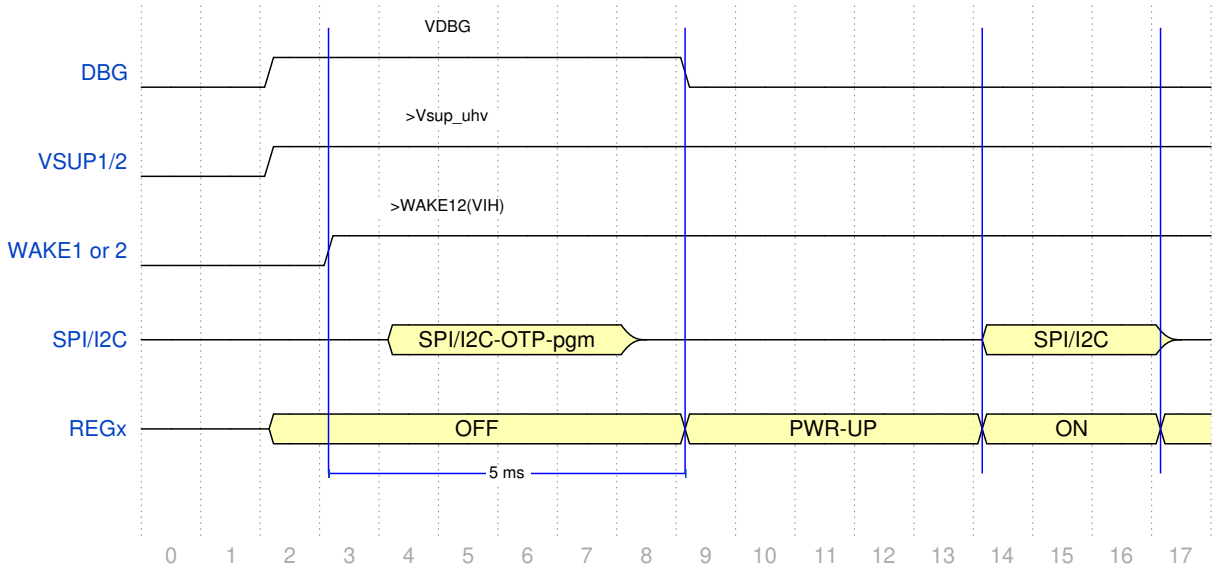
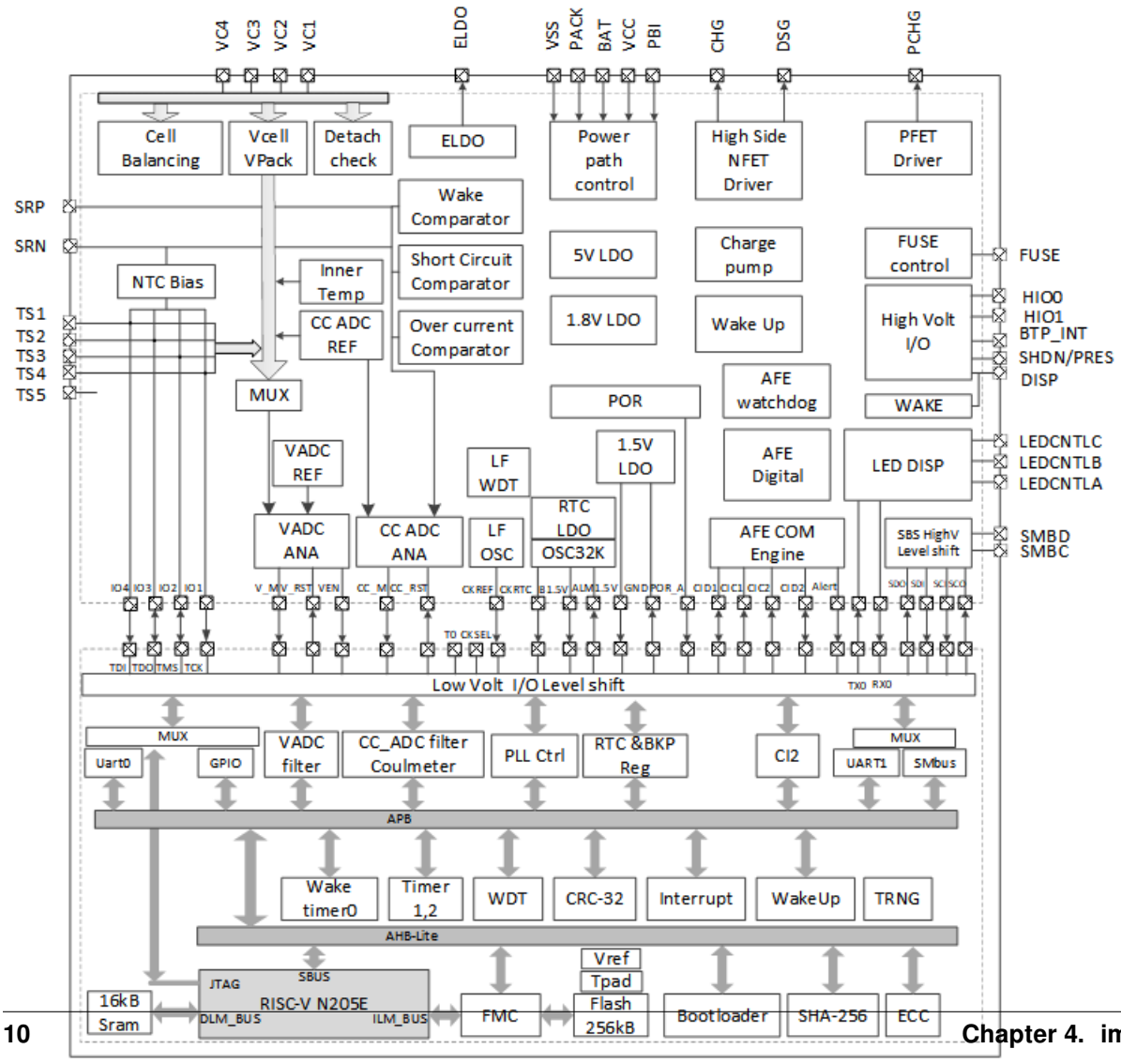


Figure 8 Debug mode entry

CHAPTER 4

image



CHAPTER 5

excel

表 5.1: registers summary

0x40070050 0x01	PHASE_CONFIG						
	8	[7:5]	PH_CFG	RW	3’b0	000b = 1+1+1+1; 100b = 2+1+1; 101b = 2+2 110b = 3+1 111b = 4+0 Others are reserved	
	===	[4:0]	CHECK	RW	5’b0	1010b = The writing command is valid data; Others = The	

CHAPTER 6

Register1

6.1 trim_vadc

表 6.1: trim_vadc

Bit	23	22	21	20	19	18	17	16
Write	0	0	0	0	0	0	0	0
Read	COM_ERR	COM_ERR	COM_ERR	COM_ERR	COM_ERR	COM_ERR	COM_ERR	COM_ERR
Reset	0	0	0	0	0	0	0	0

6.2 trim_ptc

表 6.2: trim_ptc

Address 32’h80000000			offset addr 32’h00000000				Default Value 32’h00000000			Name trim_ptc						
for reset control																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Typ	RSV															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Tpy	Reserved									R/W	RO	W1C	R/W			
Bit	Fld Name		Reset		Description											
31:0	bit31		00000000		11111111111111111111											
30	bit31				11111111111111111111											
29	bit31				11111111111111111111											
28	bit31				11111111111111111111											
27	bit31				11111111111111111111											
26	bit31				11111111111111111 2’b00 - enable 2’b01 - disable											

CHAPTER 7

Device

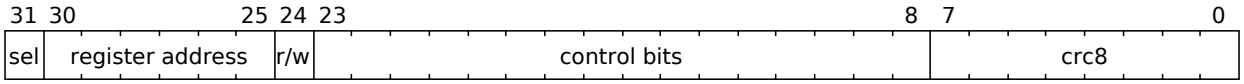
7.1 Cyclic Redundant Check generation

An 8 bit CRC is required for each Write and Read SPI and I2C command. Computation of a cyclic redundancy check is derived from the mathematics of polynomial division, modulo two. The CRC polynomial used is x^8+x^4+x^3+x^2+1 (identified by 0x1D) with a SEED value of hexadecimal ‘0xFF’ The following is an example of CRC encoding HW implementation:

7.2 spi interface

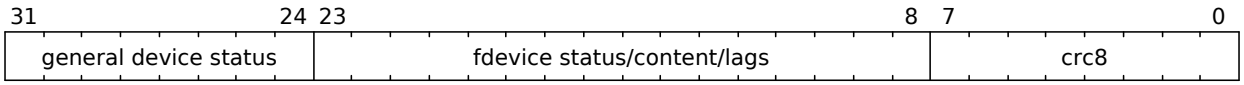
7.2.1 SPI interface overview

MOSI,master out slave in bits



–Bit 31: main or fail-safe registers selection –Bit 30 to 25: register address –Bit 24: read/write –Bit 23 to 8: control bits –Bit7 to 0: cyclic redundant check (CRC)

MISO,master in slave out bits



–Bit 31-24: general device status –bits 23 to 8: extended device status, or device internal control register content or device flags –Bit7 to 0: cyclic redundant check (CRC)

The digital SPI pins (CSB, SCLK, MOSI, MISO) are referenced to VDDIO.

7.2.2 SPI CRC calculation and results

7.2.3 Spi interface timing

CHAPTER 8

NVM-OTP

8.1 待确认

MACRO NAME: DesignWare slp_b_tsmc180bcd50_128x8_cm8s_ab 供电共有 VDD(1V8) VPP(8V18) VRR(3V) VREF(==VDD or external IO) , size 是 8bit

8.1.1 供电电压

两种供电方式，首先确认 IPS controls 是不是集成在 IP 里面，能否分离。如果使用 IPS 供电那只需要提供 VDD（1V8) 和 VDD_IO(5V)

Table 1-1. Configuration Summary

Parameter	Supply	Min[1]	Typ	Max[1]	Units
General					
Process Node			TSMC 180nm BCD50 1.8/5.0 V		
Configuration Metal Layers			M4 is thin		
Memory size			1k		
I/O Bus width (n)			8 bits		
Organization S x R x CM x bits			1 arrays x 16 rows x 8 Column Mux x 8 bits		
			128 words x 8 bits (Single Cell Mode)		
Number of Arrays			1		
Address Bus width			7		
Area			X = 188.81µm x Y = 92.18µm Area = 0.017mm^2		
Retention		10			Years
Power Supply	VDD	1.62	1.8	1.98	V
Current (Standby)	VDD		0.04	3.5	µA
Power Supply	VRR	2.7	3.0	3.3	V
Current (Standby)	VRR		0.01	0.1	µA
Program (Single Bit)					
Power Supply	VPP	7.9	8.15	8.4	V
Current[2]	VPP		250		µA
Time			100		µs/bit
Temperature Range		-40	+25	+125	°C
Read (Single ended, 8 Bits)					
Current (not including standby)	VDD	3.8	4.7	6.1	µA/MHz
Current (not including standby)	VRR	0.9	1.1	1.5	µA/MHz
Temperature Range		-40	+25	+150	°C
Storage					
Temperature Range		-55	+25	+150	°C

[1]: Across the conditions described in Corner Conditions on page 18.
[2]: One bit at a time programming.

8.1.2 位宽大小

jwq40260 spi/i2c 接口格式使用的是 8+16+8(addr+data+crc), 内部总线也是使用 16 位。如果使用的是 16 位的数据，那可以直接使用，否则需要数字逻辑转接匹配位宽。

OTP Name	Config	Bitcount[1]	X [µm]	Y [µm]	Area [mm^2]
slp_b_tsmc180bcd50_128x8_cm8s	128x8	1024	189	92	0.02
slp_b_tsmc180bcd50_256x8_cm16s	256x8	2048	243	92	0.02
slp_b_tsmc180bcd50_512x8_cm16s	512x8	4096	243	117	0.03
slp_b_tsmc180bcd50_512x8_cm16d[2]	512x8	4096	243	142	0.04
slp_b_tsmc180bcd50_512x8_cm16d_r20	512x8	4096	243	161	0.04
slp_b_tsmc180bcd50_256x16_cm16s	256x16	4096	352	92	0.03
slp_b_tsmc180bcd50_1kx8_cm16s	1kx8	8192	243	167	0.04
slp_b_tsmc180bcd50_1kx8_cm16d[2]	1kx8	8192	243	192	0.05
slp_b_tsmc180bcd50_1kx8_cm16d_r20	1kx8	8192	243	211	0.05
slp_b_tsmc180bcd50_512x16_cm16s	512x16	8192	352	117	0.04
slp_b_tsmc180bcd50_512x16_cm16d[2]	512x16	8192	352	142	0.05
slp_b_tsmc180bcd50_512x16_cm16d_r20	512x16	8192	352	161	0.06
slp_b_tsmc180bcd50_256x32_cm16s	256x32	8192	571	92	0.05

CHAPTER 9

Indices and tables

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