Instruction Formats and Addressing Modes

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Instruction Formats

- Three-Address Instruction Format
- Two-Address Instruction Format
- One-Address Instruction Format
- Zero-Address Instruction Format

Example: (A + B) * (C + D)

- **Three-Address Instructions:**

```
ADD    R1, A, B      R1 ← M[A] + M[B]
ADD    R2, C, D      R2 ← M[C] + M[D]
MUL    X, R1, R2     M[X] ← R1 * R2
```

- **Two-Address Instructions:**

```
MOV    R1, A         R1 ← M[A]
ADD    R1, B         R1 ← R1 + M[B]
MOV    R2, C         R2 ← M[C]
ADD    R2, D         R2 ← R2 + M[D]
MUL    R1,R2         R1 ← R1 * R2
MOV    X, R1         M[X] ← R1
```

Example: (A + B) * (C + D)

- **One-Address Instructions:**

```
LOAD    A    AC ← M[A]
ADD     B    AC ← AC + M[B]
STORE   T    M[T] ← AC
LOAD    C    AC ← M[C]
ADD     D    AC ← AC + M[D]
MUL     T    AC ← AC * M[T]
STORE   X    M[X] ← AC
```

- **Zero-Address Instructions:**

```
PUSH    A    TOS ← A
PUSH    B    TOS ← B
ADD          TOS ← (A + B)
PUSH    C    TOS ← C
PUSH    D    TOS ← D
ADD          TOS ← (C + D)
MUL          TOS ← (C + D) * (A + B)
POP     X    M[X] ← TOS
```

TOS*: Top of Stack*

Example: (A + B) * (C + D)

- **RISC Instructions:**

```
LOAD    R1, A          R1 ← M[A]
LOAD    R2, B          R2 ← M[B]
LOAD    R3, C          R3 ← M[C]
LOAD    R4, D          R4 ← M[D]
ADD     R1, R1, R2     R1 ← R1 + R2
ADD     R3, R3, R2     R3 ← R3 + R4
MUL     R1, R1, R3     R1 ← R1*R3
STORE   X, R1          M[X] ← R1
```

Addressing Modes

1. **Implied Mode**: The operands are specified implicitly in the definition of instruction (Example: Zero Address Instructions).

2. **Immediate Mode**: The operand is specified in the instruction itself.

3. **Register Mode**: The instruction specifies a register in the CPU that is holding the operand.

4. **Register Indirect Mode**: The instruction specifies a register in the CPU whose contents give the address of the operand in the memory.

5. **Autoincrement mode**: This is similar to register indirect mode except that the register is incremented *after* its value is used to access memory.

6. **Autodecrement mode**: This is similar to register indirect mode except that the register is decremented *before* its value is used to access memory.

Addressing Modes Cont.

7. **Direct Address Mode**: The effective address is equal to the address part of the instruction.

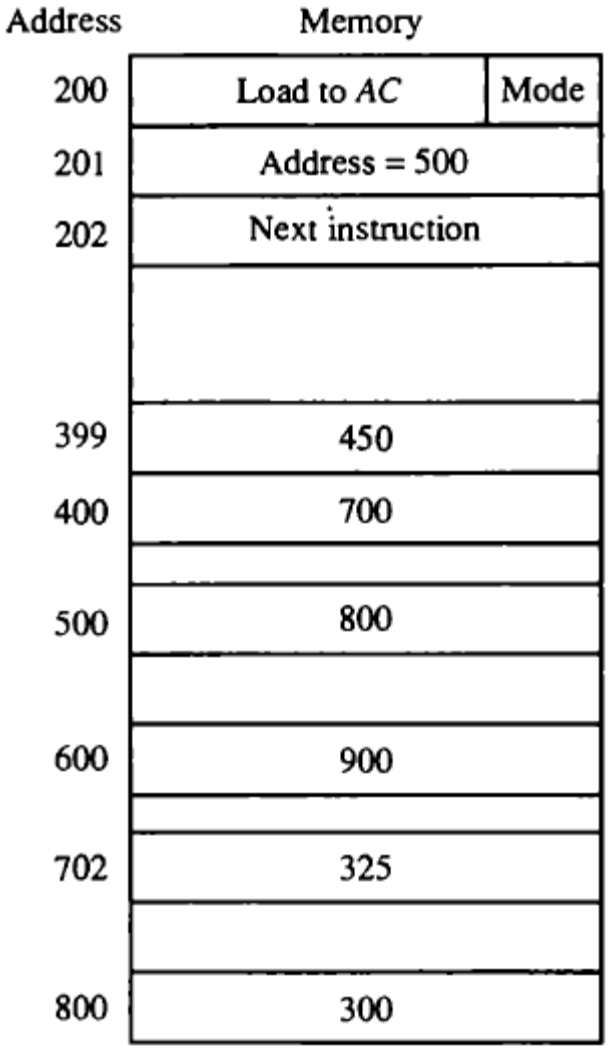
8. **Indirect Address Mode**: The address field of the instruction gives the address where the effective address is stored in memory.

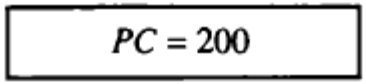
9. **Relative Address Mode**: The content of the program counter is added to the address part of the instruction in order to obtain the effective address.

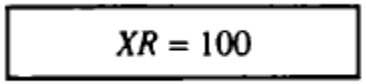
10. **Indexed Addressing Mode**: The content of an index register is added to the address part of the instruction in order to obtain the effective address.

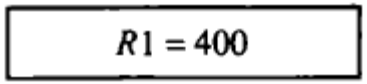
11. **Base Register Addressing Mode**: The content of a base register is added to the address part of the instruction in order to obtain the effective address.

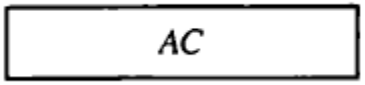
Numerical Example











Addressing Mode	Effective Address	Content of *AC*
Direct address	500	800
Immediate operand	201	500
Indirect address	800	300
Relative address	702	325
Indexed address	600	900
Register	—	400
Register indirect	400	700
Autoincrement	400	700
Autodecrement	399	450

REFERENCE

Morris Mano, Computer System Architecture, Prentice-Hall of India.