Adders play a vital role in performing any mathematical operation, especially in ALUs. In this git repository, the design of 2 bit half adder is explained in 28nm technology..

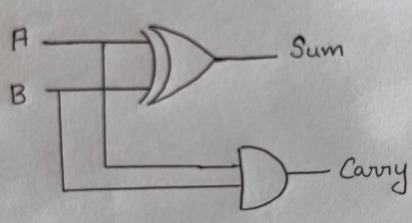
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**Introduction**

A half adder is a digital circuit that accepts 2 bits as input and generates 2 bits, a Sum and a Carry bit. Fig 1, shows a half adder.The mathematical formula of half adder is:

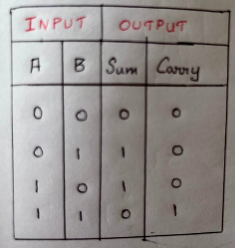
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**Fig 1: Circuit diagram of Half Adder using Logic Gates**

The circuit is designed using 2 logic gates : XOR and AND gate. Here, the same two inputs are given to the two logic gates. Thus, when a voltage is supplied, the two gates receive the same input at the same time, since they are connected. Using the CMOS logic, XOR gate is implemented, which generates the Sum bit. Carry bit is obtained using AND logic.

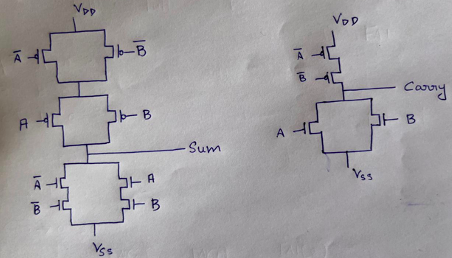
The truth table of half adder is shown in Fig 2.



**Fig 2: Truth Table of Half Adder**

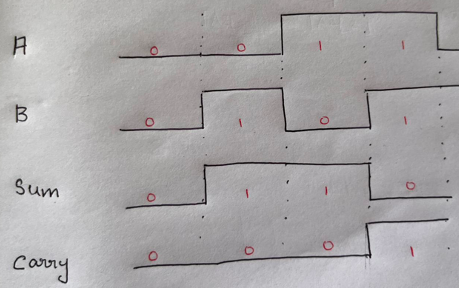
**Reference Circuit Diagram**

Fig 3, represents the transistor level implementation of half adder. In CMOS logic, PMOS and NMOS transistors are used. For the complete half adder circuit 12 transistors are used.

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**Fig 3: Half Adder implementation using CMOS logic**

**Reference Waveform**

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**Fig 4: Expected Waveform**

**Tools Used**

1. PDK (Process Design Kit)

The schematics were drawn using the transistors, voltage sources from Synopsys PDK in 28nm technology.

1. Synopsys Custom Compiler

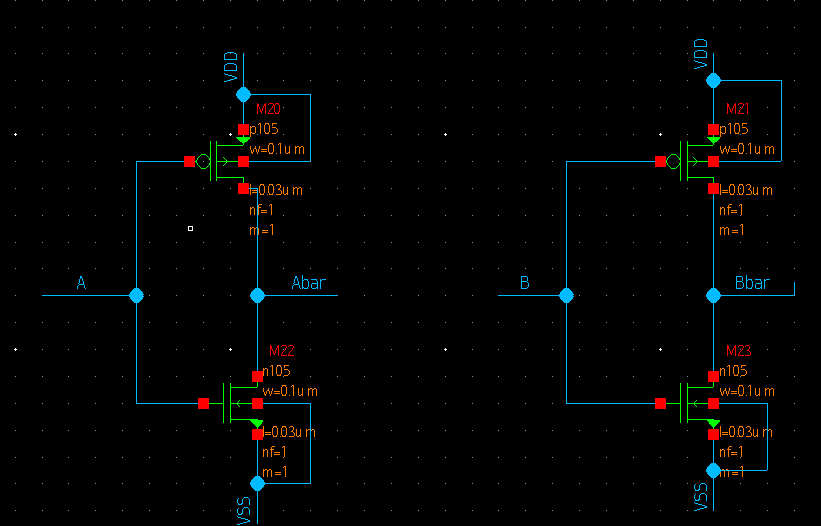
Synopsys Custom Compiler™ provides several features for design drawing, error checking and its analysis.

1. PrimeSim Spice

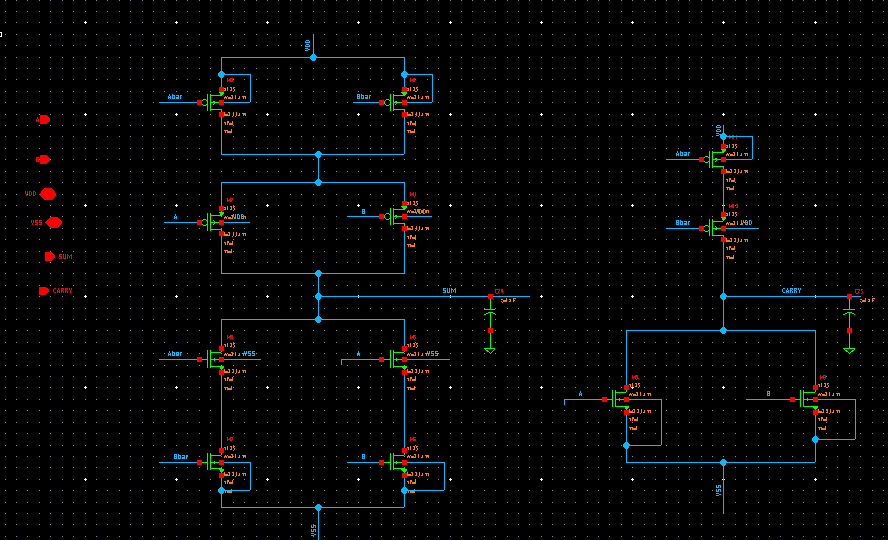
For simulations and displaying waveform PrimeSim Spice tool was used.

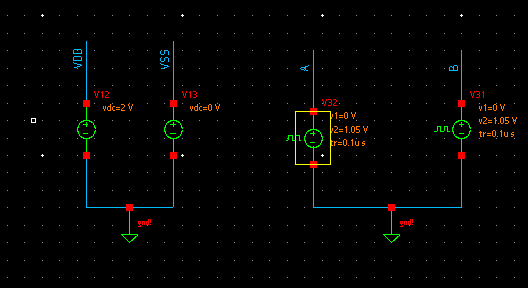
**Simulations Performed in Synopsys Tool**

1. **Generation of Abar and Bbar inputs using inverter**

****

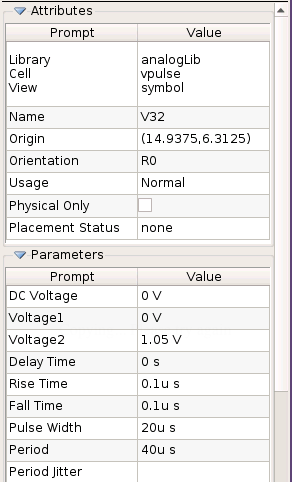
1. **Half Adder Schematics**

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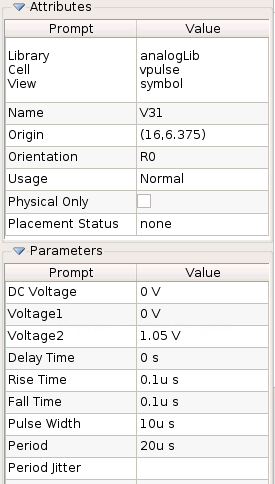
1. **Voltage Sources for A, B, Vdd and VSS**

Here, vpulse cell (from analog lib in PDK)) is used to generate voltages for A and B. Vdc cell is (from analog lib in PDK) is used to generate voltages for Vdd and Vss.

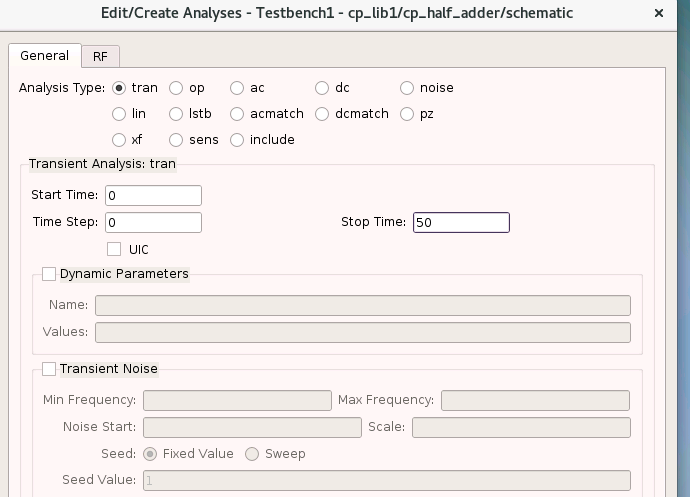
1. Parameters set for Voltage source of Input B



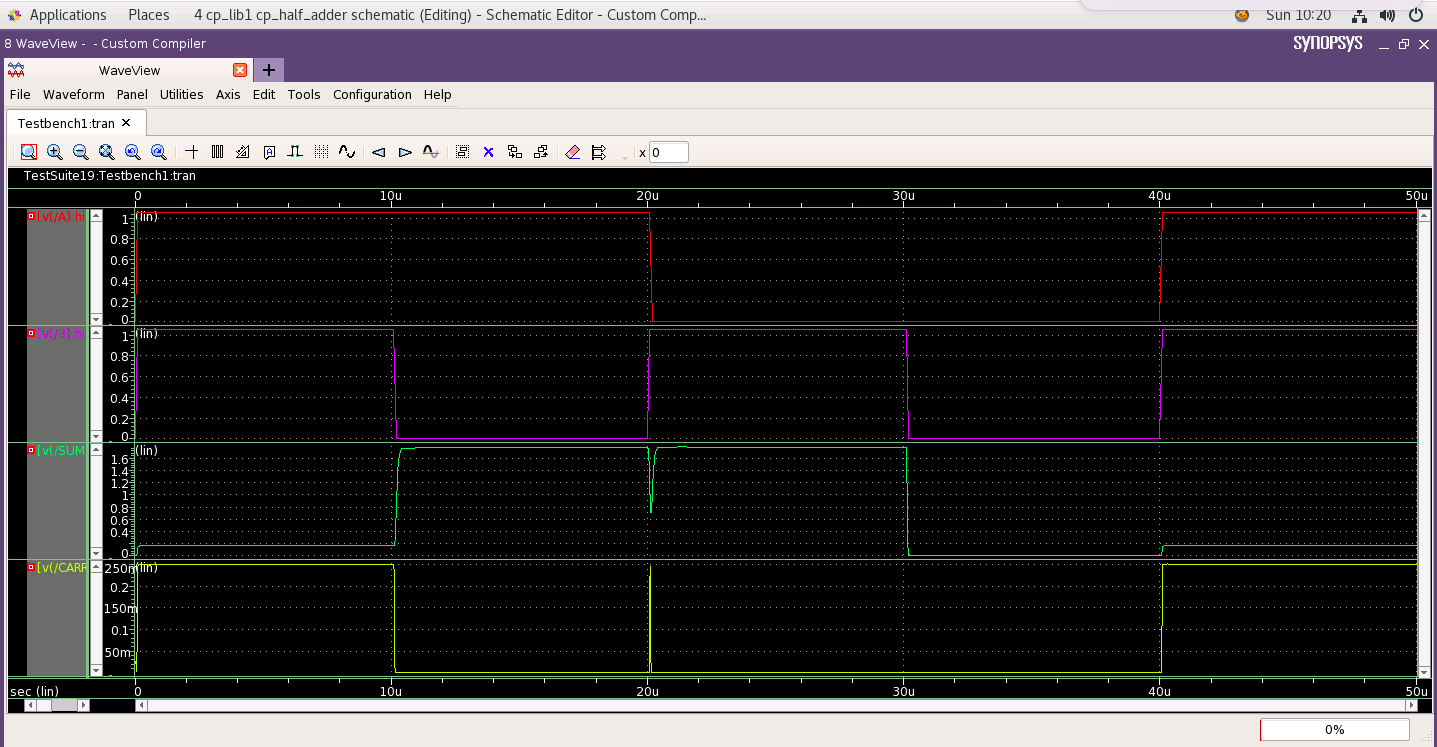
d. Parameters set for voltage source for input A



Parameters set for transient response



Output Waveform



Netlist

The netlist is given here :

Author

Darsana P M

Acknowledgements

* Cloud Based Analog IC Design Hackathon
* Synopsys India
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* Kunal Ghosh, Co-founder, VSD Corp. Pvt. Ltd.
* Chinmay panda, IIT Hyderabad
* Sameer Durgoji, NIT Karnataka

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2. U. Ko, T. Balsara and W. Lee, "Low-power design techniques for high-performance CMOS adders", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 3, no. 2, pp. 327-333, 1995.