# Chapter 14 - Semiconductor Electronics: Materials, Devices and Simple Circuits

**Multiple Choice Questions (MCQs)**

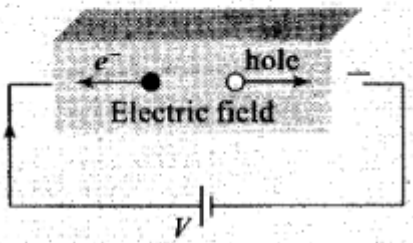
**Single Correct Answer Type**

**Question 1. The conductivity of a semiconductor increases with increase in temperature, because**
**(a) number density of free current carries increases**
**(b) relaxation time increases**
**(c) both number density of carries and relaxation time increase**
**(d) number density of carries increases, relaxation time decreases but effect of decrease in relaxation time is much less than increase in number density .**
**Solution:** (d)

**Key concept:** *Conductivity of Semiconductor:*

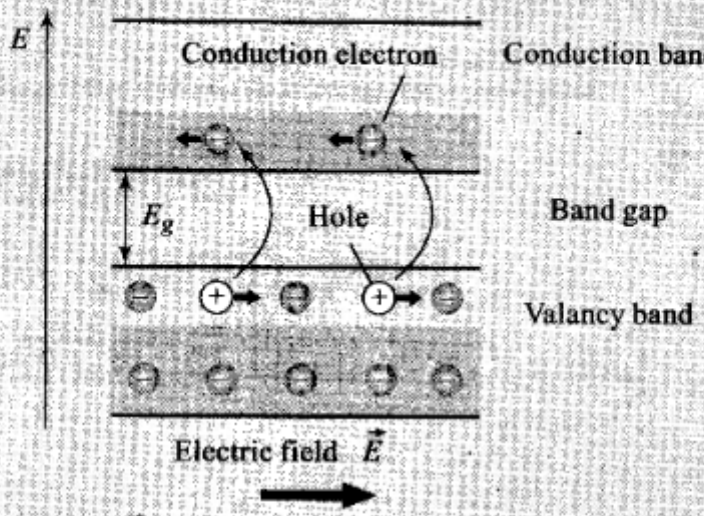
(1) In intrinsic semiconductors $n_e = n_h$. Both electron and holes contributes in current conduction.

(2) When some potential difference is applied across a piece of intrinsic semiconductor current flows in it due to both electron and holes, i.e. $i = i_e + i_h \Rightarrow i = eA[n_e v_e + n_h v_h]$




(3) As we know $\sigma = \frac{J}{E} = \frac{i}{AE}$. Hence conductivity of semiconductor is $\sigma = e[n_e\mu_e + n_h\mu_h]$; where $v_e$ = drift velocity of electron, $v_h$ = drift velocity of holes, $E$ = Applied electric field, $\mu_e = \frac{v_e}{E}$ = mobility of electron and $\mu_h = \frac{v_h}{E}$ = mobility of holes

(4) Motion of electrons in the conduction band and of holes in the valence band under the action of electric field is shown below:




(5) At absolute zero temperature (0 K) conduction band of semiconductor is completely empty, i.e., $\sigma = 0$. Hence the semiconductor behaves as an insulator.

We know that $\sigma = \frac{ne^2\tau}{m}$,

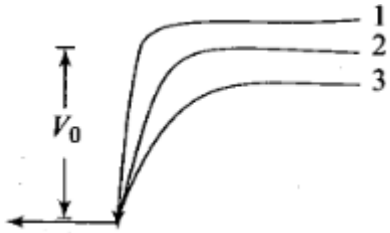
So, $\sigma \propto n\tau$

where, $n$ = number density and $\tau$ = relaxation time

In semiconductors conductivity increases with increase in temperature, because the number density of current carries increases, relaxation time decreases but effect of decrease in relaxation is much less than increase in number density.

**Question 2.**

In figure given alongside, $V_0$ is the potential barrier across a *p-n* junction, when no battery is connected across the junction.




(a) 1 and 3 both correspond to forward bias of junction

(b) 3 corresponds to forward bias of junction and 1 corresponds to reverse bias of junction

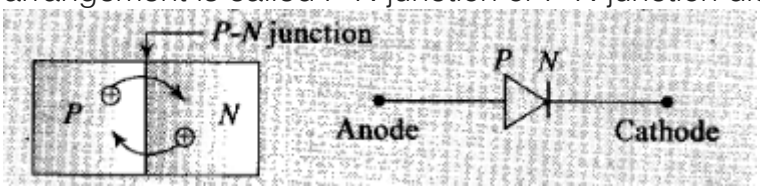
(c) 1 corresponds to forward bias and 3 corresponds to reverse bias of junction

(d) 3 and 1 both correspond to reverse bias of junction

**Solution:** (b)

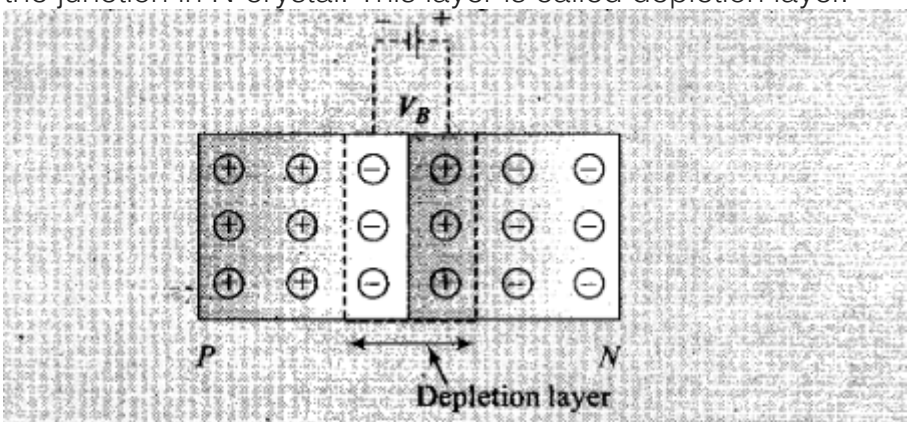
Key concept: P-N Junction Diode:

– When a P-type semiconductor is suitably joined to an N-type semiconductor, then resulting arrangement is called P-N junction or P-N junction diode.




(1) Depletion region: On account of difference in concentration of charge carrier in the two sections of P-N junction, the electrons from N-region diffuse through the junction into P-region and the hole from P region diffuse into N-region.

Due to diffusion, neutrality of both N and P-type semiconductor is disturbed, a layer of negative charged ions appear near the junction in the P-crystal and a layer of positive ions, appears near the junction in N-crystal. This layer is called depletion layer.




(i) The thickness of depletion layer is 1 micron = $10^{-6}$ m.

(ii) Width of depletion layer $\propto \frac{1}{\text{Dopping}}$

(iii) Depletion is directly proportional to temperature.

(iv) The *P-N* junction diode is equivalent to capacitor in which the depletion layer acts as a dielectric.

(2) Potential barrier: The potential difference created across the P-N junction due to the diffusion of electron and holes is called potential barrier.

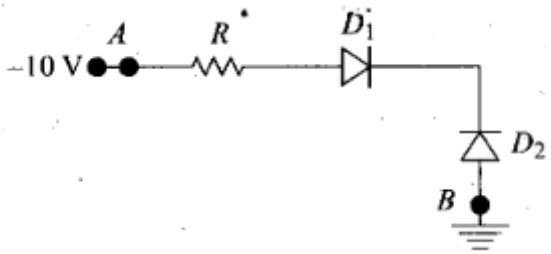
For *Ge*, $V_B = 0.3$ V and for silicon $V_B = 0.7$ V

On the average the potential barrier in *P-N* junction is ~0.5 V and the width of depletion region $\sim 10^{-6}$ m.

So the barrier electric field $E = \frac{V}{d} = \frac{0.5}{10^{-6}} = 5 \times 10^5$ V/m

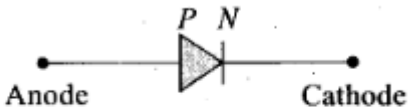
Height of potential barrier is decreases when p-n junction is forward biased, it opposes the potential barrier junction, when p-n junction is reverse biased, it supports the potential barrier junction, resulting increase in potential barrier across the junction.

**Question 3. In figure given on next page, assuming the diodes to be ideal**
**(a) $D_1$ is forward biased and $D_2$ is reverse biased and hence current flows from A to B**
**(b) $D_2$ is forward biased and $D_1$ is reverse biased and hence no current flows from B to A and vice-versa**
**(c) $D_1$ and $D_2$ are both forward biased and hence current flows from A to B**
**(d) $D_1$ and $D_2$ are both reverse biased and hence no current flows from A to B and vice-versa**



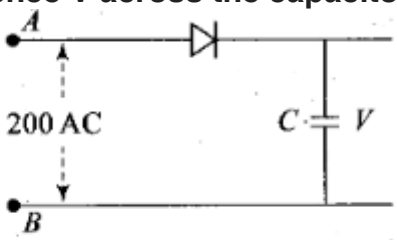

**Solution:**

**(b)** A symbol of the diode is represented like this:



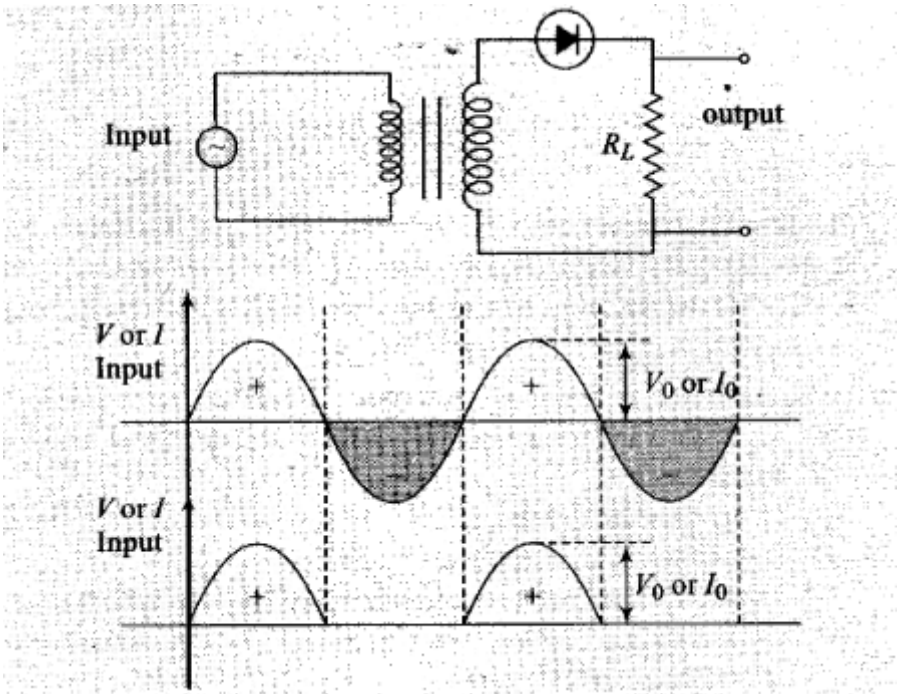

In this problem first we have to check the polarity of the diodes. −10 V is the lower voltage in the circuit. Now $p$-side of $p$-$n$ junction $D_1$ is connected to lower voltage and $n$-side of $D_1$ to higher voltage. Thus $D_1$ is reverse biased.
Now, let us analyse 2nd diode of the given circuit. The $p$-side of $p$-$n$ junction $D_2$ is at higher potential and $n$-side of $D_2$ is at lower potential. Therefore $D_2$ is forward biased.
Hence, current flows through the junction from $B$ to $A$.

**Question 4. A 220 V AC supply is connected between points A and B (figure). What will be the potential difference V across the capacitor?**




(a) 220 V (b) 110 V (c) 0 V (d) $220\sqrt{2}$ V

**Solution:** (d)
Key concept: Half wave rectifier: When the P-N junction diode rectifies half of the ac wave, it is called half wave rectifier.




(i) During positive half cycle,
Diode ⟶ forward biased
Output signal ⟶ obtained

(ii) During negative half cycle,
Diode ⟶ reverse biased
Output signal ⟶ not obtained

(iii) Output voltage is obtained across the load resistance $R_L$. It is not constant but pulsating (mixture of *ac* and *dc*) in nature.

(iv) Average output in one cycle

$$I_{dc} = \frac{I_0}{\pi} \text{ and } V_{dc} = \frac{V_0}{\pi};\ I_0 = \frac{V_0}{r_f + R_L}$$

($r_f$ = forward biased resistance)

(v) r.m.s. output: $I_{rms} = \frac{I_0}{2}, V_{rms} = \frac{V_0}{2}$

As *p-n* junction diode will conduct during positive half cycle only, during negative half cycle diode is reverse biased. During this diode will not give any output. So, potential difference across capacitor $C$ = peak voltage of the given AC voltage

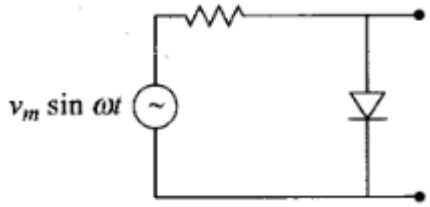
$$= V_0 = V_{rms}\sqrt{2} = 220\ \sqrt{2}\ \text{V}$$

**Question 5. Hole is**
**(a) an anti-particle of electron**
**(b) a vacancy created when an electron leaves a covalent bond**
**(c) absence of free electrons**
**(d) an artificially created particle**
**Solution:** (b) Concept of holes in the semiconductor:

1. .When an electron is removed from a covalent bond, it leaves a vacancy behind. An electron from a neighbouring atom can move into this vacancy, leaving the neighbour with a vacancy. In this way the vacancy formed is called a hole (or cotter), and can travel through the material and serve as an additional current carriers.

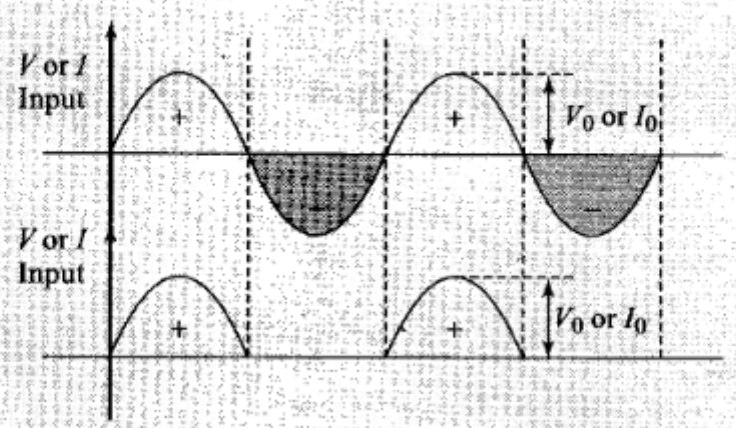
2. A hole is considered as a seat of positive charge, having magnitude of charge equal to that of an electron.
3. Holes acts as a virtual charge, although there is no physical charge on it.
4. Effective mass of hole is more than an electron.
5. Mobility of hole is less than an electron.

**Question 6. The output of the given circuit in figure is given below.**




**(a) would be zero at all times**
**(b) would be like a half wave rectifier with positive cycles in output**
**(c) would be like a half wave rectifier with negative cycles in output**
**(d) would be like that of a full wave rectifier**
**Solution:** (c)

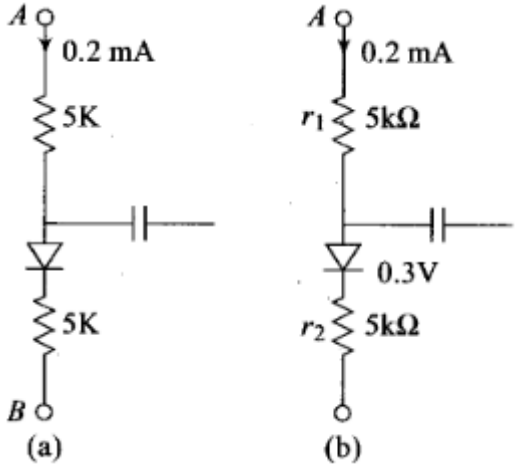
**Key concept:**




(i) During positive half cycle,
Diode ⟶ forward biased
Output signal ⟶ obtained
(ii) During negative half cycle,
Diode ⟶ reverse biased
Output signal ⟶ not obtained
(iii) Output voltage is obtained across the load resistance $R_L$. It is not constant but pulsating (mixture of *ac* and *dc*) in nature.
(iv) Average output in one cycle
(v) r.m.s. output: $I_{rms} = \frac{I_0}{2}, V_{rms} = \frac{V_0}{2}$

When the diode is forward biased during positive half cycle of input AC voltage, the resistance of p-n junction is low. The current in the circuit is maximum. In this situation, a maximum potential difference will appear across resistance connected in a series of circuit. This result into zero output voltage across p-n junction.
And when the diode is reverse biased during negative half cycle of AC voltage, the p-n junction is reverse biased. The resistance of p-n junction becomes high which will be more than resistance in series. That is why, there will be voltage across p-n junction with negative cycle in output, hence option (c) is correct.

**Question 7. In the circuit shown in figure given below, if the diode forward voltage between A and B is**




**(a) 1.3 V (b) 2.3 V (c) 0 (d) 0.5 V**
**Solution:**

**(b)** Let us consider the fig. (b) given above in the problem, suppose the potential difference between $A$ and $B$ is $V_{AB}$.

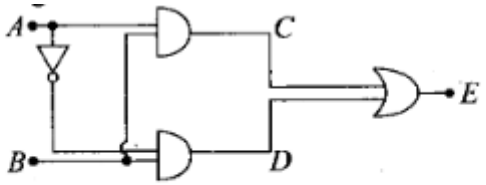
Then, $V_{AB} - 0.3 = [(r_1 + r_2)10^3] \times (0.2 \times 10^{-3})$ $[\because V_{AB} = ir]$

$= [(5 + 5)10^3] \times (0.2 \times 10^{-3})$

$= 10 \times 10^3 \times 0.2 \times 10^{-3} = 2$

$\Rightarrow$ $V_{AB} = 2 + 0.3 = 2.3$ V

**Question 8. Truth table for the given circuit is**




(a)

| A | B | E |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

(b)

| A | B | E |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

(c)

| A | B | E |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

(d)

| A | B | E |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Solution:**

**(c)** In this problem the input $C$ of OR gate and which is an output of AND gate. So, "$C$ equals $A$ **AND** $B$" or $C = A \cdot B$ and "$D$ equals **Not** $A$ **AND** $B$" or $D = \bar{A} \cdot B$
and "$E$ equals $C$ **AND** $D$" or $E = C + D = (A \cdot B) + (A \cdot B)$
Now we can generate the truth table of this arrangement of gates can be given by

| $A$ | $B$ | $\bar{A}$ | $C = A \cdot B$ | $d = \bar{A} \cdot B$ | $E = (C + D)$ |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 |

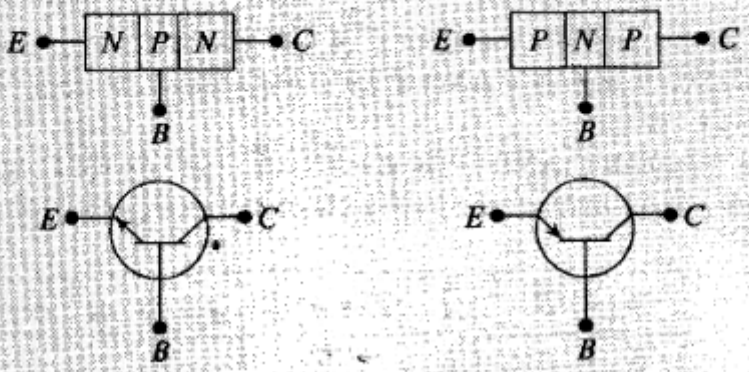
**One or More Than One Correct Answer Type**

**Question 9. When an electric field is applied across a semiconductor**
**(a) electrons move from lower energy level to higher energy level in the conduction band**
**(b) electrons move from higher energy level to lower energy level in the conduction band**
**(c) holes in the valence band move from higher energy level to lower energy level**
**(d) holes in the valence band move from lower energy level to higher energy level**
**Solution:** (a, c)
In valence band electrons are not capable of gaining energy from external electric field. While in conduction band the electrons can gain energy from external electric field.
When electric field is applied across a semiconductor, the electrons in the conduction band (which is partially filled with electrons) get accelerated and acquire energy. They move from lower energy level to higher energy level. While the holes in valence band move from higher energy level to lower energy level, where they will be having more energy.

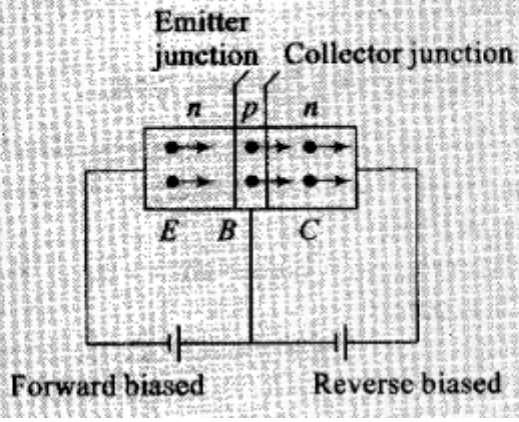
**Question 10. Consider an n-p-n transistor with its base-emitter junction forward biased and collector base junction reverse biased. Which of the following statements are true?**
**(a) Electrons crossover from emitter to collector**
**(b) Holes move from base to collector**
**(c) Electrons move from emitter to base**
**(d) Electrons from emitter move out of base without going to the collector.**
**Solution:** (a, c)

**Key concept:** *Transistor:*

A junction transistor is formed by sandwiching a thin layer of *P*-type semiconductor between two *N*-type semiconductors or by sandwiching a thin layer of *N*-type semiconductor between two *P*-type semiconductors.




*E*— Emitter (emits majority charge carriers)
*C*— Collects majority charge carriers
*B*— Base (provide proper interaction between *E* and *C*)

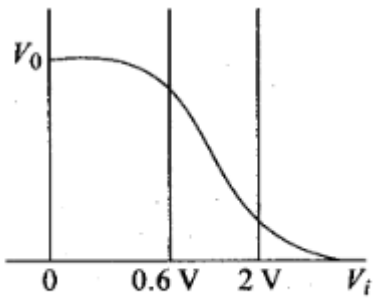



In normal operation base-emitter is forward biased, i.e., the positive pole of emitter base battery is connected to base and its negative pole is connected to the emitter. And collector base junction is reverse biased, i.e., the positive pole of the collector base battery is connected to collector and negative pole to base. Thus, electron moves from emitter to base and crossover from emitter to collector.

**Question 11.**

Figure given alongside shows that transfer characteristics of a base biased *CE* transistor. Which of the following statements are true?

(a) At $V_i = 0.4$ V, transistor is in active state
(b) At $V_i = 1$ V, it can be used as an amplifier
(c) At $V_i = 0.5$ V, it can be used as a switch turned off
(d) At $V_i = 2.5$ V, it can be used as a switch turned on




**Solution:** (b, c, d) According to above graph transfer characteristics of a base biased common emitter transistor, we note that .

(a) when $V_i$= 0.4 V, output voltage remain same,there is no collection current. So, transistor circuit is not in active state.

(b) when $V_i$ = 1 V (This is in between 0.6 V to 2 V), the transistor circuit is in active state and when input is increasing output is decreasing because when CE is used as an amplifier input and output voltages are 180° out of phase. Then it is used as an amplifier.

(c) when $V_i$ = 0.5 V, there is no collector current. The transistor is in cut off state. The transistor

circuit can be used as a switch to be turned off.
(d) when $V_i$ = 2.5 V, the collector current becomes maximum and transistor is in a saturation state and can used as switch turned on state.

**Question 12. In a n-p-n transistor circuit, the collector current is 10 mA. If 95 per cent of the electrons emitted reach the collector, which of the following statements are true?**
**(a) The emitter current will be 8 mA**
**(b) The emitter current will be 10.53 mA**
**(c) The base current will be 0.53 mA**
**(d) The base current will be 2 mA**
**Solution:** (b, c) According to the problem, the collector current is 95% of electrons reaching the collector after emission. And collector current, $I_C$ = 10 mA

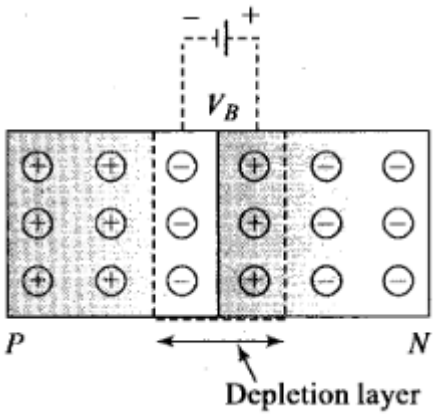
$I_E$ = emiter current

$$\text{Also,} \quad I_C = \frac{95}{100} I_E$$

$$\Rightarrow \quad I_E = \frac{10 \times 100}{95} = 10.53\,\text{mA}$$

$$\text{Also,} \quad I_B = I_E - I_C = 10.53 - 10 = 0.53\ \text{mA}$$

**Question 13. In the depletion region of a diode**
**(a) there are no mobile charges**
**(b) equal number of holes and elections exist, making the region neutral**
**(c) recombination of holes and electrons has taken place**
**(d) immobile charged ions exist**
**Solution:** (a, b, d) On account of difference in concentration of charge carrier in the two sections of P-N junction, the electrons from N-rcgion diffuse through the junction into P-region and the hole from P-region diffuse into N-region.




Due to diffusion, neutrality of both N-and P-type semiconductor is disturbed, a layer of negative charged ions appear near the junction in the P-crystal and a layer of positive ions appears near the junction in N-crystal. This layer is called depletion layer.
The thickness of depletion layer is 1 micron = $10^{-6}$ m.
Width of depletion layer $\propto$ 1/Dopping
Depletion is directly proportional to temperature.
Important point: The P-N junction diode is equivalent to capacitor in which the depletion layer acts as a dielectric.

**Question 14. What happens during regulation action of a Zener diode?**
**(a) The current and voltage across the Zener remains fixed**
**(b) The current through the series Resistance ($R_s$) changes**

**(c) The Zener resistance is constant**
**(d) The resistance offered by the Zener changes**

**Solution:** (b, d) Symbolically zener diode represents like this:
In the forward bias, the zener diode acts as an ordinary diode. It can be used as a voltage regulator.

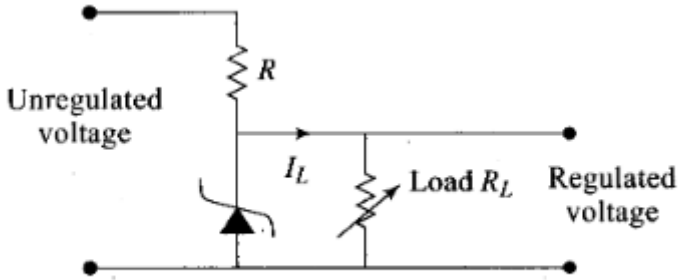



**Fig: Zener diode as a voltage regulator**

A zener diode when reverse biases offers constant voltage drop across in terminals as unregulated voltage is applied across circuit to regulate. Then during regulation action of a Zener diode, the current through the series resistance $R_s$ changes and resistance offered by the Zener changes. The current through the Zener changes but the voltage across the Zener remains constant.

**Question 15. To reduce the ripples in rectifier circuit with capacitor filter**
**(a) $R_L$ should be increased**
**(b) input frequency should be decreased .**
**(c) input frequency should be increased**
**(d) capacitors with high capacitance should be used**
**Solution:** (a, c, d)
Ripple factor may be defined as the ratio of r.m.s. value of the ripple voltage to the absolute value of the DC component of the output voltage, usually expressed as a percentage. However ripple voltage is also commonly expressed as the peak-to-peak value. Ripple factor (r) of a full wave rectifier using capacitor filter is given by

$$r = \frac{0.236R}{\omega L}$$

Where, $L$ is inductance of the coil and $\omega$ is the angular frequency.

· or Ripple factor can also be given by

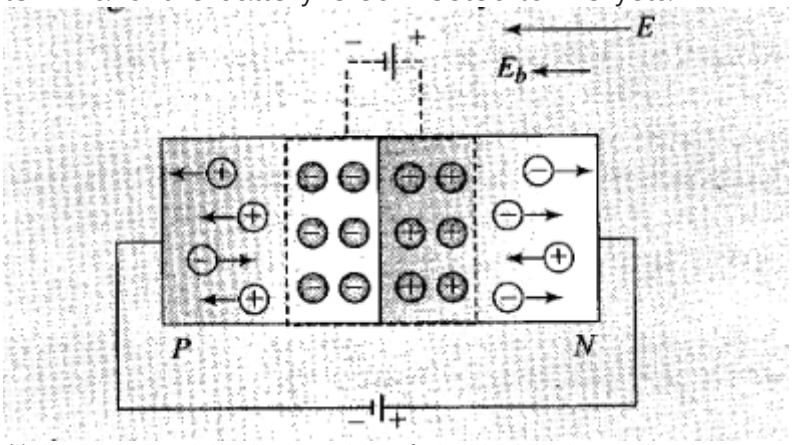
$$r = \frac{1}{4\sqrt{3}vR_L C_V}$$

$$i.e., \quad r \propto \frac{1}{R_L} \Rightarrow r \propto \frac{1}{C}, \; r \propto \frac{1}{V}$$

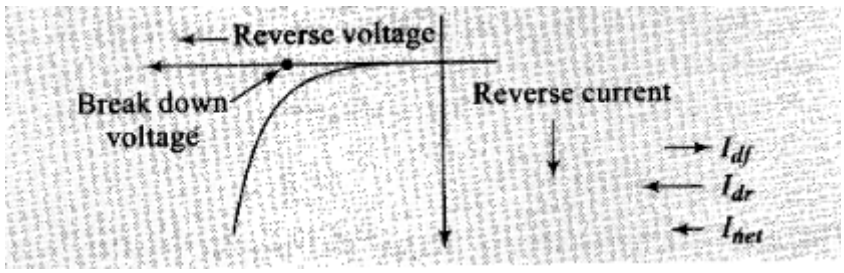
Ripple factor is inversely proportional to $R_L$, C and v.
Thus to reduce r, $R_L$ should be increased, input frequency v should be increased and capacitance C should be increased.

**Question 16. The breakdown in a reverse biased p-n junction is more likely to occur due to**
**(a) large velocity of the minority charge carriers if the doping concentration is small**
**(b) large velocity of the minority charge carriers if the doping concentration is large**
**(c) strongelectricfieldinadepletionregionifthedopingconcentrationissmall**

**(d) strong electric field in the depletion region if the doping concentration is large**
**Solution:** (a, d)
Reverse biasing: Positive terminal of the battery is connected to the N-crystal and negative terminal of the battery is connected to P-crystal.




(i) In reverse biasing width of depletion layer increases
(ii) In reverse biasing resistance offered $R_{Reverse} = 10^5\ \Omega$
(iii) Reverse bias supports the potential barrier and no current flows across the junction due to the diffusion of the majority carriers.
(A very small reverse current may exist in the circuit due to the drifting of minority carriers across the junction)
(iv) Break down voltage: Reverse voltage at which break down of semiconductor occurs. For Ge it is 25 V and for Si it is 35 V.




So, we conclude that in reverse biasing, ionization takes place because the minority charge carriers will be accelerated due to reverse biasing and striking with atoms which in turn cause secondary electrons and thus more number of charge carriers.
When doping concentration is large, there will be a large number of ions in the depletion region, which will give rise to a strong electric field.

**Very Short Answer Type Questions**

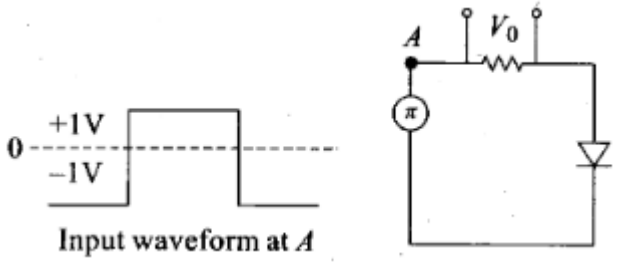
**Question 17. Why are elemental dopants for Silicon or Germanium usually chosen from group XIII or group XV?**
**Solution:** When pure semiconductor material is mixed with small amounts of certain specific impurities with valency different from that of the parent material, the number of mobile electrons/holes drastically changes. The process of addition of impurity is called doping. The size of the dopant atom should be compatible such that their presence in the pure semiconductor does not distort the semiconductor but easily contribute the charge carriers on forming covalent bonds with Silicon or Germanium atoms, which are provided by group XIII or group XV elements.

**Question 18. Sn, C and Si, Ge are all group XIV elements. Yet, Sn is a conductor, C is an insulator while Si and Ge are semiconductors. Why?**
**Solution:** The conduction level of any element depends on the energy gap between its conduction band and valence band.
In conductors, there is no energy gap between conduction band and valence band. For insulator, the energy gap is large and for semiconductor the energy gap is moderate.

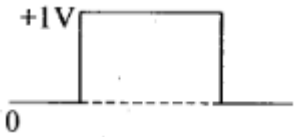
The energy gap for Sn is 0 eV, for C is 5.4 eV, for Si is 1.1 eV and for Ge is 0.7 eV related to their atomic size. Therefore Sn is a conductor, C is an insulator, and Ge and Si are semiconductors

**Question 19. Can the potential barrier across a p-n junction be measured by simply connecting a voltmeter across the junction?**
**Solution:** We cannot measure the potential barrier across a p-n junction by a voltmeter because the resistance of voltmeter is very high as compared to the junction resistance. Potential of potential barrier for Ge is $V_B = 0.3$ V and for silicon is $V_B = 0.7$ V.
On the average the potential barrier in P-N junction is ~0.5 V.

**Question 20. Draw the output waveform across the resistor in the given figure.**




**Solution:** The diode act as a half wave rectifier, it offers low resistance when forward biased and high resistance when reverse biased. So the output is obtained only when positive input is given,so the output waveform is




**Question 21. The amplifiers X, Y and Z are connected in series. If the voltage gains of X, Y and Z are 10,20 and 30, respectively and the input signal is 1 mV peak value, then what is the output signal voltage (peak value).**
**(i) if DC supply voltage is 10 V?**
**(ii) if DC supply voltage is 5 V?**
**Solution:** Total voltage amplification is defined as the ratio of output signal voltage and input signal voltage.

According to the problem, voltage gain in $X$, $v_x = 10$,
voltage gain in $Y$, $v_y = 20$,
voltage gain in $Z$, $v_z = 30$;
$\Delta V_i = 1 \text{ mV} = 10^{-3} \text{ V}$

And Total voltage amplification $= v_x \times v_y \times v_z$

$$\Delta V_0 = v_x \times v_y \times v_z \times \Delta V_i$$
$$= 10 \times 20 \times 30 \times 10^{-3} = 6 \text{ V}$$

(i) If DC supply voltage is 10 V, then output is 6 V, since theoretical gain is equal to practical gain, i.e., output can never be greater than 6 V.
(ii) If DC supply voltage is 5 V, i.e., $V_{cc} = 5$ V. Then, output peak will not exceed 5 V. Hence $V_0 = 5$ V.

**Question 22. In a CE transistor amplifier, there is a current and voltage gain associated with the circuit. In other words there is a power gain. Considering power a measure of energy, does the circuit violate conservation of energy?**
**Solution:**

**Key concept:** Different gain in CE transistor amplifier:

(i) *ac current gain:* $\beta_{ac} = \left(\frac{\Delta i_c}{\Delta i_b}\right) V_{CE}$ =constant

(ii) *dc current gain:* $\beta_{dc} = \frac{i_c}{i_b}$

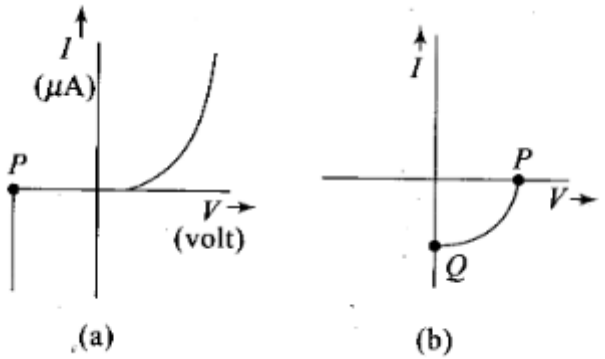
(iii) *Voltage gain:* $A_v = \frac{\Delta V_o}{\Delta V_i} = \beta_{ac} \times$ Resistance gain

(iv) *Power gain:* $= \frac{\Delta P_o}{\Delta P_i} = \beta_{ac}^2 \times$ Resistance gain

The power gain is very high in CE transistor amplifier. In this circuit, the extra power required for amplified output is obtained from DC source. Thus, the circuit used does not violate the law of conservation.

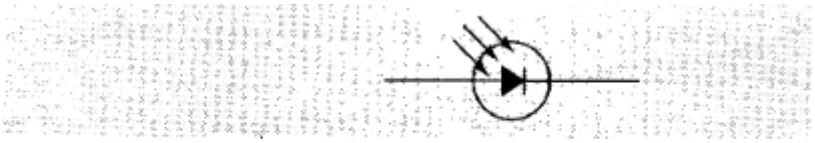
**Short Answer Type Questions**

**Question 23. (i) Name the type of a diode whose characteristics are shown in figure (a) and (b).**
**(ii) What does the point P in fig. (a) represent?**
**(iii) What does the points P and Q in fig. (b) represent?**




**Solution:**
(i) Fig. (a) represents the characteristics of Zener diode and curve (b) is of solar cell.
(ii) In fig. (a), point P represents Zener breakdown voltage.
(iii) In fig. (b), the point Q represents zero voltage and negative current. Which means the light falling on solar cell with atleast minimum threshold frequency gives the current in opposite direction to that due to a battery connected to solar cell. But for the point Q the battery is short circuited. Hence it represents the short circuit current.
And the point Pin fig. (b) represents some open circuit, voltage on solar cell with zero current through solar cell.
It means, there is a battery connected to a solar cell which gives rise to the equal and opposite current to that in solar cell by virtue of light falling on it.

**Question 24. Three photo diodes $D_1$, $D_2$ and $D_3$ are made of semiconductors having band gaps of 2.5 eV, 2 eV and 3 eV, respectively. Which ones will be able to detect light of wavelength 6000 Å ?**
**Solution:**Key concept: In Photo diodes electron and hole pairs are created by junction photoelectric effect. That is the covalent bonds are broken by the EM radiations absorbed by the electron in the V.B. These are used for detecting light signals.



According to the problem,

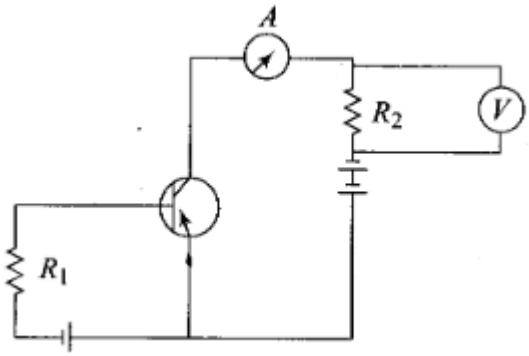
Wavelength of light $\lambda = 6000\ \text{Å} = 6000 \times 10^{-10}\ \text{m}$

Energy of the light photon

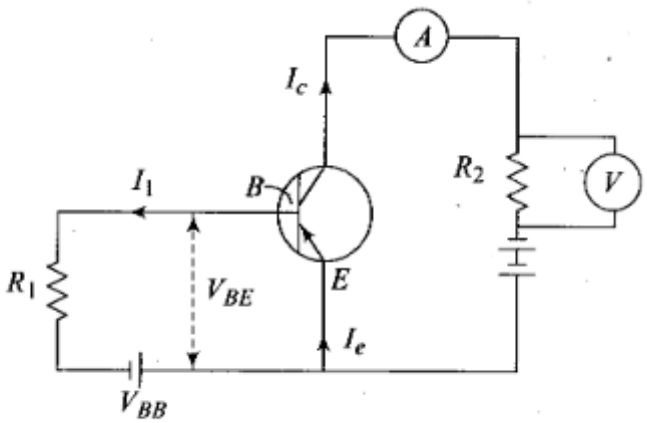
$$E = \frac{hc}{\lambda} = \frac{6.6 \times 10^{-34} \times 3 \times 10^{8}}{6000 \times 10^{-10} \times 1.6 \times 10^{-19}}\ \text{eV} = 2.06\ \text{eV}$$

The incident radiation which is detected by the photodiode $D_2$ because energy of incident radiation is greater than the band-gap.

**Question 25. If the resistance $R_1$ is increased (see figure), how will the readings of the ammeter and voltmeter change?**




**Solution:** Let us redrawn the circuit diagram to find the change in reading of ammeter and voltmeter.




So, $I_B R_1 + V_{BE} = V_{BB}$

Base current, $I_B = \dfrac{V_{BB} - V_{BE}}{R_1}$

$$I_B \propto \frac{1}{R_1}$$

So, $R_1$ is increased, $I_B$ is decreased.

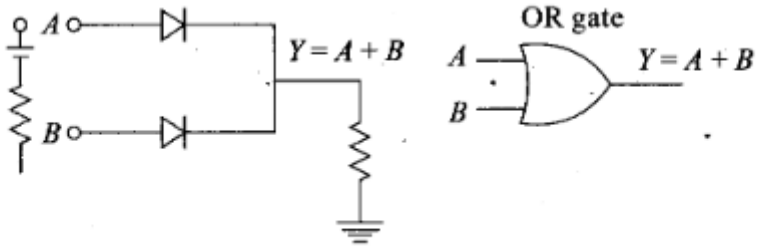
Now, the current in ammeter is collector current $I_C$.

$I_C = \beta I_B$ as $I_B$ is decreased, $I_C$ is also decreased and the reading of voltmeter and ammeter also decreased.

**Question 26. Two car garages have a common gate which needs to open automatically when a car enters either of the garages or cars enter both. Draw a circuit that resembles this situation using diodes for this situation.**

**Solution:** As car enters in either of the garages or both, the common gate opened automatically. This means that if any one input is high, output will high otherwise low.

The device is shown like this:




So, OR gate gives the desired output.

| A | B | Y = A + B |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

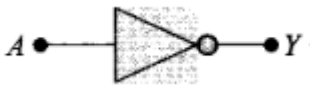
**Question 27. How would you set up a circuit to obtain NOT gate using a transistor?**

**Solution:**

(1)It has only one input and only one output.

(2)Boolean expression is Y = $\bar{A}$ and is read as "y equals not A" .

Logical symbol of NOT gate.

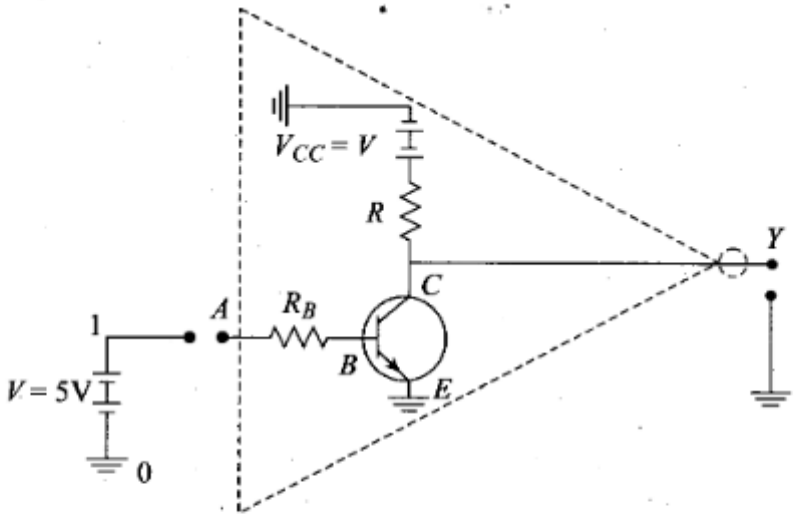



(3)Realization of NOT gate: The transistor is so biased that the collector voltage $V_{CC}$ = V (Voltage corresponding to 1 state)

The resistors R and $R_B$ are so chosen that if the input is low, i.e. 0, the transistor is in the cut off and hence the voltage appearing at the output will be the same as applied V = 5 V. Hence Y= V(or state I)

If the input is high, the transistor current is in saturation and the net voltage at the output Y is 0 (in

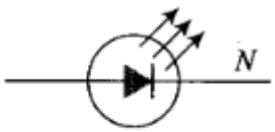
state 0).




(4) Truth table for NOT gate:

| $A$ | $Y = \overline{A}$ |
|---|---|
| 0 | 1 |
| 1 | 0 |

**Question 28. Explain why elemental semiconductor cannot be used to make visible LEDs.**
**Solution:**



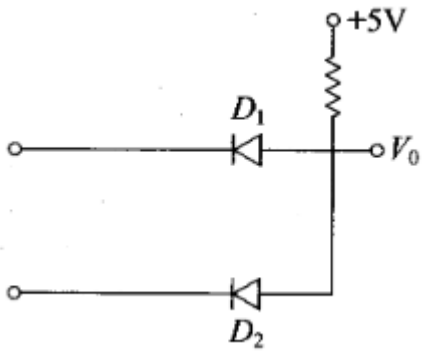

Specially designed diodes, which give out light radiations when forward biases. LED's are made of *GaAsp*, *Gap* etc.
These are forward biased *P-N* junctions which emits spontaneous radiation.
In elemental semiconductor, the band gap is such that the emission are in infrared region and not in visible region.

$$\lambda = \frac{hc}{E_g} = \frac{1242\ \text{eVnm}}{E_g}$$

$$\text{for Si; } E_g = 1.1\ \text{eV}, \lambda = \frac{1242}{1.1} = 1129\ \text{nm}$$

$$\text{for Ge; } E_g = 0.7\ \text{eV}, \lambda = \frac{1242}{0.7} = 1725\ \text{nm}$$

**Question 29. Write the truth table for the circuit shown in figure given below. Name the gate that the circuit resembles.**



**Solution:**

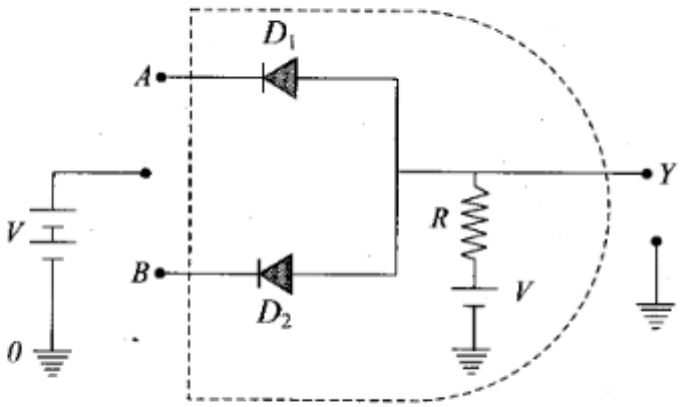
This is 'AND' Gate and its characteristics are as follows:

(1) It has two inputs ($A$ and $B$) and only one output ($Y$).

(2) Boolean expression is $Y = A \cdot B$ is read as "$Y$ equals $A$ AND $B$".

(3) Realization of AND gate


Logical symbol of AND gate




(i) $A = 0, B = 0$

The voltage supply through $R$ is forward biasing diodes $D_1$ and $D_2$ (offers low resistance), the voltage $V$ would drop across $R$.

The output voltage at $Y$ = the voltage across diode = 0

(ii) $A = 0, B = 1$

$D_1$ = Conducts, $D_2$ = Not Conducts

The out voltage at $Y$ = The voltage across the diode ($D_1$) = 0

(iii) $A = 1, B = 0$

$D_1$ = Conducts, $D_2$ = Not conducts

The out voltage at $Y$ = The voltage across the diode ($D_2$) = 0

(iv) $A = 1, B = 1$

None of the diode conducts

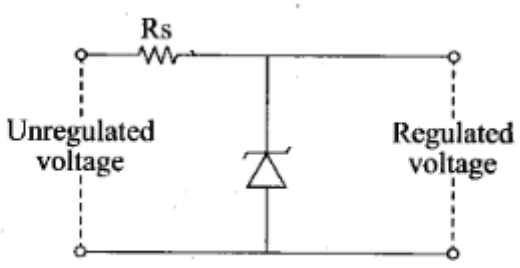
The out voltage at $Y$ = Battery voltage = 1

(4) Truth table for 'AND' gate

| $A$ | $B$ | $V_0 = A \cdot B$ |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**Question 30.**

A Zener of power rating 1 W is to be used as a voltage regulator. If Zener has a breakdown of 5 V and it has to regulate voltage which fluctuated between 3 V and 7 V, what should be the value of $R_s$ for safe operation (see figure)?



**Solution:**

According to the problem, power = 1 W
Zener breakdown voltage, $V_z = 5$ V
Minimum voltage, $V_{min} = 3$ V
Maximum voltage, $V_{max} = 7$ V
We know, $P = VI$

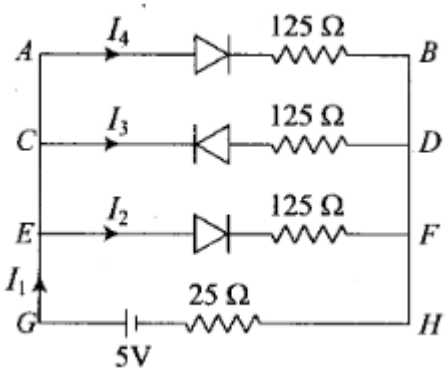
So, current $I_{Z_{max}} = \frac{P}{V_Z} = \frac{1}{5} = 0.2\,\text{A}$

For safe operation $R_s$ will be equal to

$$R_s = \frac{V_{max} - V_Z}{I_{Z_{max}}} = \frac{7-5}{0.2} = \frac{2}{0.2} = 10\Omega$$

**Long Answer Type Questions**

**Question 31. If each diode in figure has a forward bias resistance of 25 Ω and infinite resistance in reverse bias, what will be the values of the currents $I_1$, $I_2$, $I_3$ and $I_4$?**




**Solution:**

According to the problem, forward biased resistance = 25 Ω and reverse biased resistance = ∞.
As shown in the figure, the diode in branch $CD$ is in reverse biased which having infinite resistance.
So, current in that branch is zero, *i.e.* $I_3 = 0$
Resistance in branch $AB = 25 + 125 = 150\ \Omega$, say $R_1$
Resistance in branch $EF = 25 + 125 = 150\ \Omega$, say $R_2$
$AB$ is parallel to $EF$.
So, effective resistance

$$\frac{1}{R'} = \frac{1}{R_1} + \frac{1}{R_2} = \frac{1}{150} + \frac{1}{150} = \frac{2}{150}$$

$\Rightarrow \quad R' = 75\ \Omega$
Total resistance $R$ of the circuit $= R' + 25 = 75 + 25 = 100\ \Omega$

$$\text{Current } I_1 = \frac{V}{R} = \frac{5}{100} = 0.05\ \text{A}$$

According to the kirchoff's, current law (KCL),

$I_1 = I_4 + I_2 + I_3$ (Here $I_3 = 0$)

So, $I_1 = I_4 + I_2$

Here, the resistances $R_1$ and $R_2$ is same.

*i.e.*, $I_4 = I_2$

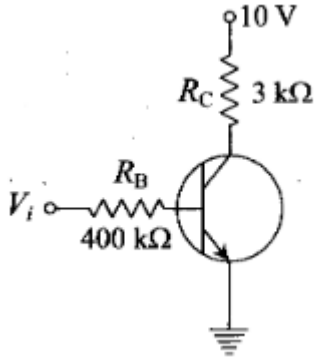
$\therefore \quad I_1 = 2I_2$

$$\Rightarrow \quad I_2 = \frac{I_1}{2} = \frac{0.05}{2} = 0.025\ \text{A}$$

and $I_4 = 0.025$ A

Therefore, we get, $I_1 = 0.05$ A, $I_2 = 0.025$ A, $I_3 = 0$ and $I_4 = 0.025$ A

**Question 32. In the circuit shown in figure, when the input voltage of the base resistance is 10 V, $V_{BE}$ is zero and $V_{CE}$ is also zero. Find the values of $I_B$, $I_C$ and β .**




**Solution:**

According to the problem, $V_i$ = 10 V, Resistance, $R_B$ = 400 kΩ, $V_{BE}$ = 0, $V_{CE}$ = 0 and $R_C$ = 3 kΩ

$$V_i - V_{BE} = R_B I_B$$

$$I_B = \frac{\text{Voltage across } R_B}{R_B}$$

$$= \frac{10}{400 \times 10^3} = 25 \times 10^{-6}\ \text{A} = 25\,\mu\text{A}$$

Voltage across $R_C$ = 10 V

$$V_{CC} - V_{CE} = I_C R_C$$

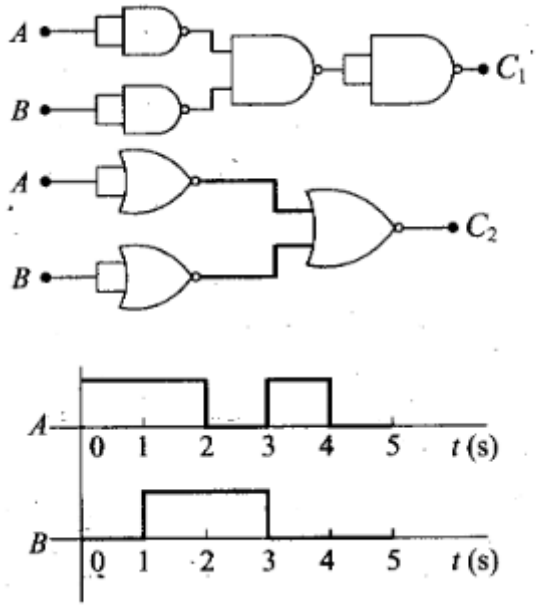
$$I_C = \frac{\text{Voltage across } R_C}{R_C} = \frac{10}{3 \times 10^3}$$

$$= 3.33 \times 10^{-3}\ \text{A} = 3.33\ \text{mA}$$

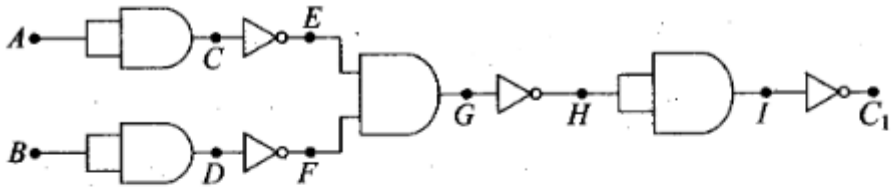
$$\beta = \frac{I_C}{I_B} = \frac{3.33 \times 10^{-3}}{25 \times 10^{-6}}$$

$$= 1.33 \times 10^2 = 133$$

**Question 33. Draw the output signals $C_1$ and $C_2$ in the given combination of gates.**

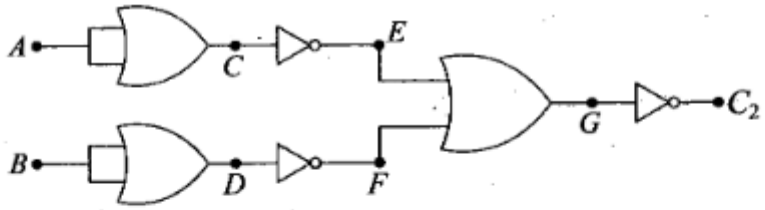



**Solution:**



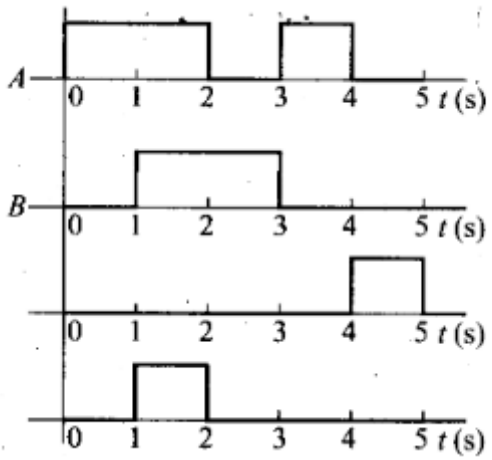

$$C_1 = \overline{\overline{A}\cdot\overline{B}} = \overline{\overline{A}+\overline{B}} = \overline{A+B}$$

| A | B | C | D | E | F | G | H | I | $C_1$ |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

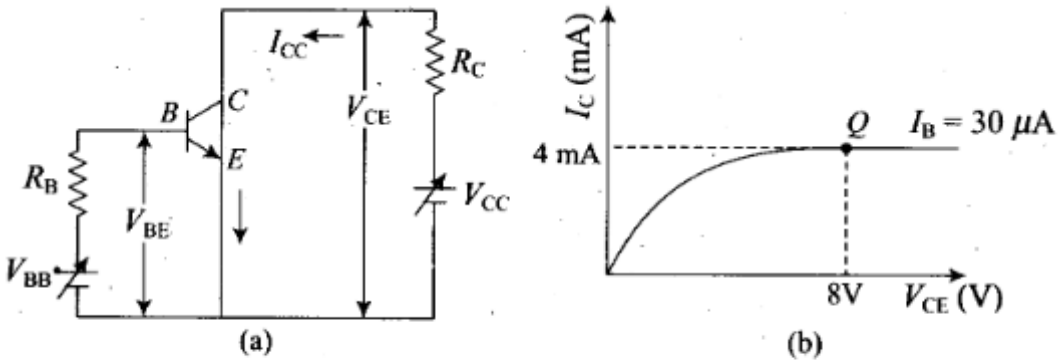



$$C_2 = \overline{\overline{A}\cdot\overline{B}} = \overline{\overline{A}}\cdot\overline{\overline{B}} = A\cdot B$$

| A | B | C | D | E | F | G | $C_2$ |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |




**Question 34. Consider the circuit arrangement shown in figure for studying input and output characteristics of n-p-n transistor in.CE configuration.**
**Select the values of $R_B$ and $R_C$ for a transistor whose $V_{BE}$ = 0.7 V so that the transistor is operating at point Q as shown in the characteristics (see figure).**




Given that the input impedance of the transistor is very small and $V_{cc} = V_{BB}$ = 16 V, also find the voltage gain and power gain of circuit making appropriate assumptions.

**Solution:**

According to the problem, at point $Q$, from graph $V_{BE} = 0.7$ V, $V_{CC} = V_{BB} =$ 16 V and $V_{CE} = 8$ V

$$I_C = 4\text{ mA} = 4 \times 10^{-3}\text{ A}$$

$$I_B = 30\ \mu\text{A} = 30 \times 10^{-6}\text{ A}$$

Since, $V_{CC} = I_C R_C + V_{CE}$

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{16 - 8}{4 \times 10^{-3}} = \frac{8 \times 1000}{4} = 2\text{ k}\Omega$$

Similarly, $V_{BB} = I_B R_B + V_{BE}$

$$R_B = \frac{V_{BB} - V_{BE}}{I_B} = \frac{16 - 0.7}{30 \times 10^{-6}}$$

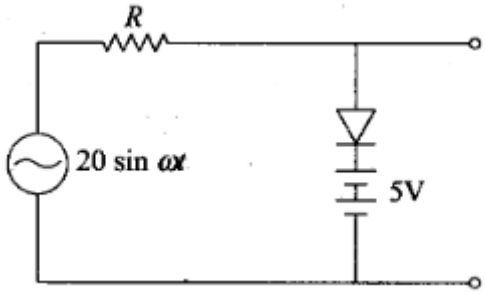
$$= 510 \times 10^3\ \Omega = 510\text{ k}\Omega$$

$$\text{Current gain, } \beta = \frac{I_C}{I_B} = \frac{4 \times 10^{-3}}{30 \times 10^{-6}} = 133\,3$$

$$\text{Voltage gain } = \beta \frac{R_C}{R_B} = \frac{133 \times 2 \times 10^3}{510 \times 10^3} = 0.52$$

$$\text{Power gain} = \beta \times \text{Voltage gain} = 133 \times 0.52 = 69$$

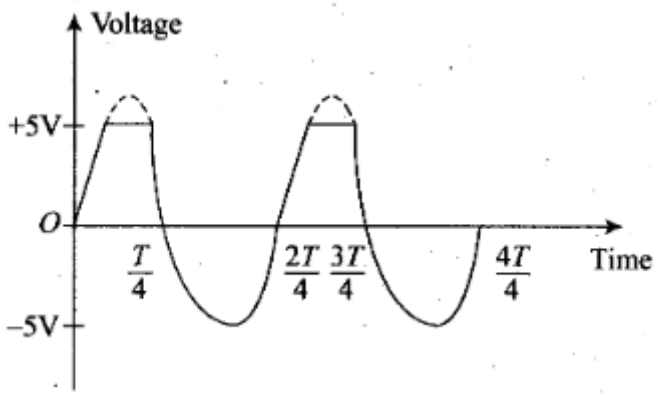
**Question 35. Assuming the ideal diode, draw the output waveform for the circuit given in figure, explain the waveform.**




**Solution:**

Key concept: An ideal diode is a diode in which it has a very large resistance in reverse biased and very, low resistance in forward biased. So, it acts like a perfect conductor when voltage is applied forward biased and like a perfect insulator when voltage is applied reverse biased.
In reverse biased when the input voltage is equal to or less than 5 V diode,then it will offer high resistance in comparison to resistance (R) in series. Now, diode appears in open circuit. The input waveform is then passed to the output terminals. The result with sin wave input is to dip off all

positive going portion above 5 V.
If input voltage is greater than +5 V, diode is in conducting state, then it will be conducting as if forward biased offering low resistance in comparison to R. But there will be no voltage in output beyond 5 V as the voltage beyond +5 V will appear across R.
When input voltage is negative, there will be opposition to 5 V battery in p-n junction input voltage becomes more than -5 V, the diode will be reverse biased. It will offer high resistance in comparison to resistance R in series. Now junction diode appears in open circuit. The input wave form is then passed on to the output terminals.
The output waveform will be like this (as shown below).




**Question 36. Suppose a n-type wafer is'created by doping Si crystal having 5 x $10^{28}$ atoms/$m^3$ with 1 ppm concentration of As. On the surface 200 ppm boron is added to create 'p' region in this wafer. Considering $n_i = 1.5 \times 10^{16}$ $m^{-3}$,**
**(i) Calculate the densities of the charge carriers in the n and p regions,**
**(ii) Comment which charge carriers would contribute largely for the reverse saturation current when diode is reverse biased.**
**Solution:** n-type wafer is created when As is implanted in Si crystal. The number of majority carriers electrons due to doping of As is

$$n_e = N_D = 10^{-6} \times 5 \times 10^{28} \text{ atoms/m}^3$$
$$= 5 \times 10^{22}/\text{m}^3$$

Number of minority carriers (holes) in *n*-type wafer is

$$n_h = \frac{n_i^2}{n_e} = \frac{(1.5 \times 10^{16})^2}{5 \times 10^{22}}$$
$$= 0.45 \times 10^{10}/\text{m}^3$$

*p*-type wafer is created with number of holes, when *Boron* is implanted in *Si* crystal,

$$n_h = N_A = 200 \times 10^{-6} \times (5 \times 10^{28}) = 1 \times 10^{25}/\text{m}^3$$

Minority carriers (electrons) created in *p*-type wafer is

$$n_e = \frac{n_i^2}{n_h} = \frac{(1.5 \times 10^{16})^2}{1 \times 10^{25}}$$
$$= 2.25 \times 10^{7}/\text{m}^3$$

(ii) The minority carrier holes of *n*-region wafer ($n_h = 0.45 \times 10^{10}/\text{m}^3$) would contribute more to the reverse saturation current than minority carrier electrons ($n_e = 2.25 \times 10^{7}/\text{m}^3$) of *p*-region wafer when *p-n* junction is reverse biased.

**Question 37. An XOR gate has the following truth table.**

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

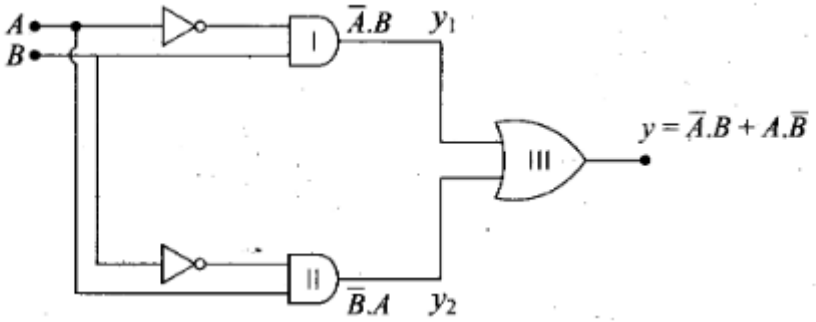
**It is represented by following logic relation Y = Ā . B + A . B' . Build this gate using AND, OR and NOT gates.**

**Solution:** XOR gate can be realized by the combination of two NOT gates, two AND gates and one OR gate. According to the problem, the logic relation for the . given truth table is

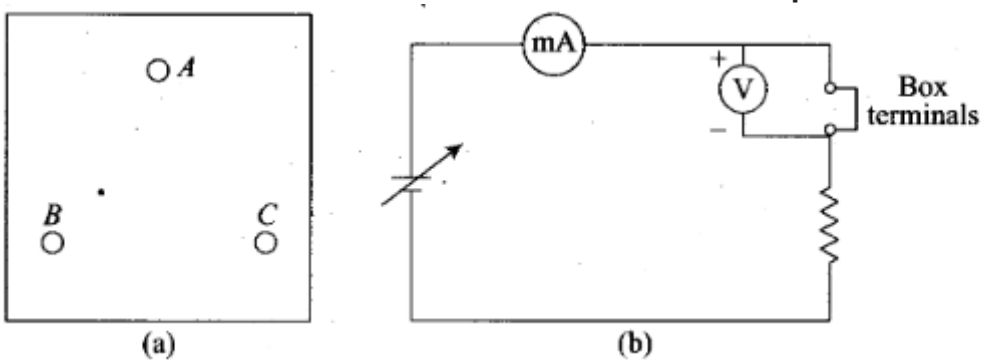
$$Y = \overline{A} \cdot B + A \cdot \overline{B} = Y_1 + Y_2$$

when $Y_1 = A \cdot B$ and $Y_2 = A \cdot \overline{B}$

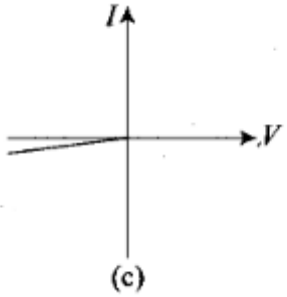
$Y_1$ can be obtained as output of AND gate I for which one input is of $A$ through NOT gate and another input is of $B$. $Y_2$ can be obtained as output of AND gate II for which one input is of $A$ and other input is of $B$ through NOT gate.
Now $Y$ can be obtained as output from OR gate, where $Y_1$ and $Y_2$ are inputs of OR gate.
Thus, the logic circuit of this relation is given below.




**Question 38. Consider a box with three terminals on top of it as shown in figure.**

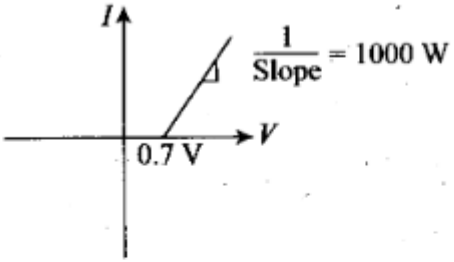



**Three components namely, two germanium diodes and one resistor are connected across these three terminals in some arrangement.**
**A student performs an experiment in which any two of these three terminals are connected in the circuit as shown in figure.**
**The student obtains graphs of current-voltage characteristics for unknown combination of components between the two terminals connected in the circuit. The graphs are**
**(i) when A is positive and B is negative .**



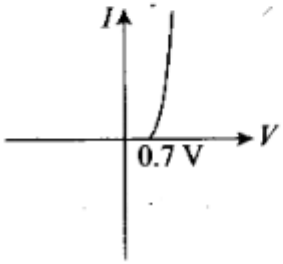

(c)

(ii) when $A$ is negative and $B$ is positive



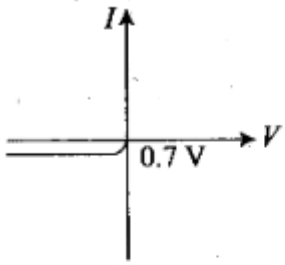

(d)

(iii) when $B$ is negative and $C$ is positive



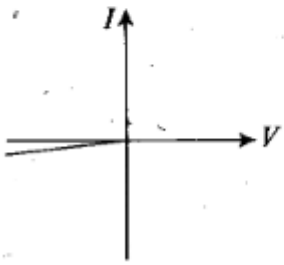

(e)

(iv) when $B$ is positive and $C$ is negative



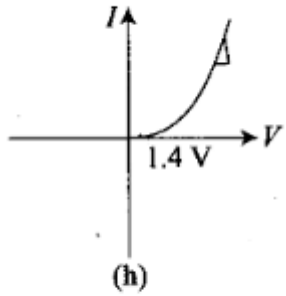

(f)

(v) when $A$ is positive and $C$ is negative




(g)

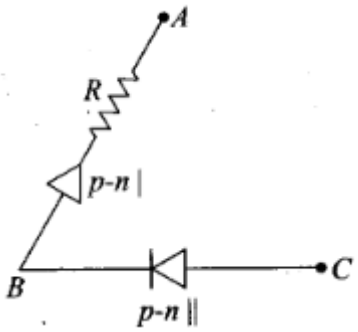
(vi) when $A$ is negative and $C$ is positive



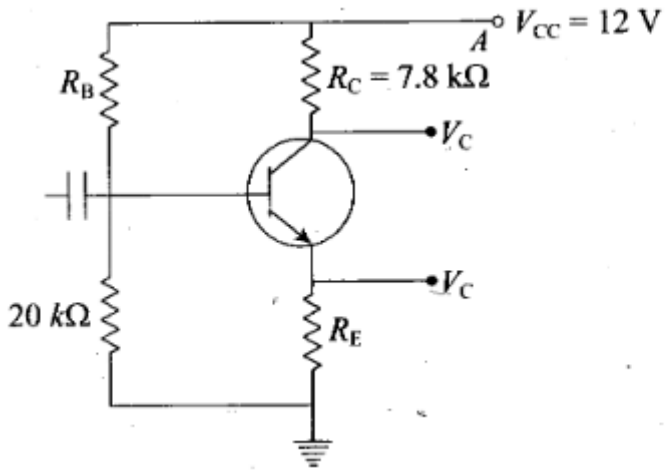

(h)

From these graphs of current-voltage characteristic shown in fig. (c) to (h), determine the arrangement of components between $A$, $B$ and $C$.

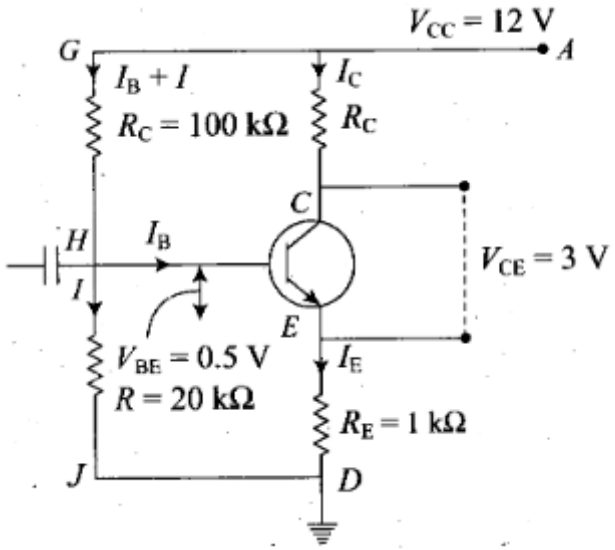
**Solution:** The V-I characteristics of these graph is discussed in points:
(a)In V-I graph of condition (i), a reverse characteristics is shown in fig. (c). Here A is connected to n-side of p-n junction I and B is connected top-side of p-n junction I with a resistance in series.
(b)In V-I graph of condition (ii), a forward characteristics is shown in fig. (d), where 0.7 V is the knee voltage of p-n junction I. 1/slope = (1/1000) Ω.
It means A is connected to n-side of p-n junction I and B is connected to p-side of p-n junction I and resistance R is in series of p-n junction I between A and B.
(c)In V-I graph of condition (iii), a forward characteristics is shown in figure (e) , where 0.7 V is the knee voltage. In this case p-side of p-n junction II is connected to C and n-side of p-n junction II to B.
(d)In V-I graphs of conditions (iv), (v), (vi) also concludes the above connection of p-n junctions I and II along with a resistance R.
Thus, the arrangement of p-n I, p-n II and resistance R between A, B and C will be as shown in the figure.




**Question 39. For the transistor circuit shown in figure, evaluate $V_E$, $R_B$, $R_E$, given $I_C$= 1 mA, $V_{CE}$= 3, $V_{BE}$ = 0.5 V and $V_{CC}$= 12 V, β= 100.**




**Solution:** Let us redraw the circuit diagram given here to solve this problem.




As we know the base current is very small. So,

$I_C \approx I_E$

$R_C = 7.8$ kΩ

From the figure, $I_C(R_C + R_E) + V_{CE} = 12$

$(R_E + R_C) \times 1 \times 10^{-3} + 3 = 12$

$R_E + R_C = 9 \times 10^3 = 9$ kΩ

$R_E = 9 - 7.8 = 1.2$ kΩ

$V_E = I_E \times R_E$

$= 1 \times 10^{-3} \times 1.2 \times 10^3 = 1.2$ V

Voltage $V_B = V_E + V_{BE} = 1.2 + 0.5 = 1.7$ V

Current, $I = \dfrac{V_B}{20 \times 10^3} = \dfrac{1.7}{20 \times 10^3} = 0.085$ mA

Resistance, $R_B = \dfrac{12 - 1.7}{\dfrac{I_C}{\beta} + 0.085} \times 10^3 = \dfrac{10.3}{0.01 + 0.085}$ [Given, $\beta = 100$]

$= 108$ kΩ

**Question 40. In the circuit shown in figure, find the value of $R_C$.**

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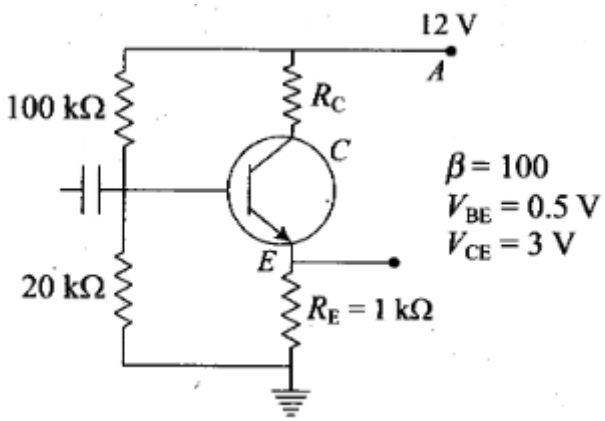



**Solution:**

Let us consider the circuit diagram to solve this problem,

$I_E = I_C + I_B$ and $I_C = \beta I_B$ ...(i)

$I_C R_C + V_{CE} + I_E R_E = V_{CC}$ ...(ii)

$RI_B + V_{BE} + I_E R_E = V_{CC}$ ...(iii)

$\because \quad I_E \approx I_C = \beta I_B$

From (iii),

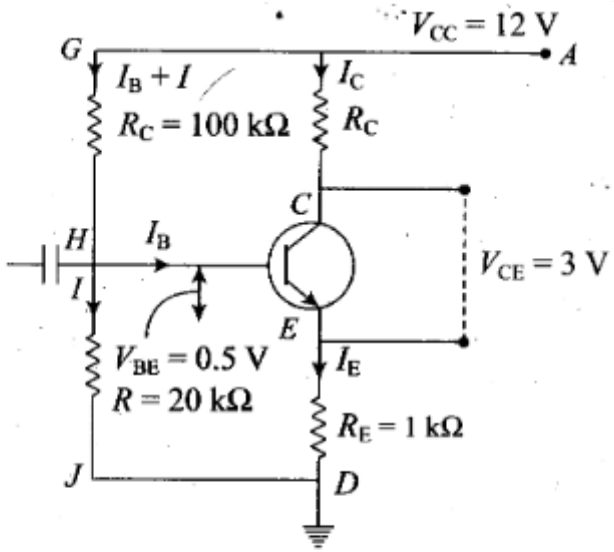
$$(R + \beta R_E) I_B = V_{CC} - V_{BE}$$

$$\Rightarrow \quad I_B = \frac{V_{CC} - V_{BE}}{R + \beta \cdot R_E}$$

$$= \frac{12 - 0.5}{80 + 1.2 \times 100} = \frac{11.5}{200} \text{ mA}$$

From (ii),

$$(R_C + R_E) = \frac{V_{CE} - V_{BE}}{I_C} = \frac{V_{CC} - V_{CE}}{\beta I_B} \qquad (\because I_C = \beta I_B)$$




$$(R_C + R_E) = \frac{2}{11.5}(12 - 3)\,\text{k}\Omega = 1.56\,\text{k}\Omega$$

$R_C + R_E = 1.56$

$R_C = 1.56 - 1 = 0.56$ kΩ or 560 Ω