Microprocessor Core Final Project Report
EE E4321: Digital VLSI Design

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1 Introduction

1.1 Problem Description

This project involves the full custom transistor-level design of a simple microprocessor core. The design includes an ALU, shifter, 8-bit latches, a 3-to-1 multiplexer, an 8-bit tristate bus driver, memory, and a PLA-based instruction decoder. The objective is to complete layout, verify functionality through extracted simulation, measure timing using Spectre, and estimate average and worst-case dynamic power.

1.2 Microarchitecture Overview

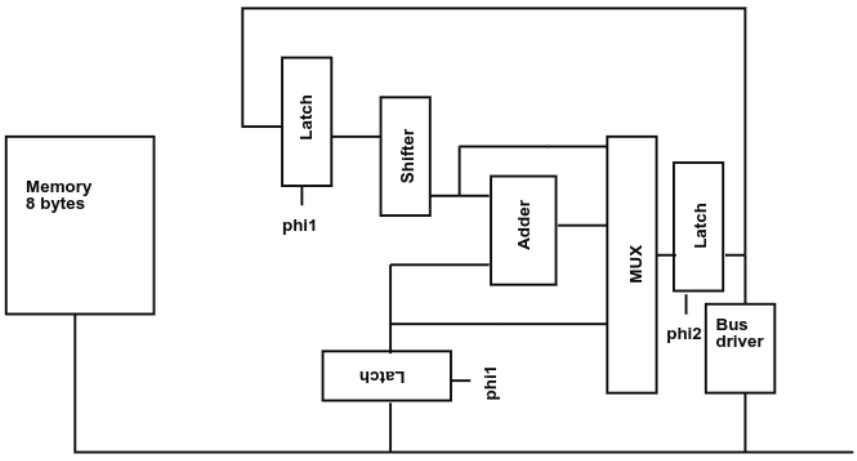

Figure 1: Microarchitecture of the Designed Microprocessor Core.

A two-phase non-overlapping clocking scheme (phi1/phi2) governs the datapath. All control signals derived from the instruction word are latched on phi1 to provide phi1-stable operation. The datapath integrates memory, accumulator latches, an 8-bit adder, shifter, and a shared internal bus.

2 Schematics and Layout of Sub-Blocks

This section contains each block's schematic and layout grouped under their respective subsection titles.

2.1 8-Bit Adder

Schematic

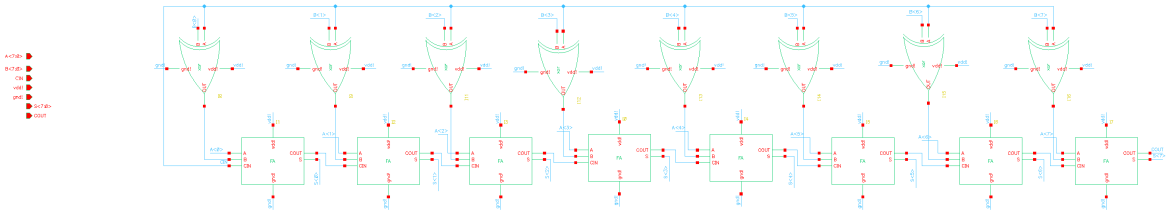

Figure 2: 8-Bit Adder Schematic.

Layout

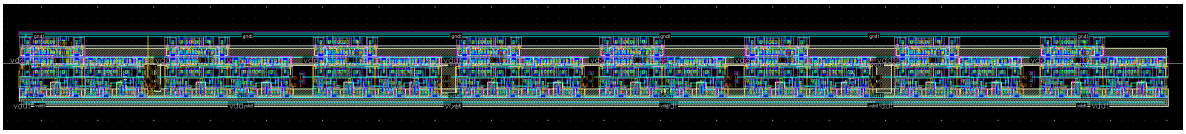

Figure 3: 8-Bit Adder Layout.

Description goes here.

2.2 8-Bit Level-Sensitive Latch

Schematic

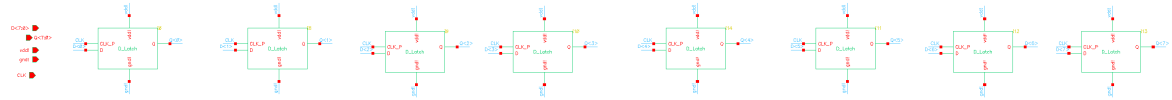

Figure 4: 8-Bit Latch Schematic.

Layout

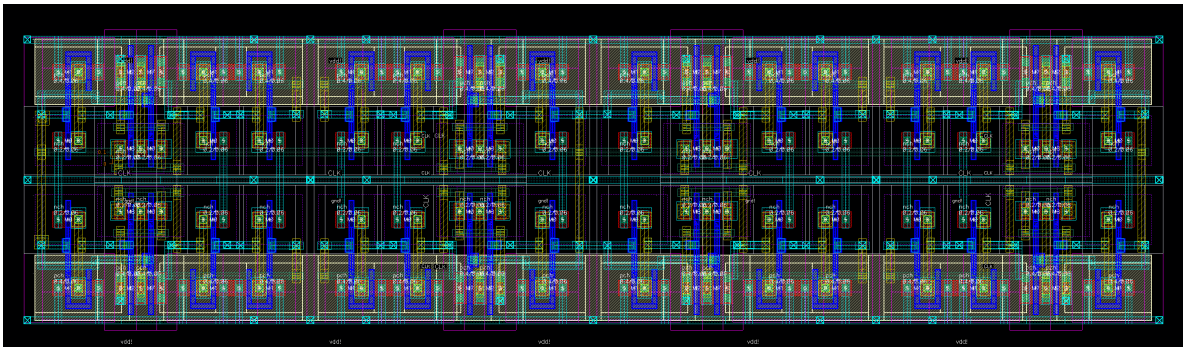

Figure 5: 8-Bit Latch Layout.

Description goes here.

2.3 8-Bit Tristate Bus Driver

Schematic

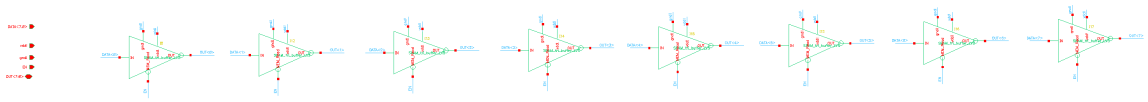

Figure 6: 8-Bit Tristate Bus Driver Schematic.

Layout

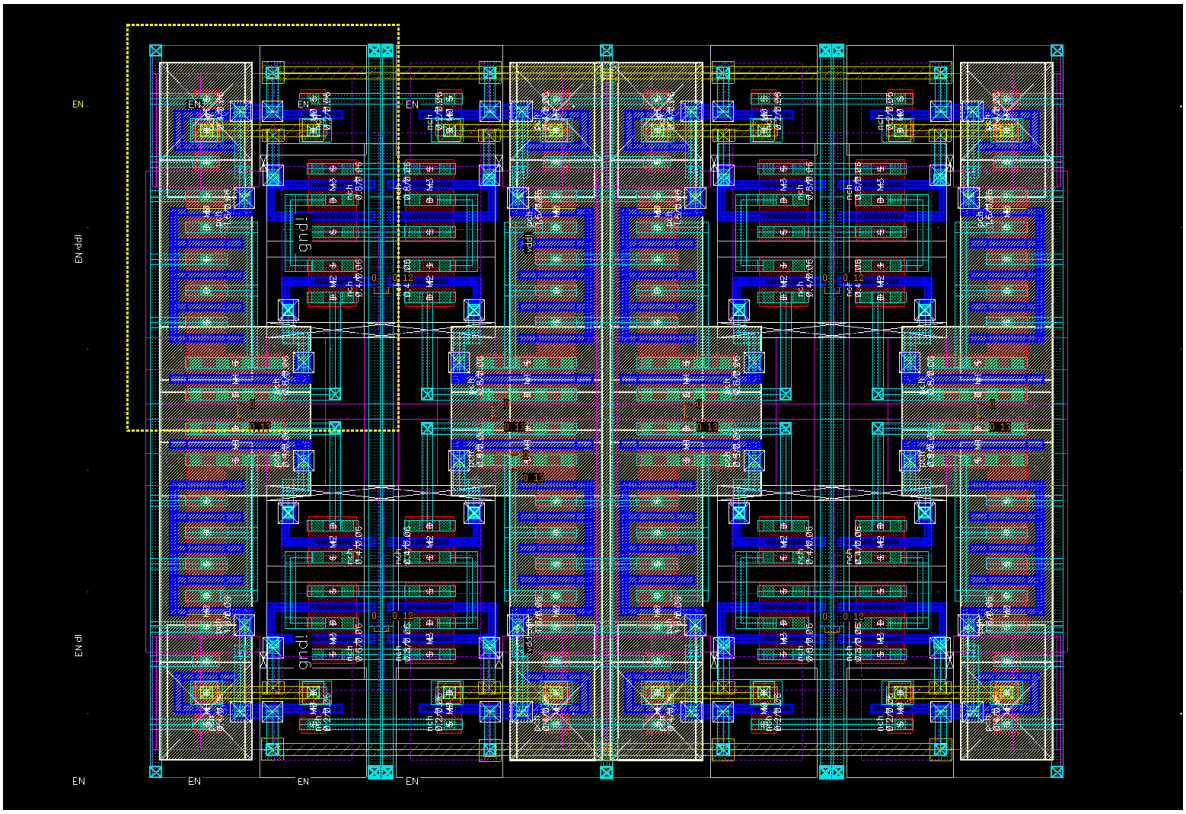

Figure 7: 8-Bit Tristate Bus Driver Layout.

2.4 8-Bit 3-to-1 Multiplexer

Schematic

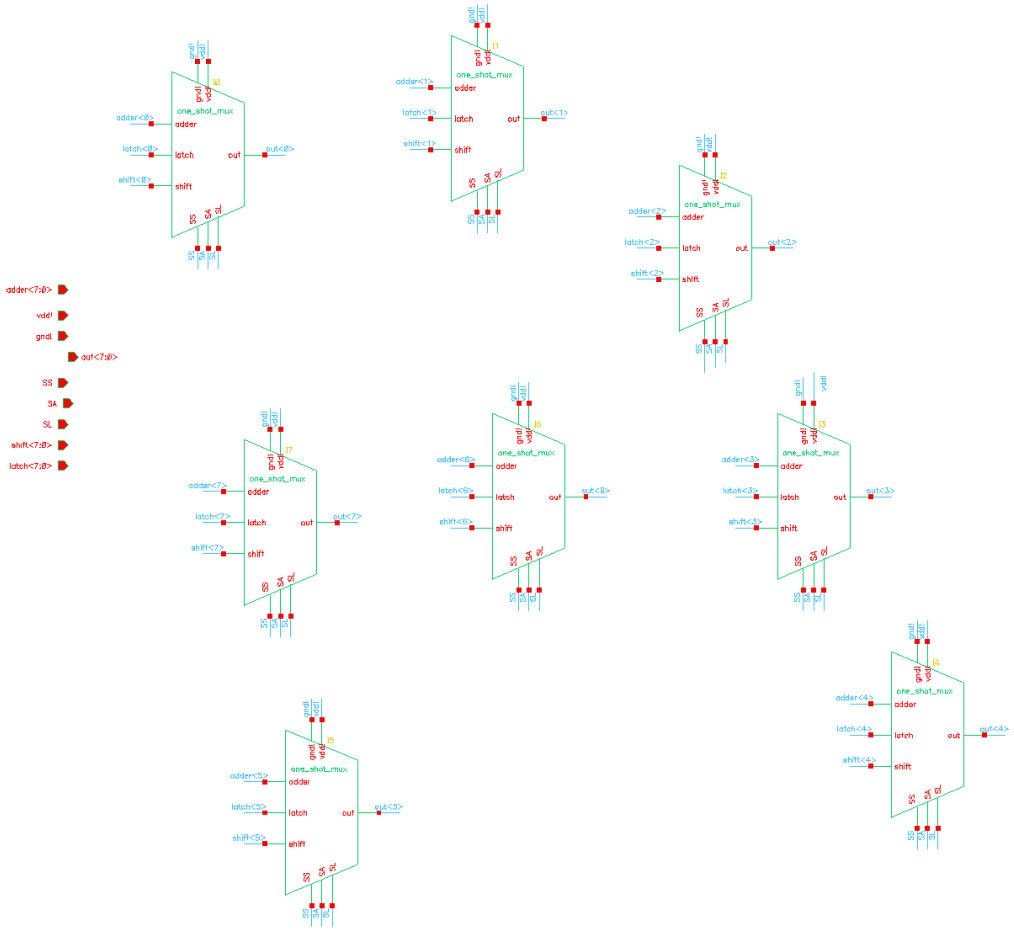

Figure 8: 8-Bit 3-to-1 MUX Schematic.

Layout

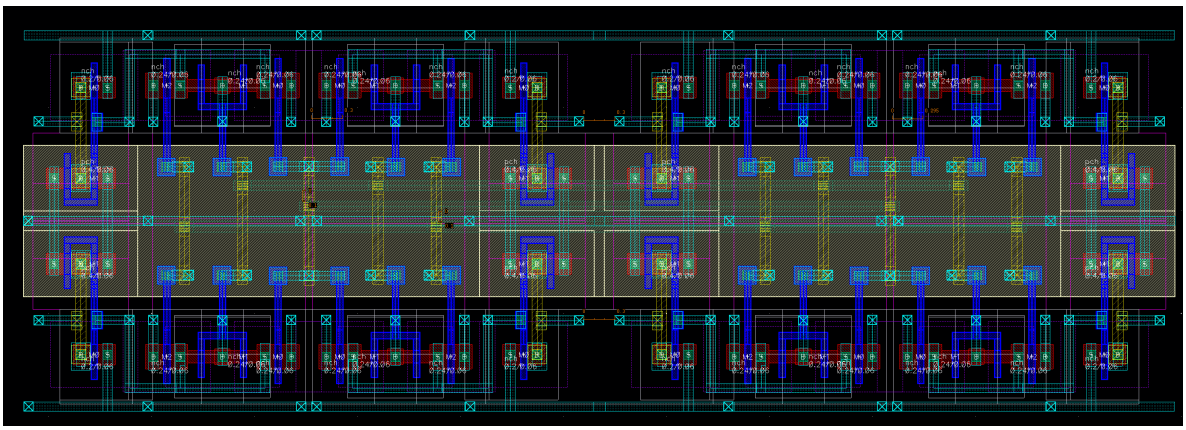

Figure 9: 8-Bit 3-to-1 MUX Layout.

2.5 SRAM / Memory Block

Schematic

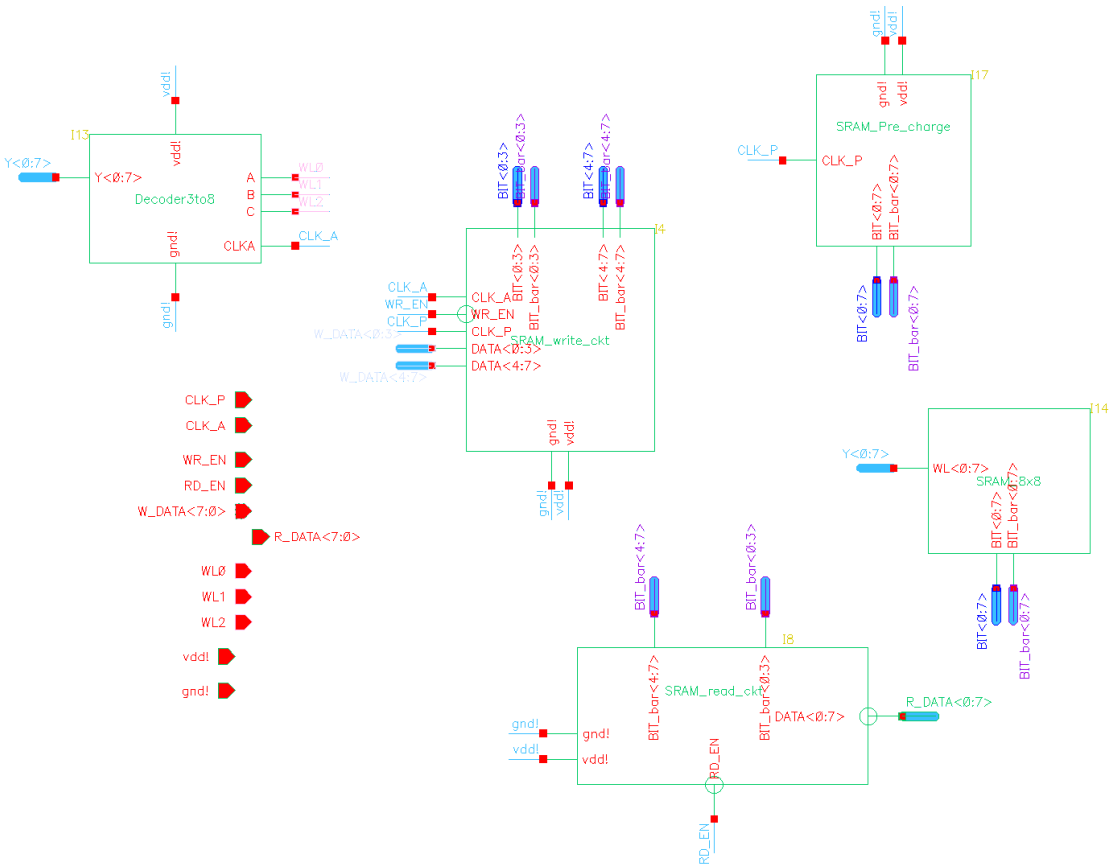

Figure 10: SRAM Schematic.

Layout

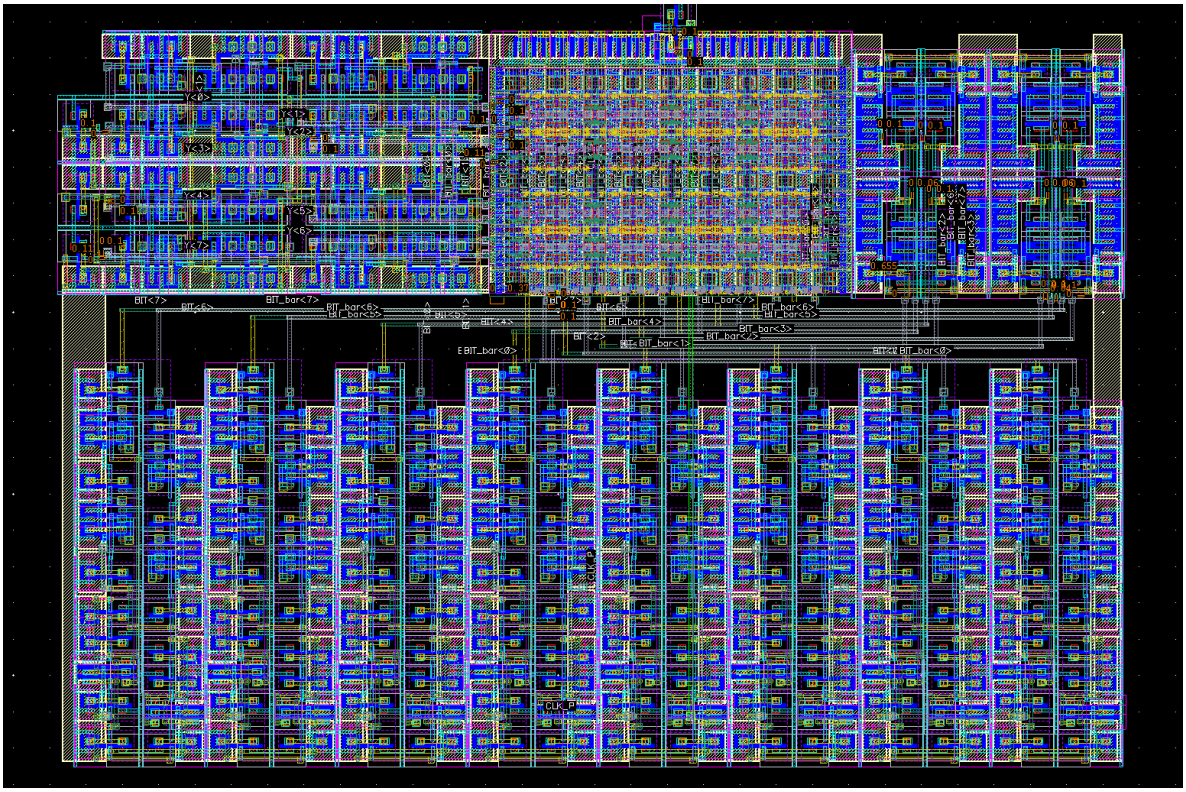

Figure 11: SRAM Layout.

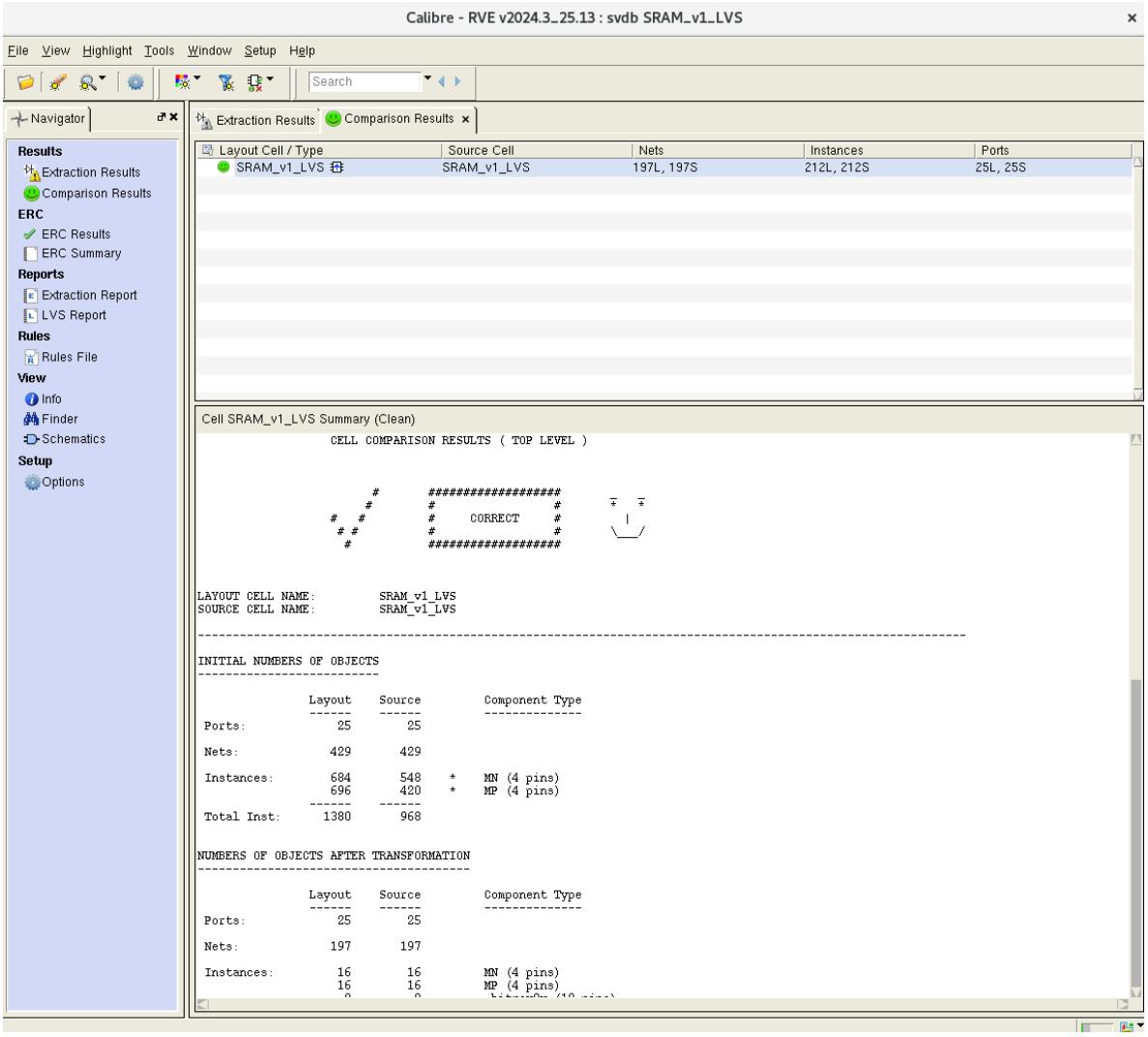

Figure 12: SRAM Lvs.

2.6 8bit shifter

Schematic

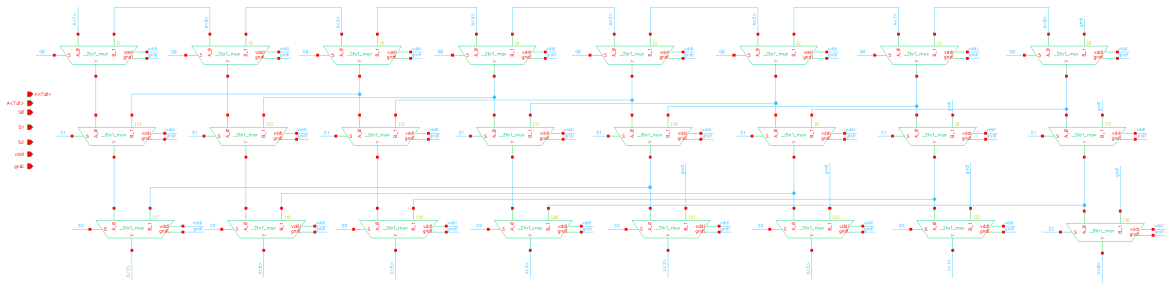

Figure 13: 8bit shifter Schematic.

Layout

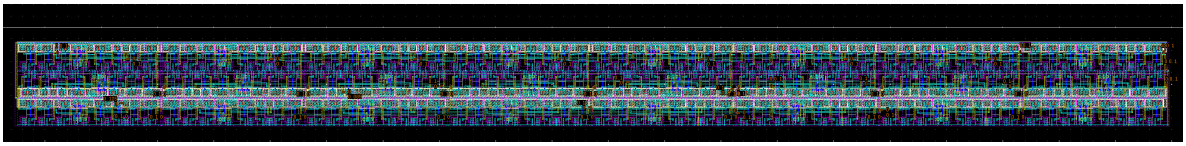

Figure 14: 8bit shifter.

2.7 PLA Instruction Decoder

Schematic

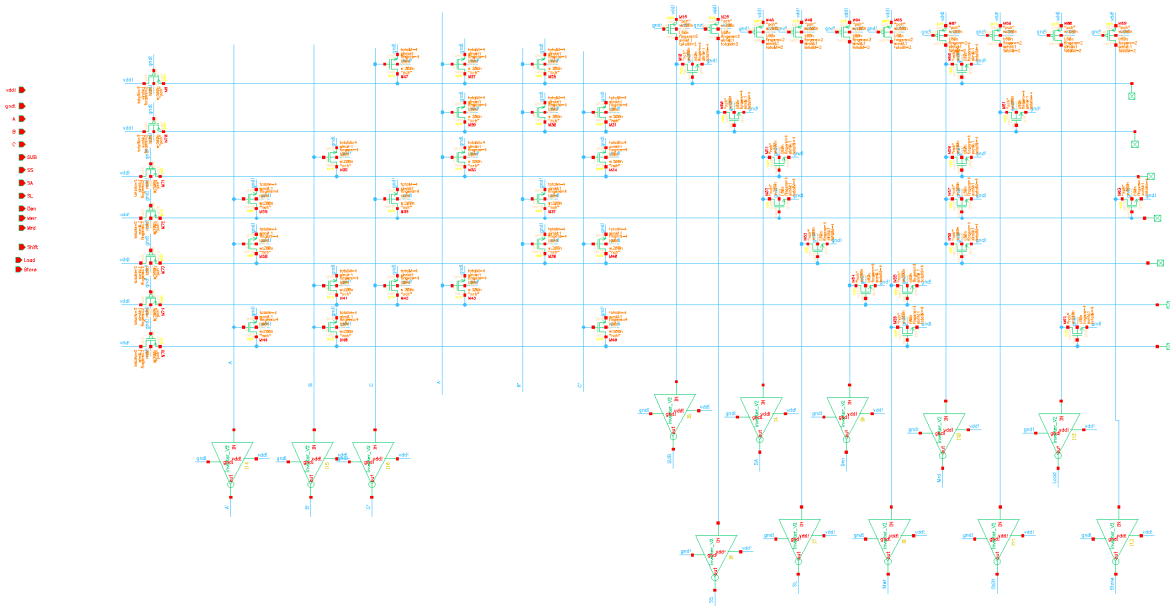

Figure 15: PLA Instruction Decoder Schematic.

Layout

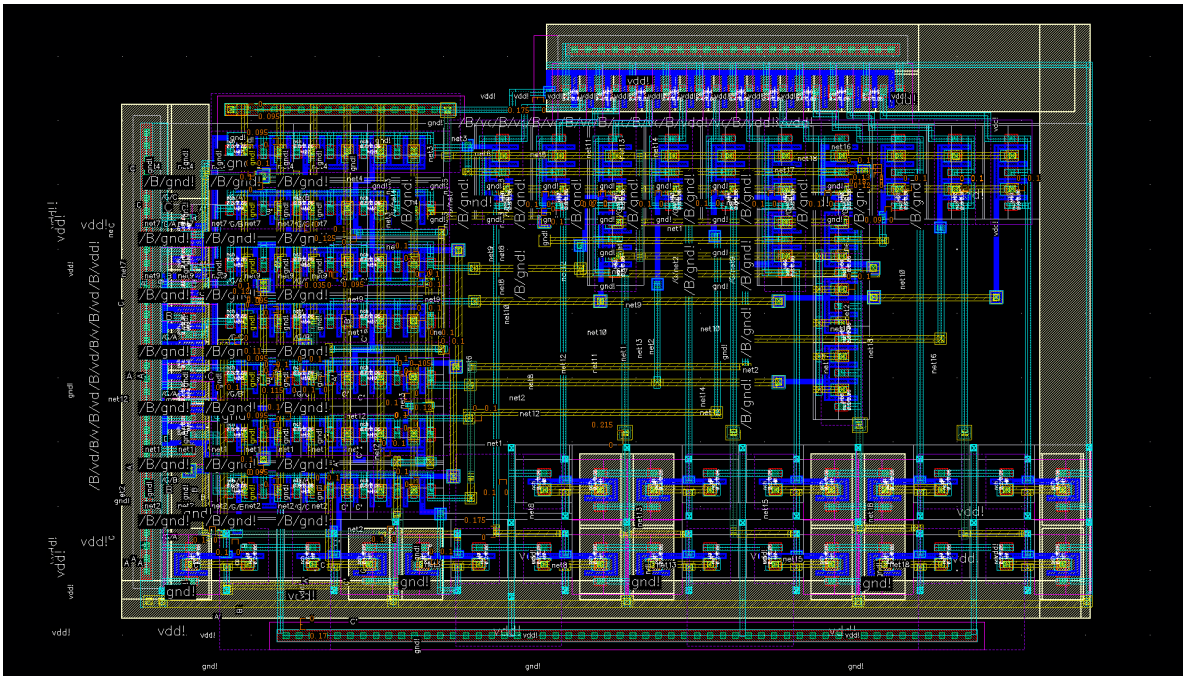

Figure 16: PLA Instruction Decoder Layout.

3 Full Chip Schematic

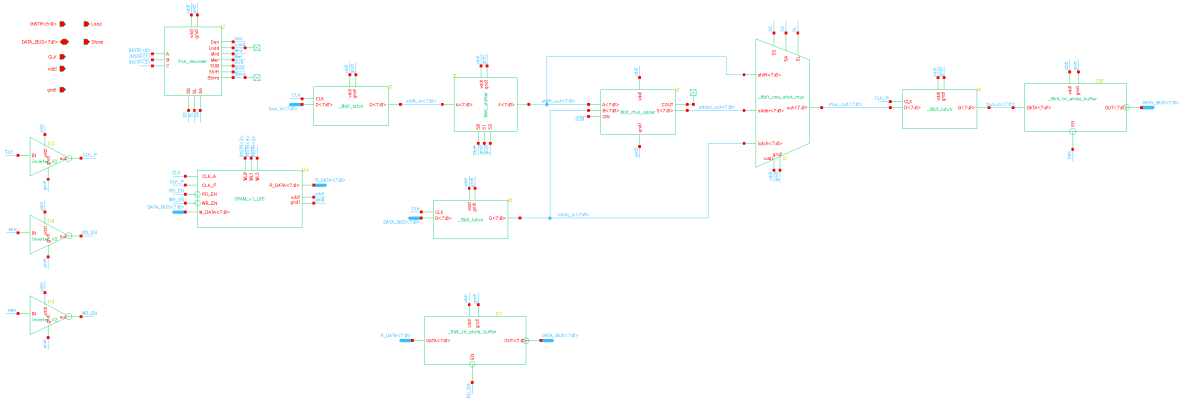

Figure 17: Full Chip Schematic of the Microprocessor Core.

4 Full Microprocessor Integration

Top-Level Layout

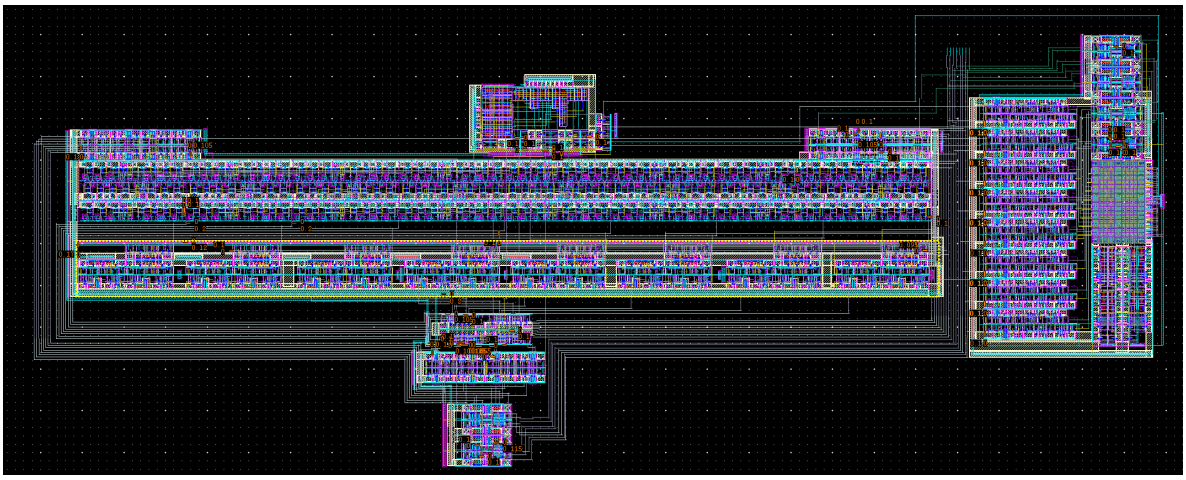

Figure 18: Top-Level Microprocessor Layout.

Top-Level Layout DRC

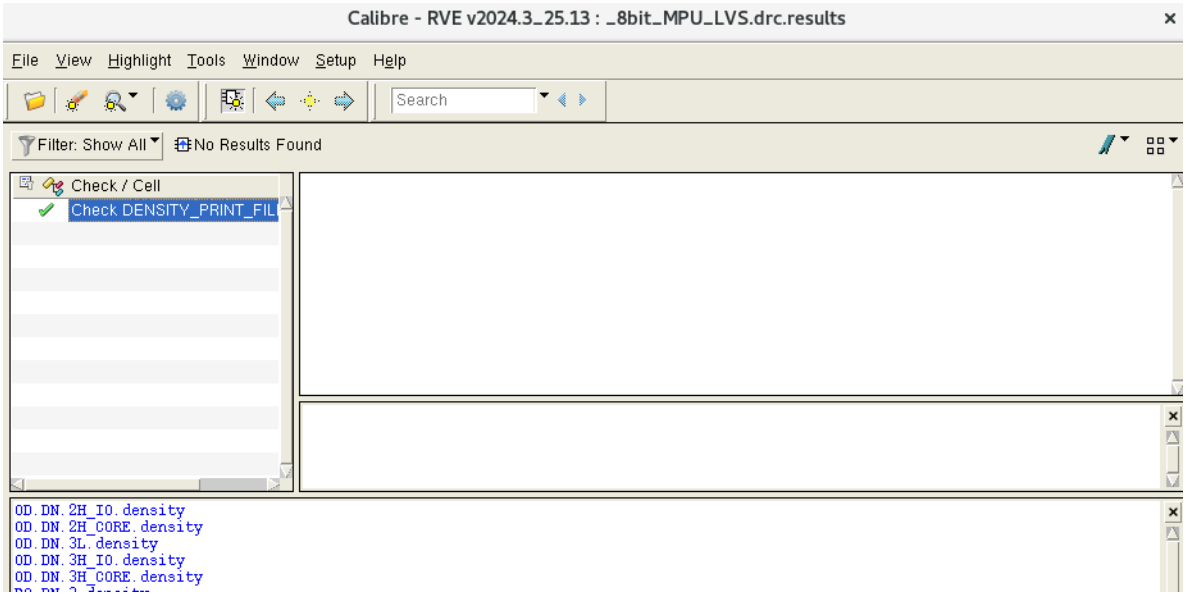

Figure 19: DRC clean.

5 Results and Simulations

5.1 Testbench Configuration

The testbench consists of an 8-bit microprocessor, two ADCs for converting voltage inputs into 8-bit digital data for the data bus, and a 6-bit instruction set. Additionally, an 8-bit tristate buffer with a control signal is used to drive the data bus during a load opcode. Otherwise, the buffer remains in a high-impedance (Hi-Z) state to avoid bus contention.

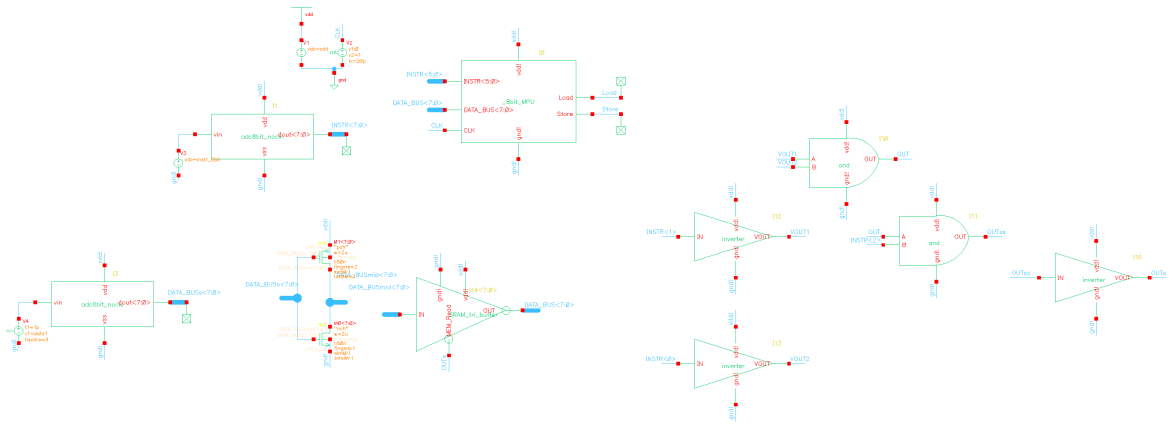

Figure 20: Simulation Testbench.

5.2 Functional Verification

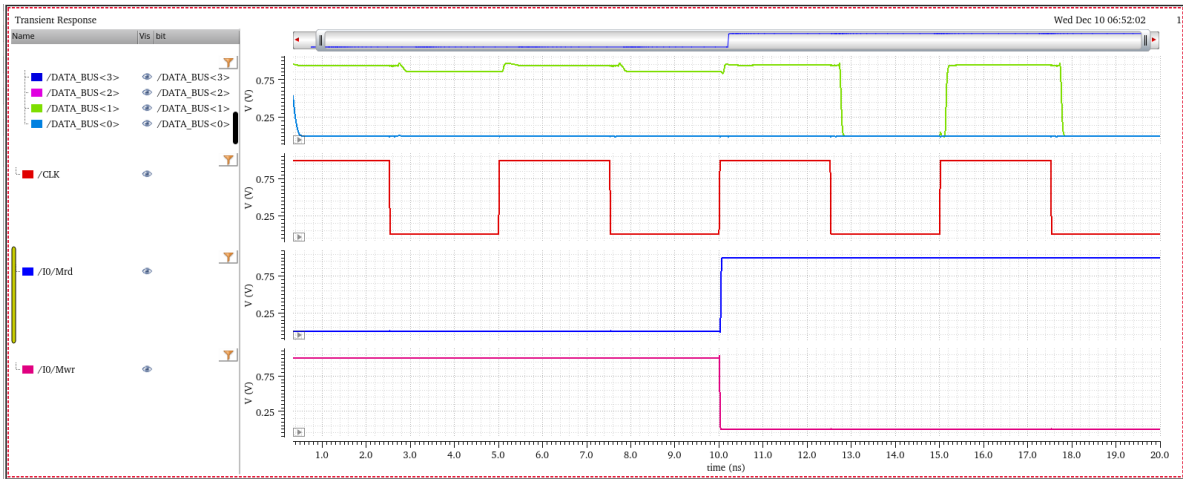

Figure 21: Memory read and write with load and store Opcode.

The data corresponding to December 255 is initially loaded, which can be inferred from the memory write signal initially. Subsequently, the data is read from the SRAM at 10ns, indicated by the memory read signal being high. During the phi1 phase, the same data appears on the data bus.

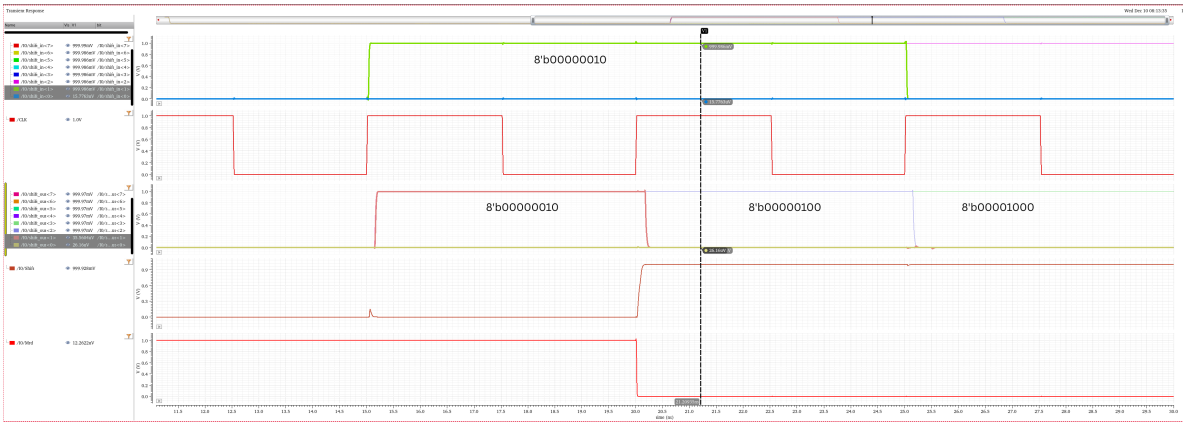

Figure 22: Data out with shift Opcode.

The shifter receives an initial data value of 2. Shifting begins at 20ns, indicated by the shift signal going high. In the subsequent ph1 clock phases, the data successively becomes 4 and then 8.

Figure 23: ALU performing add operation.

At 12ns, the memory read signal goes high, indicating the start of the addition operation. The inputs to the adder are 2 (obtained from the shifter after shifting) and 3 (from the latch). The adder produces an output of 5, as expected.

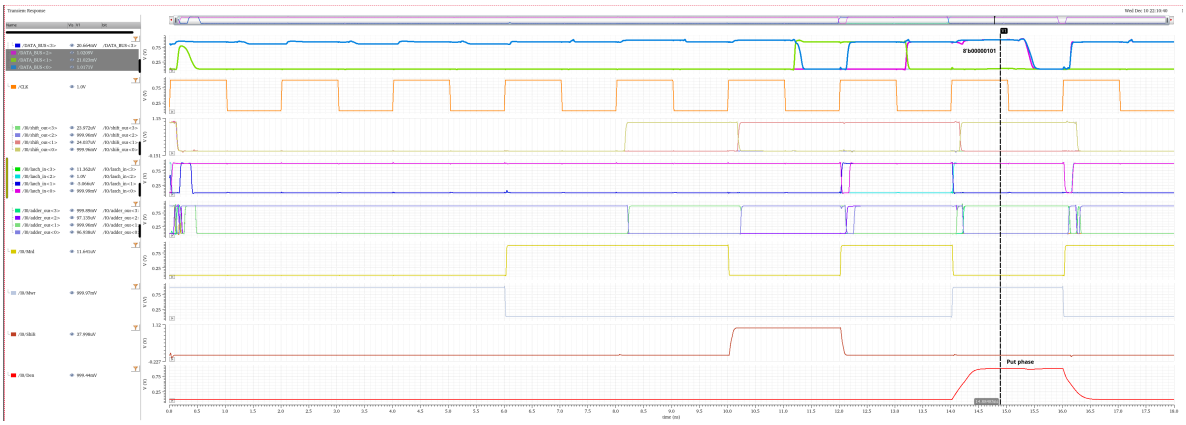

Figure 24: Data is written into SRAM and data-bus using Put Opcode .

After the addition, at 14ns, the Put opcode is executed, which writes the result into the data bus and SRAM. This is indicated by the Den signal and the memory write signal going high. The data bus shows the expected value of 5

5.3 Critical Path Timing (Spectre)

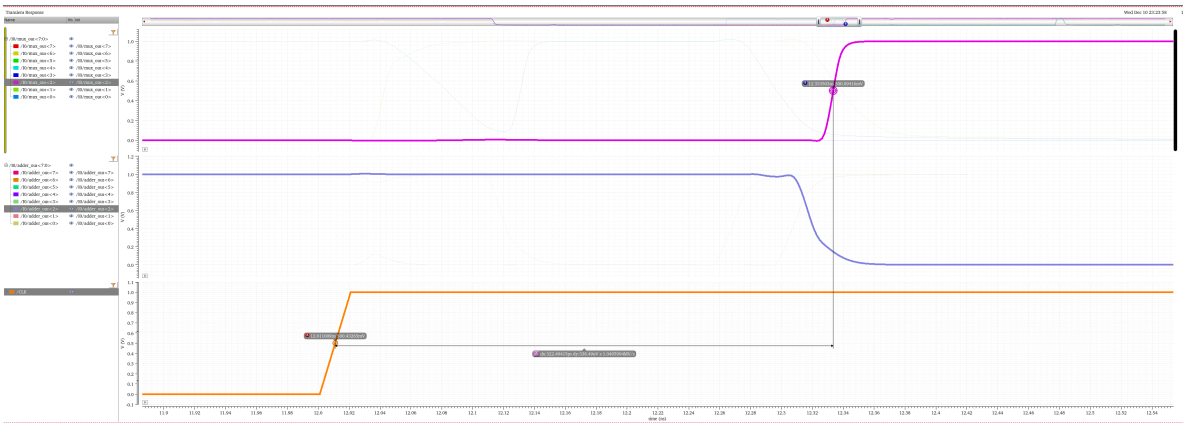

Figure 25: Critical Path Timing using Spectre.

The critical path in the microprocessor extends from the latch output → adder → multiplexer output. This entire path must complete within a single ϕ (phi) clock phase. From simulations, the delay from the clock edge to the multiplexer output is measured to be 350 ps. Therefore, the maximum clock frequency $f_{\max}$ can be estimated as:

$$f_{\max} = \frac{1}{2T_{\text{clk}}} = \frac{1}{350\ \text{ps}} \approx 1.4\ \text{GHz}$$

This indicates that the microprocessor can operate reliably at a maximum frequency of approximately 2.86 GHz.

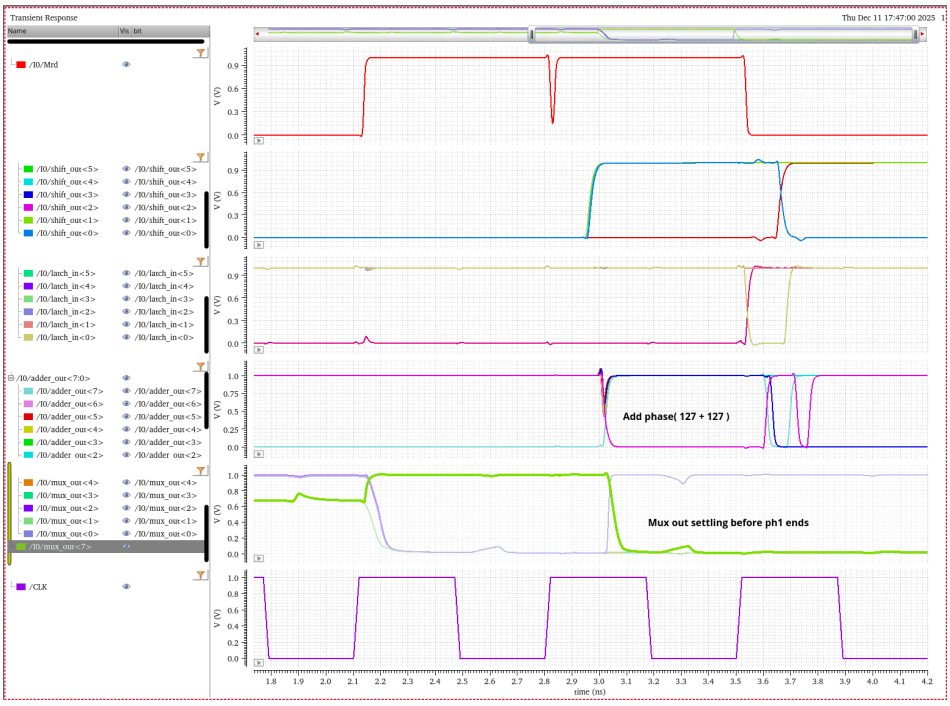

Figure 26: Add Opcode running at 1.4GHz CLK and giving correct results at Mux out.

The `ADD` opcode was successfully verified to operate correctly at a clock frequency of 1.4 GHz, as illustrated in the preceding results. Additional tests further confirm the functional correctness of the microprocessor design.

5.4 Power Analysis

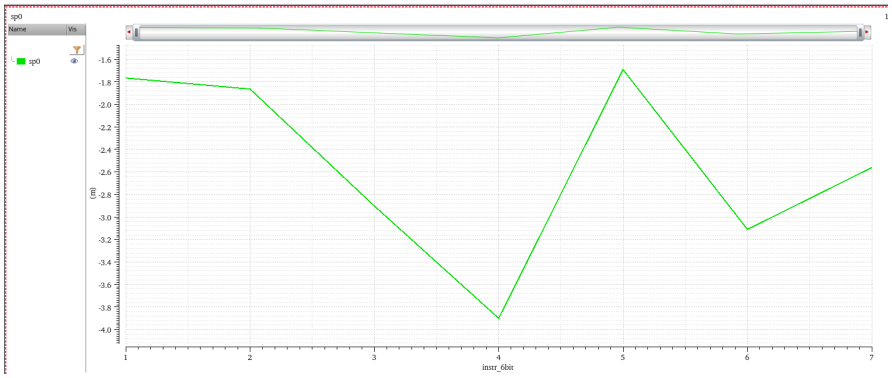

Figure 27: Power Analysis Results for different Opcodes in mW.

The dynamic power consumption of the microprocessor is primarily due to bit transitions, i.e., when a node switches from 0 to 1 or from 1 to 0. Each such transition charges or discharges the capacitance associated with the transistor, gate, or interconnect, drawing current from the supply. Consequently, nodes that switch more frequently, or wide buses with multiple bits toggling simultaneously, contribute significantly to the overall power consumption. The clock network also plays a major role in dynamic power, as it toggles every cycle and drives large capacitive loads.

Static power, which results from leakage currents even when the circuit is idle, is generally small in CMOS designs compared to dynamic power. Therefore, in the designed 8-bit microprocessor, the total power is largely dictated by the switching activity of the datapath, memory elements, and control signals. Reducing unnecessary toggling, optimizing the clock distribution, and minimizing bus activity are key strategies to limit dynamic power consumption.

6 Summary

The designed 8-bit microprocessor core has been functionally verified using simulations and testbench results. The processor operates correctly at a maximum frequency of 1.4 GHz. The total area of the design is $135u \times 56u\ \mu m^2$ (to be measured from the layout). The maximum dynamic power consumption is 4 mW, while the static (leakage) power is approximately 1.4 mW. Overall, the processor demonstrates correct functionality and meets the expected performance and power specifications.