ODD-EWEN COUNTER USING J-K FLIPFLOP FUNDAMENTAL OF DIGITAL ELECTRONICS

Reference

BOOK: Digital Logic and Computer Design

AUTHOR : M. MORRIS MANO

Project Engineers

Chiatanya Patel (11BCE069)

Darshil Patel (11BCE070)

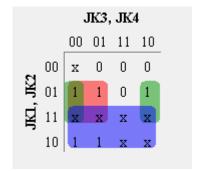
Vivek Patel (11BCE073)

Computer Engineering Department
Institute of Technology
Nirma University

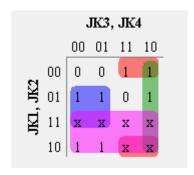
K-MAPS

10th DIGIT GENERATOR IC Segment A Segment B

JK2' JK3 + JK3 JK4' + JK2 JK3' + JK1

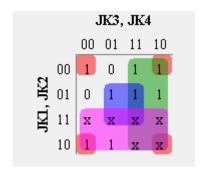


JK3' JK4' + JK2 JK3' + JK2 JK4' + JK1



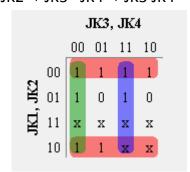
Segment C

JK2' JK4' + JK3 + JK2 JK4 + JK1



Segment D

JK2' + JK3' JK4' + JK3 JK4

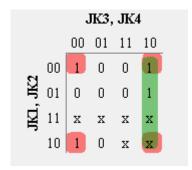


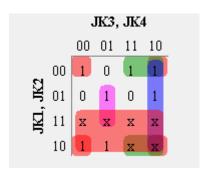
Segment E

Segment F

JK2' JK4' + JK3 JK4'

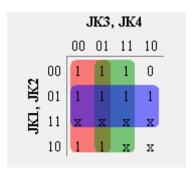
JK2' JK4' + JK2 ' JK3 + JK3 JK4' + JK2 JK3' JK4 + JK1





Segment G

JK3 '+ JK4 + JK2



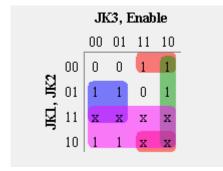
K-MAPS

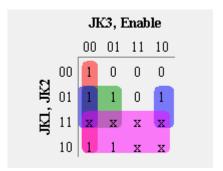
UNIT DIGIT GENERATOR IC

Segment A

Segment B

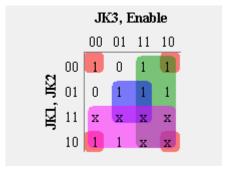
JK2' JK3 + JK3 Enable' + JK2 JK3' + JK1 JK3' Enable' + JK2 JK3' + JK2 Enable' + JK1





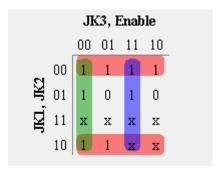
Segment C

JK2' Enable' + JK3 + JK2 Enable + JK1



Segment D

JK2' + JK3' Enable' + JK3 Enable



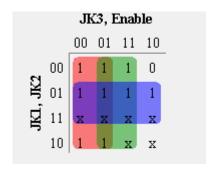
Segment E

JK2' Enable' + JK3 Enable'

		JK3, Enable			
		00	01	11	10
JK1, JK2	00		0		1
	01		0		1
	11	х	Х	X	x
	10	-	0		x

Segment G

JK3' + Enable + JK2



Segment F

JK2' Enable' + JK2' JK3 + JK3 Enable' + JK2 JK3' Enable + JK1

