One Bit Half Adder Carry Only with CPL

Special Assignment Report

2EC501 VLSI

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Abstract

- The design of a one-bit half adder with carry propagation logic (CPL) is shown in this study. A fundamental part of digital circuits used for binary addition is the one-bit half adder. Two essential components of the design are an AND gate for carry (C) determination and an XOR gate for sum (S) calculation.
- Two NMOS and two PMOS transistors are used in the construction of the XOR gate, which computes the exclusive OR of two binary inputs, A and B, to produce the sum output (S). Concurrently, the AND gate uses comparable transistor designs to determine the carry output (C) using the same inputs.
- Multi-bit binary addition is made possible by cascading one-bit half adders thanks to the carry propagation logic of the architecture. One half adder's carry output is used as the carry.

Introduction

The purpose of this report is to detail the design of a one-bit half adder with complementary pass transistor logic (CPL). The one-bit half adder is a fundamental building block of digital circuits, used for binary addition. In this design, we will focus on creating a half adder with a CPL structure.

Components:

- NMOS transistors (for pass transistors)
- PMOS transistors (for pass transistors)
- XOR gate (using complementary pass transistor logic)
- AND gate (using complementary pass transistor logic)

Design:

XOR Gate with Complementary Pass Transistor Logic:

- Use NMOS and PMOS transistors to implement the XOR gate with complementary pass transistor logic.
- Connect one input (A) to the gate terminal of an NMOS transistor and the other input (B) to the gate terminal of a PMOS transistor.
- Connect the source of the NMOS transistor to ground (GND) and the source of the PMOS transistor to the positive power supply (VDD).
- Connect the drains of both transistors to a common node, which represents the XOR output.

AND Gate with Complementary Pass Transistor Logic:

- Use NMOS and PMOS transistors to implement the AND gate with complementary pass transistor logic.
- Connect one input (A) to the gate terminal of an NMOS transistor and the other input (B) to the gate terminal of a PMOS transistor.
- Connect the source of the NMOS transistor to the common node where the XOR output is located.
- Connect the source of the PMOS transistor to the positive power supply (VDD).
- Connect the drains of both transistors to a common node, which represents the AND output.

COMPLEMENTARY PASS-TRANSISTOR LOGIC (CPL):

Complementary-pass-transistor logic which is abbreviated as CPL is an integral part of pass-transistor logic (PTL). Unlike CMOS where for pull-up or pull-down networks different MOS are used, in CPL either PMOS or NMOS is used. Control signals are applied in the gate and another set of signals are applied to the sources. As the mobility of holes is lesser than that of electrons, so PMOS is not preferred. Another advantage of NMOS PTL logic style is low input load. In CPL style, complementary inputs/outputs are obtained by using NMOS PTL with CMOS output inverters. However main disadvantages are threshold voltage drop (VDD – Vth) at the output and high static power dissipation. So, it uses external circuitry for good voltage swing restoration.

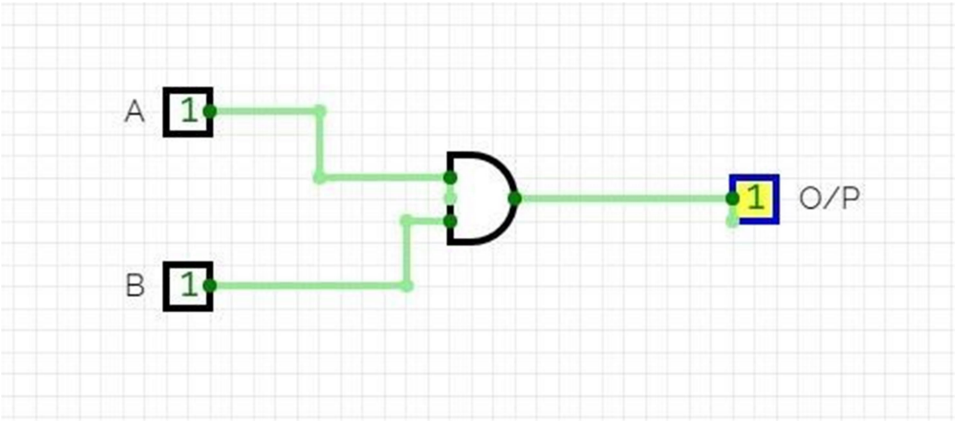
Design Problem:

1. **Find out the optimized Boolean equation (If not given).**

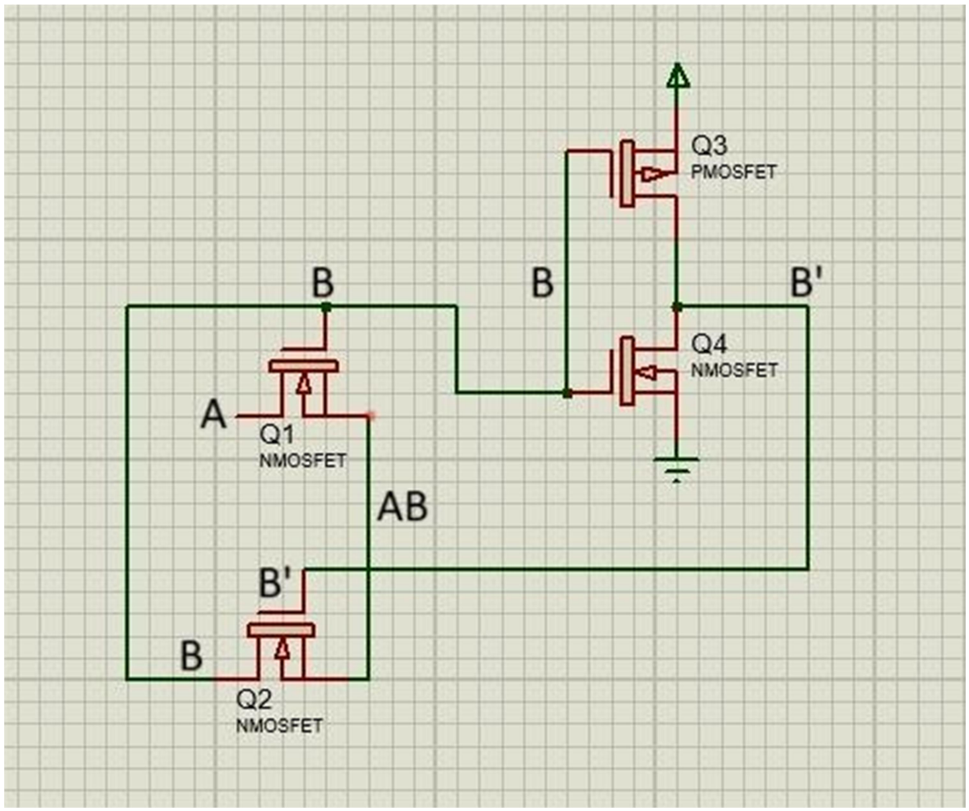
Ans: Sum = AB where, A & B are inputs and sum is output of Half Adder.

2. **Draw the optimized gate level circuit diagram.**

Ans:

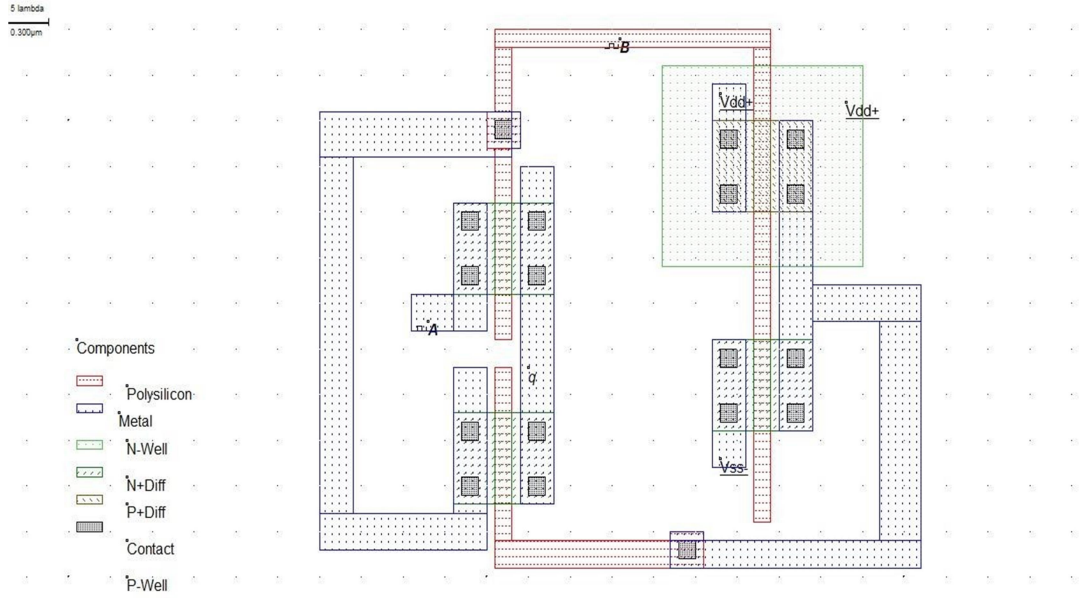


3.Draw the transistor level schematic for CMOS/MOS implementation.Ans:



4.Draw stick diagram for above implementation level using proper colour code.

Ans:

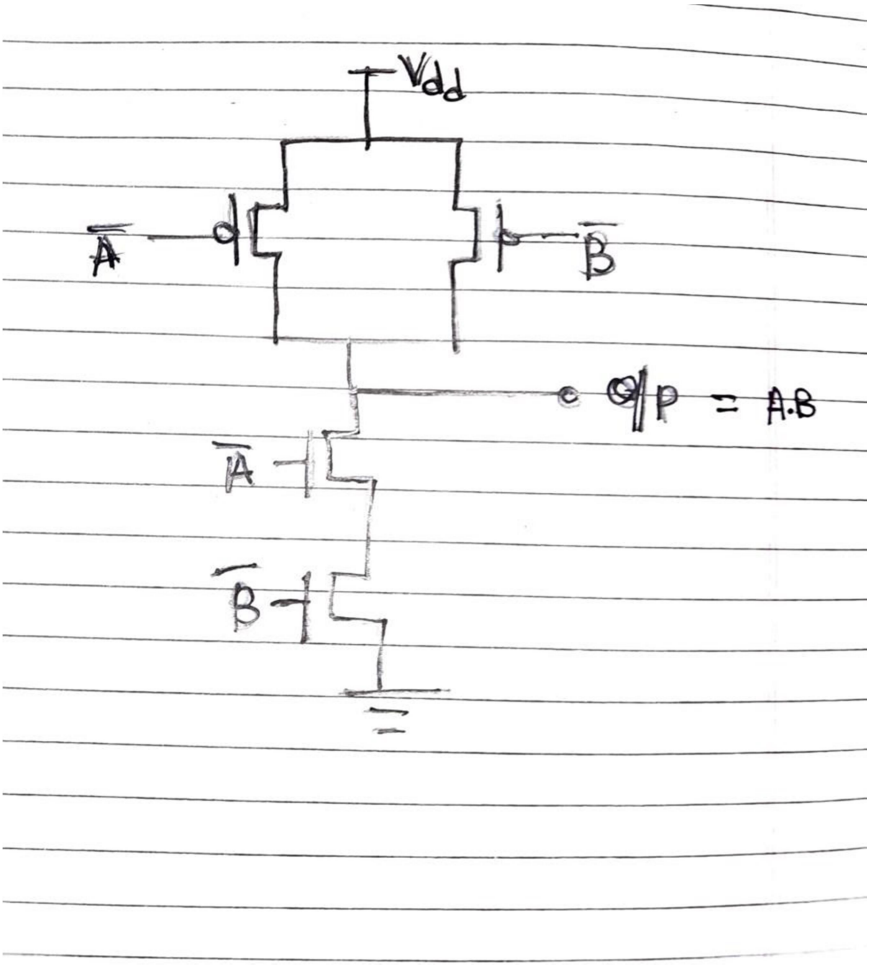


5.State the various level of VOL corresponding to various transistor statuses.

Ans: Transistor will work only in cut-off and linear region & for output low voltage (Low logic = 0) transistor operates only in cut-off region & for logical = 1 where output voltage is high transistor works only in linear region so, for low logic level 0 transistor operates in cut-off region so, VOL voltage will be 0V for any input combination.

6.Find an equivalent CMOS inverter circuit.

Ans:



7.For CMOS/MOS implementation, what input patterns give the lowest output resistance when the output is low? What is the value ofthat resistance?

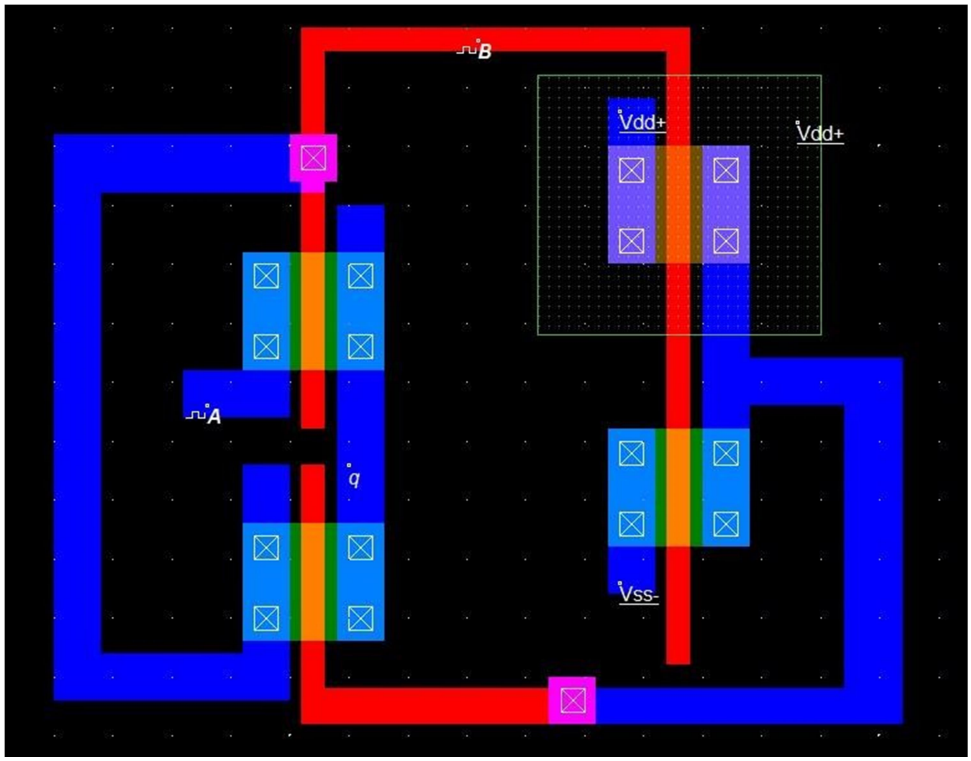
Ans: For given input pattern where output is Low value of resistance will be 40k ohm approx. Due to any one of transistor operates in cut-off region for given worst case resistance in each transistor of 20k ohm.

8.For CMOS/MOS implementation, what input patterns give the lowest output resistance when the output is high? What is the valueof that resistance?

Ans: For given input pattern where output is High value of resistance will be 5k ohm approx. Due to any one of transistor operates in linear region for given worst case resistance in each transistor of 20k ohm.

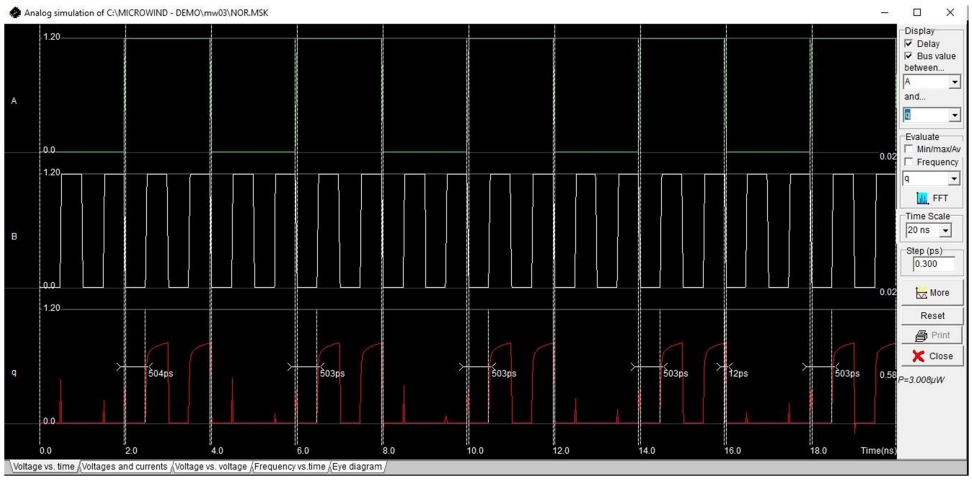
9.Prepare the layout using Micro-wind tool.

Ans:



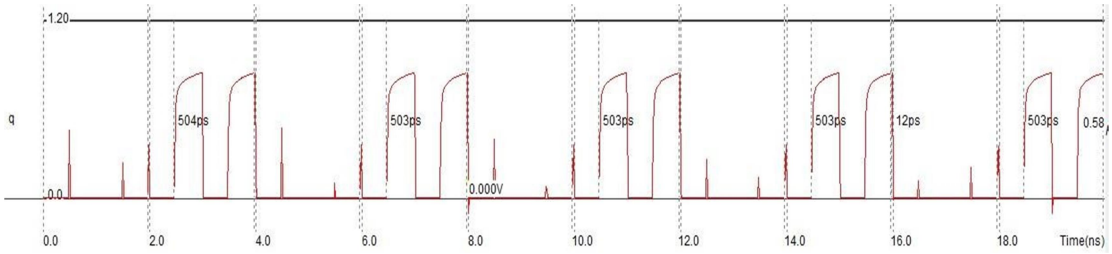
10.Simulate it for various combinations of inputs.

Ans:



11.Measure the rise time, fall time, propagation delay and other parameters.

Ans:



□ pHL = 504 ps

□ pLH = 503 ps

□ r (rise time) = 0.488ns

□ f (fall time) = 0.454ns

□ (propagation delay) = (□ pHL + □ pLH) / 2 = 503.5ps

Conclusion:

- To sum up, we have successfully created a half adder that is one bit and has carry propagation logic. This fundamental building block can be cascaded to form multi-bit adders for more complicated arithmetic operations. It is necessary for binary addition in digital circuits. For sum and carry computations, the design uses AND gates and XOR gates, respectively.
- In order to efficiently perform binary addition on multi-bit values, we can connect together many one-bit half adders using the carry propagation logic.