CLASS PROJECT

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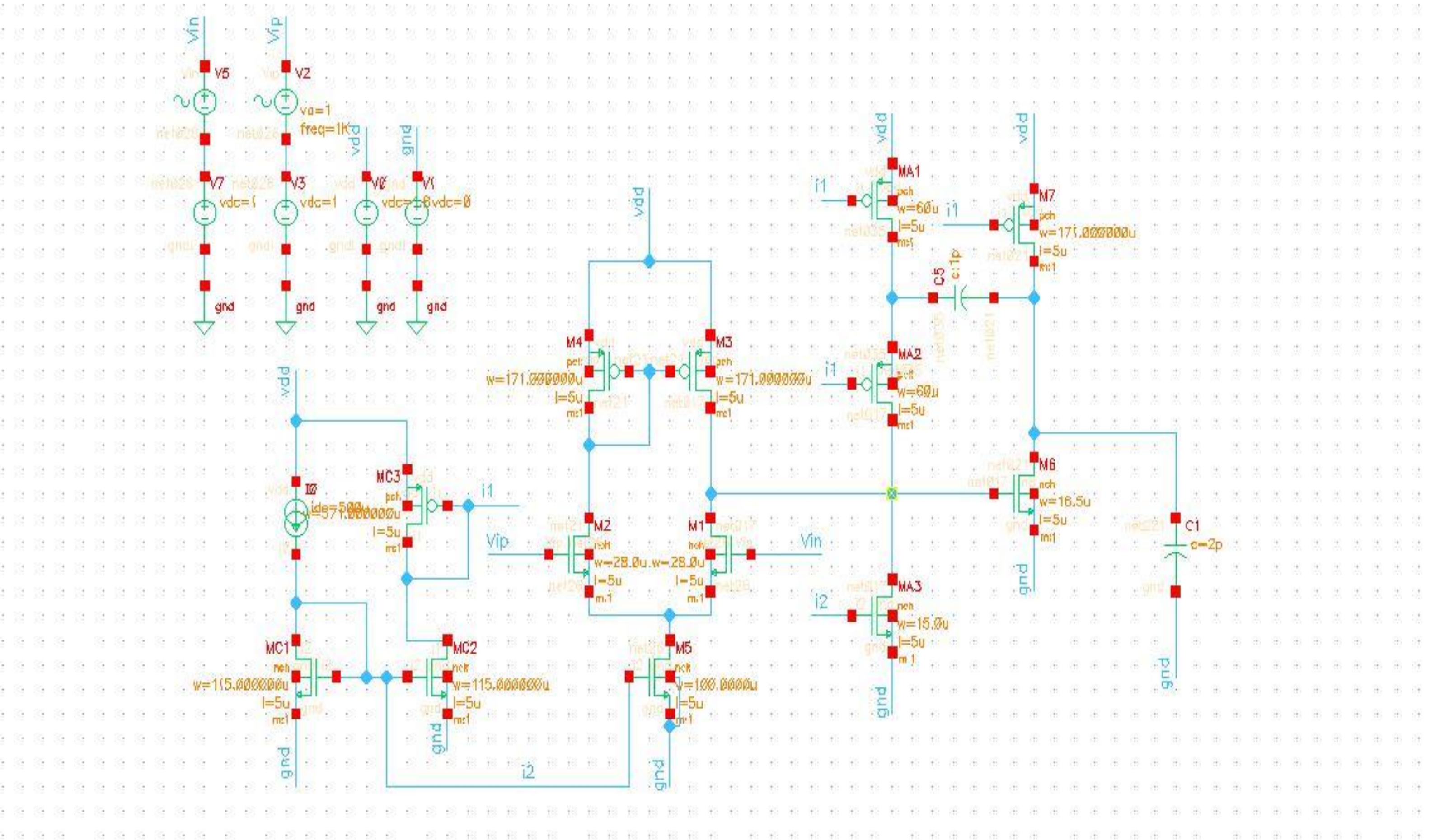
Aim:-To design of a two-stage op-amp with indirect Ahuja compensation.

Schematic:-



Note:- The size of transistor are not the one in schematic.

* Final Project *

1: Given that.

Gain > 60 db > 1000.

Phase Margin $> 50°$

Unity gain freq > 100 MHz

Power < 1 mW

$V_{dd} = 1.8$ V

$C_L = 2$pF.

For two stage amplifier.

A_v(total gain) $= A_1 * A_2$

from above diagram

$$A_1 = g_{m1}(r_{o2} \| r_{o4})$$
$$A_2 = g_{m6}(r_{o6} \| r_{o7}).$$

$$A_v = g_{m1}(r_{o2} \| r_{o4}) * g_{m6}(r_{o6} \| r_{o7})$$

$$\boxed{1000 < g_{m1}(r_{o2} \| r_{o4}) * g_{m6}(r_{o6} \| r_{o7})} \quad \text{—(1)}$$

Given Power budget < 1m W

$P = V_{dd}(I_{davg})$

i.e $(1.8)(I_{davg}) < 1$m W

$$I_{davg} < \frac{10^{-3}}{1.8}$$

$$\boxed{I_{d(avg)} < 555.5\ \mu A}$$

Thus we have to divide current in stage-1 stage-2 and buffers stage in such a way that Phase margin and all criteria are satisfied. For ease of calculation take total drain current $\boxed{I_d = 500\ \mu A}$.

* $\underline{G.B.W = 2\pi \times \text{Unity gain freq.}}$

For PM $> 50°$.

$$\tan^{-1}\left(\frac{GBW}{P_2}\right) + \tan^{-1}\left(\frac{GBW}{Z_1}\right) < 40°$$

$$Z_1 = g_{m2}/C_c,\quad GBW = \frac{g_{m1}}{C_c},\quad P_2 = \frac{g_{m2}}{(C_c + C_L)}\left(\frac{g_{m_{CC}}}{3}\right)$$

Assume that $\frac{GBW}{Z_1} = \boxed{\frac{1}{5} = \frac{g_m}{g_{m2}}}$

$$\tan^{-1}\left(\frac{GBW}{P_2}\right) + \tan^{-1}\left(\frac{1}{5}\right) < 40°$$

$$\tan^{-1}\left(\frac{GBW}{P_2}\right) < 40° - 11.301$$

$$\tan\left(\frac{GBW}{P_2}\right) < \tan(28.699)$$

$$\frac{GBW}{P_2} < 0.5475$$

$$(0.5475)P_2 > GBW$$

$$P_2 > 1.827\ GBW$$

Keeping values of P_2 & GBW & Assume $\frac{g_{m_{CC}}}{3} = 3$

$$3\frac{g_{m2}}{C_c + C_2} > 1.827 \times \frac{g_{m1}}{C_c}$$

$$\frac{g_{m2}}{C_C + C_L} > 0.61 \frac{g_{m1}}{C_C}$$

$$(g_{m2} = 5 g_{m1})$$

$$\therefore \frac{5}{C_C + C_L} > \frac{0.61}{C_C}$$

$$5C_C > 0.61 C_C + 0.61 C_L$$

$$C_C > 0.2\cancel{7}8 \; C_L$$

$$C_C > \boxed{C_C > 0.287 \text{ pF.}}$$

keeping parasitic capacitance in mind.

lets take

$C_C = 500$ fF. i.e. 0.5pF.

U.G.F

GBW > 100 MHz

lets take it 110 MHz

$$\therefore g_{m1} = 2\pi \times (110 \text{ MHz}) \times 0.5\text{pF.}$$

$$g_{m1} = 2 \times 3.14 \times 1.1 \times 10^{-4}$$

$$\boxed{g_{m1} = 345.4 \; \mu}$$

lets take $g_{m1} = 350 \mu$.

$$\therefore g_{m2} = 350\mu \times 5 = \boxed{1.75 \text{ m}}$$

From HW 4.

$$g_m = \frac{2 I_D}{(V_G - V_{TH})}$$

$(V_{gs} - V_t)_{nmos} = 0.446$ V

$(V_g - V_{th})_{pmos} = 0.4213$ V

$$\frac{gm_1}{2} \times 0.446 = I_{D5}$$

$I_{D5} = 78.09\ \mu$

$$\boxed{I_{D5} \simeq 80\ \mu A}$$

For 2^{nd} stage

$$\frac{gm_2}{2} \times 0.4312 = I_{D7}$$

$I_{D7} = 368.63\ \mu A$

$I_{D7} \simeq 370\ \mu A.$

$I_{D5} + I_{D7} = 450\ \mu A.$

Rest $50\ \mu A$ is given to buffer stage.

Thus current through

$\boxed{\begin{array}{lcl} \text{Stage 1} & = & 80\ \mu A \\ \text{Stage 2} & = & 370\ \mu A. \\ \text{Buffer} & = & 50\ \mu A. \end{array}}$

* In order to set gain = 3 of buffer stage, as assumed previously value of I_D buffer can be changed.

But total I_D is always kept < 555. to get Power < 1 mW.

From the schematics :-
MC_1, MC_2 & MC_3 are transistor of Current ref stage.
MA1, MA2 & MA_3 are of Buffer stage.
& M_1 to M_7 are gain stages amplifier.

* Designing MOSFETS of current mirror.

For calculation of all the transistor & make it easy L is kept to 5u for all the transistors.
Value of L selected from gm/gds vs gm/Id.

For Nmos

$$gm = \frac{2I_D}{V_{GS}-V_{th}}$$

$$\frac{gm}{I_D} = \frac{2}{V_{GS}-V_{th}}$$

For Pmos

$$gm = \frac{2I_D}{V_{GS}-V_{th}}$$

$$\frac{gm}{I_D} = \frac{2}{V_{GS}-V_{th}}$$

Thus for constant L gm/ID will remain constant.

$gm/I_D \approx 4.5$ $\quad$ $gm/I_D \approx 4.75$.

From gm/Id V/s Id/W from figures in Appendix.

$Id/W = 4.33$ $\quad$ $Id/W = 0.875$.

$$\therefore W = \frac{Id}{4.33} \qquad W = \frac{Id}{0.875}.$$

For 500 μA I_d.

Pmos

$$w = \frac{500}{4.33} \qquad\qquad w = \frac{500}{0.875}$$

$$w = 115.47 \qquad\qquad w = 571.42\ \mu$$

$$w \approx 116\ \mu m \qquad\qquad w \approx 572\ \mu m.$$

$$\therefore \boxed{MG_1 = MG_2 = \frac{116\ \mu m}{5\ \mu m.}} \qquad \boxed{MG_3 = \frac{572\ \mu m}{5\ \mu m}}$$

For M5 $I_5 = 80\ \mu A$.

$$\therefore\ w = \frac{80}{4.33}$$

$$w = 18.48\ \mu$$

$$w = 19\ \mu m.$$

$$\boxed{(W/L)_{M5} = (19/5)}$$

For M7 $I_7 = 370\ \mu A$.

$$w = \frac{370}{\cancel{4.33}\ 0.875}$$

$$w = \cancel{85.45\ \mu}\ 422.86$$

$$w \approx \cancel{86\ \mu}.\ 423\ \mu$$

$$\boxed{(W/L)_{M7} = (423/5)\ \mu.}$$

Previously we assumed that $g_{mc} r_0/3 = 3$

i.e $g_m r_0 = 9$ (gain of Buffer stage).

From gm/gds curve at $L = 5\mu$ & $W = 5\mu$

$r_0 \approx 300K$

$$g_m = \frac{9}{300 \times 10^3}$$

$$g_m = 30\mu.$$

This gives $I_D = 30 \times 0.446/2$

$= 6.7\mu A.$

$I_D \approx 7\mu A$

$$W = \frac{I_D}{0.875}$$

$$W = 8\mu m.$$

$$W = \frac{I_D}{4.33}$$

$$= 1.62\mu$$

For MA_1 & MA_2 $\left(\frac{W}{L}\right)_2 = \boxed{\left(\frac{8}{5}\right)}$

$\boxed{\text{For } MA_3 \left(W/L\right) = \left(\frac{1.62}{5}\right)}$

* I_D flowing through M_5 is divided into two equal parts each flowing through M_1 and M_2.

$(I_d)_{M_1, M_2} = 40\mu A.$

$\therefore \; W_{m_1,m_2} = \frac{1}{2} \times W_{m_5} = \frac{19}{2} = 9.5\mu$

$$\boxed{(W/L)_{m_1,m_2} = (9.5/5).}$$

* For M_3 & M_4.

$I_d = 40\mu$

$W = \frac{40\mu}{0.875}$

$W \simeq 45.71$

$W = 45\mu$

$$\boxed{(W/L)_{m_3,m_4} = \left(\frac{45}{5}\right)}$$

For M_6.

$I_d = 370\,\mu A$

$W = \frac{\cancel{370}}{\cancel{0.875}} \approx \cancel{422.85}$

$W = \frac{370}{4.33} = 85.45$

$W \simeq 86\,\mu m$

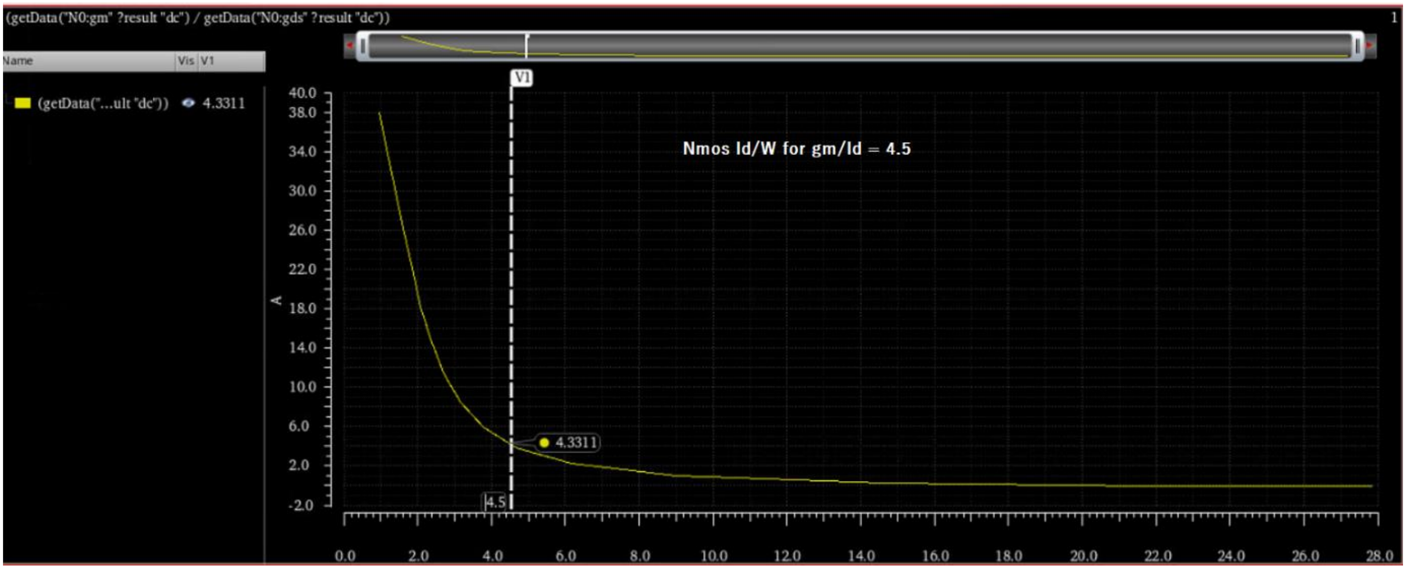
$(W/L)_{M_6} = (86/5)\mu$

* Transistor Size Summary

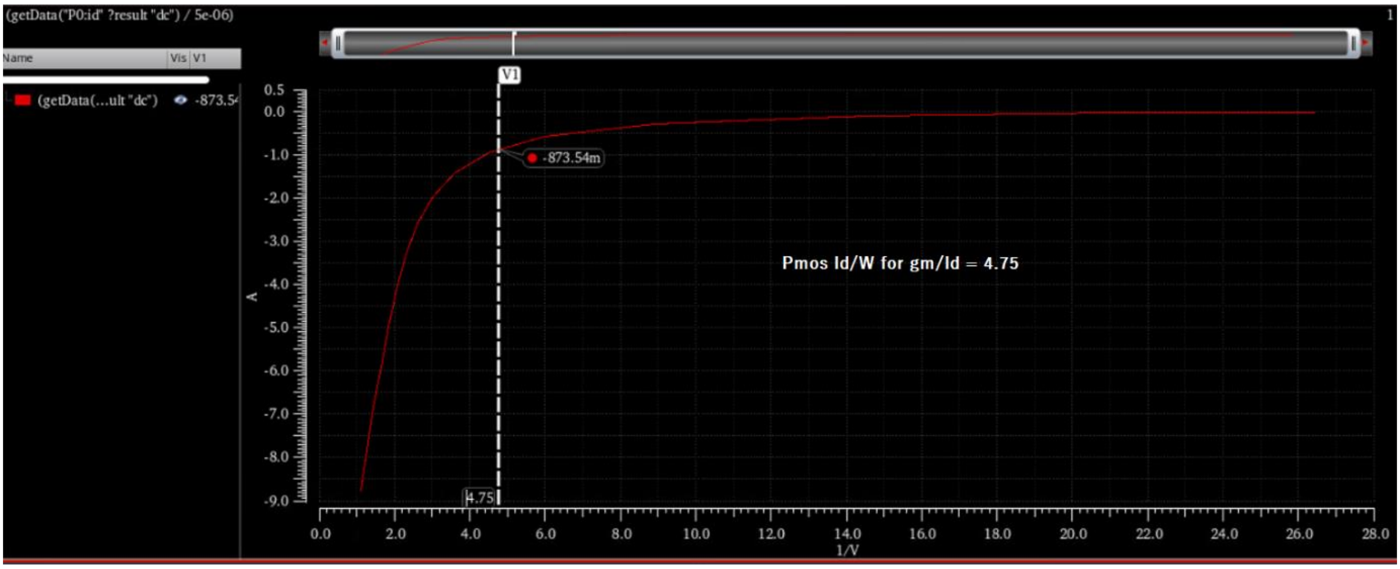
Transistor	(W/L) (values in μ)
M_1, M_2	(9.5/5)
M_3, M_4	(45/5)
M_5	(19/5)
M_6	(86/5)
M_7	(423/5)
MC_1, MC_2	(116/5)
MC_3	(572/5)
MA_1; MA_2	(8/5)
MA_3	(1.62/5)

Note value of L is selected 5u because from gm/gds V/s gm/Id. It gives high value of ro. Thus gain requirement is satisfied.

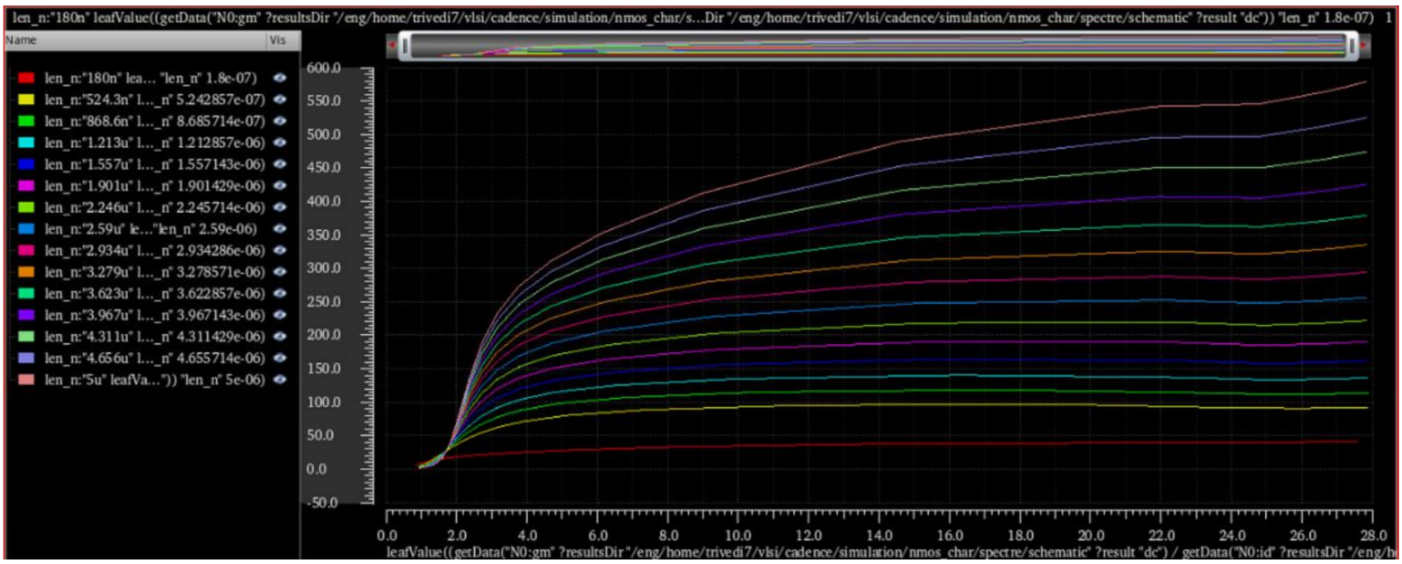
Appendix:-



(getData("N0:gm" ?result "dc") / getData("N0:gds" ?result "dc"))
(getData("...ult "dc")) 4.3311
Nmos Id/W for gm/Id = 4.5
4.3311
4.5



(getData("P0:id" ?result "dc") / 5e-06)
(getData(...ult "dc") -873.54
-873.54m
Pmos Id/W for gm/Id = 4.75
4.75
1/V



len_n:"180n" leafValue((getData("N0:gm" ?resultsDir "/eng/home/trivedi7/vlsi/cadence/simulation/nmos_char/s...Dir "/eng/home/trivedi7/vlsi/cadence/simulation/nmos_char/spectre/schematic" ?result "dc")) "len_n" 1.8e-07)
len_n:"180n" lea... "len_n" 1.8e-07)
len_n:"524.3n" l... _n" 5.242857e-07)
len_n:"868.6n" l... _n" 8.685714e-07)
len_n:"1.213u" l... _n" 1.212857e-06)
len_n:"1.557u" l... _n" 1.557143e-06)
len_n:"1.901u" l... _n" 1.901429e-06)
len_n:"2.246u" l... _n" 2.245714e-06)
len_n:"2.59u" le..."len_n" 2.59e-06)
len_n:"2.934u" l... _n" 2.934286e-06)
len_n:"3.279u" l... _n" 3.278571e-06)
len_n:"3.623u" l... _n" 3.622857e-06)
len_n:"3.967u" l... _n" 3.967143e-06)
len_n:"4.311u" l... _n" 4.311429e-06)
len_n:"4.656u" l... _n" 4.655714e-06)
len_n:"5u" leafVa...")) "len_n" 5e-06)
leafValue((getData("N0:gm" ?resultsDir "/eng/home/trivedi7/vlsi/cadence/simulation/nmos_char/spectre/schematic" ?result "dc") / getData("N0:id" ?resultsDir "/eng/h