→ In Innovus

min & max
worst & best

→ File → import design

→ Netlist → browse and arrow key → select the netlist file → Add → close.

→ In Tech / Phy libraries →

Select LEF files → browse → arrow key → select 90nm → select 2 LEF files inside it

→ ~~LEF~~file → macrofile. select → add → close.

→ In Powed nets, VDD

~~VDD~~ Ground nets, Vss

→ Create Ananlysis Config → Click → window opens → choose library sets → right click → new → name → wc_lib.

→ Add lib files → /home/install/Foundry/digital/90nm/dig/lib/slow lib

(timing lib → add)

→ Add → Close → OK.

→ Repeat this to choose fast lib / BC_lib.

→ RC corner → new → name → rccorner

→ captable → browse → Select.

→ tempr → 25

→ other values r default. donot change.

→ QRC tech file → browse → /home/install/foundry/digital/90nm/dig/qrc/qpdk090_9i.

→ OK

→ Delay corners → new → name → ~~delaycorner~~ wc_delay

→ Attributes → RCcorner → rccorner → lib → wc_lib

→ " " → lib → bc_lib.

→ Constraint modes → RClick → new → name → constraint → SDC constraint file → Add → add the synthesised file after synthesis not user written file → Count.sdc.sdc

→ Analysis View → new → name → WC-analysis
→ C.mode → constraint → D.corner → WC-delay

→ similarly do for BC-analysis.

→ Add both analysis.

→ setup Analysis → New → A.View → WC-analysis → OK.

→ Hold " → New → A.View → BC-analysis → OK.

→ Save & close.

→ File name → Default.view. → save.

→ Save → Default.globals → save → OK.

→ In Innovus Imp window,

→ floorplan → specify f.plan. →

innovus → source Default.globals → init_design > → in terminal. <if stucks>

→ Rdtio (H/W) → 1
Core utilisation → 0.45
Core to left, top, right, bottom → 5.

→ OK.

→ Power → Power planning → Add ring → browse.
→ Net selection → select VDD VSS → Add → OK.

→ Ring confin → (because of low resistance)
higher metal layers M9(9) <T&B> & M8(8) <L&R>
spacing → All → 0.5
width → All → 1
offset → All → 1.8.
select the offset → ok.

→ Power → P.plan → Add Stripes → browse Nets →
select VDD Vss → Add → OK.

→ Vertical → metal 8(8) → width → 1 (lesser values to satisfy Area constraint), spacing → 0.5

→ set pattern →
set-to-set → dist → 100
no of sets → 2

→ Apply

→ Repeat for horizontal · M9(9) spacing → 0.5 width → 1. → Apply → OK

→ Route → special Route → browse Net → choose Vdd Vss

→ ~~Add~~ → OK .

→ Vdd Vss routed to the whole area.

→ to place std cells → wch was present in netlist file.

→ Place → P.Std cell → Place window → mode

→ select (tick) Place I/O cells → OK. → OK in mode

→ Rightcorner → physical view → to view the cells.

→ Timing → Report timing → Pre CTS → Setup - OK

→ check Violation path in terminal if it is zero it fine.

→ Again Timing → Report timing → post CTS → hold.

→ Here Violating path is not zero.

→ we have to make that to zero.

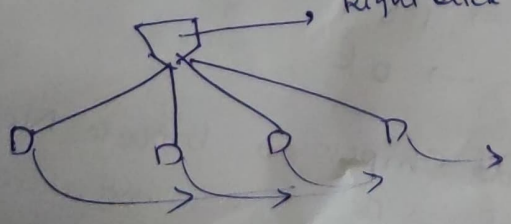
→ It shd be optimised.

→ ECO → optimie design → post CTS → uncheck setup & seled the hold → OK.

→ Repeat the Analysis for Post CTS → to check the violation is zero or not.

→ Clock → debugger → CTD Config → window Id name - ctd_window

OK → yes →




→ File → save design → Innovus → Filename → upcount.enc → OK.

→ To Restore the design → File → Restore design.

→ File → save → GDS → browse → up_count.enc

→

Files of type → All files →

→ OK.