Kyle Daruwalla

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Education

2016 – Present **Ph.D. in Electrical Engineering**,
University of Wisconsin, Madison WI, *GPA – 3.78*.
Fourth Year

2012 – 2016 **B.S. in Computer Engineering and Continuous Applied Mathematics**,
Rose-Hulman Institute of Technology, Terre Haute IN, *GPA – 3.65*.
Magna Cum Laude

Academic Experience

Research

Sept. 2016 – Present **Research Assistant**, *University of Wisconsin – Madison*, Madison, WI.
Working on:

- stochastic computing algorithms and paradigms
- biological learning mechanisms (eg. Hebbian learning, STDP)
- reinforcement learning for complex navigational tasks
- non-traditional architectures to facilitate low-power, online learning

Studying:

- optimization
- machine learning
- biological learning/computational neuroscience
- computer architecture
- digital design

2014 – 2016 **Research Assistant**, *Rose-Hulman Institute of Technology*, Terre Haute, IN.
Developed configurable architecture for simulating Hodgkin-Huxley neural systems.

Detailed work:

- Identified computational bottle necks in solving differential equations that described the neural model
- Used numerical analysis techniques to optimize computation of bottle necks
- Designed specialized hardware units to further optimize computation of bottle necks
- Synthesized, implemented, and programmed hardware units to FPGAs for efficiency analysis
- Co-authored papers on numerical techniques and specialized hardware designs

Teaching

Sept. 2018 – Aug. 2019 **ECE532: Matrix Methods for ML Teaching Assistant**, *University of Wisconsin – Madison*, Madison, WI.
Instructing flipped class room course on linear algebra and machine learning.

Sept. 2017 – Dec. 2018 **ECE315: Intro. to Microprocessor Laboratory Teaching Assistant**, *University of Wisconsin – Madison*, Madison, WI.
Instructing lab course on designing, assembling, and programming a printed circuit board.

Detailed work:
- Performs duties of sole instructor during class hours
- Helps develop material and teaching strategy for a new course
- Manages lab equipment and coordinates student purchases from suppliers
- Grades all course work and exams
- Supervises students in a lab environment, providing instructions on propering soldering technique, etc

Jan. 2017 – May 2018 **ECE353: Intro. to Microprocessor Systems Teaching Assistant**, *University of Wisconsin – Madison*, Madison, WI.
Taught as an in-class TA for a flipped-classroom course on embedded systems.

Detailed work:
- Helped debug and correct errors in course material
- Assisted instructor with developing exam questions

March 2016 – May 2016 **ECE530: Advanced Microcomputers Teaching Assistant**, *Rose-Hulman Institute of Technology*, Terre Haute, IN.
Assisted as lab TA for a graduate class on designing microcomputer systems on Dual ARM/FPGA boards.

Detailed work:
- Taught students how to use and implement digital systems on Digilent ZYBO board
- Created guides on Xilinx Vivado Tools and Digilent ZYBO boards for professor
- Developed some labs for professor

March 2014 – May 2014 **CSSE332: Operating Systems Teaching Assistant**, *Rose-Hulman Institute of Technology*, Terre Haute, IN.
Assisted as lab TA for a class on designing operating systems.

Publications

Nov. 2019 **BitSAD v2: Compiler Optimization and Analysis for Bitstream Computing**, *ACM Transactions on Architecture and Code Optimization (TACO).*
Authors: *K. Daruwalla*, H. Zhuo, R. Shukla, M. Lipasti

Jun. 2019 **BitBench: A Benchmark for Bitstream Computing**, *Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES '19).*
Authors: *K. Daruwalla*, H. Zhuo, C. Schulz, M. Lipasti

Jun. 2019 **BitSAD: A Domain-Specific Language for Bitstream Computing**, *First ISCA Workshop on Unary Computing (WUC '19)*.
Authors: *K. Daruwalla*, H.Zhuo, M. Lipasti

Jan. 2019 **A quantitative analysis of the performance of computing architectures used in neural simulations**, *Journal of Neuroscience Methods*.
Authors: *K. Daruwalla*, N. Olivero, A. Pluger, S. Rao, D. W. Chang, M. Simoni

Presentations

Oral

Jan. 2020 **BitSAD v2: A Domain-Specific Language for Bitstream Computing**,
High-performance Embedded Architecture and Compilation Conference (HiPEAC '20), Bologna, Italy.

Oct. 2019 **BitSAD v2**,
Industry Affiliates Meeting, Madison, WI.

Jun. 2019 **BitSAD: A Domain-Specific Language for Bitstream Computing**,
First ISCA Workshop on Unary Computing, Phoenix, AZ.

Jun. 2019 **BitBench: A Benchmark for Bitstream Computing**,
Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES '19), Phoenix, AZ.

Oct. 2018 **BitSAD: A Domain-specific language for Bitstream Computing**,
Industry Affiliates Meeting, Madison, WI.

Oct. 2017 **Seeing Through the FoG: A Biologically Inspired Navigation System**,
Industry Affiliates Meeting, Madison, WI.

Poster

Oct. 2019 **BitSAD v2**,
Industry Affiliates Meeting, Madison, WI.

Jun. 2019 **BitBench: A Benchmark for Bitstream Computing**,
Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES '19), Phoenix, AZ.

Oct. 2018 **BitSAD: A Domain-specific language for Bitstream Computing**,
Industry Affiliates Meeting, Madison, WI.

Oct. 2017 **Seeing Through the FoG: A Biologically Inspired Navigation System**,
Industry Affiliates Meeting, Madison, WI.

Nov. 2016 **Drone Control with Map-Seeking Circuits**,
Industry Affiliates Meeting, Madison, WI.

Industry

May 2017 – Aug 2017 **Digital Design Intern**, *Texas Instruments*, Dallas, TX.
Performed IP design for multimedia IPs.

Detailed work:
- Fully responsible for designing two video encoding IPs – H.264/265 video encoder and decoder
- Worked with SoC designers to make IP functionality and black box model compatible with overall architecture
- Worked with third party IP vendors to relay issues and RTL fixes
- Automated tools and flows used by design team, and created documentation for the toolsets

June 2016 – Aug 2016 **Digital Design Intern**, *Texas Instruments*, Dallas, TX.
Performed design verification for high speed I/O IPs.

Detailed work:
- Interfaced with designers to debug RTL issues and modify IP specs
- Worked with third party vendors to debug integration issues
- Helped develop and improve internal IP library
- Created flow to replay third party vendor test sequences in internal environment, greatly reducing design verification timeline

Sept 2015 – May 2016 **Project Intern**, *Rose-Hulman Ventures*, Terre Haute, IN.
Worked with project team to design various products for several clients.

Detailed work:
- Interfaced with clients on a regular basis through face-to-face and telecom meetings
- Helped clients understand requirements within technical limitations
- Assisted clients to develop an efficient path to meet product deadlines
- Optimized image processing code for corn stalk detection
- Researched radar systems for FPGAs
- Converted traditional radar algorithms for DSPs to FPGAs

June 2015 – Aug 2015 **Digital Design Intern**, *Texas Instruments*, Dallas, TX.
Performed design verification for high speed I/O IPs.

Detailed work:
- Designed workflows and simulation environments for design verification engineers
- Performed design verification for different IP modules
- Organized and led team meetings
- Produced documentation for IP design verfication workflows
- Worked with management, designers, and design verification engineers

Sept 2013 – May 2015 **Project Intern**, *Rose-Hulman Ventures*, Terre Haute, IN.
Worked with project team to design various products for several clients.

Detailed work:
- Worked on designing a trash compaction control system powered using solar energy
- Revamped code and circuitry for old control systems with little knowledge of previous systems
- Worked and conferenced with third party clients in order to deliver a complete product
- Was lead engineer on project groups; worked in project teams of several different engineering majors

Sept 2012 – Sept 2013 **EE Shop Assistant**, *Rose-Hulman Ventures*, Terre Haute, IN.
Performed various duties as EE shop assistant at engineering solutions firm.

Detailed work:
- Redesigned inventory system
  - Introduced a robust database capable of handling load
  - Designed a web front-end with dynamic HTML capable of handling mobile, table, and desktop form factors
  - Single-handedly proposed the project to employers, implemented the project, and maintained the project after deployment
- Often assisted more than one project group at a time – able to produce results without being told the full system
- Taught other engineers basic circuitry and operation of lab equipment

Awards

May 2018 Gerald Holdridge Teaching Excellence Award

Undergrad Made the Dean's List every quarter

Feb. 2016 Honor Student Award

Hardware Skills

Basic Semiconductor fabrication

Intermediate Analog IC layout, VLSI

Advanced FPGA development, digital design verification, design for test (DFT)

Software Skills

Basic Windows development, HTML

Intermediate Python, Java, VHDL, Scala

Advanced Verilog, SystemVerilog, C/C++, MATLAB, Linux, Bash, CSH, LaTeX, Julia

Leadership Skills

2019 – Present Vice-President of ECE Graduate Student Association – Assists with presidential duties, plans events

2017 – 2019 President of ECE Graduate Student Association – Coordinated meetings, events, and acted as face of graduate student body in the department

2012 – 2016 President of Linux Users Group – Gave presentations, organized meetings, interfaced with administration

2014 – 2016 Operations Manager of Rose Tech Radio Club – Took inventory of equipment, organized presentations on ham radio, interfaced with local community organizations

2015 – 2016 Founder of Rose Maker Lab – Coordinated with administrative and safety personnel to create a novel club benefitting all students in the Rose-Hulman community