Kyle Daruwalla

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Education

2016 – Present **Ph.D. in Electrical Engineering**,
University of Wisconsin, Madison WI, *GPA – 3.79*.
Sixth Year

2016 – 2019 **M.S. in Electrical Engineering**,
University of Wisconsin, Madison WI, *GPA – 3.79*.

2012 – 2016 **B.S. in Computer Engineering and Continuous Applied Mathematics**,
Rose-Hulman Institute of Technology, Terre Haute IN, *GPA – 3.65*.
Magna Cum Laude

Publications

Nov. 2021 **Accelerating Deep Learning with Dynamic Data Pruning**, *Preprint under review*.
Authors: R. S. Raju, *K. Daruwalla*, M. Lipasti

Sep. 2021 **Information Bottleneck-Based Hebbian Learning Rule Naturally Ties Working Memory and Synaptic Updates**, *Preprint under review*.
Authors: *K. Daruwalla*, M. Lipasti

Nov. 2019 **BitSAD v2: Compiler Optimization and Analysis for Bitstream Computing**, *ACM Transactions on Architecture and Code Optimization (TACO)*.
Authors: *K. Daruwalla*, H. Zhuo, R. Shukla, M. Lipasti

Jun. 2019 **BitBench: A Benchmark for Bitstream Computing**, *Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES '19)*.
Authors: *K. Daruwalla*, H. Zhuo, C. Schulz, M. Lipasti

Jun. 2019 **Resource Efficient Navigation Using Bitstream Computing**, *First ISCA Workshop on Unary Computing (WUC '19)*.
Authors: *K. Daruwalla*, M. Lipasti

Jun. 2019 **BitSAD: A Domain-Specific Language for Bitstream Computing**, *First ISCA Workshop on Unary Computing (WUC '19)*.
Authors: *K. Daruwalla*, H.Zhuo, M. Lipasti

Jan. 2019 **A quantitative analysis of the performance of computing architectures used in neural simulations**, *Journal of Neuroscience Methods*.
Authors: *K. Daruwalla*, N. Olivero, A. Pluger, S. Rao, D. W. Chang, M. Simoni

Academic Experience

Research

Sept. 2016 – Present **Research Assistant**, *University of Wisconsin – Madison*, Madison, WI.

Working on:

- stochastic computing algorithms and paradigms
- biological learning mechanisms (eg. Hebbian learning, STDP)
- reinforcement learning for complex navigational tasks
- non-traditional architectures to facilitate low-power, online learning

Studying:

- machine learning
- biological learning/computational neuroscience
- computer architecture

2014 – 2016 **Research Assistant**, *Rose-Hulman Institute of Technology*, Terre Haute, IN.

Developed configurable architecture for simulating Hodgkin-Huxley neural systems.

Detailed work:

- Identified computational bottle necks in solving differential equations that described the neural model
- Used numerical analysis techniques to optimize computation of bottle necks
- Designed specialized hardware units to further optimize computation of bottle necks
- Synthesized, implemented, and programmed hardware units to FPGAs for efficiency analysis
- Co-authored papers on numerical techniques and specialized hardware designs

Teaching

Sept. 2021 – Present **ECE252: Intro. to Comp. Eng. *Lecturer***, *University of Wisconsin – Madison*, Madison, WI.

Independently responsible for instructing a course section on introductory material for computer engineering.

Detailed work:

- Teaching in flipped class room setting without TA help
- Gives lectures to reinforce material learned in flipped setting

Sept. 2018 – Aug. 2019 **ECE532: Matrix Methods for ML Teaching Assistant**, *University of Wisconsin – Madison*, Madison, WI.

Instructed flipped class room course on linear algebra and machine learning.

Sept. 2017 – Dec. 2018 **ECE315: Intro. to Microprocessor Laboratory Teaching Assistant**, *University of Wisconsin – Madison*, Madison, WI.

Instructed lab course on designing, assembling, and programming a printed circuit board.

Detailed work:

- Performed duties of sole instructor during class hours
- Helped develop material and teaching strategy for a new course
- Managed lab equipment and coordinates student purchases from suppliers

Jan. 2017 – May 2018 **ECE353: Intro. to Microprocessor Systems Teaching Assistant**, *University of Wisconsin – Madison*, Madison, WI.

Taught as an in-class TA for a flipped-classroom course on embedded systems.

March 2016 – May 2016 **ECE530: Advanced Microcomputers Teaching Assistant**,
Rose-Hulman Institute of Technology, Terre Haute, IN.
Assisted as lab TA for a graduate class on designing microcomputer systems on Dual ARM/FPGA boards.

March 2014 – May 2014 **CSSE332: Operating Systems Teaching Assistant**,
Rose-Hulman Institute of Technology, Terre Haute, IN.
Assisted as lab TA for a class on designing operating systems.

Presentations

Oral

Jan. 2020 **BitSAD v2: A Domain-Specific Language for Bitstream Computing**,
High-performance Embedded Architecture and Compilation Conference (HiPEAC '20), Bologna, Italy.

Oct. 2019 **BitSAD v2**,
Industry Affiliates Meeting, Madison, WI.

Jun. 2019 **Resource Efficient Navigation Using Bitstream Computing**,
First ISCA Workshop on Unary Computing, Phoenix, AZ.

Jun. 2019 **BitBench: A Benchmark for Bitstream Computing**,
Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES '19), Phoenix, AZ.

Oct. 2018 **BitSAD: A Domain-specific language for Bitstream Computing**,
Industry Affiliates Meeting, Madison, WI.

Oct. 2017 **Seeing Through the FoG: A Biologically Inspired Navigation System**,
Industry Affiliates Meeting, Madison, WI.

Poster

Nov. 2021 **A Biologically Plasible Learning Rule Based on the Information Bottleneck**,
Spiking Neural networks as Universal Function Approximators (SNUFA '21), Virtual.

Oct. 2019 **BitSAD v2**,
Industry Affiliates Meeting, Madison, WI.

Jun. 2019 **BitBench: A Benchmark for Bitstream Computing**,
Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES '19), Phoenix, AZ.

Oct. 2018 **BitSAD: A Domain-specific language for Bitstream Computing**,
Industry Affiliates Meeting, Madison, WI.

Oct. 2017 **Seeing Through the FoG: A Biologically Inspired Navigation System**,
Industry Affiliates Meeting, Madison, WI.

Nov. 2016 **Drone Control with Map-Seeking Circuits**,
Industry Affiliates Meeting, Madison, WI.

Industry

Jun 2020 – Dec 2020 **Research Co-op Intern**, *AMD*, Austin, TX.
Explored neural network sensitvity to input perturbations.

Detailed work:
- Characterized neural network sensitvity to input perturbations based on matrix decompositions of the parameters
- Worked on an indenpendently driven research project
- Presented progress to AMD Research team

May 2017 – Aug 2017 **Digital Design Intern**, *Texas Instruments*, Dallas, TX.
Performed IP design for multimedia IPs.

Detailed work:
- Fully responsible for designing two video encoding IPs – H.264/265 video encoder and decoder
- Worked with SoC designers to make IP functionality and black box model compatible with overall architecture
- Worked with third party IP vendors to relay issues and RTL fixes
- Automated tools and flows used by design team, and created documentation for the toolsets

June 2016 – Aug 2016 **Digital Design Intern**, *Texas Instruments*, Dallas, TX.
Performed design verification for high speed I/O IPs.

Detailed work:
- Interfaced with designers to debug RTL issues and modify IP specs
- Worked with third party vendors to debug integration issues
- Helped develop and improve internal IP library
- Created flow to replay third party vendor test sequences in internal environment, greatly reducing design verification timeline

Sept 2015 – May 2016 **Project Intern**, *Rose-Hulman Ventures*, Terre Haute, IN.
Worked with project team to design various products for several clients.

Detailed work:
- Interfaced with clients on a regular basis through face-to-face and telecom meetings
- Helped clients understand requirements within technical limitations
- Assisted clients to develop an efficient path to meet product deadlines
- Optimized image processing code for corn stalk detection
- Researched radar systems for FPGAs
- Converted traditional radar algorithms for DSPs to FPGAs

June 2015 – Aug 2015 **Digital Design Intern**, *Texas Instruments*, Dallas, TX.
Performed design verification for high speed I/O IPs.

Detailed work:
- Designed workflows and simulation environments for design verification engineers
- Performed design verification for different IP modules
- Organized and led team meetings
- Produced documentation for IP design verfication workflows
- Worked with management, designers, and design verification engineers

Sept 2013 – May 2015 **Project Intern**, *Rose-Hulman Ventures*, Terre Haute, IN.
Worked with project team to design various products for several clients. Contact for details.

Sept 2012 – Sept 2013 **EE Shop Assistant**, *Rose-Hulman Ventures*, Terre Haute, IN.
Performed various duties as EE shop assistant at engineering solutions firm. Contact for details

Awards

Sept. 2021 Second place – AFRL xView2 Overhead Imagery ML Hackathon

May 2018 Gerald Holdridge Teaching Excellence Award

Feb. 2016 Honor Student Award

Undergrad Made the Dean's List every quarter

Service and Leadership

2021 – Present Graduate student representative on departmental committee – Advises faculty members on graduate concerns relevant to the department

2021 – 2021 Google Summer of Code Mentor – Co-mentored an undergraduate student project building machine learning frameworks

2019 – 2020 Vice-President of ECE Graduate Student Association – Assisted with presidential duties, plans events

2017 – 2019 President of ECE Graduate Student Association – Coordinated meetings, events, and acted as face of graduate student body in the department

2012 – 2016 President of Linux Users Group – Gave presentations, organized meetings, interfaced with administration

2014 – 2016 Operations Manager of Rose Tech Radio Club – Took inventory of equipment, organized presentations on ham radio, interfaced with local community organizations

2015 – 2016 Founder of Rose Maker Lab – Coordinated with administrative and safety personnel to create a novel club benefitting all students in the Rose-Hulman community

Hardware Skills

Basic Semiconductor fabrication

Intermediate Analog IC layout, VLSI

Advanced FPGA development, digital design verification, design for test (DFT)

Software Skills

Basic Windows development, HTML

Intermediate Python, Java, VHDL, Scala, Csh

Advanced Verilog, SystemVerilog, C/C++, Matlab, Linux, Bash, LaTeX, Julia