Gal Elbaz

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An Electrical Engineering graduate from the Technion with IDF Unit 81 experience, proficient in RTL design, algorithms, and various programming languages. Skilled in verification methodologies, familiar with UVM concepts and adept with EDA tools. Passionate about engineering and dedicated to delivering high-quality solutions.

Education

Technion - Israel Institute of Technology (2017 – 2022)

Bachelor of Science in Electrical Engineering (GPA 82.3)

Military Service

Unit 81 (2022 –2024)

- Trained in analog and digital electronics, gaining knowledge in fundamental principles and circuitry design.
- Attained proficiency in basic RTL (Register Transfer Level) coding using SystemVerilog, laying the groundwork for digital circuit design and verification.
- Led a digital electronics course for future candidates of the unit.
- Integrated complex hardware systems and managed lab testing with equipment such as oscilloscopes, ammeters, and other specialized instruments.
- Developed Python scripts to automate data reading, remote equipment operation, and data analysis.

Technical Proficiencies and Project Experience

Verification Experience

Key Expertise

- Proficient in SystemVerilog, with experience in designing and simulating digital circuits.
- Debugged RTL designs using debugging tools across platforms such as Synopsys VCS Vivado Xilinx, ModelSim and EDAplayground.
- Familiar with UVM principles to develop robust testbenches and verification environments.
- Engaged in continuous learning and professional development to enhance chip design skills.

FPGA Logic Design Experience

Key Expertise

- Strong ability to implement basic digital circuits on FPGA platforms.
- Proficiency in using basic FPGA development tools such as Vivado for design entry, synthesis, and implementation.

Relevant projects

- **Verification environment for SPI/APB protocol** - Demonstrates proficiency in verification principles and functional of communication protocols. GitHub Repo / GitHub Repo.
- **Verification environment for FIFO data-structure** - Highlights ability to design and implement test scenarios for complex data structures. GitHub Repo.
- **Verification environment for Half-Adder** - Showcases the ability to apply verification principles to ensure the correctness of a fundamental building block in digital design. GitHub Repo.
- **UART Receiver** - Captures data from a computer through a terminal emulator, displaying it on FPGA 7-segment Displays. GitHub Repo.
- **Digital Clock -** Displays time in HH:MM format on FPGA 7-segment displays. GitHub Repo.

Certifications

- **SystemVerilog for Verification** - Udemy certification.
- **Digital System Design with FPGA using System Verilog** - Udemy certification.
- **Physical Design** - VLSI academy.
- **Dean's list** - Technion – Israel Institute of Technology.
- **Practical engineering course** - Israeli Military Intelligence, Unit 81.
- **Error handling course** - Israeli Military Intelligence, Unit 81.

Additional Skills

- Understanding of digital logic principles, including both combinational and sequential logic.
- Familiar with Static Timing Analysis (STA) techniques for ensuring timing closure in hardware designs.
- Capable in C and Python programming across a range of applications and domains.
- Familiar with linux environment.