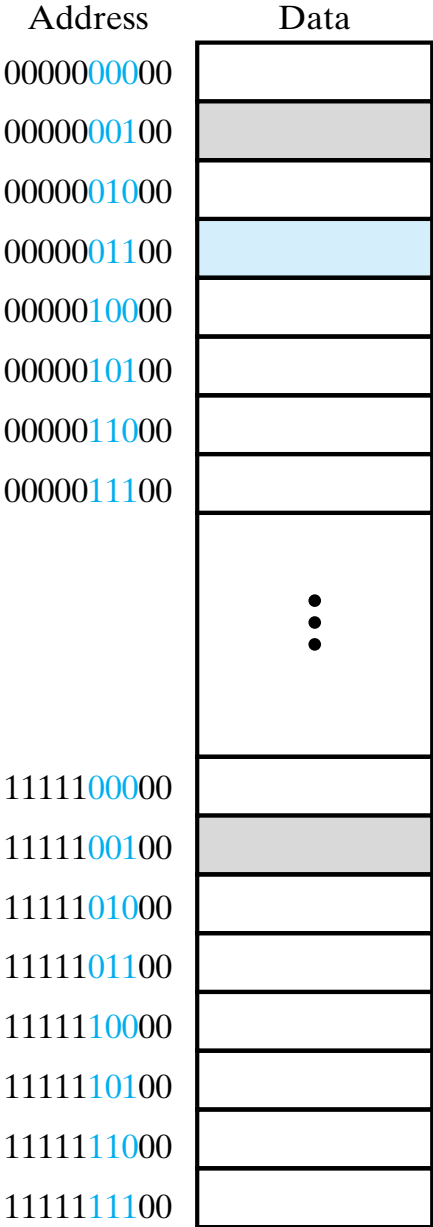
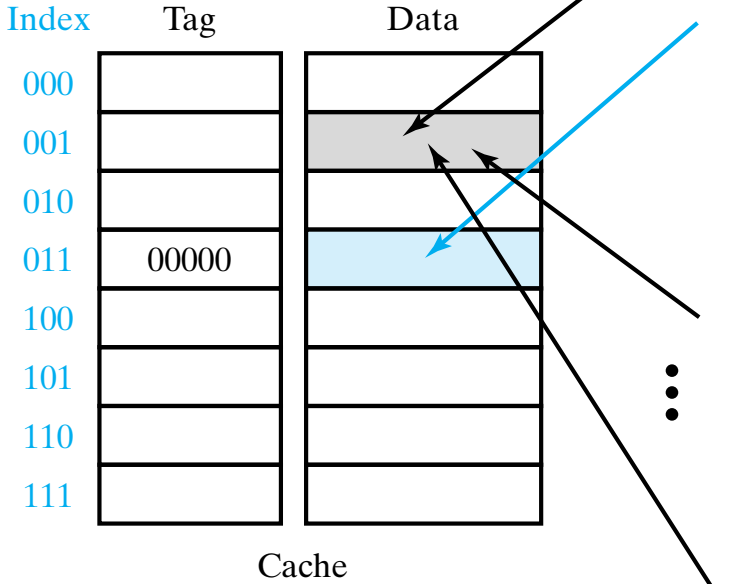
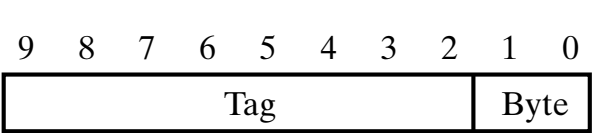


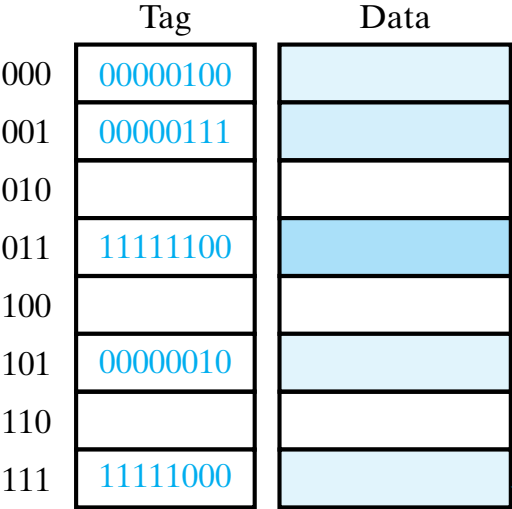
(a) Memory address



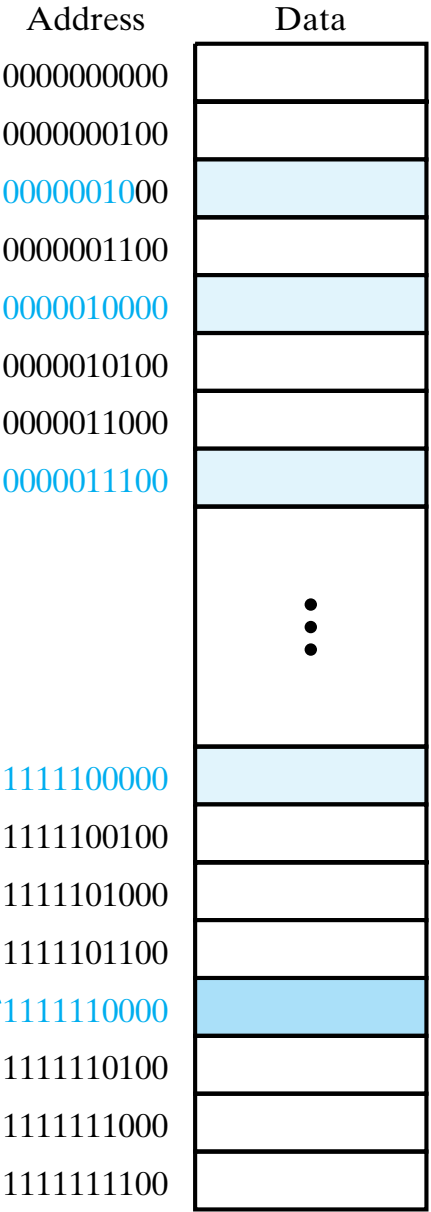
Main memory
(b) Cache mapping



(a) Memory address

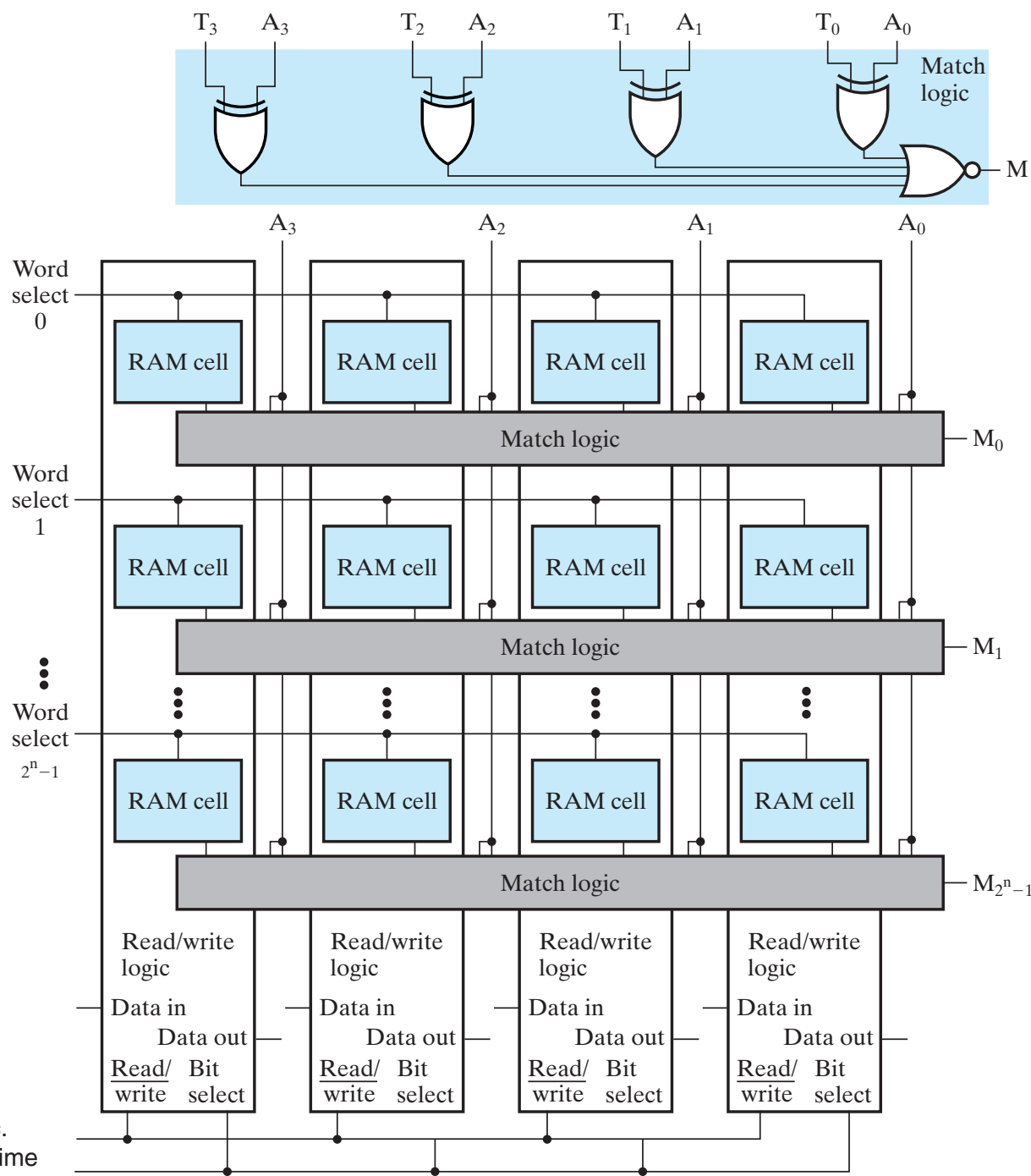


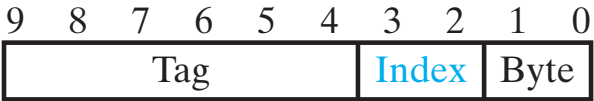
Cache



Main memory

(b) Cache mapping





(a) Memory address

Index

00

01

10

11

Tag

111111

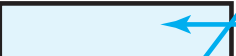
Data



Tag

000001

Data



Cache

Cache

Address

Data

0000000000

0000000100

0000001000

0000001100

0000010000

0000010100

0000011000

0000011100

⋮

1111100000

1111100100

1111101000

1111101100

1111110000

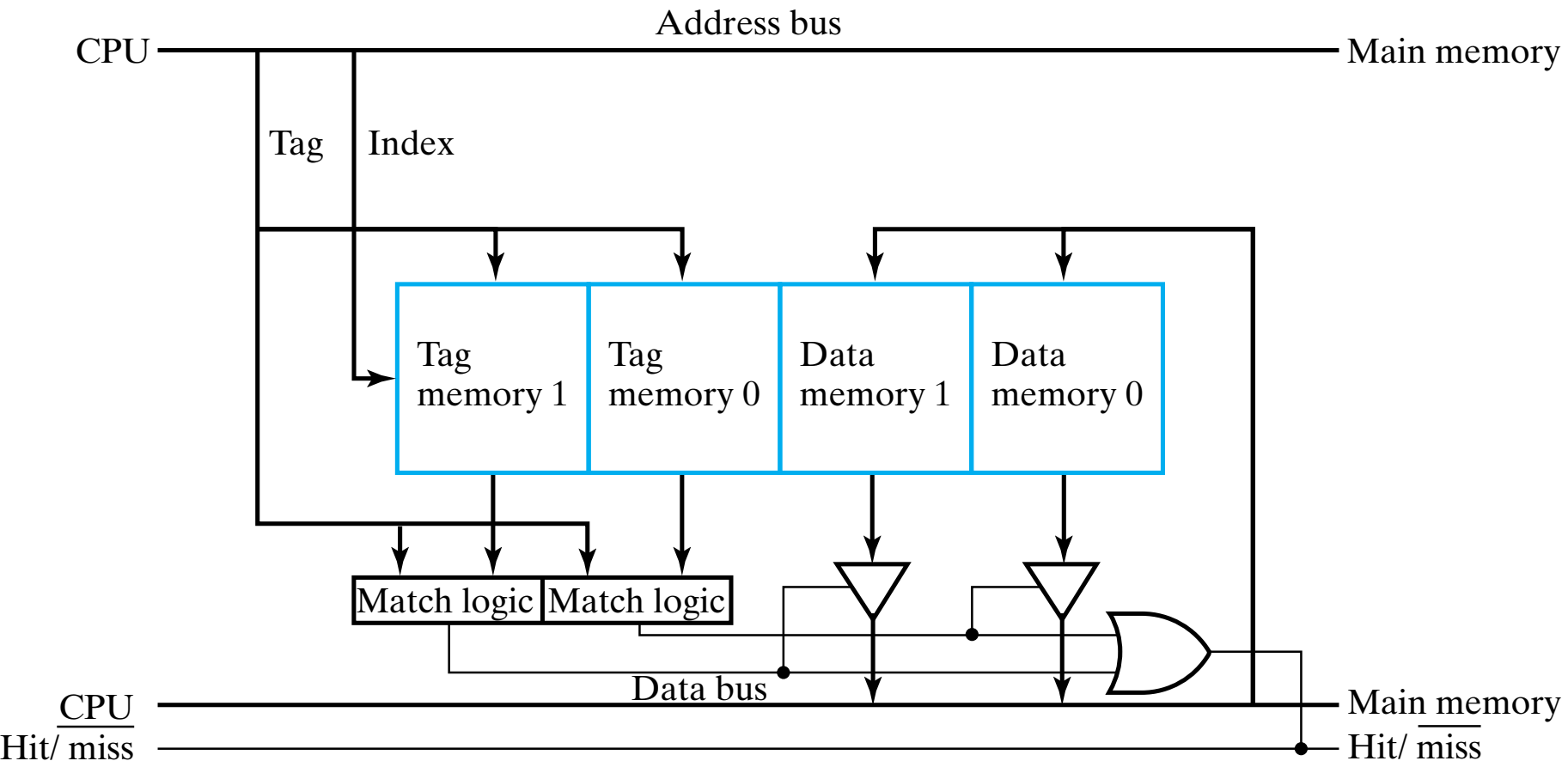
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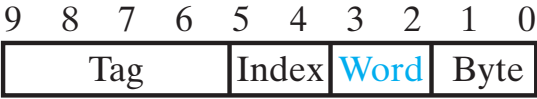
1111111000

1111111100

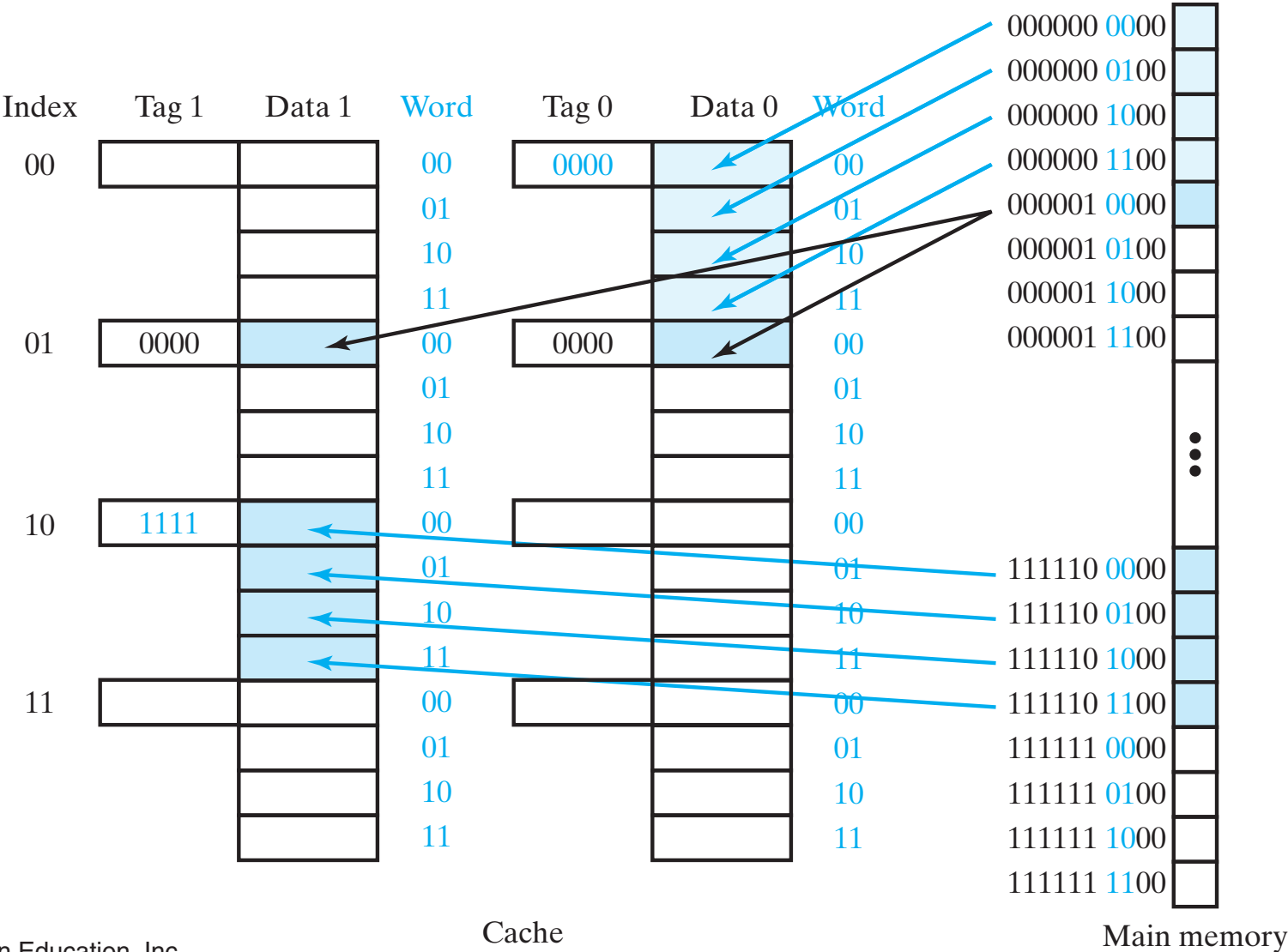
Main memory

(b) Cache mapping

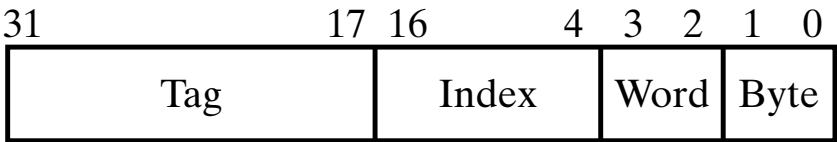




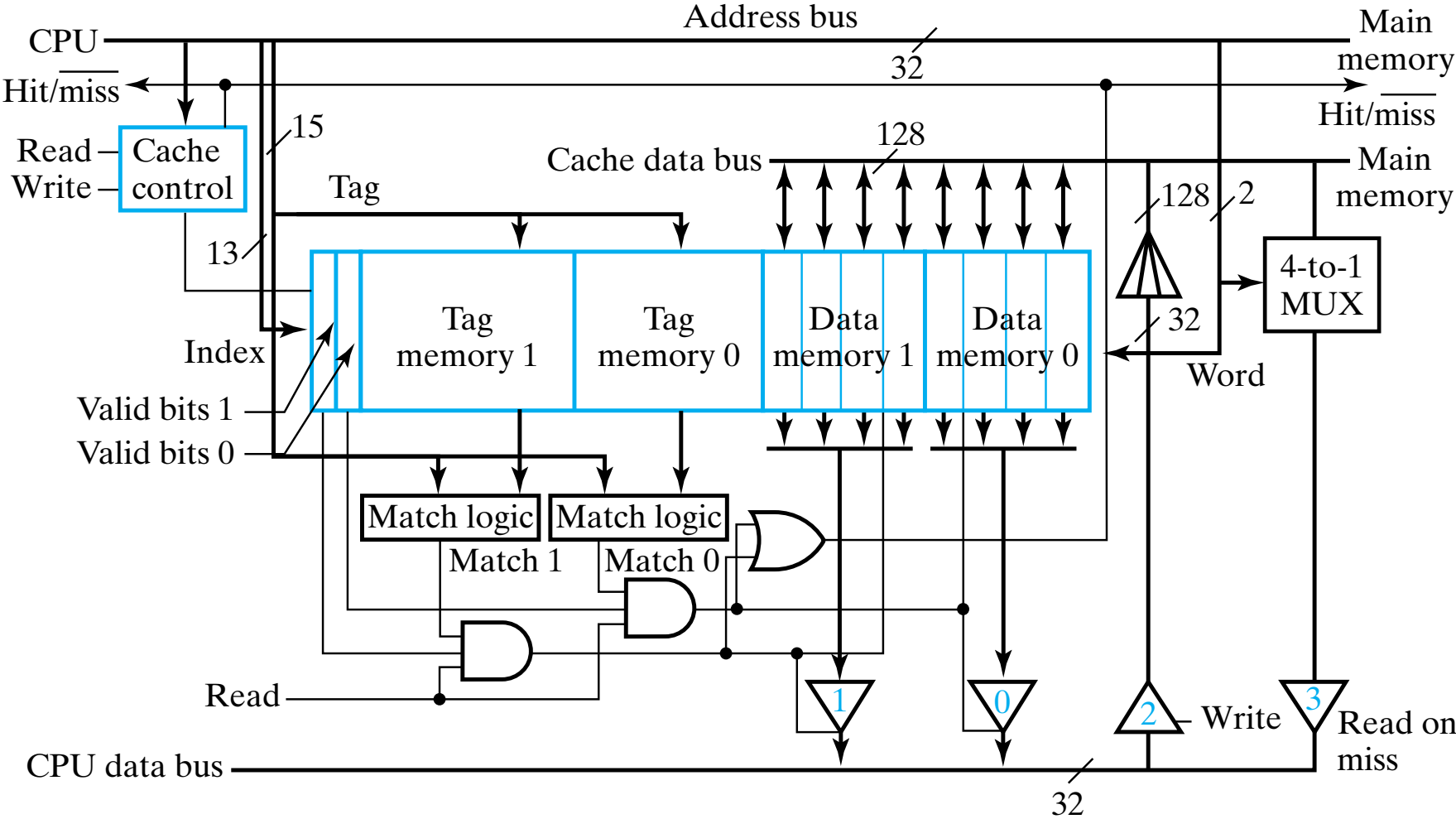
(a) Memory address



(b) Cache mapping



(a) Memory address



(b) Cache diagram

