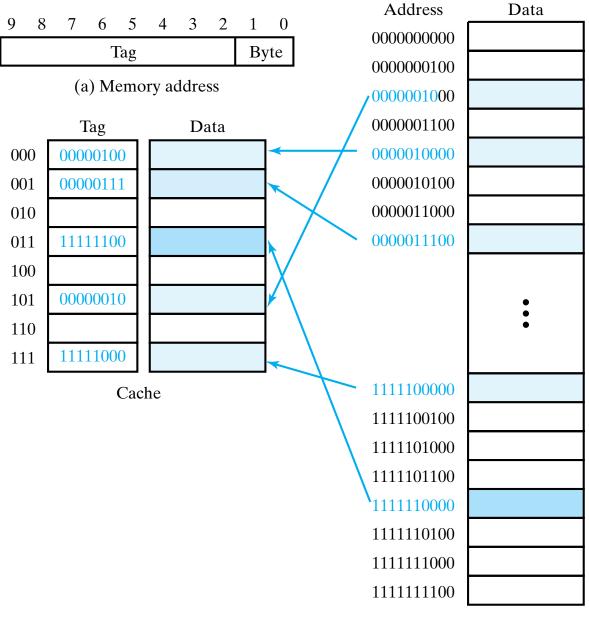


Main memory

(b) Cache mapping

© 2004 Pearson Education, Inc. M. Morris Mano & Charles R. Kime

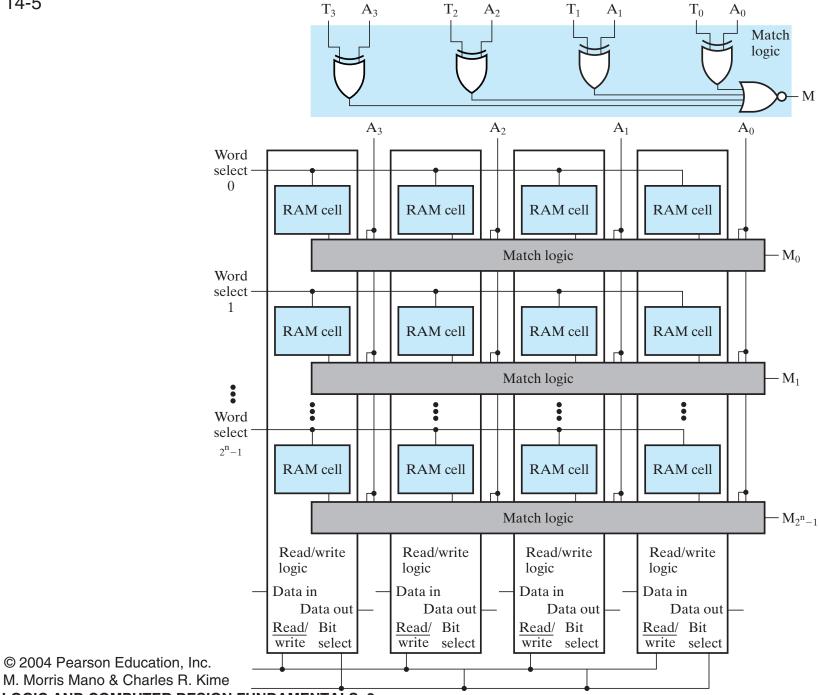


Main memory

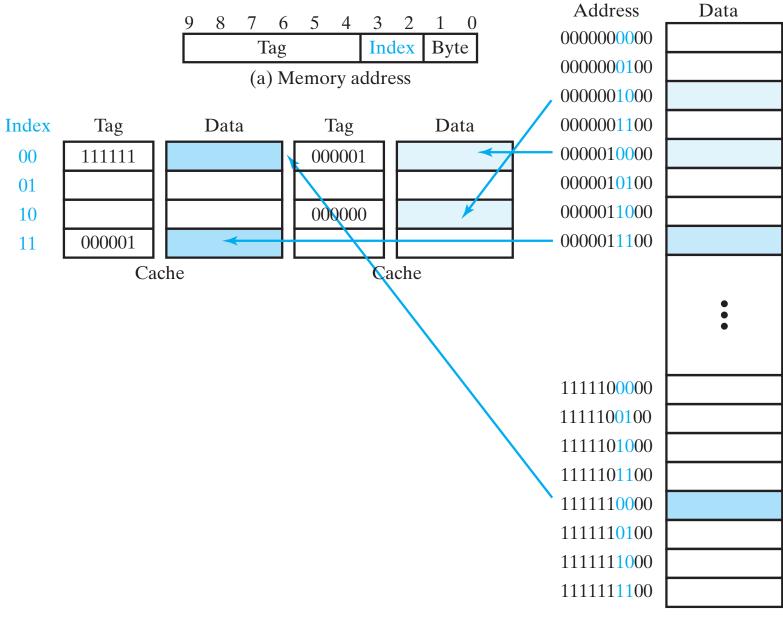
(b) Cache mapping

© 2004 Pearson Education, Inc. M. Morris Mano & Charles R. Kime

LOGIC AND COMPUTER DESIGN FUNDAMENTALS, 3e



LOGIC AND COMPUTER DESIGN FUNDAMENTALS, 3e

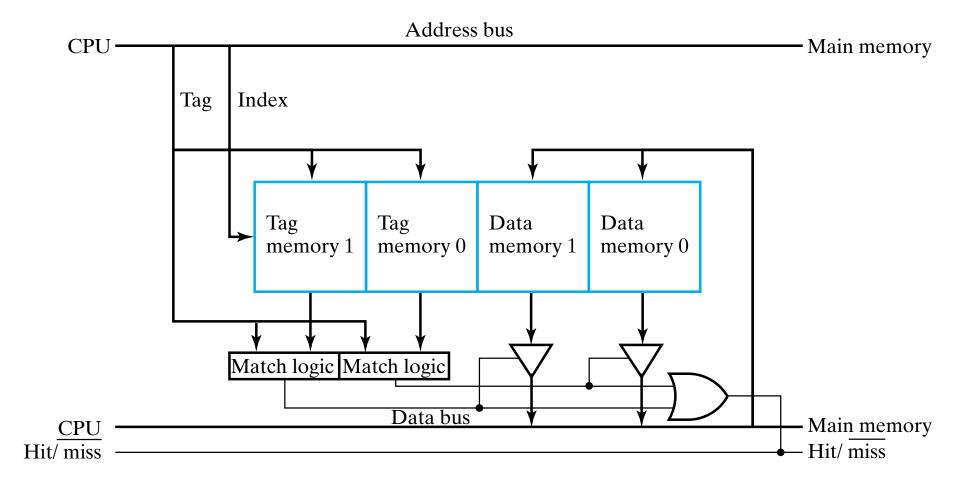


Main memory

(b) Cache mapping

© 2004 Pearson Education, Inc. M. Morris Mano & Charles R. Kime

LOGIC AND COMPUTER DESIGN FUNDAMENTALS, 3e



9	8	7	6	5	4	3	2	1	0	
	Tag				Index		Word		Byte	

(a) Memory address

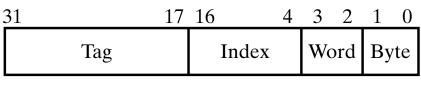
							000000 0000		
т 1	TD 1	D 4 1	XX7 1	TT. O	D (0	W 1	000000 0100		
Index	Tag 1	Data 1	Word	Tag 0	Data 0	Word	000000 1000	\blacksquare	
00			00	0000		00	000000 1100		
			01			01	000001 0000		
			10			10	000001 0100		
			11		1	11	000001 1000		
01	0000	*	00	0000		00	000001 1100		
'			01			01			
			10			10			
			11			11		:	
10	1111	—	00			00			
'		—	01			01	111110 0000		
		—	10			10	— 111110 01 00		
		—	11			11	111110 1000		
11			00			00	111110 1100		
'			01			01	111111 0000		
			10			10	111111 <mark>01</mark> 00		
			11			11	111111 10 00		
				'			111111 <mark>11</mark> 00		
on Educati	on. Inc.		Ca	ache		Mair	n mer	nory	
on Laucanon, mc.									

© 2004 Pearson Education, Inc.

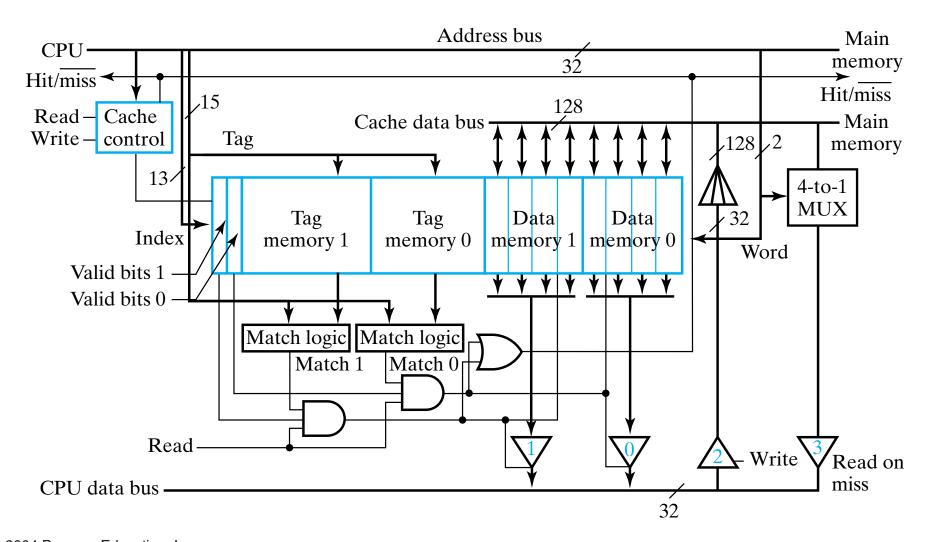
M. Morris Mano & Charles R. Kime

LOGIC AND COMPUTER DESIGN FUNDAMENTALS, 3e

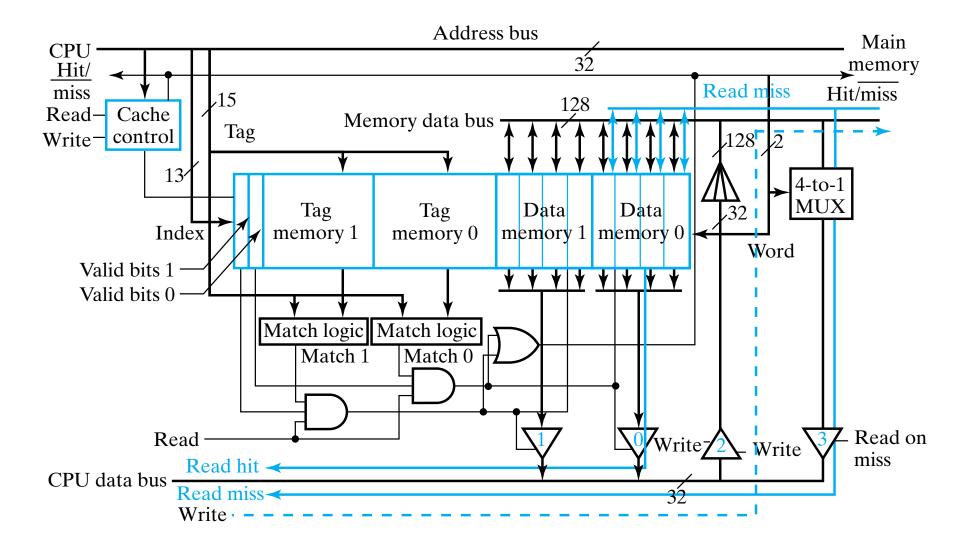
(b) Cache mapping

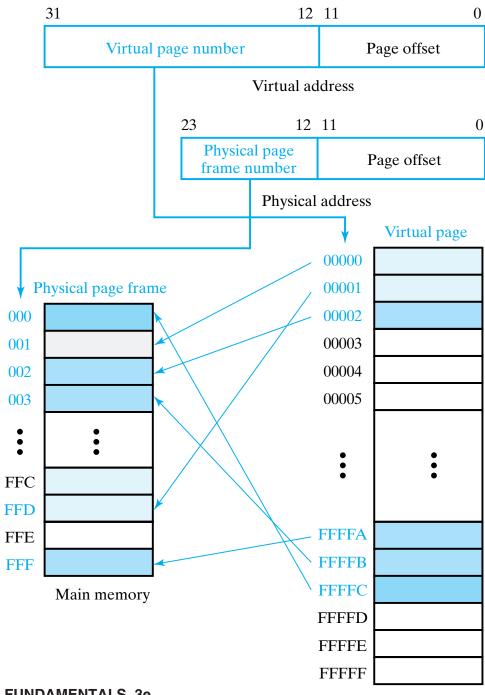


(a) Memory address



^{© 2004} Pearson Education, Inc. M. Morris Mano & Charles R. Kime

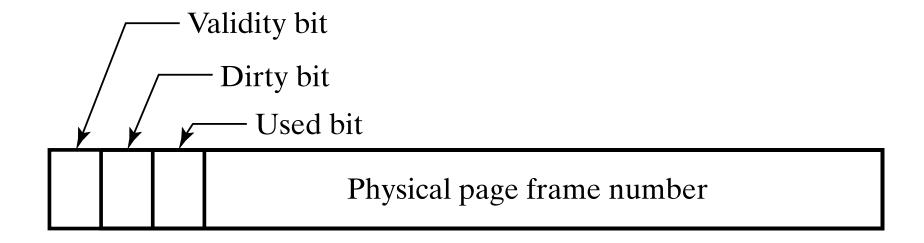


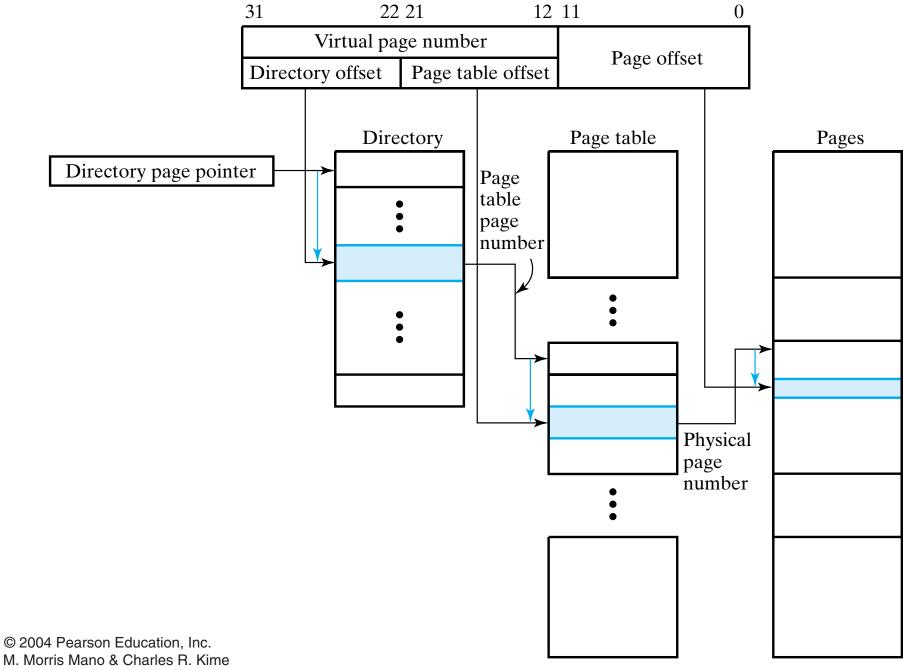


LOGIC AND COMPUTER DESIGN FUNDAMENTALS, 3e

© 2004 Pearson Education, Inc.

M. Morris Mano & Charles R. Kime





LOGIC AND COMPUTER DESIGN FUNDAMENTALS, 3e

Virtual Address from CPU Page offset Virtual page number Page number input Fully associative or set-associative cache Valid bit Dirty bit Tag Data Virtual page number Physical page frame number Page frame number output Page frame number Page offset

Physical address to main memory