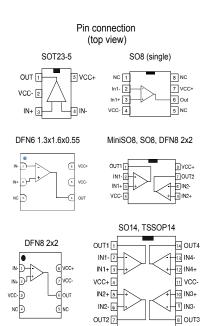


TSV991, TSV992, TSV994 TSV991A, TSV992A, TSV994A

Datasheet

Rail-to-rail input/output 20 MHz GBP operational amplifiers



Features

- Low input offset voltage: 1.5 mV max. (A grade)
- · Rail-to-rail input and output
- Wide bandwidth 20 MHz
- Stable for gain ≥ 4 or ≤ -3
- Low power consumption: 820 μA typ.
- · High output current: 35 mA
- Operating from 2.5 V to 5.5 V
- · Low input bias current, 1 pA typ.
- ESD internal protection ≥ 5 kV

Applications

- · Battery-powered applications
- Portable devices
- Signal conditioning and active filtering
- Medical instrumentation
- · Automotive applications

Description

The TSV99x and TSV99xA family of single, dual, and quad operational amplifiers offers low voltage operation and rail-to-rail input and output. These devices feature an excellent speed/power consumption ratio, offering a 20 MHz gain-bandwidth, stable for gains above 4 (100 pF capacitive load), while consuming only 1.1 mA maximum at 5 V. They also feature an ultra-low input bias current. These characteristics make the TSV99x family ideal for sensor interfaces, battery-supplied and portable applications, as well as active filtering. These characteristics make the TSV99x, TSV99xA family ideal for sensor interfaces, battery-supplied and portable applications, as well as active filtering.

Maturity status link

TSV991, TSV992, TSV994, TSV991A, TSV992A, TSV994A

Related products

See TSV911, TSV912, TSV914, TSV911A, TSV912A, TSV914A For unity-gain stable amplifiers



Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

ymbol	Parameter		Value	Unit	
V _{CC}	Supply voltage (1)		6		
V _{id}	Differential input voltage (2)		±V _{CC}	V	
V _{in}	Input voltage (3)		(V _{CC-}) - 0.2 to (V _{CC+}) + 0.2	•	
l _{in}	Input current (4)		10	mA	
T _{stg}	Storage temperature		-65 to 150	00	
Tj	Maximum junction temperature		150	°C	
		DFN8 2x2	57		
		DFN6 1.3x1.6x0.55	230		
		SOT23-5	250		
R _{thja}	Thermal resistance junction to ambient (5) (6)	SO8	125		
		MiniSO8	190	v mA °C °C/W	
		SO14	103		
		TSSOP14	100		
		SOT23-5	81		
		SO8	40		
R_{thjc}	Thermal resistance junction to case	MiniSO8	39		
		SO14	31		
		TSSOP14	32		
	HBM: human body model (7)		5	kV	
	MM: machine model (8)		400		
ESD		SOT23-5, SO8, MiniSO8, DFN8 2x2	1500	V	
	CDM: charged device model (9)	DFN6 1.3x1.6x0.55	TBD		
		TSSOP14	750		
		SO14	500		
	Latch-up immunity		200	mA	

- 1. Value is with respect to the V_{CC} pin.
- 2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
- 3. V_{CC} V_{IN} must not exceed 6 V.
- 4. Input current must be limited by a resistor in series with the inputs.
- 5. Short-circuits can cause excessive heating and destructive dissipation.
- 6. Rth are typical values.
- 7. Human body model: 100 pF discharged through a 1.5 k Ω resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
- 8. Machine model: 200 pF charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor $< 5 \Omega$), done for all couples of pin combinations with other pins floating.
- 9. Charged device model: all pins plus packages are charged together to the specified voltage and then discharged directly to the ground.

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Absolute maximum ratings and operating conditions

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V _{CC}	Supply voltage	2.5 to 5.5	V
V _{icm}	Common mode input voltage range	(V_{CC-}) - 0.1 to (V_{CC+}) + 0.1	V
T _{op}	Operating free air temperature range	-40 to 125	°C

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2 Electrical characteristics

Note:

In the electrical characteristic tables below, all parameter limits at temperatures other than 25 °C are guaranteed by correlation.

Table 3. Electrical characteristics at V_{CC^+} = 2.5 V, V_{CC^-} = 0 V, V_{icm} = $V_{CC}/2$, with R_L connected to $V_{CC}/2$, full temperature range (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
		DC performance				
	Offeet voltage TSV/00v	T _{op} = 25 °C		0.1	4.5	
V_{io}	Offset voltage, TSV99x	$T_{min} < T_{op} < T_{max}$			7.5	m\/
v 10	Officet voltage, TSV/00vA	T _{op} = 25 °C			1.5	IIIV
	Offset voltage, TSV99xA	$T_{min} < T_{op} < T_{max}$			3	
$\Delta V_{io}/\Delta T$	Input offset voltage drift			2		μV/°C
ı.	Input offset current, V _{out} = V _{CC} /2	T _{op} = 25 °C		1	10	
l _{io}	(1)	$T_{min} < T_{op} < T_{max}$			100	5 0
I	Input bias current, V _{out} = V _{CC} /2	T _{op} = 25 °C		1	10	рA
l _{ib}	(1)	$T_{min} < T_{op} < T_{max}$			100	mV
OMP	Common mode rejection ratio,	0 V to 2.5 V, V _{out} = 1.25 V, T _{op} = 25 °C	58	75		
CMR	$20 \log (\Delta V_{ic}/\Delta V_{io})$	$T_{min} < T_{op} < T_{max}$	53			
		R_L = 10 k Ω , V_{out} = 0.5 V to 2 V,	00	00		dB
A_{vd}	Large signal voltage gain	T _{op} = 25 °C	80	89		μV/°C pA dB mV MHz V/V
		$T_{min} < T_{op} < T_{max}$	75			
V V	High lavel autout valtage	$R_L = 10 \text{ k}\Omega$, $T_{min} < T_{op} < T_{max}$		15	40	
V _{CC} - V _{OH}	High-level output voltage	$R_L = 600 \Omega$, $T_{min} < T_{op} < T_{max}$		45	150	\
\/	Law law day to the ma	$R_L = 10 \text{ k}\Omega, T_{\text{min}} < T_{\text{op}} < T_{\text{max}}$		15	40	mv
V_{OL}	Low-level output voltage	$R_L = 600 \Omega$, $T_{min} < T_{op} < T_{max}$		45	150	
	1	V _o = 2.5 V, T _{op} = 25 °C	18	32		
	Isink	$T_{min} < T_{op} < T_{max}$	16			
l _{out}	1	V _o = 0 V, T _{op} = 25 °C	18	35		mA
	Isource	$T_{min} < T_{op} < T_{max}$	16			
I _{CC}	Supply current (per channel)	No load, $V_{out} = V_{CC}/2$, $T_{min} < T_{op} < T_{max}$		0.78	1.1	
		AC performance				
GBP	Gain bandwidth product	$R_L = 2 \text{ k}\Omega, C_L = 100 \text{ pF, f} = 100 \text{ kHz,}$ $T_{op} = 25 \text{ °C}$		20		MHz
Gain	Minimum gain for stability	Phase margin = 45 °, R_f = 10 k Ω , R_L = 2 k Ω , C_L = 100 pF, T_{op} = 25 °C, positive gain configuration		4		V/V
Gain	Minimum gain for stability	Phase margin = 45 °, R_f = 10 k Ω , R_L = 2 k Ω , C_L = 100 pF, T_{op} = 25 °C, negative gain configuration		-3		V/V
SR	Slew rate	R _L = 2 kΩ, C _L = 100 pF, T _{op} = 25 °C		10		V/µs

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Electrical characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
e _n	Equivalent input noise voltage	f = 10 kHz, T _{op} = 25 °C		21		nV/√Hz
THD+N	Total harmonic distortion	$G = -3$, $f = 1$ kHz, $R_L = 2$ kΩ, $Bw = 22$ kHz, $V_{icm} = V_{CC}/2$, $V_{out} = 2$ V_{pp} , $V_{op} = 25$ °C		0.0025		%

^{1.} Guaranteed by design.

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Table 4. Electrical characteristics at $V_{CC+} = 3.3 \text{ V}$, $V_{CC-} = 0 \text{ V}$, $V_{icm} = V_{CC}/2$, with R_L connected to $V_{CC}/2$, full temperature range (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
		DC performance				
		T _{op} = 25 °C		0.1	4.5	
	Offset voltage, TSV99x	T _{min} < T _{op} < T _{max}			7.5	mV μV/°C pA dB
V _{io}		T _{op} = 25 °C			1.5	
	Offset voltage, TSV99xA	$T_{min} < T_{op} < T_{max}$			3	
$\Delta V_{io}/\Delta T$	Input offset voltage drift			2		μV/°C
	Input offset current, V _{out} = V _{CC} /2	T _{op} = 25 °C		1	10	
l _{io}	(1)	T _{min} < T _{op} < T _{max}			100	
	Input bias current, V _{out} = V _{CC} /2	T _{op} = 25 °C		1	10	pA
l _{ib}	(1)	T _{min} < T _{op} < T _{max}			100	
	Common mode rejection ratio,	0 V to 3.3 V, V _{out} = 1.65 V, T _{op} = 25 °C	60	78		
CMR	20 log $(\Delta V_{ic}/\Delta V_{io})$	T _{min} < T _{op} < T _{max}	55			
		$R_L = 10 \text{ k}\Omega, V_{out} = 0.5 \text{ V to } 2.8 \text{ V},$				dB
A_{vd}	Large signal voltage gain	T _{op} = 25 °C	80	89		
		T _{min} < T _{op} < T _{max}	75			
		$R_L = 10 \text{ k}\Omega$, $T_{min} < T_{op} < T_{max}$		15	40	
V _{CC} - V _{OH}	High-level output voltage	$R_L = 600 \Omega$, $T_{min} < T_{op} < T_{max}$		45	150	
.,		$R_L = 10 \text{ k}\Omega$, $T_{min} < T_{op} < T_{max}$		15	40	mV
V_{OL}	Low-level output voltage	$R_L = 600 \Omega$, $T_{min} < T_{op} < T_{max}$		45	150	1
		V _o = 3.3 V, T _{op} = 25 °C	18	32		
	I _{sink}	$T_{min} < T_{op} < T_{max}$	16			
l _{out}		V _o = 0 V, T _{op} = 25 °C	18	35		mA
	Isource	$T_{min} < T_{op} < T_{max}$	16			
I _{CC}	Supply current (per channel)	No load, $V_{out} = V_{CC}/2$, $T_{min} < T_{op} < T_{max}$		0.8	1.1	
		AC performance				
GBP	Gain bandwidth product	$R_L = 2 k\Omega$, $C_L = 100 pF$, $f = 100 kHz$, $T_{op} = 25 °C$		20		MHz
Gain	Minimum gain for etability	Phase margin = 45 °, R_f = 10 $k\Omega$, R_L = 2 $k\Omega$, C_L = 100 pF, T_{op} = 25 °C, positive gain configuration		4		V/V
Gaill	Minimum gain for stability	Phase margin = 45 °, R_f = 10 $k\Omega$, R_L = 2 $k\Omega$, C_L = 100 pF, T_{op} = 25 °C, negative gain configuration		-3		VIV
SR	Slew rate	$R_L = 2 k\Omega$, $C_L = 100 pF$, $f = 100 kHz$, $T_{op} = 25 °C$		10		V/µs
e _n	Equivalent input noise voltage	f = 10 kHz, T _{op} = 25 °C		21		nV/√H:
THD+N	Total harmonic distortion	$G = -3$, $f = 1$ kHz, $R_L = 2$ kΩ, $Bw = 22$ kHz, $V_{icm} = V_{CC}/2$, $V_{out} = 2.8$ V_{pp} , $V_{op} = 25$ °C		0.0018		%

^{1.} Guaranteed by design.

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Table 5. Electrical characteristics at $V_{CC+} = 5 \text{ V}$, $V_{CC-} = 0 \text{ V}$, $V_{icm} = V_{CC}/2$, with R_L connected to $V_{CC}/2$, full temperature range (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit	
		DC performance					
		T _{op} = 25 °C		0.1	4.5		
	Offset voltage, TSV99x	$T_{min} < T_{op} < T_{max}$			7.5		
V _{io}		T _{op} = 25 °C			1.5	mV	
	Offset voltage, TSV99xA	$T_{min} < T_{op} < T_{max}$			3		
$\Delta V_{io}/\Delta T$	Input offset voltage drift			2		μV/°C	
	Input offset current, V _{out} = V _{CC} /2	T _{op} = 25 °C		1	10		
l _{io}	(1)	$T_{min} < T_{op} < T_{max}$			100		
	Input bias current, V _{out} = V _{CC} /2	T _{op} = 25 °C		1	10	pA	
l _{ib}	(1)	$T_{min} < T_{op} < T_{max}$			100		
		0 V to 5 V, V _{out} = 2.5 V,					
CMR	Common mode rejection ratio, 20 log $(\Delta V_{ic}/\Delta V_{io})$	T _{op} = 25 °C	62	82			
	20 10g (AV ₁₀ , AV ₁₀)	$T_{min} < T_{op} < T_{max}$	57				
SVR	Supply voltage rejection ratio, 20 $\log (\Delta V_{cc}/\Delta V_{io})$	V _{CC} = 2.5 V to 5 V	70	86		dB	
		$R_L = 10 \text{ k}\Omega, V_{\text{out}} = 0.5 \text{ V to } 4.5 \text{ V},$	80	91			
A _{vd}	Large signal voltage gain	T _{op} = 25 °C					
		$T_{min} < T_{op} < T_{max}$	75				
V _{CC} - V _{OH}	High-level output voltage	$R_L = 10 \text{ k}\Omega, T_{\text{min}} < T_{\text{op}} < T_{\text{max}}$		15	40		
		$R_L = 600 \Omega$, $T_{min} < T_{op} < T_{max}$		45	150	mV	
V_{OL}	Low-level output voltage	$R_L = 10 \text{ k}\Omega, T_{\text{min}} < T_{\text{op}} < T_{\text{max}}$		15	40		
		$R_L = 600 \Omega$, $T_{min} < T_{op} < T_{max}$		45	150		
	Isink	$V_0 = 5 \text{ V}, T_{op} = 25 ^{\circ}\text{C}$	18	32			
l _{out}	SHIK	$T_{min} < T_{op} < T_{max}$	16				
·out	I _{source}	$V_0 = 0 \text{ V}, T_{op} = 25 ^{\circ}\text{C}$	18	35		mA	
	Source	$T_{min} < T_{op} < T_{max}$	16				
I_{CC}	Supply current (per channel)	No load, V_{out} = 2.5 V, T_{min} < T_{op} < T_{max}		0.82	1.1		
		AC performance					
GBP	Gain bandwidth product	$R_L = 2 \text{ k}\Omega$, $C_L = 100 \text{ pF}$, $f = 100 \text{ kHz}$, $T_{op} = 25 ^{\circ}\text{C}$		20		MHz	
0-1	Malana	Phase margin = 45 °, R_f = 10 k Ω , R_L = 2 k Ω , C_L = 100 pF, T_{op} = 25 °C, positive gain configuration		4		10.	
Gain	Minimum gain for stability	Phase margin = 45 °, R_f = 10 k Ω , R_L = 2 k Ω , C_L = 100 pF, T_{op} =25 °C, negative gain configuration		-3		V/V	
SR	Slew rate	$R_L = 2 \text{ k}\Omega$, $C_L = 100 \text{ pF}$, $f = 100 \text{ kHz}$, $T_{op} = 25 \text{ °C}$		10		V/µs	
e _n	Equivalent input noise voltage	f = 10 kHz, T _{op} = 25 °C		21		nV/√H	

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Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
THD+N	Total harmonic distortion	$G = -3$, $f = 1$ kHz, $R_L = 2$ kΩ, $Bw = 22$ kHz, $V_{icm} = V_{CC}/2$, $V_{out} = 4.4$ V_{pp} , $V_{op} = 25$ °C		0.0014		%

^{1.} Guaranteed by design.

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Electrical characteristic curves

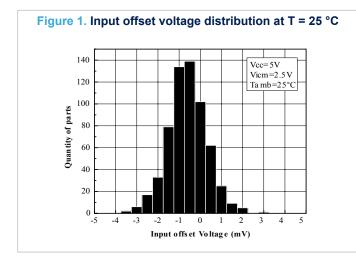


Figure 2. Input offset voltage distribution at T = 125 °C

40

40

Voc=5V
Vicm=2.5V
Tamb=125°C

10

10

10

10

10

11

11

12

3 4 5

Input offset Voltage (mV)

Figure 3. Supply current vs. input common-mode voltage at $V_{CC} = 2.5 \text{ V}$

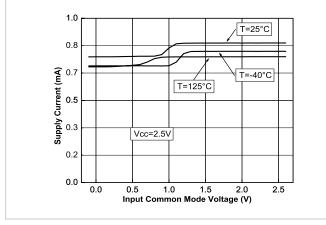


Figure 4. Supply current vs. input common-mode voltage at V_{CC} = 5 V

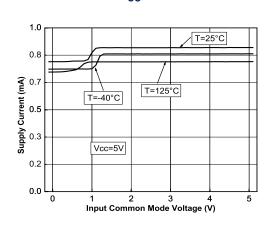


Figure 5. Output current vs. output voltage at V_{CC} = 2.5 V

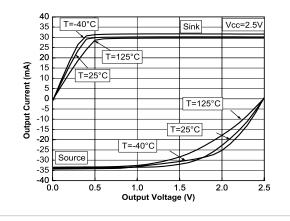
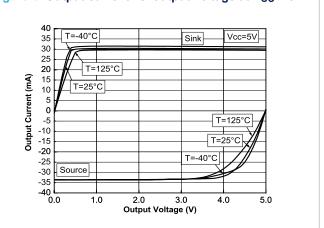


Figure 6. Output current vs. output voltage at $V_{CC} = 5 \text{ V}$



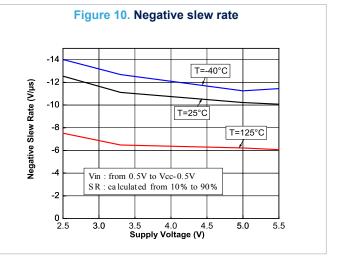
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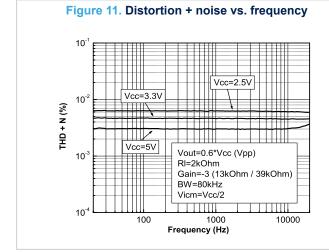


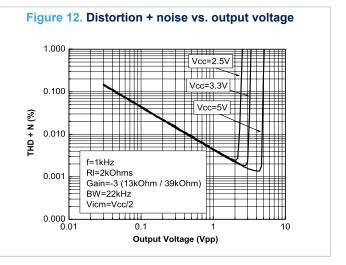
Figure 7. Voltage gain and phase vs. frequency at $V_{CC} = 5$ V and V_{icm} = 0.5 V 40 160 Gain 30 120 Phase 20 80 40 10 Gain (dB) 0 0 -10 -40 -80 -20 Vcc=5V, Vicm=0.5V CI=100pF, RI=2KOhm, VrI=Vcc/2 -30 120 Tamb=25°C -160 10⁵ 10⁶ 10⁷ Frequency (Hz)

Figure 8. Voltage gain and phase vs. frequency at $V_{CC} = 5$ V and V_{icm} = 2.5 V 40 160 Gain Phase 30 120 20 80 40 10 Gain (dB) 0 0 -10 -40 -20 -80 Vcc=5V, Vicm=2.5V Cl=100pF, Rl=2KOhm, Vrl=Vcc/2 Tamb=25°C -30 -120 10 107 Frequency (Hz)

Figure 9. Positive slew rate 14 12 T=25°C Positive Slew Rate (V/µs) T=125°C T=-40°C Vin: from 0.5V to Vcc-0.5V $S\,R$: calculated from 10% to 90% 2 0 L 2.5 3.0 4.0 5.0 5.5 Supply Voltage (V)





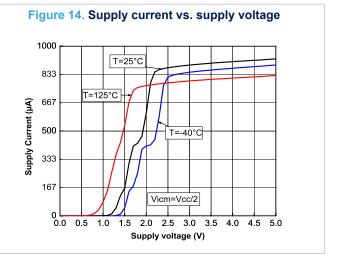


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Figure 13. Noise vs. frequency

(AHAVA)



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4 Application information

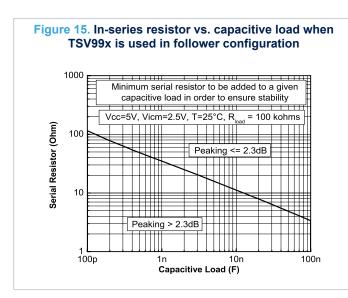
4.1 Driving resistive and capacitive loads

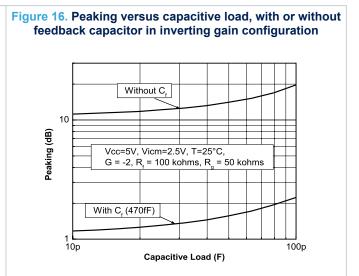
These products are low-voltage, low-power operational amplifiers optimized to drive rather large resistive loads above $2 \text{ k}\Omega$.

The TSV99x products are not unity gain stable. To ensure proper stability they must be used in a gain configuration, with a minimum gain of -3 or 4.

However, they can be used in a "follower" configuration by adding a small, in-series resistor at the output, which drastically improves the stability of the device (Figure 15 shows the recommended in-series resistor values). Once the in-series resistor value has been selected, the stability of the circuit should be tested on the bench and simulated with the simulation model.

Another way to improve stability and reduce peaking is to add a capacitor in parallel with the feedback resistor. As shown in Figure 16, the feedback capacitor drastically reduces the peaking versus capacitive load (inverting gain configuration, gain = -2).





4.2 PCB layouts

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

4.3 Macromodel

An accurate macromodel of the TSV99x is available on STMicroelectronics' web site at www.st.com. This model is a trade-off between accuracy and complexity (that is, time simulation) of the TSV99x operational amplifiers. It emulates the nominal performance of a typical device within the specified operating conditions mentioned in the datasheet. It helps to validate a design approach and to select the right operational amplifier, however, it does not replace on-board measurements.

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5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

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5.1 SOT23-5 package information

Figure 17. SOT23-5 package outline

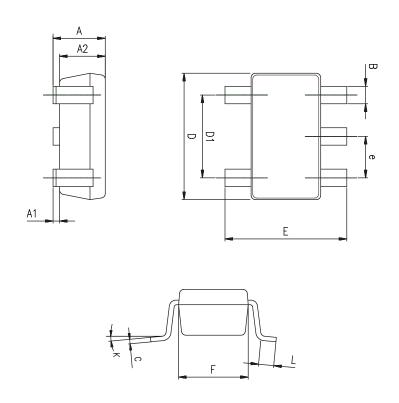


Table 6. SOT23-5 mechanical data

			Dimer	nsions		
Ref.		Millimeters			Inches	
	Min.	Тур.	Max.	Min.	Тур.	Max.
Α	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
В	0.35	0.40	0.50	0.014	0.016	0.020
С	0.09	0.15	0.20	0.004	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
е		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.014	0.024
K	0 degrees		10 degrees	0 degrees		10 degrees

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5.2 DFN8 2 x 2 package information

SEATING PLANE

C

PIN#1 ID

PIN#1 ID

BOTTOM VIEW

Figure 18. DFN8 2 x 2 package outline

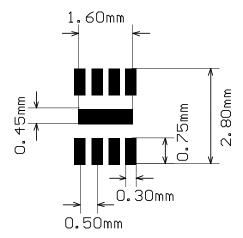
Table 7. DFN8 2 x 2 mechanical data

			Dime	nsions		
Ref.		Millimeters			Inches	
	Min.	Тур.	Max.	Min.	Тур.	Max.
Α	0.51	0.55	0.60	0.020	0.022	0.024
A1			0.05			0.002
А3		0.15			0.006	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	1.85	2.00	2.15	0.073	0.079	0.085
D2	1.45	1.60	1.70	0.057	0.063	0.067
E	1.85	2.00	2.15	0.073	0.079	0.085
E2	0.75	0.90	1.00	0.030	0.035	0.039
е		0.50			0.020	
L			0.425			0.017
ddd			0.08			0.003

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Figure 19. DFN8 2 x 2 recommended footprint



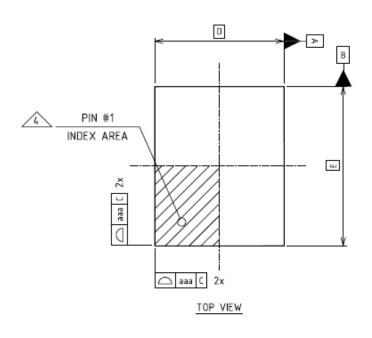
Note: The exposed pad of the DFN8 2x2 package is not internally connected. It can be set to V_{CC}^- or left floating.

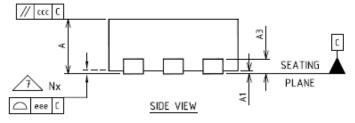
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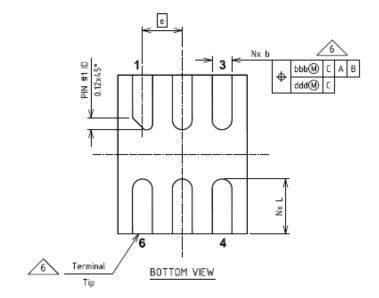


5.3 DFN6 1.3 x 1.6 x 0.55 package information

Figure 20. DFN6 1.3 x 1.6 x 0.55 package outline







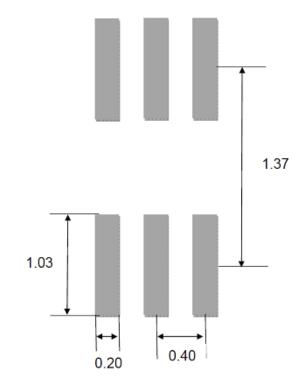
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Table 8. DFN6 1.3 x 1.6 x 0.55 mechanical data

			Dimer	nsions		
Ref.		Millimeters			Inches	
	Min.	Тур.	Max.	Min.	Тур.	Max.
А	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.15			0.006	
В	0.15	0.20	0.25	0.006	0.008	0.010
D		1.30			0.051	
E		1.60			0.063	
е		0.40			0.016	
L	0.453	0.553	0.653	0.018	0.022	0.026
N		6			0.236	
aaa		0.05			0.002	
bbb		0.07			0.003	
ccc		0.10			0.004	
ddd		0.05			0.002	
eee		0.08			0.003	

Figure 21. DFN6 1.3 x 1.6 x 0.55 recommended footprint



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5.4 MiniSO8 package information

Figure 22. MiniSO8 package outline

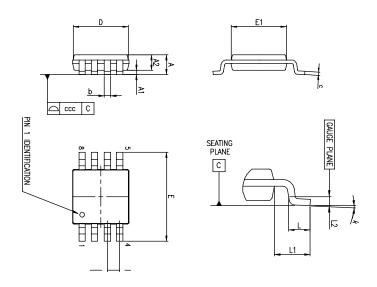


Table 9. MiniSO8 package mechanical data

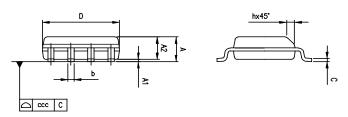
			Dime	nsions		
Ref.		Millimeters			Inches	
	Min.	Тур.	Max.	Min.	Тур.	Max.
Α			1.1			0.043
A1	0		0.15	0		0.0006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
С	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
е		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

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5.5 SO8 package information

Figure 23. SO8 package outline



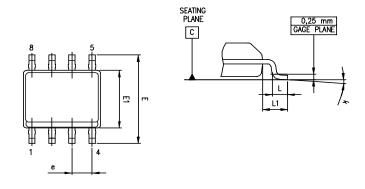


Table 10. SO8 package mechanical data

			Dime	nsions		
Ref.		Millimeters			Inches	
	Min.	Тур.	Max.	Min.	Тур.	Max.
А			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
С	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
е		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	0°		8°	0°		8°
ccc			0.10			0.004

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5.6 SO14 package information

Figure 24. SO14 package outline

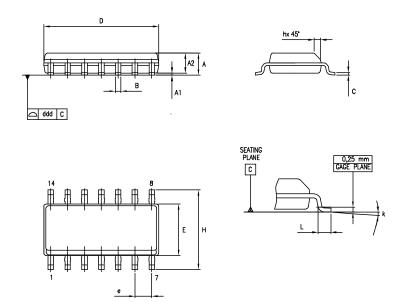


Table 11. SO14 package mechanical data

	Dimensions						
Ref.	Millimeters			Inches			
	Min.	Тур.	Max.	Min.	Тур.	Max.	
Α	1.35		1.75	0.05		0.068	
A1	0.10		0.25	0.004		0.009	
A2	1.10		1.65	0.04		0.06	
В	0.33		0.51	0.01		0.02	
С	0.19		0.25	0.007		0.009	
D	8.55		8.75	0.33		0.34	
E	3.80		4.0	0.15		0.15	
е		1.27			0.05		
Н	5.80		6.20	0.22		0.24	
h	0.25		0.50	0.009		0.02	
L	0.40		1.27	0.015		0.05	
k	8° (max.)						
ddd			0.10			0.004	

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5.7 TSSOP14 package information

Figure 25. TSSOP14 package outline

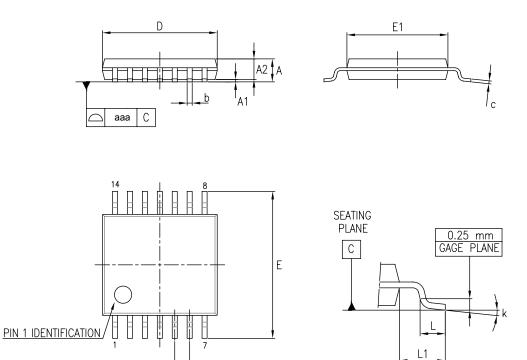


Table 12. TSSOP14 package mechanical data

	Dimensions						
Ref.	Millimeters			Inches			
	Min.	Тур.	Max.	Min.	Тур.	Max.	
А			1.20			0.047	
A1	0.05		0.15	0.002	0.004	0.006	
A2	0.80	1.00	1.05	0.031	0.039	0.041	
b	0.19		0.30	0.007		0.012	
С	0.09		0.20	0.004		0.0089	
D	4.90	5.00	5.10	0.193	0.197	0.201	
Е	6.20	6.40	6.60	0.244	0.252	0.260	
E1	4.30	4.40	4.50	0.169	0.173	0.176	
е		0.65			0.0256		
L	0.45	0.60	0.75	0.018	0.024	0.030	
L1		1.00			0.039		
k	0°		8°	0°		8°	
aaa			0.10			0.004	

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6 Ordering information

Table 13. Order code

Order code	Temperature range	Package	Packing	Marking
TSV991ILT		SOT23-5		K130
TSV991AILT		30123-3		K129
TSV991IQ2T		DFN8 2x2		K1F
TSV991AIQ2T		DFN8 2X2		K1E
TSV991AIQ1T		DFN6 1.3x1.6x0.55		K5
TSV992IST		MiniCOO		K132
TSV992AIST	-40 °C to 125 °C	MiniSO8		K135
TSV992IDT	-40 C to 125 C	000		V992I
TSV992AIDT		SO8		V992AI
TSV992IQ2T		DFN8 2x2		K38
TSV994IPT		T000D44		V994I
TSV994AIPT		TSSOP14		V994AI
TSV994IDT		SO14	Tana and real	V994I
TSV994AIDT		5014	Tape and reel	V994AI
TSV991IYLT		SOT23-5		K149
TSV991AIYLT		50123-5		K150
TSV991IYDT				V991IY
TSV991AIYDT		SO8		V991AY
TSV992IYDT		508		V992IY
TSV992AIYDT	-40 °C to 125 °C			V992AY
TSV992IYST	automotive grade (1)	MiniCOO		K149
TSV992AIYST		MiniSO8		K150
TSV994IYDT		0044		V994IY
TSV994AIYDT		SO14		V994AY
TSV994IYPT		T000044		V994IY
TSV994AIYPT		TSSOP14		V994AY

Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.

Note: In the table above, all packages except the SO14 are "moisture sensitivity level 1" as per JEDEC J-STD-020-C. SO14 is JEDEC level 3.

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Revision history

Table 14. Document revision history

Date	Revision	Changes
10-Mar-2014	10	Table 13: "Order codes": added new commercial product TSV991AlQ2T; corrected "Marking" error for TSV991IQ2T from K1E to K1F.
		Added DFN6 1.3 x 1.6 x 0.55 package for new order code TSV991AIQ1T.
12-Jun-2015	11	Updated "L" dimension of Section 4: "DFN8 2 x 2 mm (NB) package information".
		Updated min "k" value of Section 4.5: "SO8 package information".
	12	Table 3, Table 4, and Table 5: modified that R_L = 600 Ω (not 600 $k\Omega$) for the high-level and low-level output voltage parameters.
27-Nov-2015		Section 5.2: updated name of package and titles of drawings and table; added note about exposed pad.
		Section 5.3: updated name of package.
03-Apr-2018	13	Updated cover image and Table 13. Order code.
19-Jun-2019	14	Updated the related product table in cover page.
44.0 2022	15	Updated figure on the cover page.
14-Sep-2022		Added TSV991IYDT and TSV991AIYDT new order codes in Table 13. Order code.

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