Altera FPGA SDRAM (16-bit data port)

SDRAM controller input address [21:0]

SDRAM address: SA[11:0]

256 columns Column address [7: 0]

4096 rows Row address[19:8]

4 banks Bank address [21:20]

Micron mt48lc8m16a2 (16-bit data port)

512 columns Column address [8: 0]

Reset\_n (SDRAM controller) ; Reset (others)

Modification of cache controller

1. Eliminate WAIT state

2. Eliminate w\_ack and r\_ack signals

3. Separate data input and output port connected to SDRAM controller

4. 1 cycle delay from the SDRAM controller data input to SDRAM DQ port (default is 2). Otherwise, the data cannot be driven to DQ port on time

Modification of SDRAM controller

1. SDRAM read and write have different ST states:

//////////////////////////////////////////////

// Zheming Jin

//

// ST goes to state zero at different point

// for read and write operation respectively

//////////////////////////////////////////////

//else if(ST==SC\_CL+SC\_RCD+LENGTH+2)

//ST <= 0;

if(Read)

begin

if(ST==SC\_CL+SC\_RCD+2)

OUT\_VALID <= 1;

else if(ST==SC\_CL+SC\_RCD+LENGTH+2)

begin

OUT\_VALID <= 0;

Read <= 0;

ST <= 0;

end

end

if(Write)

begin

if(ST==SC\_CL-1)

IN\_REQ <= 1;

else if(ST==SC\_CL+LENGTH-1)

begin

IN\_REQ <= 0;

Write <= 0;

ST <= 0;

end

end